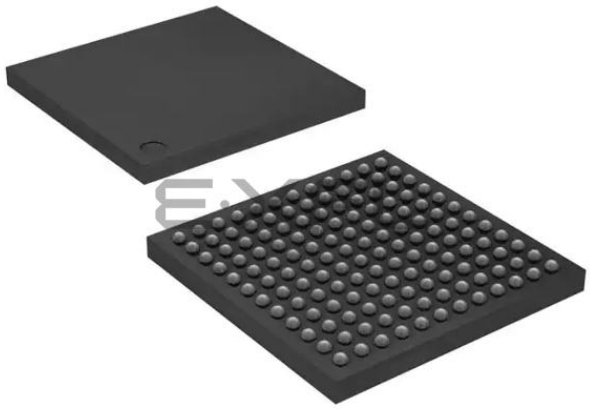

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	EBI/EMI, I²C, IrDA, SD, SPI, UART/USART, USB, USB OTG
Peripherals	DMA, I²S, LVD, POR, PWM, WDT
Number of I/O	96
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 41x16b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LBGA
Supplier Device Package	144-MAPBGA (13x13)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mk50dx256cmd10

Field	Description	Values
FFF	Program flash memory size	• 32 = 32 KB • 64 = 64 KB • 128 = 128 KB • 256 = 256 KB • 512 = 512 KB • 1M0 = 1 MB • 2M0 = 2 MB
R	Silicon revision	• Z = Initial • (Blank) = Main • A = Revision after main
T	Temperature range (°C)	• V = –40 to 105 • C = –40 to 85
PP	Package identifier	• FM = 32 QFN (5 mm x 5 mm) • FT = 48 QFN (7 mm x 7 mm) • LF = 48 LQFP (7 mm x 7 mm) • LH = 64 LQFP (10 mm x 10 mm) • MP = 64 MAPBGA (5 mm x 5 mm) • LK = 80 LQFP (12 mm x 12 mm) • LL = 100 LQFP (14 mm x 14 mm) • MC = 121 MAPBGA (8 mm x 8 mm) • LQ = 144 LQFP (20 mm x 20 mm) • MD = 144 MAPBGA (13 mm x 13 mm) • MJ = 256 MAPBGA (17 mm x 17 mm)
CC	Maximum CPU frequency (MHz)	• 5 = 50 MHz • 7 = 72 MHz • 10 = 100 MHz • 12 = 120 MHz • 15 = 150 MHz
N	Packaging type	• R = Tape and reel • (Blank) = Trays

2.4 Example

This is an example part number:

MK50DN512ZVMD10

3 Terminology and guidelines

3.1 Definition: Operating requirement

An *operating requirement* is a specified value or range of values for a technical characteristic that you must guarantee during operation to avoid incorrect operation and possibly decreasing the useful life of the chip.

Table 5. Power mode transition operating behaviors

Symbol	Description	Min.	Max.	Unit	Notes
t_{POR}	After a POR event, amount of time from the point V_{DD} reaches 1.71 V to execution of the first instruction across the operating temperature range of the chip. • V_{DD} slew rate ≥ 5.7 kV/s • V_{DD} slew rate < 5.7 kV/s	 — —	 300 1.7 V / (V_{DD} slew rate)	µs	1
	• VLLS1 → RUN	—	130	µs	
	• VLLS2 → RUN	—	92	µs	
	• VLLS3 → RUN	—	92	µs	
	• LLS → RUN	—	5.9	µs	
	• VLPS → RUN	—	5.0	µs	
	• STOP → RUN	—	5.0	µs	

1. Normal boot (FTFL_OPT[LPBOOT]=1)

5.2.5 Power consumption operating behaviors

Table 6. Power consumption operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I_{DDA}	Analog supply current	—	—	See note	mA	1
I_{DD_RUN}	Run mode current — all peripheral clocks disabled, code executing from flash • @ 1.8V • @ 3.0V	 — —	 37 38	 63 64	 mA mA	2

I_{DD_RUN}	Run mode current — all peripheral clocks enabled, code executing from flash
	• @ 1.8V
	• @ 3.0V
	  • @ 25°C
	  • @ 125°C
		
		—
		
		—
		—
			
			46
			
			47
			58
				
				77
				
				63
				79
					
					mA
					
					mA
					mA
						3, 4

I_{DD_WAIT}	Wait mode high frequency current at 3.0 V — all peripheral clocks disabled	—	20	—	mA	2
I_{DD_WAIT}	Wait mode reduced frequency current at 3.0 V — all peripheral clocks disabled	—	9	—	mA	5
I_{DD_VLPR}	Very-low-power run mode current at 3.0 V — all peripheral clocks disabled	—	1.12	—	mA	6

Table continues on the next page...

Table 6. Power consumption operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I_{DD_VBAT}	Average current when CPU is not accessing RTC registers					10
	• @ 1.8V					
	• @ –40 to 25°C	—	0.57	0.67	µA	
	• @ 70°C	—	0.90	1.2	µA	
	• @ 105°C	—	2.4	3.5	µA	
	• @ 3.0V					
	• @ –40 to 25°C	—	0.67	0.94	µA	
	• @ 70°C	—	1.0	1.4	µA	
	• @ 105°C	—	2.7	3.9	µA	

1. The analog supply current is the sum of the active or disabled current for each of the analog modules on the device. See each module's specification for its supply current.
2. 100MHz core and system clock, 50MHz bus and FlexBus clock, and 25MHz flash clock . MCG configured for FEI mode. All peripheral clocks disabled.
3. 100MHz core and system clock, 50MHz bus and FlexBus clock, and 25MHz flash clock. MCG configured for FEI mode. All peripheral clocks enabled.
4. Max values are measured with CPU executing DSP instructions.
5. 25MHz core and system clock, 25MHz bus clock, and 12.5MHz FlexBus and flash clock. MCG configured for FEI mode.
6. 4 MHz core, system, FlexBus, and bus clock and 1MHz flash clock. MCG configured for BLPE mode. All peripheral clocks disabled. Code executing from flash.
7. 4 MHz core, system, FlexBus, and bus clock and 1MHz flash clock. MCG configured for BLPE mode. All peripheral clocks enabled but peripherals are not in active operation. Code executing from flash.
8. 4 MHz core, system, FlexBus, and bus clock and 1MHz flash clock. MCG configured for BLPE mode. All peripheral clocks disabled.
9. Data reflects devices with 128 KB of RAM.
10. Includes 32kHz oscillator current and RTC operation.

5.2.5.1 Diagram: Typical IDD_RUN operating behavior

The following data was measured under these conditions:

- MCG in FBE mode for 50 MHz and lower frequencies. MCG in FEE mode at greater than 50 MHz frequencies.
- USB regulator disabled
- No GPIOs toggled
- Code execution from flash with cache enabled
- For the ALLOFF curve, all peripheral clocks are disabled except FTFL

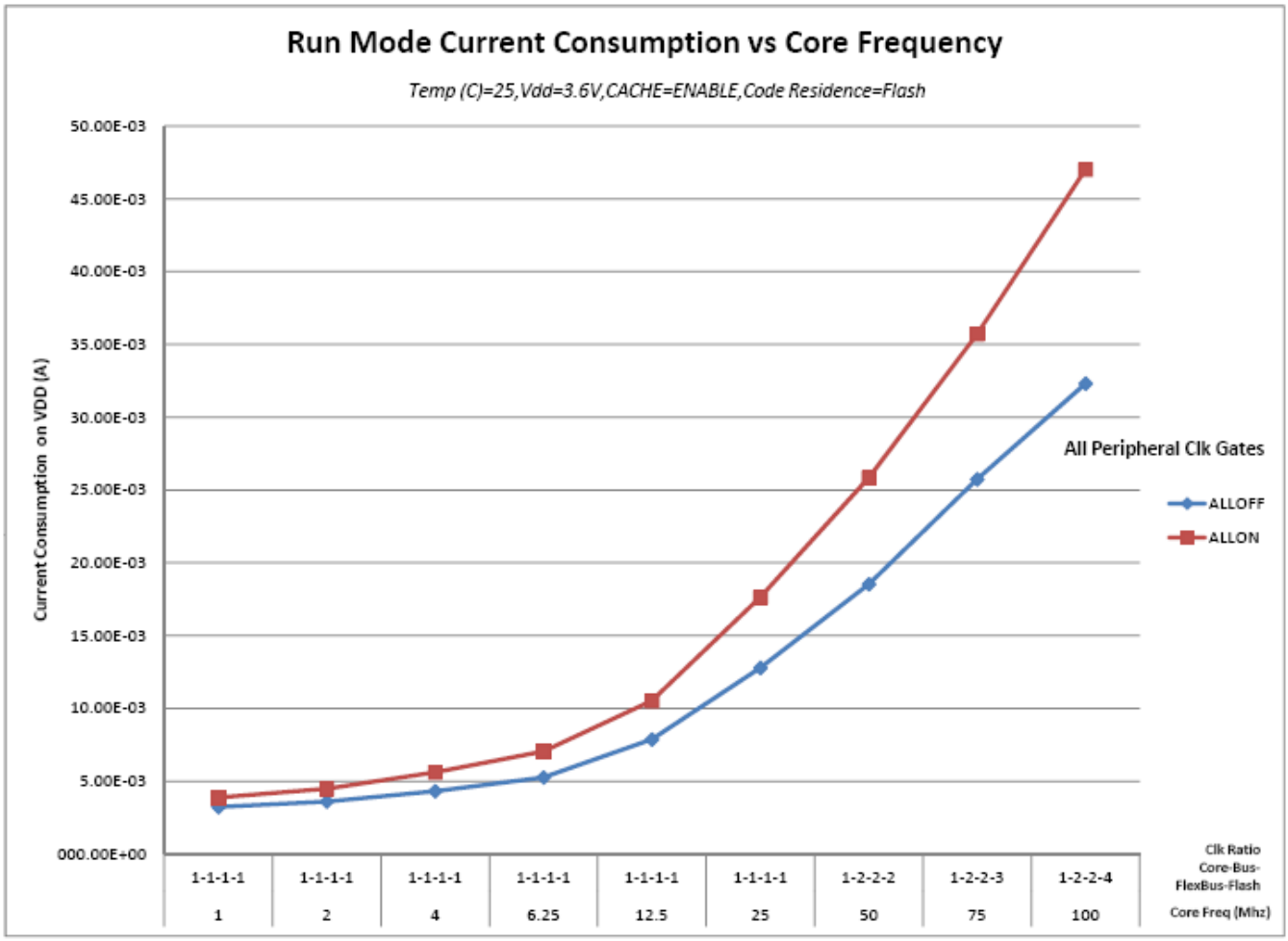

Figure 2. Run mode supply current vs. core frequency

5.2.6 EMC radiated emissions operating behaviors

Table 7. EMC radiated emissions operating behaviors for 144LQFP and 144MAPBGA

Symbol	Description	Frequency band (MHz)	144LQFP	144MAPBGA	Unit	Notes
V_{RE1}	Radiated emissions voltage, band 1	0.15–50	23	12	dBµV	1, 2
V_{RE2}	Radiated emissions voltage, band 2	50–150	27	24	dBµV	
V_{RE3}	Radiated emissions voltage, band 3	150–500	28	27	dBµV	
V_{RE4}	Radiated emissions voltage, band 4	500–1000	14	11	dBµV	
V_{RE_IEC}	IEC level	0.15–1000	K	K	—	2, 3

1. Determined according to IEC Standard 61967-1, *Integrated Circuits - Measurement of Electromagnetic Emissions, 150 kHz to 1 GHz Part 1: General Conditions and Definitions* and IEC Standard 61967-2, *Integrated Circuits - Measurement of Electromagnetic Emissions, 150 kHz to 1 GHz Part 2: Measurement of Radiated Emissions—TEM Cell and Wideband TEM Cell Method*. Measurements were made while the microcontroller was running basic application code. The reported emission level is the value of the maximum measured emission, rounded up to the next whole number, from among the measured orientations in each frequency range.

Board type	Symbol	Description	144 LQFP	144 MAPBGA	Unit	Notes
Four-layer (2s2p)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	36	29	°C/W	1
Single-layer (1s)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./ min. air speed)	36	38	°C/W	1
Four-layer (2s2p)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./ min. air speed)	30	25	°C/W	1
—	$R_{\theta JB}$	Thermal resistance, junction to board	24	16	°C/W	2
—	$R_{\theta JC}$	Thermal resistance, junction to case	9	9	°C/W	3
—	Ψ_{JT}	Thermal characterization parameter, junction to package top outside center (natural convection)	2	2	°C/W	4

1. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)*, or EIA/JEDEC Standard JESD51-6, *Integrated Circuit Thermal Test Method Environmental Conditions—Forced Convection (Moving Air)*.
2. Determined according to JEDEC Standard JESD51-8, *Integrated Circuit Thermal Test Method Environmental Conditions—Junction-to-Board*.
3. Determined according to Method 1012.1 of MIL-STD 883, *Test Method Standard, Microcircuits*, with the cold plate temperature used for the case temperature. The value includes the thermal resistance of the interface material between the top of the package and the cold plate.
4. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)*.

6 Peripheral operating requirements and behaviors

6.1 Core modules

Table 16. Oscillator DC electrical specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{pp}[5]	Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, low-power mode (HGO=0)	—	0.6	—	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, high-gain mode (HGO=1)	—	V_{DD}	—	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, low-power mode (HGO=0)	—	0.6	—	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, high-gain mode (HGO=1)	—	V_{DD}	—	V	

1. V_{DD}=3.3 V, Temperature =25 °C
2. See crystal or resonator manufacturer's recommendation
3. C_x,C_y can be provided by using either the integrated capacitors or by using external components.
4. When low power mode is selected, R_F is integrated and must not be attached externally.
5. The EXTAL and XTAL pins should only be connected to required oscillator components and must not be connected to any other devices.

6.3.2.2 Oscillator frequency specifications

Table 17. Oscillator frequency specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
f_{osc_lo}	Oscillator crystal or resonator frequency — low frequency mode (MCG_C2[RANGE]=00)	32	—	40	kHz	
$f_{osc\_hi\_1}$	Oscillator crystal or resonator frequency — high frequency mode (low range) (MCG_C2[RANGE]=01)	3	—	8	MHz	
$f_{osc\_hi\_2}$	Oscillator crystal or resonator frequency — high frequency mode (high range) (MCG_C2[RANGE]=1x)	8	—	32	MHz	
f_{ec_extal}	Input clock frequency (external clock mode)	—	—	50	MHz	1, 2
t_{dc_extal}	Input clock duty cycle (external clock mode)	40	50	60	%	
t_{cst}	Crystal startup time — 32 kHz low-frequency, low-power mode (HGO=0)	—	750	—	ms	3, 4
	Crystal startup time — 32 kHz low-frequency, high-gain mode (HGO=1)	—	250	—	ms	
	Crystal startup time — 8 MHz high-frequency (MCG_C2[RANGE]=01), low-power mode (HGO=0)	—	0.6	—	ms	
	Crystal startup time — 8 MHz high-frequency (MCG_C2[RANGE]=01), high-gain mode (HGO=1)	—	1	—	ms	

1. Other frequency limits may apply when external clock is being used as a reference for the FLL or PLL.
2. When transitioning from FBE to FEI mode, restrict the frequency of the input clock so that, when it is divided by FRDIV, it remains within the limits of the DCO input clock frequency.
3. Proper PC board layout procedures must be followed to achieve specifications.

Table 21. Flash command timing specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	Swap Control execution time					
$t_{swapx01}$	• control code 0x01	—	200	—	µs	
$t_{swapx02}$	• control code 0x02	—	70	150	µs	
$t_{swapx04}$	• control code 0x04	—	70	150	µs	
$t_{swapx08}$	• control code 0x08	—	—	30	µs	

1. Assumes 25 MHz flash clock frequency.
2. Maximum times for erase parameters based on expectations at cycling end-of-life.

6.4.1.3 Flash high voltage current behaviors

Table 22. Flash high voltage current behaviors

Symbol	Description	Min.	Typ.	Max.	Unit
I_{DD_PGM}	Average current adder during high voltage flash programming operation	—	2.5	6.0	mA
I_{DD_ERS}	Average current adder during high voltage flash erase operation	—	1.5	4.0	mA

6.4.1.4 Reliability specifications

Table 23. NVM reliability specifications

Symbol	Description	Min.	Typ.[1]	Max.	Unit	Notes
	Program Flash					
$t_{nvmretp10k}$	Data retention after up to 10 K cycles	5	50	—	years	
$t_{nvmretp1k}$	Data retention after up to 1 K cycles	20	100	—	years	
$n_{nvmcycp}$	Cycling endurance	10 K	50 K	—	cycles	2

1. Typical data retention values are based on measured response accelerated at high temperature and derated to a constant 25°C use profile. Engineering Bulletin EB618 does not apply to this technology. Typical endurance defined in Engineering Bulletin EB619.
2. Cycling endurance represents number of program/erase cycles at -40°C ≤ T_j ≤ 125°C.

6.4.2 EzPort switching specifications

Table 24. EzPort switching specifications

Num	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
EP1	EZP_CK frequency of operation (all commands except READ)	—	$f_{SYS}/2$	MHz

Table continues on the next page...

Table 29. 16-bit ADC with PGA operating conditions (continued)

Symbol	Description	Conditions	Min.	Typ.[1]	Max.	Unit	Notes
C_{rate}	ADC conversion rate	≤ 13 bit modes No ADC hardware averaging Continuous conversions enabled Peripheral clock = 50 MHz	18.484	—	450	Ksps	7
		16 bit modes No ADC hardware averaging Continuous conversions enabled Peripheral clock = 50 MHz	37.037	—	250	Ksps	8

1. Typical values assume V_{DDA} = 3.0 V, Temp = 25°C, f_{ADCK} = 6 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
2. ADC must be configured to use the internal voltage reference (VREF_OUT)
3. PGA reference is internally connected to the VREF_OUT pin. If the user wishes to drive VREF_OUT with a voltage other than the output of the VREF module, the VREF module must be disabled.
4. For single ended configurations the input impedance of the driven input is $R_{PGAD}/2$
5. The analog source resistance (R_{AS}), external to MCU, should be kept as minimum as possible. Increased R_{AS} causes drop in PGA gain without affecting other performances. This is not dependent on ADC clock frequency.
6. The minimum sampling time is dependent on input signal frequency and ADC mode of operation. A minimum of 1.25µs time should be allowed for F_{in}=4 kHz at 16-bit differential mode. Recommended ADC setting is: ADLSMP=1, ADLSTS=2 at 8 MHz ADC clock.
7. ADC clock = 18 MHz, ADLSMP = 1, ADLST = 00, ADHSC = 1
8. ADC clock = 12 MHz, ADLSMP = 1, ADLST = 01, ADHSC = 1

6.6.1.4 16-bit ADC with PGA characteristics with Chop enabled (ADC_PGA[PGACHPb] =0)

Table 30. 16-bit ADC with PGA characteristics

Symbol	Description	Conditions	Min.	Typ.[1]	Max.	Unit	Notes
I_{DDA_PGA}	Supply current	Low power (ADC_PGA[PGALPb]=0)	—	420	644	µA	2
I_{DC_PGA}	Input DC current		$\frac{2}{R_{PGAD}}\left(\frac{(V_{REFPGA}\times 0.583)-V_{CM}}{(Gain+1)}\right)$			A	3
		Gain =1, V_{REFPGA}=1.2V, V_{CM}=0.5V	—	1.54	—	µA	
		Gain =64, V_{REFPGA}=1.2V, V_{CM}=0.1V	—	0.57	—	µA	

Table continues on the next page...

Table 31. Comparator and 6-bit DAC electrical specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit
V_H	Analog comparator hysteresis[1]				
	• CR0[HYSTCTR] = 00	—	5	—	mV
	• CR0[HYSTCTR] = 01	—	10	—	mV
	• CR0[HYSTCTR] = 10	—	20	—	mV
	• CR0[HYSTCTR] = 11	—	30	—	mV
V_{CMPOh}	Output high	V_{DD} – 0.5	—	—	V
V_{CMPOl}	Output low	—	—	0.5	V
t_{DHS}	Propagation delay, high-speed mode (EN=1, PMODE=1)	20	50	200	ns
t_{DLS}	Propagation delay, low-speed mode (EN=1, PMODE=0)	80	250	600	ns
	Analog comparator initialization delay[2]	—	—	40	µs
I_{DAC6b}	6-bit DAC current adder (enabled)	—	7	—	µA
INL	6-bit DAC integral non-linearity	–0.5	—	0.5	LSB[3]
DNL	6-bit DAC differential non-linearity	–0.3	—	0.3	LSB

1. Typical hysteresis is measured with input voltage range limited to 0.6 to V_{DD}-0.6 V.
2. Comparator initialization delay is defined as the time between software writes to change control inputs (Writes to DACEN, VRSEL, PSEL, MSEL, VOSEL) and the comparator output settling to a stable level.
3. 1 LSB = $V_{reference}$/64

6.6.3.2 12-bit DAC operating behaviors

Table 33. 12-bit DAC operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I_{DDA_DACLP}	Supply current — low-power mode	—	—	330	µA	
I_{DDA_DACHP}	Supply current — high-speed mode	—	—	1200	µA	
t_{DACLP}	Full-scale settling time (0x080 to 0xF7F) — low-power mode	—	100	200	µs	1
t_{DACHP}	Full-scale settling time (0x080 to 0xF7F) — high-power mode	—	15	30	µs	1
$t_{CCDACLP}$	Code-to-code settling time (0xBF8 to 0xC08) — low-power mode and high-speed mode	—	0.7	1	µs	1
$V_{dacoutl}$	DAC output voltage range low — high-speed mode, no load, DAC set to 0x000	—	—	100	mV	
$V_{dacouth}$	DAC output voltage range high — high-speed mode, no load, DAC set to 0xFFF	V_{DACR} −100	—	V_{DACR}	mV	
INL	Integral non-linearity error — high speed mode	—	—	±8	LSB	2
DNL	Differential non-linearity error — V_{DACR} > 2 V	—	—	±1	LSB	3
DNL	Differential non-linearity error — V_{DACR} = VREF_OUT	—	—	±1	LSB	4
V_{OFFSET}	Offset error	—	±0.4	±0.8	%FSR	5
E_G	Gain error	—	±0.1	±0.6	%FSR	5
PSRR	Power supply rejection ratio, V_{DDA} > = 2.4 V	60	—	90	dB	
T_{CO}	Temperature coefficient offset voltage	—	3.7	—	µV/C	6
T_{GE}	Temperature coefficient gain error	—	0.000421	—	%FSR/C	
Rop	Output resistance load = 3 kΩ	—	—	250	Ω	
SR	Slew rate -80h→ F7Fh→ 80h				V/µs	
	• High power (SP_{HP})	1.2	1.7	—		
	• Low power (SP_{LP})	0.05	0.12	—		
CT	Channel to channel cross talk	—	—	-80	dB	
BW	3dB bandwidth				kHz	
	• High power (SP_{HP})	550	—	—		
	• Low power (SP_{LP})	40	—	—		

1. Settling within ±1 LSB
2. The INL is measured for 0+100mV to V_{DACR}−100 mV
3. The DNL is measured for 0+100 mV to V_{DACR}−100 mV
4. The DNL is measured for 0+100mV to V_{DACR}−100 mV with V_{DDA} > 2.4V
5. Calculated by a best fit curve from V_{SS}+100 mV to V_{DACR}−100 mV
6. VDDA = 3.0V, reference select set for VDDA (DACx_CO:DACRFS = 1), high power mode(DACx_C0:LPEN = 0), DAC set to 0x800, Temp range from -40C to 105C

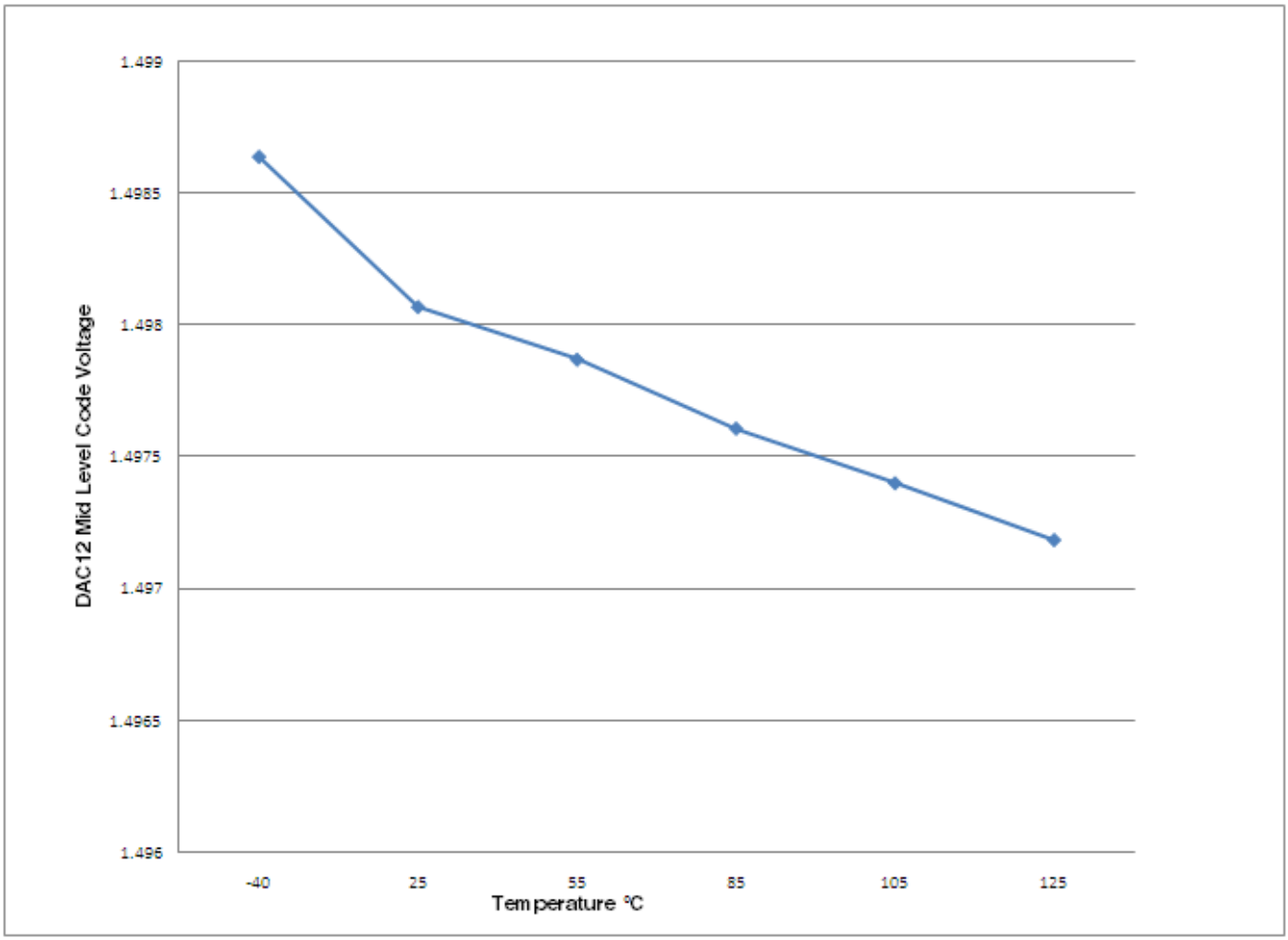

Figure 18. Offset at half scale vs. temperature

6.6.4 Op-amp electrical specifications

Table 34. Op-amp electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit
V_{DD}	Operating voltage	1.71	—	3.6	V
I_{SUPPLY}	Supply current (I_{OUT}=0mA, CL=0), low-power mode	—	92	195	µA
I_{SUPPLY}	Supply current (I_{OUT}=0mA, CL=0), high-speed mode	—	465	865	µA
V_{OS}	Input offset voltage	—	±3	±10	mV
α_{VOS}	Input offset voltage temperature coefficient	—	10	—	µV/C
I_{OS}	Typical input offset current across the following temp range (0–50°C)	—	±500	—	pA
I_{OS}	Typical input offset current across the following temp range (-40–105°C)	—	4	—	nA

Table continues on the next page...

6.8.2 USB DCD electrical specifications

Table 43. USB DCD electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit
V_{DP_SRC}	USB_DP source voltage (up to 250 µA)	0.5	—	0.7	V
V_{LGC}	Threshold voltage for logic high	0.8	—	2.0	V
I_{DP_SRC}	USB_DP source current	7	10	13	µA
I_{DM_SINK}	USB_DM sink current	50	100	150	µA
R_{DM_DWN}	D- pulldown resistance for data pin contact detect	14.25	—	24.8	kΩ
V_{DAT_REF}	Data detect voltage	0.25	0.33	0.4	V

6.8.3 USB VREG electrical specifications

Table 44. USB VREG electrical specifications

Symbol	Description	Min.	Typ.[1]	Max.	Unit	Notes
VREGIN	Input supply voltage	2.7	—	5.5	V	
I_{DDon}	Quiescent current — Run mode, load current equal zero, input supply (VREGIN) > 3.6 V	—	120	186	µA	
I_{DDstby}	Quiescent current — Standby mode, load current equal zero	—	1.1	10	µA	
I_{DDoff}	Quiescent current — Shutdown mode • VREGIN = 5.0 V and temperature=25 °C • Across operating voltage and temperature	— —	650 —	— 4	nA µA	
$I_{LOADrun}$	Maximum load current — Run mode	—	—	120	mA	
$I_{LOADstby}$	Maximum load current — Standby mode	—	—	1	mA	
$V_{Reg33out}$	Regulator output voltage — Input supply (VREGIN) > 3.6 V • Run mode • Standby mode	 3 2.1	 3.3 2.8	 3.6 3.6	 V V	
$V_{Reg33out}$	Regulator output voltage — Input supply (VREGIN) < 3.6 V, pass-through mode	2.1	—	3.6	V	2
C_{OUT}	External output capacitor	1.76	2.2	8.16	µF	
ESR	External output capacitor equivalent series resistance	1	—	100	mΩ	
I_{LIM}	Short circuit current	—	290	—	mA	

1. Typical values assume VREGIN = 5.0 V, Temp = 25 °C unless otherwise stated.
2. Operating in pass-through mode: regulator output voltage equal to the input voltage minus a drop proportional to I_{Load}.

6.8.4 DSPI switching specifications (limited voltage range)

The DMA Serial Peripheral Interface (DSPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The tables below provide DSPI timing characteristics for classic SPI timing modes. Refer to the DSPI chapter of the Reference Manual for information on the modified transfer formats used for communicating with slower peripheral devices.

Table 45. Master mode DSPI timing (limited voltage range)

Num	Description	Min.	Max.	Unit	Notes
	Operating voltage	2.7	3.6	V	
	Frequency of operation	—	25	MHz	
DS1	DSPI_SCK output cycle time	2 x t_{BUS}	—	ns	
DS2	DSPI_SCK output high/low time	(t_{SCK}/2) – 2	(t_{SCK}/2) + 2	ns	
DS3	DSPI_PCS*n* valid to DSPI_SCK delay	(t_{BUS} x 2) – 2	—	ns	1
DS4	DSPI_SCK to DSPI_PCS*n* invalid delay	(t_{BUS} x 2) – 2	—	ns	2
DS5	DSPI_SCK to DSPI_SOUT valid	—	8	ns	
DS6	DSPI_SCK to DSPI_SOUT invalid	0	—	ns	
DS7	DSPI_SIN to DSPI_SCK input setup	14	—	ns	
DS8	DSPI_SCK to DSPI_SIN input hold	0	—	ns	

1. The delay is programmable in SPIx_CTARn[PSSCK] and SPIx_CTARn[CSSCK].
2. The delay is programmable in SPIx_CTARn[PASC] and SPIx_CTARn[ASC].

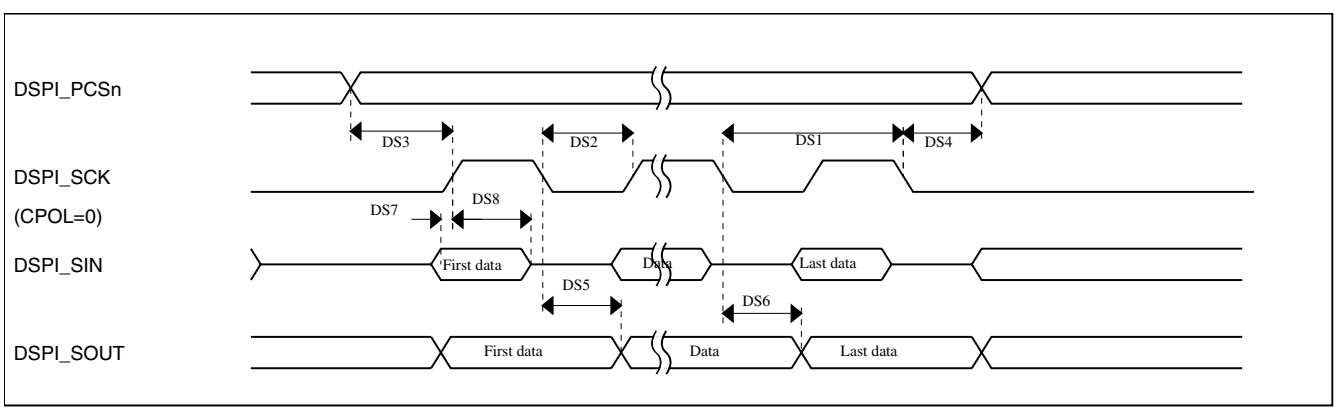

Figure 19. DSPI classic SPI timing — master mode

Table 46. Slave mode DSPI timing (limited voltage range)

Num	Description	Min.	Max.	Unit
	Operating voltage	2.7	3.6	V
	Frequency of operation		12.5	MHz
DS9	DSPI_SCK input cycle time	4 x t_{BUS}	—	ns

Table continues on the next page...

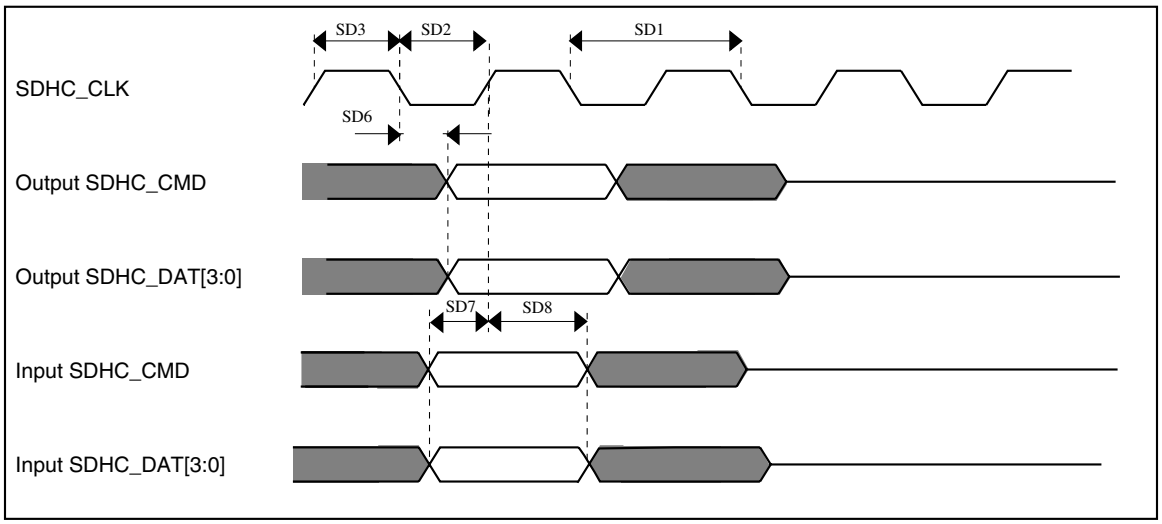

Figure 24. SDHC timing

6.8.9 I2S/SAI switching specifications

This section provides the AC timing for the I2S/SAI module in master mode (clocks are driven) and slave mode (clocks are input). All timing is given for noninverted serial clock polarity (TCR2[BCP] is 0, RCR2[BCP] is 0) and a noninverted frame sync (TCR4[FSP] is 0, RCR4[FSP] is 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the bit clock signal (BCLK) and/or the frame sync (FS) signal shown in the following figures.

6.8.9.1 Normal Run, Wait and Stop mode performance over a limited operating voltage range

This section provides the operating performance over a limited operating voltage for the device in Normal Run, Wait and Stop modes.

Table 51. I2S/SAI master mode timing in Normal Run, Wait and Stop modes (limited voltage range)

Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	2.7	3.6	V
S1	I2S_MCLK cycle time	40	—	ns
S2	I2S_MCLK pulse width high/low	45%	55%	MCLK period
S3	I2S_TX_BCLK/I2S_RX_BCLK cycle time (output)	80	—	ns
S4	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low	45%	55%	BCLK period
S5	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output valid	—	15	ns

Table continues on the next page...

Table 53. I2S/SAI master mode timing in Normal Run, Wait and Stop modes (full voltage range) (continued)

Num.	Characteristic	Min.	Max.	Unit
S7	I2S_TX_BCLK to I2S_TXD valid	—	15	ns
S8	I2S_TX_BCLK to I2S_TXD invalid	0	—	ns
S9	I2S_RXD/I2S_RX_FS input setup before I2S_RX_BCLK	20.5	—	ns
S10	I2S_RXD/I2S_RX_FS input hold after I2S_RX_BCLK	0	—	ns

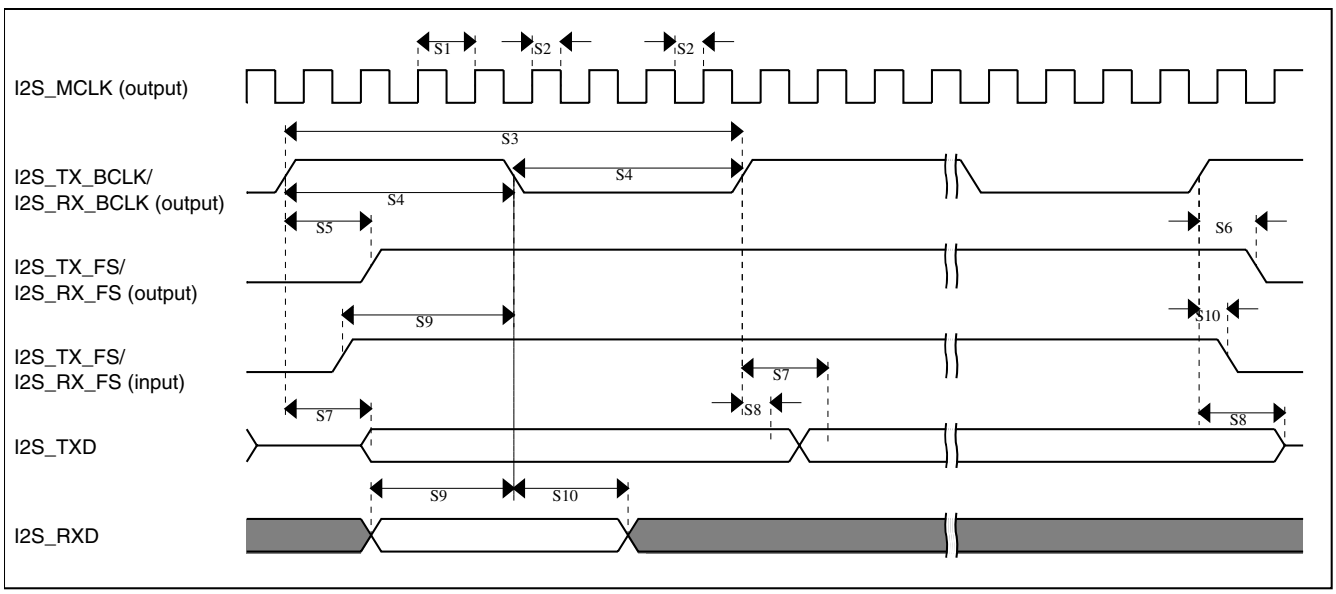

Figure 27. I2S/SAI timing — master modes

Table 54. I2S/SAI slave mode timing in Normal Run, Wait and Stop modes (full voltage range)

Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S11	I2S_TX_BCLK/I2S_RX_BCLK cycle time (input)	80	—	ns
S12	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low (input)	45%	55%	MCLK period
S13	I2S_TX_FS/I2S_RX_FS input setup before I2S_TX_BCLK/I2S_RX_BCLK	5.8	—	ns
S14	I2S_TX_FS/I2S_RX_FS input hold after I2S_TX_BCLK/I2S_RX_BCLK	2	—	ns
S15	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output valid • Multiple SAI Synchronous mode • All other modes	 — —	 24 20.6	ns
S16	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output invalid	0	—	ns

Table continues on the next page...

8.1 K50 signal multiplexing and pin assignments

The following table shows the signals available on each pin and the locations of these pins on the devices supported by this document. The Port Control Module is responsible for selecting which ALT functionality is available on each pin.

144 LQFP	144 MAP BGA	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
—	C10	NC	NC	NC								
—	B10	NC	NC	NC								
—	A10	NC	NC	NC								
1	D3	PTE0	ADC1_SE4a	ADC1_SE4a	PTE0	SPI1_PCS1	UART1_TX	SDHC0_D1		I2C1_SDA	RTC_CLKOUT	
2	D2	PTE1/ LLWU_P0	ADC1_SE5a	ADC1_SE5a	PTE1/ LLWU_P0	SPI1_SOUT	UART1_RX	SDHC0_D0		I2C1_SCL	SPI1_SIN	
3	D1	PTE2/ LLWU_P1	ADC1_SE6a	ADC1_SE6a	PTE2/ LLWU_P1	SPI1_SCK	UART1_CTS_ b	SDHC0_DCLK				
4	E4	PTE3	ADC1_SE7a	ADC1_SE7a	PTE3	SPI1_SIN	UART1_RTS_ b	SDHC0_CMD			SPI1_SOUT	
5	E5	VDD	VDD	VDD								
6	F6	VSS	VSS	VSS								
7	E3	PTE4/ LLWU_P2	DISABLED		PTE4/ LLWU_P2	SPI1_PCS0	UART3_TX	SDHC0_D3				
8	E2	PTE5	DISABLED		PTE5	SPI1_PCS2	UART3_RX	SDHC0_D2				
9	E1	PTE6	DISABLED		PTE6	SPI1_PCS3	UART3_CTS_ b	I2S0_MCLK			USB_SOF_ OUT	
10	F4	PTE7	DISABLED		PTE7		UART3_RTS_ b	I2S0_RXD0				
11	F3	PTE8	DISABLED		PTE8	I2S0_RXD1	UART5_TX	I2S0_RX_FS				
12	F2	PTE9	DISABLED		PTE9	I2S0_TXD1	UART5_RX	I2S0_RX_ BCLK				
13	F1	PTE10	DISABLED		PTE10		UART5_CTS_ b	I2S0_TXD0				
14	G4	PTE11	DISABLED		PTE11		UART5_RTS_ b	I2S0_TX_FS				
15	G3	PTE12	DISABLED		PTE12			I2S0_TX_ BCLK				
16	E6	VDD	VDD	VDD								
17	F7	VSS	VSS	VSS								
18	H3	VSS	VSS	VSS								
19	H1	USB0_DP	USB0_DP	USB0_DP								
20	H2	USB0_DM	USB0_DM	USB0_DM								
21	G1	VOUT33	VOUT33	VOUT33								
22	G2	VREGIN	VREGIN	VREGIN								
23	J1	ADC0_DP1/ OP0_DP0	ADC0_DP1/ OP0_DP0	ADC0_DP1/ OP0_DP0								

144 LQFP	144 MAP BGA	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
24	J2	ADC0_DM1/ OP0_DM0	ADC0_DM1/ OP0_DM0	ADC0_DM1/ OP0_DM0								
25	K1	ADC1_DP1/ OP1_DP0/ OP1_DM1	ADC1_DP1/ OP1_DP0/ OP1_DM1	ADC1_DP1/ OP1_DP0/ OP1_DM1								
26	K2	ADC1_DM1/ OP1_DM0	ADC1_DM1/ OP1_DM0	ADC1_DM1/ OP1_DM0								
27	L1	PGA0_DP/ ADC0_DP0/ ADC1_DP3	PGA0_DP/ ADC0_DP0/ ADC1_DP3	PGA0_DP/ ADC0_DP0/ ADC1_DP3								
28	L2	PGA0_DM/ ADC0_DM0/ ADC1_DM3	PGA0_DM/ ADC0_DM0/ ADC1_DM3	PGA0_DM/ ADC0_DM0/ ADC1_DM3								
29	M1	PGA1_DP/ ADC1_DP0/ ADC0_DP3	PGA1_DP/ ADC1_DP0/ ADC0_DP3	PGA1_DP/ ADC1_DP0/ ADC0_DP3								
30	M2	PGA1_DM/ ADC1_DM0/ ADC0_DM3	PGA1_DM/ ADC1_DM0/ ADC0_DM3	PGA1_DM/ ADC1_DM0/ ADC0_DM3								
31	H5	VDDA	VDDA	VDDA								
32	G5	VREFH	VREFH	VREFH								
33	G6	VREFL	VREFL	VREFL								
34	H6	VSSA	VSSA	VSSA								
35	K3	ADC1_SE16/ OP1_OUT/ CMP2_IN2/ ADC0_SE22/ OP0_DP2/ OP1_DP2	ADC1_SE16/ OP1_OUT/ CMP2_IN2/ ADC0_SE22/ OP0_DP2/ OP1_DP2	ADC1_SE16/ OP1_OUT/ CMP2_IN2/ ADC0_SE22/ OP0_DP2/ OP1_DP2								
36	J3	ADC0_SE16/ OP0_OUT/ CMP1_IN2/ ADC0_SE21/ OP0_DP1/ OP1_DP1	ADC0_SE16/ OP0_OUT/ CMP1_IN2/ ADC0_SE21/ OP0_DP1/ OP1_DP1	ADC0_SE16/ OP0_OUT/ CMP1_IN2/ ADC0_SE21/ OP0_DP1/ OP1_DP1								
37	M3	VREF_OUT/ CMP1_IN5/ CMP0_IN5/ ADC1_SE18	VREF_OUT/ CMP1_IN5/ CMP0_IN5/ ADC1_SE18	VREF_OUT/ CMP1_IN5/ CMP0_IN5/ ADC1_SE18								
38	L3	TRI0_OUT/ OP1_DM2	TRI0_OUT/ OP1_DM2	TRI0_OUT/ OP1_DM2								
39	L4	TRI0_DM	TRI0_DM	TRI0_DM								
40	M4	TRI0_DP	TRI0_DP	TRI0_DP								
41	L5	TRI1_DM	TRI1_DM	TRI1_DM								
42	M5	TRI1_DP	TRI1_DP	TRI1_DP								
43	K5	TRI1_OUT/ CMP2_IN5/ ADC1_SE22	TRI1_OUT/ CMP2_IN5/ ADC1_SE22	TRI1_OUT/ CMP2_IN5/ ADC1_SE22								

144 LQFP	144 MAP BGA	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
66	L10	PTA14	DISABLED		PTA14	SPI0_PCS0	UART0_TX			I2S0_RX_BCLK	I2S0_TXD1	
67	L11	PTA15	DISABLED		PTA15	SPI0_SCK	UART0_RX			I2S0_RXD0		
68	K10	PTA16	DISABLED		PTA16	SPI0_SOUT	UART0_CTS_b/ UART0_COL_b			I2S0_RX_FS	I2S0_RXD1	
69	K11	PTA17	ADC1_SE17	ADC1_SE17	PTA17	SPI0_SIN	UART0_RTS_b			I2S0_MCLK		
70	E8	VDD	VDD	VDD								
71	G8	VSS	VSS	VSS								
72	M12	PTA18	EXTAL0	EXTAL0	PTA18		FTM0_FLT2	FTM_CLKIN0				
73	M11	PTA19	XTAL0	XTAL0	PTA19		FTM1_FLT0	FTM_CLKIN1		LPTMR0_ALT1		
74	L12	RESET_b	RESET_b	RESET_b								
75	K12	PTA24	DISABLED		PTA24					FB_A29		
76	J12	PTA25	DISABLED		PTA25					FB_A28		
77	J11	PTA26	DISABLED		PTA26					FB_A27		
78	J10	PTA27	DISABLED		PTA27					FB_A26		
79	H12	PTA28	DISABLED		PTA28					FB_A25		
80	H11	PTA29	DISABLED		PTA29					FB_A24		
81	H10	PTB0/ LLWU_P5	ADC0_SE8/ ADC1_SE8/ TSI0_CH0	ADC0_SE8/ ADC1_SE8/ TSI0_CH0	PTB0/ LLWU_P5	I2C0_SCL	FTM1_CH0			FTM1_QD_PHA		
82	H9	PTB1	ADC0_SE9/ ADC1_SE9/ TSI0_CH6	ADC0_SE9/ ADC1_SE9/ TSI0_CH6	PTB1	I2C0_SDA	FTM1_CH1			FTM1_QD_PHB		
83	G12	PTB2	ADC0_SE12/ TSI0_CH7	ADC0_SE12/ TSI0_CH7	PTB2	I2C0_SCL	UART0_RTS_b			FTM0_FLT3		
84	G11	PTB3	ADC0_SE13/ TSI0_CH8	ADC0_SE13/ TSI0_CH8	PTB3	I2C0_SDA	UART0_CTS_b/ UART0_COL_b			FTM0_FLT0		
85	G10	PTB4	ADC1_SE10	ADC1_SE10	PTB4					FTM1_FLT0		
86	G9	PTB5	ADC1_SE11	ADC1_SE11	PTB5					FTM2_FLT0		
87	F12	PTB6	ADC1_SE12	ADC1_SE12	PTB6				FB_AD23			
88	F11	PTB7	ADC1_SE13	ADC1_SE13	PTB7				FB_AD22			
89	F10	PTB8	DISABLED		PTB8		UART3_RTS_b		FB_AD21			
90	F9	PTB9	DISABLED		PTB9	SPI1_PCS1	UART3_CTS_b		FB_AD20			
91	E12	PTB10	ADC1_SE14	ADC1_SE14	PTB10	SPI1_PCS0	UART3_RX		FB_AD19	FTM0_FLT1		
92	E11	PTB11	ADC1_SE15	ADC1_SE15	PTB11	SPI1_SCK	UART3_TX		FB_AD18	FTM0_FLT2		
93	H7	VSS	VSS	VSS								
94	F5	VDD	VDD	VDD								

144 LQFP	144 MAP BGA	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
95	E10	PTB16	TSI0_CH9	TSI0_CH9	PTB16	SPI1_SOUT	UART0_RX		FB_AD17	EWM_IN		
96	E9	PTB17	TSI0_CH10	TSI0_CH10	PTB17	SPI1_SIN	UART0_TX		FB_AD16	EWM_OUT_b		
97	D12	PTB18	TSI0_CH11	TSI0_CH11	PTB18		FTM2_CH0	I2S0_TX_BCLK	FB_AD15	FTM2_QD_PHA		
98	D11	PTB19	TSI0_CH12	TSI0_CH12	PTB19		FTM2_CH1	I2S0_TX_FS	FB_OE_b	FTM2_QD_PHB		
99	D10	PTB20	DISABLED		PTB20	SPI2_PCS0			FB_AD31	CMP0_OUT		
100	D9	PTB21	DISABLED		PTB21	SPI2_SCK			FB_AD30	CMP1_OUT		
101	C12	PTB22	DISABLED		PTB22	SPI2_SOUT			FB_AD29	CMP2_OUT		
102	C11	PTB23	DISABLED		PTB23	SPI2_SIN	SPI0_PCS5		FB_AD28			
103	B12	PTC0	ADC0_SE14/ TSI0_CH13	ADC0_SE14/ TSI0_CH13	PTC0	SPI0_PCS4	PDB0_EXTRG		FB_AD14	I2S0_TXD1		
104	B11	PTC1/ LLWU_P6	ADC0_SE15/ TSI0_CH14	ADC0_SE15/ TSI0_CH14	PTC1/ LLWU_P6	SPI0_PCS3	UART1_RTS_b	FTM0_CH0	FB_AD13	I2S0_TXD0		
105	A12	PTC2	ADC0_SE4b/ CMP1_IN0/ TSI0_CH15	ADC0_SE4b/ CMP1_IN0/ TSI0_CH15	PTC2	SPI0_PCS2	UART1_CTS_b	FTM0_CH1	FB_AD12	I2S0_TX_FS		
106	A11	PTC3/ LLWU_P7	CMP1_IN1	CMP1_IN1	PTC3/ LLWU_P7	SPI0_PCS1	UART1_RX	FTM0_CH2	CLKOUT	I2S0_TX_BCLK		
107	H8	VSS	VSS	VSS								
108	—	VDD	VDD	VDD								
109	A9	PTC4/ LLWU_P8	DISABLED		PTC4/ LLWU_P8	SPI0_PCS0	UART1_TX	FTM0_CH3	FB_AD11	CMP1_OUT		
110	D8	PTC5/ LLWU_P9	DISABLED		PTC5/ LLWU_P9	SPI0_SCK	LPTMR0_ALT2	I2S0_RXD0	FB_AD10	CMP0_OUT		
111	C8	PTC6/ LLWU_P10	CMP0_IN0	CMP0_IN0	PTC6/ LLWU_P10	SPI0_SOUT	PDB0_EXTRG	I2S0_RX_BCLK	FB_AD9	I2S0_MCLK		
112	B8	PTC7	CMP0_IN1	CMP0_IN1	PTC7	SPI0_SIN	USB_SOF_OUT	I2S0_RX_FS	FB_AD8			
113	A8	PTC8	ADC1_SE4b/ CMP0_IN2	ADC1_SE4b/ CMP0_IN2	PTC8			I2S0_MCLK	FB_AD7			
114	D7	PTC9	ADC1_SE5b/ CMP0_IN3	ADC1_SE5b/ CMP0_IN3	PTC9			I2S0_RX_BCLK	FB_AD6	FTM2_FLT0		
115	C7	PTC10	ADC1_SE6b	ADC1_SE6b	PTC10	I2C1_SCL		I2S0_RX_FS	FB_AD5			
116	B7	PTC11/ LLWU_P11	ADC1_SE7b	ADC1_SE7b	PTC11/ LLWU_P11	I2C1_SDA		I2S0_RXD1	FB_RW_b			
117	A7	PTC12	DISABLED		PTC12		UART4_RTS_b		FB_AD27			
118	D6	PTC13	DISABLED		PTC13		UART4_CTS_b		FB_AD26			
119	C6	PTC14	DISABLED		PTC14		UART4_RX		FB_AD25			
120	B6	PTC15	DISABLED		PTC15		UART4_TX		FB_AD24			
121	—	VSS	VSS	VSS								
122	—	VDD	VDD	VDD								

Table 58. Revision history (continued)

Rev. No.	Date	Substantial Changes
2	12/2012	Replaced TBDs throughout.
3	6/2013	• In ESD handling ratings, added a note for ILAT. • Updated "Voltage and current operating requirements" Table 1. • Updated I_{OL} data for V_{OL} row in "Voltage and current operating behaviors" Table 4. • Updated wakeup times and t_{POR} value in "Power mode transition operating behaviors" Table 5. • In "EMC radiated emissions operating behaviors . . ." Table 7, added a column for 144MAPBGA. • In "16-bit ADC operating conditions" Table 27, updated the max spec of VADIN. • In "16-bit ADC electrical characteristics" Table 28, updated the temp sensor slope and voltage specs. • Updated Inter-Integrated Circuit Interface (I^2C) timing. • In SDHC specifications, added operating voltage row.