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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z0h
Core Size	32-Bit Single-Core
Speed	64MHz
Connectivity	CANbus, LINbus, SPI, UART/USART
Peripherals	DMA, POR, PWM, WDT
Number of I/O	67
Program Memory Size	384KB (384K x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	36K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 26x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/spc560p44l3beaay

List of figures

Table 4. SPC560P44Lx, SPC560P50Lx series block summary

Block	Function
Analog-to-digital converter (ADC)	Multi-channel, 10-bit analog-to-digital converter
Boot assist module (BAM)	Block of read-only memory containing VLE code which is executed according to the boot mode of the device
Clock generation module (MC_CGM)	Provides logic and control required for the generation of system and peripheral clocks
Controller area network (FlexCAN)	Supports the standard CAN communications protocol
Cross triggering unit (CTU)	Enables synchronization of ADC conversions with a timer event from the eMIOS or from the PIT
Crossbar switch (XBAR)	Supports simultaneous connections between two master ports and three slave ports; supports a 32-bit address bus width and a 32-bit data bus width
Cyclic redundancy check (CRC)	CRC checksum generator
Deserial serial peripheral interface (DSPI)	Provides a synchronous serial interface for communication with external devices
Enhanced direct memory access (eDMA)	Performs complex data transfers with minimal intervention from a host processor via "*n*" programmable channels
Enhanced timer (eTimer)	Provides enhanced programmable up/down modulo counting
Error correction status module (ECSM)	Provides a myriad of miscellaneous control functions for the device including program-visible information about configuration and revision levels, a reset status register, wakeup control for exiting sleep modes, and optional features such as information on memory errors reported by error-correcting codes
External oscillator (XOSC)	Provides an output clock used as input reference for FMPLL_0 or as reference clock for specific modules depending on system needs
Fault collection unit (FCU)	Provides functional safety to the device
Flash memory	Provides non-volatile storage for program code, constants and variables
Frequency-modulated phase-locked loop (FMPLL)	Generates high-speed system clocks and supports programmable frequency modulation
Interrupt controller (INTC)	Provides priority-based preemptive scheduling of interrupt requests
JTAG controller	Provides the means to test chip functionality and connectivity while remaining transparent to system logic when not in test mode
LINFlex controller	Manages a high number of LIN (Local Interconnect Network protocol) messages efficiently with minimum load on CPU
Mode entry module (MC_ME)	Provides a mechanism for controlling the device operational mode and mode transition sequences in all functional states; also manages the power control unit, reset generation module and clock generation module, and holds the configuration, control and status registers accessible for applications
Periodic interrupt timer (PIT)	Produces periodic interrupts and triggers
Peripheral bridge (PBRIDGE)	Interface between the system bus and on-chip peripherals
Power control unit (MC_PCU)	Reduces the overall power consumption by disconnecting parts of the device from the power supply via a power switching device; device components are grouped into sections called "power domains" which are controlled by the PCU

1.5.13 System timer module (STM)

The STM module implements these features:

- One 32-bit up counter with 8-bit prescaler
- Four 32-bit compare channels
- Independent interrupt source for each channel
- Counter can be stopped in debug mode

1.5.14 Software watchdog timer (SWT)

The SWT has the following features:

- 32-bit time-out register to set the time-out period
- Programmable selection of system or oscillator clock for timer operation
- Programmable selection of window mode or regular servicing
- Programmable selection of reset or interrupt on an initial time-out
- Master access protection
- Hard and soft configuration lock bits
- Reset configuration inputs allow timer to be enabled out of reset

1.5.15 Fault collection unit (FCU)

The FCU provides an independent fault reporting mechanism even if the CPU is malfunctioning.

The FCU module has the following features:

- FCU status register reporting the device status
- Continuous monitoring of critical fault signals
- User selection of critical signals from different fault sources inside the device
- Critical fault events trigger 2 external pins (user selected signal protocol) that can be used externally to reset the device and/or other circuitry (for example, safety relay or FlexRay transceiver)
- Faults are latched into a register

1.5.16 System integration unit – Lite (SIUL)

The SPC560P44Lx, SPC560P50Lx SIUL controls MCU pad configuration, external interrupt, general purpose I/O (GPIO), and internal peripheral multiplexing.

The pad configuration block controls the static electrical characteristics of I/O pins. The GPIO block provides uniform and discrete input/output control of the I/O pins of the MCU.

1.5.22 FlexRay

The FlexRay module provides the following features:

- Full implementation of FlexRay Protocol Specification 2.1
- 32 configurable message buffers can be handled
- Dual channel or single channel mode of operation, each as fast as 10 Mbit/s data rate
- Message buffers configurable as Tx, Rx or RxFIFO
- Message buffer size configurable
- Message filtering for all message buffers based on FrameID, cycle count and message ID
- Programmable acceptance filters for RxFIFO message buffers

1.5.23 Serial communication interface module (LINFlex)

The LINFlex (local interconnect network flexible) on the SPC560P44Lx, SPC560P50Lx features the following:

- Supports LIN Master mode, LIN Slave mode and UART mode
- LIN state machine compliant to LIN1.3, 2.0, and 2.1 specifications
- Handles LIN frame transmission and reception without CPU intervention
- LIN features
  - Autonomous LIN frame handling
  - Message buffer to store Identifier and as much as 8 data bytes
  - Supports message length as long as 64 bytes
  - Detection and flagging of LIN errors (sync field, delimiter, ID parity, bit framing, checksum, and time-out)
  - Classic or extended checksum calculation
  - Configurable Break duration as long as 36-bit times
  - Programmable baud rate prescalers (13-bit mantissa, 4-bit fractional)
  - Diagnostic features: Loop back; Self Test; LIN bus stuck dominant detection
  - Interrupt-driven operation with 16 interrupt sources
- LIN slave mode features
  - Autonomous LIN header handling
  - Autonomous LIN response handling
- UART mode
  - Full-duplex operation
  - Standard non return-to-zero (NRZ) mark/space format
  - Data buffers with 4-byte receive, 4-byte transmit
  - Configurable word length (8-bit or 9-bit words)
  - Error detection and flagging
  - Parity, Noise and Framing errors
  - Interrupt-driven operation with four interrupt sources
  - Separate transmitter and receiver CPU interrupt sources
  - 16-bit programmable baud-rate modulus counter and 16-bit fractional
  - 2 receiver wake-up methods

Digital part:

- 2 × 13 input channels including 4 channels shared between the 2 converters
- 4 analog watchdogs comparing ADC results against predefined levels (low, high, range) before results are stored in the appropriate ADC result location,
- 2 modes of operation: Normal mode or CTU control mode
- Normal mode features
  - Register-based interface with the CPU: control register, status register, 1 result register per channel
  - ADC state machine managing 3 request flows: regular command, hardware injected command, software injected command
  - Selectable priority between software and hardware injected commands
  - 4 analog watchdogs comparing ADC results against predefined levels (low, high, range)
  - DMA compatible interface
- CTU control mode features
  - Triggered mode only
  - 4 independent result queues (2 × 16 entries, 2 × 4 entries)
  - Result alignment circuitry (left justified; right justified)
  - 32-bit read mode allows to have channel ID on one of the 16-bit part
  - DMA compatible interfaces

1.5.28 Cross triggering unit (CTU)

The cross triggering unit allows automatic generation of ADC conversion requests on user selected conditions without CPU load during the PWM period and with minimized CPU load for dynamic configuration.

It implements the following features:

- Double buffered trigger generation unit with as many as eight independent triggers generated from external triggers
- Trigger generation unit configurable in sequential mode or in triggered mode
- Each Trigger can be appropriately delayed to compensate the delay of external low pass filter
- Double buffered global trigger unit allowing eTimer synchronization and/or ADC command generation
- Double buffered ADC command list pointers to minimize ADC-trigger unit update
- Double buffered ADC conversion command list with as many as 24 ADC commands
- Each trigger has the capability to generate consecutive commands
- ADC conversion command allows to control ADC channel from each ADC, single or synchronous sampling, independent result queue selection

1.5.29 Nexus development interface (NDI)

The NDI (Nexus Development Interface) block provides real-time development support capabilities for the SPC560P44Lx, SPC560P50Lx Power Architecture based MCU in compliance with the IEEE-ISTO 5001-2003 standard. This development support is supplied for MCUs without requiring external address and data pins for internal visibility. The NDI

block is an integration of several individual Nexus blocks that are selected to provide the development support interface for this device. The NDI block interfaces to the host processor and internal busses to provide development support as per the IEEE-ISTO 5001-2003 Class 2+ standard. The development support provided includes access to the MCU's internal memory map and access to the processor's internal registers during run time.

The Nexus Interface provides the following features:

- Configured via the IEEE 1149.1
- All Nexus port pins operate at V_{DDIO} (no dedicated power supply)
- Nexus 2+ features supported
  - Static debug
  - Watchpoint messaging
  - Ownership trace messaging
  - Program trace messaging
  - Real time read/write of any internally memory mapped resources through JTAG pins
  - Overrun control, which selects whether to stall before Nexus overruns or keep executing and allow overwrite of information
  - Watchpoint triggering, watchpoint triggers program tracing
- Auxiliary Output Port
  - 4 MDO (Message Data Out) pins
  - MCKO (Message Clock Out) pin
  - 2 $\overline{\text{MSEO}}$ (Message Start/End Out) pins
  - $\overline{\text{EVTO}}$ (Event Out) pin
- Auxiliary Input Port
  - $\overline{\text{EVTI}}$ (Event In) pin

1.5.30 Cyclic redundancy check (CRC)

The CRC computing unit is dedicated to the computation of CRC off-loading the CPU. The CRC module features:

- Support for CRC-16-CCITT (*x*25 protocol):
  - $x^{16} + x^{12} + x^5 + 1$
- Support for CRC-32 (Ethernet protocol):
  - $x^{32} + x^{26} + x^{23} + x^{22} + x^{16} + x^{12} + x^{11} + x^{10} + x^8 + x^7 + x^5 + x^4 + x^2 + x + 1$
- Zero wait states for each write/read operations to the CRC_CFG and CRC_INP registers at the maximum frequency

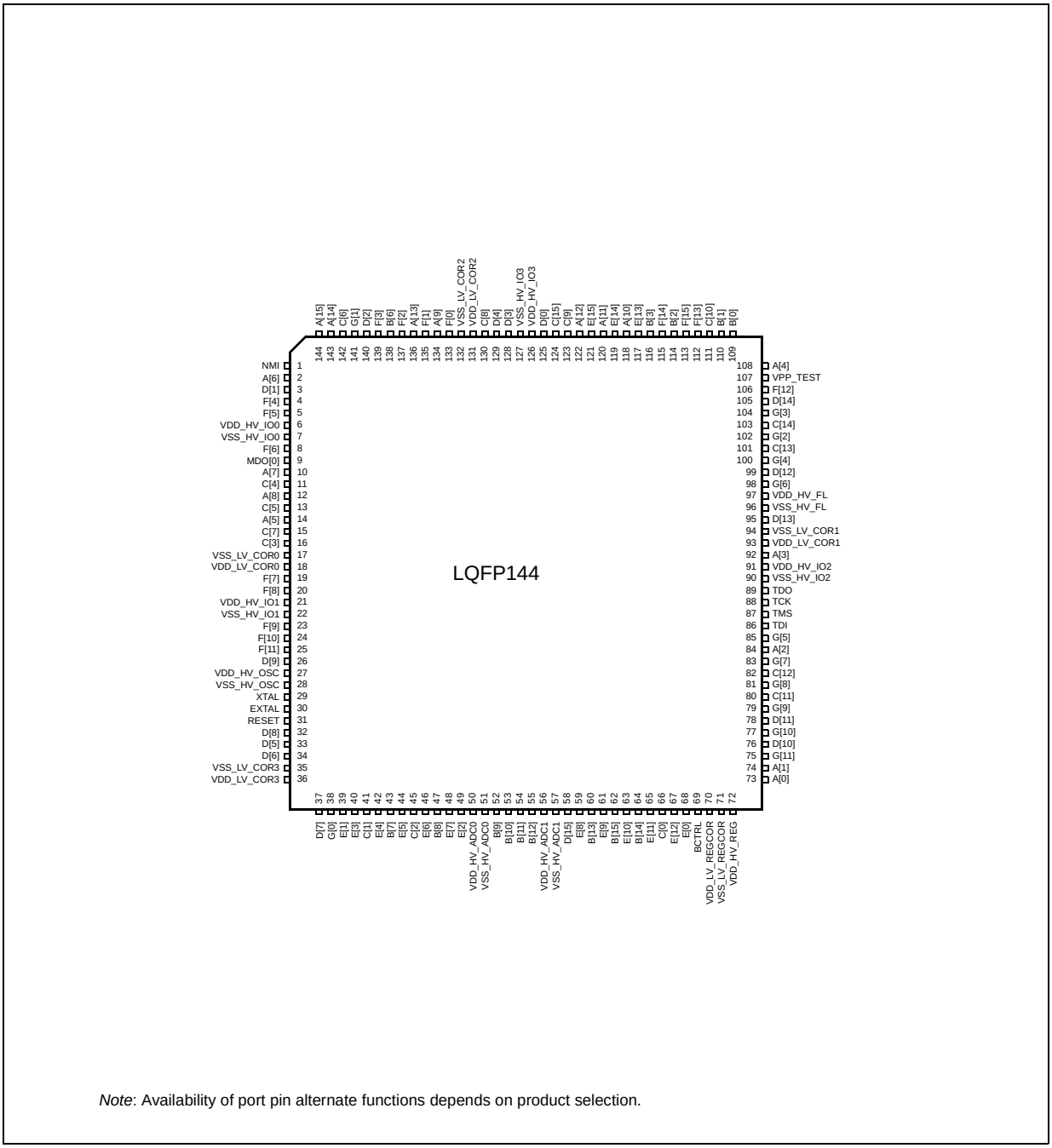
1.5.31 IEEE 1149.1 JTAG controller

The JTAG controller (JTAGC) block provides the means to test chip functionality and connectivity while remaining transparent to system logic when not in test mode. All data input to and output from the JTAGC block is communicated in serial format. The JTAGC block is compliant with the IEEE standard.

2 Package pinouts and signal descriptions

2.1 Package pinouts

The LQFP pinouts are shown in the following figures.



Note: Availability of port pin alternate functions depends on product selection.

Figure 2. 144-pin LQFP pinout – Full featured configuration (top view)

Table 7. Pin muxing (continued)

Port pin	Pad configuration register (PCR)	Alternate function[1],[2]	Functions	Peripheral[3]	I/O direction[4]	Pad speed[5]		Pin No.	
						SRC = 0	SRC = 1	100-pin	144-pin
C[5]	PCR[37]	ALT0 ALT1 ALT2 ALT3 — —	GPIO[37] SCK — DEBUG[5] FAULT[3] EIRQ[23]	SIUL DSPI_0 — SSCM FlexPWM_0 SIUL	I/O I/O — — I I	Slow	Medium	7	13
C[6]	PCR[38]	ALT0 ALT1 ALT2 ALT3 —	GPIO[38] SOUT B[1] DEBUG[6] EIRQ[24]	SIUL DSPI_0 FlexPWM_0 SSCM SIUL	I/O I/O O — I	Slow	Medium	98	142
C[7]	PCR[39]	ALT0 ALT1 ALT2 ALT3 —	GPIO[39] — A[1] DEBUG[7] SIN	SIUL — FlexPWM_0 SSCM DSPI_0	I/O — O — I	Slow	Medium	9	15
C[8]	PCR[40]	ALT0 ALT1 ALT2 ALT3 —	GPIO[40] CS1 — CS6 FAULT[2]	SIUL DSPI_1 — DSPI_0 FlexPWM_0	I/O O — O I	Slow	Medium	91	130
C[9]	PCR[41]	ALT0 ALT1 ALT2 ALT3 —	GPIO[41] CS3 — X[3] FAULT[2]	SIUL DSPI_2 — FlexPWM_0 FlexPWM_0	I/O O — I/O I	Slow	Medium	84	123
C[10]	PCR[42]	ALT0 ALT1 ALT2 ALT3 —	GPIO[42] CS2 — A[3] FAULT[1]	SIUL DSPI_2 — FlexPWM_0 FlexPWM_0	I/O O — O I	Slow	Medium	78	111
C[11]	PCR[43]	ALT0 ALT1 ALT2 ALT3	GPIO[43] ETC[4] CS2 CS0	SIUL eTimer_0 DSPI_2 DSPI_3	I/O I/O O I/O	Slow	Medium	55	80
C[12]	PCR[44]	ALT0 ALT1 ALT2 ALT3	GPIO[44] ETC[5] CS3 CS1	SIUL eTimer_0 DSPI_2 DSPI_3	I/O I/O O O	Slow	Medium	56	82

Table 7. Pin muxing (continued)

Port pin	Pad configuration register (PCR)	Alternate function[1],[2]	Functions	Peripheral[3]	I/O direction[4]	Pad speed[5]		Pin No.	
						SRC = 0	SRC = 1	100-pin	144-pin
D[5]	PCR[53]	ALT0 ALT1 ALT2 ALT3	GPIO[53] CS3 F[0] SOUT	SIUL DSPI_0 FCU_0 DSPI_3	I/O O O O	Slow	Medium	22	33
D[6]	PCR[54]	ALT0 ALT1 ALT2 ALT3 —	GPIO[54] CS2 SCK — FAULT[1]	SIUL DSPI_0 DSPI_3 — FlexPWM_0	I/O O I/O — I	Slow	Medium	23	34
D[7]	PCR[55]	ALT0 ALT1 ALT2 ALT3 —	GPIO[55] CS3 F[1] CS4 SIN	SIUL DSPI_1 FCU_0 DSPI_0 DSPI_3	I/O O O O I	Slow	Medium	26	37
D[8]	PCR[56]	ALT0 ALT1 ALT2 ALT3 —	GPIO[56] CS2 — CS5 FAULT[3]	SIUL DSPI_1 — DSPI_0 FlexPWM_0	I/O O — O I	Slow	Medium	21	32
D[9]	PCR[57]	ALT0 ALT1 ALT2 ALT3	GPIO[57] X[0] TXD —	SIUL FlexPWM_0 LIN_1 —	I/O I/O O —	Slow	Medium	15	26
D[10]	PCR[58]	ALT0 ALT1 ALT2 ALT3	GPIO[58] A[0] CS0 —	SIUL FlexPWM_0 DSPI_3 —	I/O O I/O —	Slow	Medium	53	76
D[11]	PCR[59]	ALT0 ALT1 ALT2 ALT3	GPIO[59] B[0] CS1 SCK	SIUL FlexPWM_0 DSPI_3 DSPI_3	I/O O O I/O	Slow	Medium	54	78
D[12]	PCR[60]	ALT0 ALT1 ALT2 ALT3 —	GPIO[60] X[1] — — RXD	SIUL FlexPWM_0 — — LIN_1	I/O I/O — — I	Slow	Medium	70	99
D[13]	PCR[61]	ALT0 ALT1 ALT2 ALT3	GPIO[61] A[1] CS2 SOUT	SIUL FlexPWM_0 DSPI_3 DSPI_3	I/O O O O	Slow	Medium	67	95

Table 7. Pin muxing (continued)

Port pin	Pad configuration register (PCR)	Alternate function[1], [2]	Functions	Peripheral[3]	I/O direction [4]	Pad speed[5]		Pin No.	
						SRC = 0	SRC = 1	100-pin	144-pin
F[5]	PCR[85]	ALT0 ALT1 ALT2 ALT3	GPIO[85] MDO[2] — —	SIUL NEXUS_0 — —	I/O O — —	Slow	Fast	—	5
F[6]	PCR[86]	ALT0 ALT1 ALT2 ALT3	GPIO[86] MDO[1] — —	SIUL NEXUS_0 — —	I/O O — —	Slow	Fast	—	8
F[7]	PCR[87]	ALT0 ALT1 ALT2 ALT3	GPIO[87] MCKO — —	SIUL NEXUS_0 — —	I/O O — —	Slow	Fast	—	19
F[8]	PCR[88]	ALT0 ALT1 ALT2 ALT3	GPIO[88] MSEO1 — —	SIUL NEXUS_0 — —	I/O O — —	Slow	Fast	—	20
F[9]	PCR[89]	ALT0 ALT1 ALT2 ALT3	GPIO[89] MSEO0 — —	SIUL NEXUS_0 — —	I/O O — —	Slow	Fast	—	23
F[10]	PCR[90]	ALT0 ALT1 ALT2 ALT3	GPIO[90] EVTO — —	SIUL NEXUS_0 — —	I/O O — —	Slow	Fast	—	24
F[11]	PCR[91]	ALT0 ALT1 ALT2 ALT3 —	GPIO[91] — — — EVTI	SIUL — — — NEXUS_0	I/O — — — I	Slow	Medium	—	25
F[12]	PCR[92]	ALT0 ALT1 ALT2 ALT3	GPIO[92] ETC[3] — —	SIUL eTimer_1 — —	I/O I/O — —	Slow	Medium	—	106
F[13]	PCR[93]	ALT0 ALT1 ALT2 ALT3	GPIO[92] ETC[4] — —	SIUL eTimer_1 — —	I/O I/O — —	Slow	Medium	—	112

3. The difference between ADC voltage supplies must be less than 100 mV, $|V_{DD\_HV\_ADC1} - V_{DD\_HV\_ADC0}| < 100$ mV.
4. To be connected to emitter of external NPN. Low voltage supplies are not under user control—they are produced by an on-chip voltage regulator—but for the device to function properly the low voltage grounds ($V_{SS\_LV\_xxx}$) must be shorted to high voltage grounds ($V_{SS\_HV\_xxx}$) and the low voltage supply pins ($V_{DD\_LV\_xxx}$) must be connected to the external ballast emitter.
5. The low voltage supplies ($V_{DD\_LV\_xxx}$) are not all independent.

$V_{DD\_LV\_COR1}$ and $V_{DD\_LV\_COR2}$ are shorted internally via double bonding connections with lines that provide the low voltage supply to the data flash module. Similarly, $V_{SS\_LV\_COR1}$ and $V_{SS\_LV\_COR2}$ are internally shorted.

$V_{DD\_LV\_REGCOR}$ and $V_{DD\_LV\_REGCORx}$ are physically shorted internally, as are $V_{SS\_LV\_REGCOR}$ and $V_{SS\_LV\_CORx}$.

Table 11. Recommended operating conditions (3.3 V)

Symbol		Parameter	Conditions	Value		Unit
				Min	Max(1)	
V_{SS}	SR	Device ground	—	0	0	V
$V_{DD\_HV\_IOx}$(2)	SR	3.3 V input/output supply voltage	—	3.0	3.6	V
$V_{SS\_HV\_IOx}$	SR	Input/output ground voltage	—	0	0	V
$V_{DD\_HV\_FL}$	SR	3.3 V code and data flash supply voltage	—	3.0	3.6	V
			Relative to $V_{DD\_HV\_IOx}$	$V_{DD\_HV\_IOx} - 0.1$	$V_{DD\_HV\_IOx} + 0.1$	
$V_{SS\_HV\_FL}$	SR	Code and data flash ground	—	0	0	V
$V_{DD\_HV\_OSC}$	SR	3.3 V crystal oscillator amplifier supply voltage	—	3.0	3.6	V
			Relative to $V_{DD\_HV\_IOx}$	$V_{DD\_HV\_IOx} - 0.1$	$V_{DD\_HV\_IOx} + 0.1$	
$V_{SS\_HV\_OSC}$	SR	3.3 V crystal oscillator amplifier reference voltage	—	0	0	V
$V_{DD\_HV\_REG}$	SR	3.3 V voltage regulator supply voltage	—	3.0	3.6	V
			Relative to $V_{DD\_HV\_IOx}$	$V_{DD\_HV\_IOx} - 0.1$	$V_{DD\_HV\_IOx} + 0.1$	
$V_{DD\_HV\_ADC0}$(3)	SR	3.3 V ADC_0 supply and high reference voltage	—	3.0	5.5	V
			Relative to $V_{DD\_HV\_REG}$	$V_{DD\_HV\_REG} - 0.1$	5.5	
$V_{SS\_HV\_ADC0}$	SR	ADC_0 ground and low reference voltage	—	0	0	V
$V_{DD\_HV\_ADC1}$(3)	SR	3.3 V ADC_1 supply and high reference voltage	—	3.0	5.5	V
			Relative to $V_{DD\_HV\_REG}$	$V_{DD\_HV\_REG} - 0.1$	5.5	
$V_{SS\_HV\_ADC1}$	SR	ADC_1 ground and low reference voltage	—	0	0	V
$V_{DD\_LV\_REGCOR}$(4),(5)	CC	Internal supply voltage	—	—	—	V
$V_{SS\_LV\_REGCOR}$(4)	SR	Internal reference voltage	—	0	0	V
$V_{DD\_LV\_CORx}$(4),(5)	CC	Internal supply voltage	—	—	—	V

3.10.2 DC electrical characteristics (5 V)

Table 21 gives the DC electrical characteristics at 5 V (4.5 V < $V_{DD\_HV\_IOx}$ < 5.5 V, NVUSRO[PAD3V5V] = 0); see *Figure 14*.

Table 21. DC electrical characteristics (5.0 V, NVUSRO[PAD3V5V] = 0)

Symbol	C	Parameter	Conditions	Value		Unit
				Min	Max	
V_{IL}	D	Low level input voltage	—	–0.1(1)	—	V
	P		—	—	0.35 $V_{DD\_HV\_IOx}$	V
V_{IH}	P	High level input voltage	—	0.65 $V_{DD\_HV\_IOx}$	—	V
	D		—	—	$V_{DD\_HV\_IOx}$ + 0.1(1)	V
V_{HYS}	T	Schmitt trigger hysteresis	—	0.1 $V_{DD\_HV\_IOx}$	—	V
V_{OL_S}	P	Slow, low level output voltage	I_{OL} = 3 mA	—	0.1 $V_{DD\_HV\_IOx}$	V
V_{OH_S}	P	Slow, high level output voltage	I_{OH} = –3 mA	0.8 $V_{DD\_HV\_IOx}$	—	V
V_{OL_M}	P	Medium, low level output voltage	I_{OL} = 3 mA	—	0.1 $V_{DD\_HV\_IOx}$	V
V_{OH_M}	P	Medium, high level output voltage	I_{OH} = –3 mA	0.8 $V_{DD\_HV\_IOx}$	—	V
V_{OL_F}	P	Fast, low level output voltage	I_{OL} = 3 mA	—	0.1 $V_{DD\_HV\_IOx}$	V
V_{OH_F}	P	Fast, high level output voltage	I_{OH} = –3 mA	0.8 $V_{DD\_HV\_IOx}$	—	V
V_{OL_SYM}	P	Symmetric, low level output voltage	I_{OL} = 3 mA	—	0.1 $V_{DD\_HV\_IOx}$	V
V_{OH_SYM}	P	Symmetric, high level output voltage	I_{OH} = –3 mA	0.8 $V_{DD\_HV\_IOx}$	—	V
I_{PU}	P	Equivalent pull-up current	V_{IN} = V_{IL}	–130	—	µA
			V_{IN} = V_{IH}	—	–10	
I_{PD}	P	Equivalent pull-down current	V_{IN} = V_{IL}	10	—	µA
			V_{IN} = V_{IH}	—	130	
I_{IL}	P	Input leakage current (all bidirectional ports)	T_A = –40 to 125 °C	–1	1	µA
I_{IL}	P	Input leakage current (all ADC input-only ports)	T_A = –40 to 125 °C	–0.5	0.5	µA
C_{IN}	D	Input capacitance	—	—	10	pF
I_{PU}	D	$\overline{\text{RESET}}$, equivalent pull-up current	V_{IN} = V_{IL}	–130	—	µA
			V_{IN} = V_{IH}	—	–10	

1. “SR” parameter values must not exceed the absolute maximum ratings shown in *Table 9*.

Table 22. Supply current (5.0 V, NVUSRO[PAD3V5V] = 0)

Symbol	C	Parameter		Conditions		Value		Unit
						Typ	Max	
$I_{DD\_LV\_CORx}$	T	Supply current	RUN—Maximum mode(1)	$V_{DD\_LV\_CORx}$ externally forced at 1.3 V	40 MHz	62	77	mA
					64 MHz	71	88	
			RUN—Typical mode(2)		40 MHz	45	56	
					64 MHz	52	65	
	P		RUN—Maximum mode(3)	$V_{DD\_LV\_CORx}$ externally forced at 1.3 V	64 MHz	60	75	
			HALT mode(4)	$V_{DD\_LV\_CORx}$ externally forced at 1.3 V	—	1.5	10	
			STOP mode(5)	$V_{DD\_LV\_CORx}$ externally forced at 1.3 V	—	1	10	
I_{DD_FLASH}	T		Flash during read	$V_{DD\_HV\_FL}$ at 5.0 V	—	10	12	
			Flash during erase operation on 1 flash module	$V_{DD\_HV\_FL}$ at 5.0 V	—	15	19	
I_{DD_ADC}	T		ADC—Maximum mode(1)	$V_{DD\_HV\_ADC0}$ at 5.0 V $V_{DD\_HV\_ADC1}$ at 5.0 V f_{ADC} = 16 MHz	ADC_1	3.5	5	
					ADC_0	3	4	
			ADC—Typical mode(2)		ADC_1	0.8	1	
					ADC_0	0.005	0.006	
I_{DD_OSC}	T		Oscillator	V_{DD_OSC} at 5.0 V	8 MHz	2.6	3.2	

1. Maximum mode: FlexPWM, ADCs, CTU, DSPI, LINFlex, FlexCAN, 15 output pins, 1st and 2nd PLL enabled. I/O supply current excluded.
2. Typical mode configurations: DSPI, LINFlex, FlexCAN, 15 output pins, 1st PLL only. I/O supply current excluded.
3. Code fetched from RAM, PLL_0: 64 MHz system clock (x4 multiplier with 16 MHz XTAL), PLL_1 is ON at PHI_div2 = 120 MHz and PHI_div3 = 80 MHz, auxiliary clock sources set that all peripherals receive maximum frequency, all peripherals enabled.
4. Halt mode configurations: code fetched from RAM, code and data flash memories in low power mode, OSC/PLL_0/PLL_1 are OFF, core clock frozen, all peripherals are disabled.
5. STOP “P” mode Device Under Test (DUT) configuration: code fetched from RAM, code and data flash memories OFF, OSC/PLL_0/PLL_1 are OFF, core clock frozen, all peripherals are disabled.

3.10.3 DC electrical characteristics (3.3 V)

Table 23 gives the DC electrical characteristics at 3.3 V ($3.0\ V < V_{DD\_HV\_IOx} < 3.6\ V$, NVUSRO[PAD3V5V] = 1); see *Figure 14*.

Table 23. DC electrical characteristics (3.3 V, NVUSRO[PAD3V5V] = 1)(1)

Symbol	C	Parameter	Conditions	Value		Unit
				Min	Max	
V_{IL}	D	Low level input voltage	—	–0.1(2)	—	V
	P		—	—	0.35 $V_{DD\_HV\_IOx}$	V

Table 26. I/O weight (continued)

Pad	LQFP144		LQFP100	
	Weight 5V	Weight 3.3V	Weight 5V	Weight 3.3V
PAD[86]	9%	6%	—	—
MODO[0]	12%	8%	—	—
PAD[7]	4%	4%	11%	10%
PAD[36]	5%	4%	11%	9%
PAD[8]	5%	4%	10%	9%
PAD[37]	5%	4%	10%	9%
PAD[5]	5%	4%	9%	8%
PAD[39]	5%	4%	9%	8%
PAD[35]	5%	4%	8%	7%
PAD[87]	12%	9%	—	—
PAD[88]	9%	6%	—	—
PAD[89]	10%	7%	—	—
PAD[90]	15%	11%	—	—
PAD[91]	6%	5%	—	—
PAD[57]	8%	7%	8%	7%
PAD[56]	13%	11%	13%	11%
PAD[53]	14%	12%	14%	12%
PAD[54]	15%	13%	15%	13%
PAD[55]	25%	22%	25%	22%
PAD[96]	27%	24%	—	—
PAD[65]	1%	1%	1%	1%
PAD[67]	1%	1%	—	—
PAD[33]	1%	1%	1%	1%
PAD[68]	1%	1%	—	—
PAD[23]	1%	1%	1%	1%
PAD[69]	1%	1%	—	—
PAD[34]	1%	1%	1%	1%
PAD[70]	1%	1%	—	—
PAD[24]	1%	1%	1%	1%
PAD[71]	1%	1%	—	—
PAD[66]	1%	1%	1%	1%
PAD[25]	1%	1%	1%	1%
PAD[26]	1%	1%	1%	1%

Table 26. I/O weight (continued)

Pad	LQFP144		LQFP100	
	Weight 5V	Weight 3.3V	Weight 5V	Weight 3.3V
PAD[13]	10%	9%	12%	11%
PAD[82]	10%	9%	—	—
PAD[22]	10%	9%	13%	12%
PAD[83]	10%	9%	—	—
PAD[50]	10%	9%	14%	12%
PAD[97]	10%	9%	—	—
PAD[38]	10%	9%	14%	13%
PAD[14]	9%	8%	14%	13%
PAD[15]	9%	8%	15%	13%

Table 27. I/O consumption

Symbol		C	Parameter	Conditions[1]		Value			Unit
						Min	Typ	Max	
I_{SWTSLW}[2]	CC	D	Dynamic I/O current for SLOW configuration	C_L = 25 pF	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	20	mA
					V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	16	
I_{SWTMED}[2]	CC	D	Dynamic I/O current for MEDIUM configuration	C_L = 25 pF	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	29	mA
					V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	17	
I_{SWTFST}[2]	CC	D	Dynamic I/O current for FAST configuration	C_L = 25 pF	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	110	mA
					V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	50	
I_{RMSSLW}	CC	D	Root medium square I/O current for SLOW configuration	C_L = 25 pF, 2 MHz	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	2.3	mA
				C_L = 25 pF, 4 MHz		—	—	3.2	
				C_L = 100 pF, 2 MHz		—	—	6.6	
				C_L = 25 pF, 2 MHz	V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	1.6	
				C_L = 25 pF, 4 MHz		—	—	2.3	
				C_L = 100 pF, 2 MHz		—	—	4.7	

Table 27. I/O consumption (continued)

Symbol		C	Parameter	Conditions[1]		Value			Unit
						Min	Typ	Max	
I_{RMSMED}	CC	D	Root medium square I/O current for MEDIUM configuration	C_L = 25 pF, 13 MHz	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	6.6	mA
				C_L = 25 pF, 40 MHz		—	—	13.4	
				C_L = 100 pF, 13 MHz		—	—	18.3	
				C_L = 25 pF, 13 MHz	V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	5	
				C_L = 25 pF, 40 MHz		—	—	8.5	
				C_L = 100 pF, 13 MHz		—	—	11	
I_{RMSFST}	CC	D	Root medium square I/O current for FAST configuration	C_L = 25 pF, 40 MHz	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	22	mA
				C_L = 25 pF, 64 MHz		—	—	33	
				C_L = 100 pF, 40 MHz		—	—	56	
				C_L = 25 pF, 40 MHz	V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	14	
				C_L = 25 pF, 64 MHz		—	—	20	
				C_L = 100 pF, 40 MHz		—	—	35	
I_{AVGSEG}	SR	D	Sum of all the static I/O current within a supply segment	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0		—	—	70	mA
				V_{DD} = 3.3 V ± 10%, PAD3V5V = 1		—	—	65	

1. V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified
2. Stated maximum values represent peak consumption that lasts only a few ns during I/O transition.

3.11 Main oscillator electrical characteristics

The SPC560P44Lx, SPC560P50Lx provides an oscillator/resonator driver.

Table 28. Main oscillator output electrical characteristics (5.0 V, NVUSRO[PAD3V5V] = 0)

Symbol		C	Parameter	Value		Unit
				Min	Max	
f_{OSC}	SR	—	Oscillator frequency	4	40	MHz
g_m	—	P	Transconductance	6.5	25	mA/V
V_{OSC}	—	T	Oscillation amplitude on XTAL pin	1	—	V
t_{OSCSU}	—	T	Start-up time[1],[2]	8	—	ms

1. The start-up time is dependent upon crystal characteristics, board leakage, etc., high ESR and excessive capacitive loads can cause long start-up time.
2. Value captured when amplitude reaches 90% of XTAL

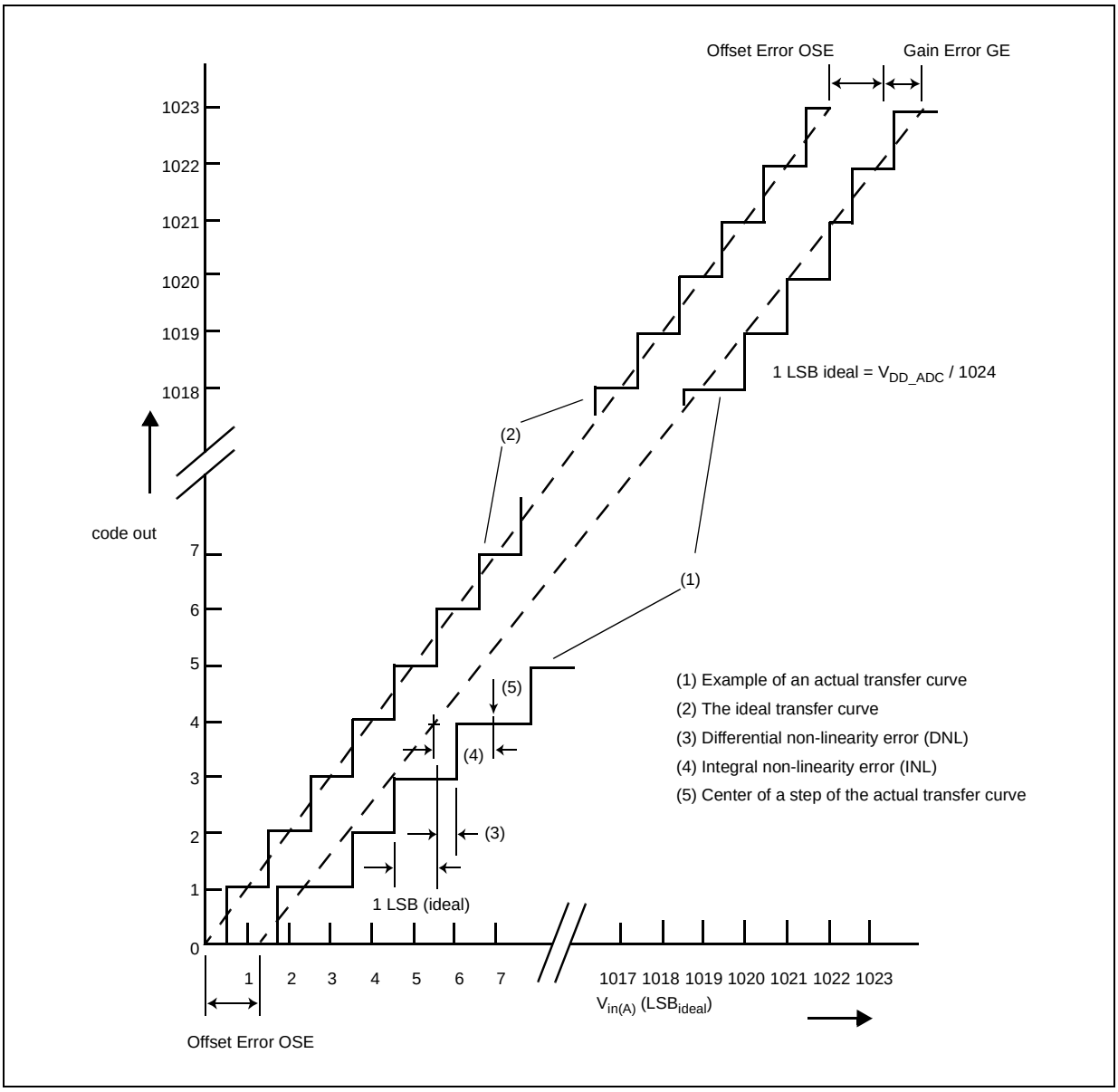


Figure 15. ADC characteristics and error definitions

3.14.1 Input impedance and ADC accuracy

To preserve the accuracy of the A/D converter, it is necessary that analog input pins have low AC impedance. Placing a capacitor with good high frequency characteristics at the input pin of the device can be effective: the capacitor should be as large as possible, ideally infinite. This capacitor contributes to attenuating the noise present on the input pin; further, it sources charge during the sampling phase, when the analog signal source is a high-impedance source.

A real filter can typically be obtained by using a series resistance with a capacitor on the input pin (simple RC filter). The RC filtering may be limited according to the source impedance value of the transducer or circuit supplying the analog signal to be measured.

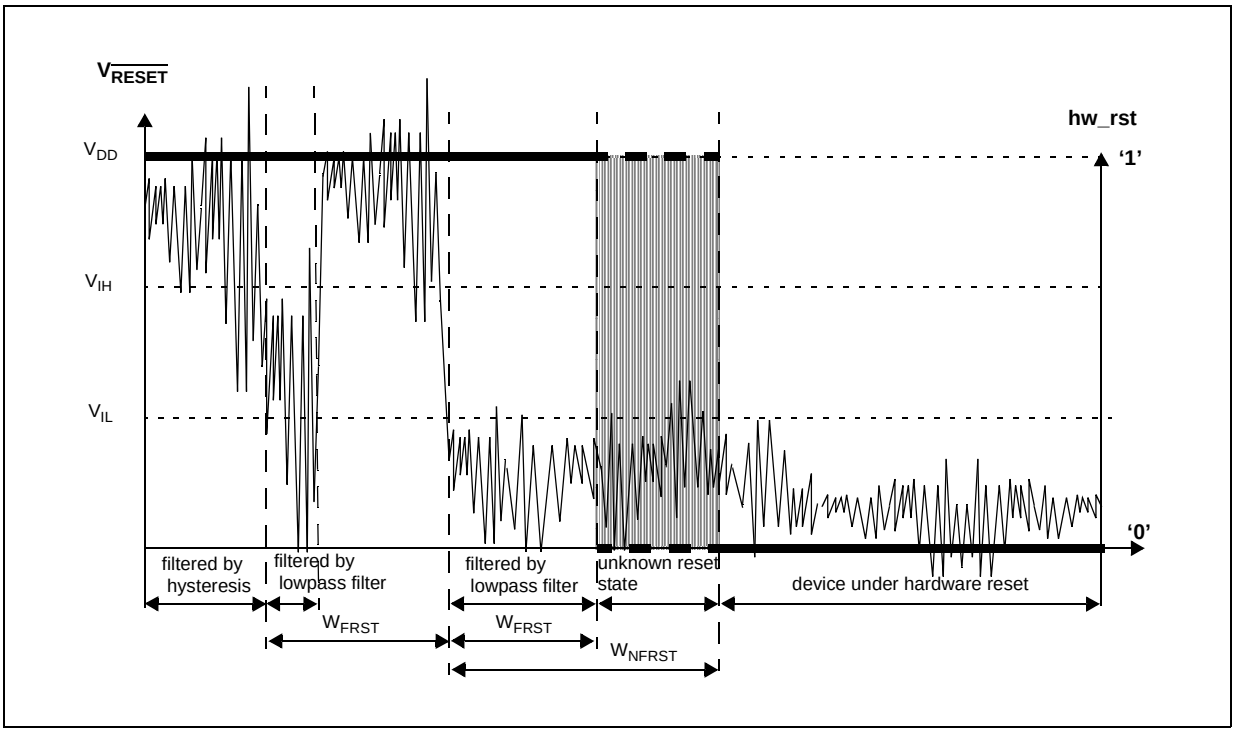


Figure 21. Noise filtering on reset signal

Table 38. $\overline{RESET}$ electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
V_{IH}	SR	P	Input High Level CMOS (Schmitt Trigger)	—	0.65V_{DD}	—	V_{DD}+0.4	V
V_{IL}	SR	P	Input low Level CMOS (Schmitt Trigger)	—	–0.4	—	0.35V_{DD}	V
V_{HYS}	CC	C	Input hysteresis CMOS (Schmitt Trigger)	—	0.1V_{DD}	—	—	V
V_{OL}	CC	P	Output low level	Push Pull, I_{OL} = 2mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0 (recommended)	—	—	0.1V_{DD}	V
				Push Pull, I_{OL} = 1mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 1[2]	—	—	0.1V_{DD}	
				Push Pull, I_{OL} = 1mA, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1 (recommended)	—	—	0.5	

Table 39. JTAG pin AC electrical characteristics (continued)

No.	Symbol		C	Parameter	Conditions	Value		Unit
						Min	Max	
5	t_{TMSH}, t_{TDIH}	CC	D	TMS, TDI data hold time	—	25	—	ns
6	t_{TDOV}	CC	D	TCK low to TDO data valid	—	—	40	ns
7	t_{TDOI}	CC	D	TCK low to TDO data invalid	—	0	—	ns
8	t_{TDOHZ}	CC	D	TCK low to TDO high impedance	—	40	—	ns
11	t_{BSDV}	CC	D	TCK falling edge to output valid	—	—	50	ns
12	t_{BSDVZ}	CC	D	TCK falling edge to output valid out of high impedance	—	—	50	ns
13	t_{BSDHZ}	CC	D	TCK falling edge to output high impedance	—	—	50	ns
14	t_{BSDST}	CC	D	Boundary scan input valid to TCK rising edge	—	50	—	ns
15	t_{BSDHT}	CC	D	TCK rising edge to boundary scan input invalid	—	50	—	ns

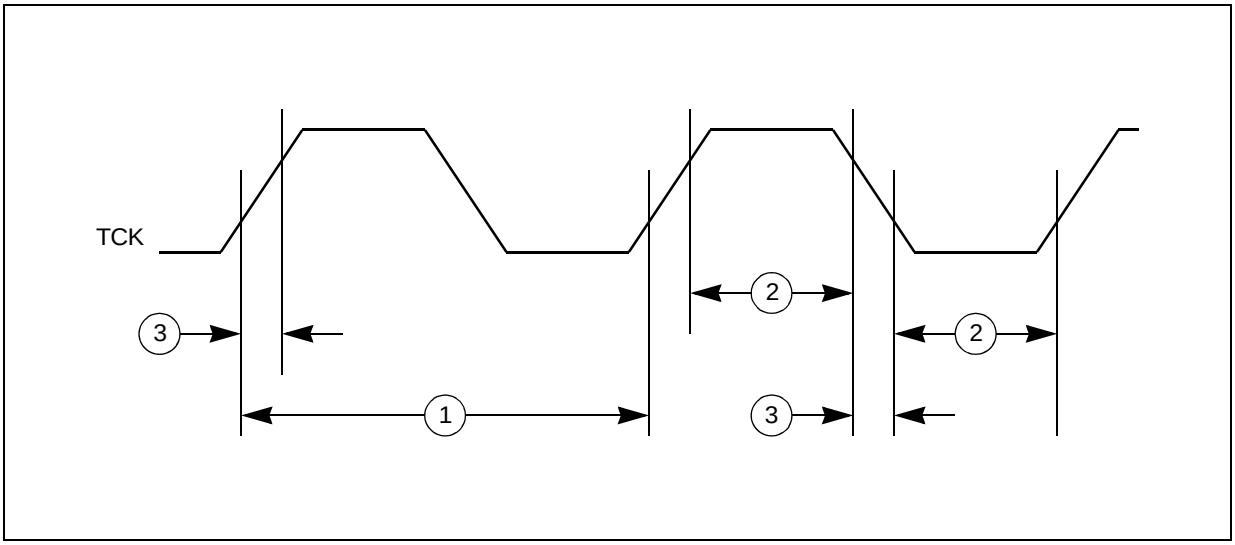


Figure 22. JTAG test clock input timing

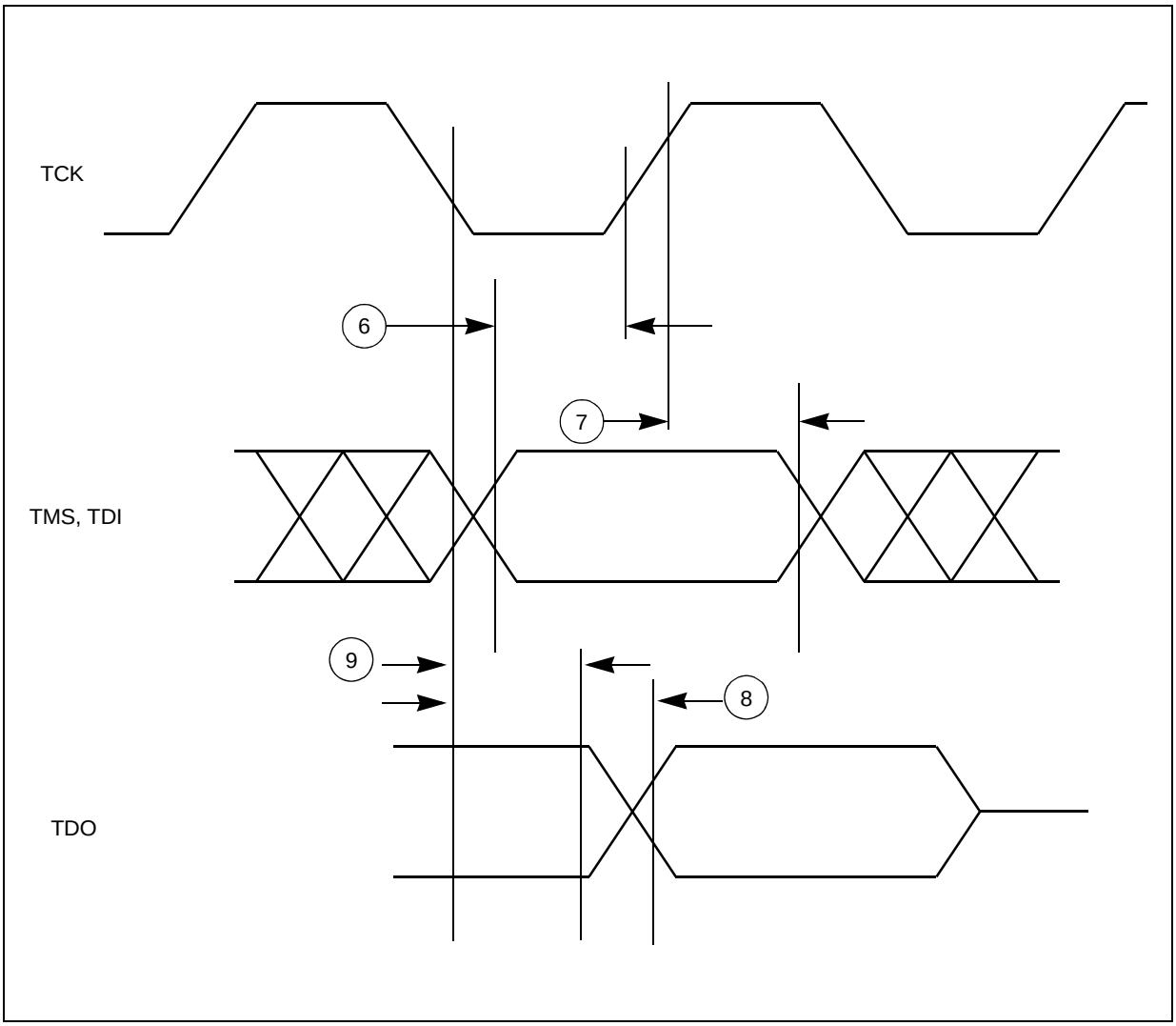


Figure 27. Nexus TDI, TMS, TDO timing

3.17.4 External interrupt timing (IRQ pin)

Table 41. External interrupt timing(1)

No.	Symbol		C	Parameter	Conditions	Value		Unit
						Min	Max	
1	t_{IPWL}	CC	D	IRQ pulse width low	—	4	—	t_{CYC}
2	t_{IPWH}	CC	D	IRQ pulse width high	—	4	—	t_{CYC}
3	t_{ICYC}	CC	D	IRQ edge to edge time(2)	—	4 + N (3)	—	t_{CYC}

1. IRQ timing specified at f_{SYS} = 64 MHz and $V_{DD\_HV\_IOx}$ = 3.0 V to 5.5 V, $T_A = T_L$ to T_H, and C_L = 200 pF with SRC = 0b00.
2. Applies when IRQ pins are configured for rising edge or falling edge events, but not both.
3. N = ISR time to clear the flag