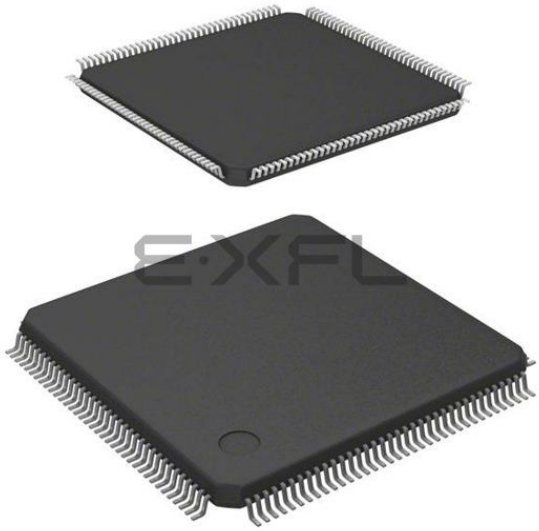

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z0h
Core Size	32-Bit Single-Core
Speed	64MHz
Connectivity	CANbus, LINbus, SPI, UART/USART
Peripherals	DMA, POR, PWM, WDT
Number of I/O	80
Program Memory Size	384KB (384K x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	36K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 26x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/spc560p44l5cefby

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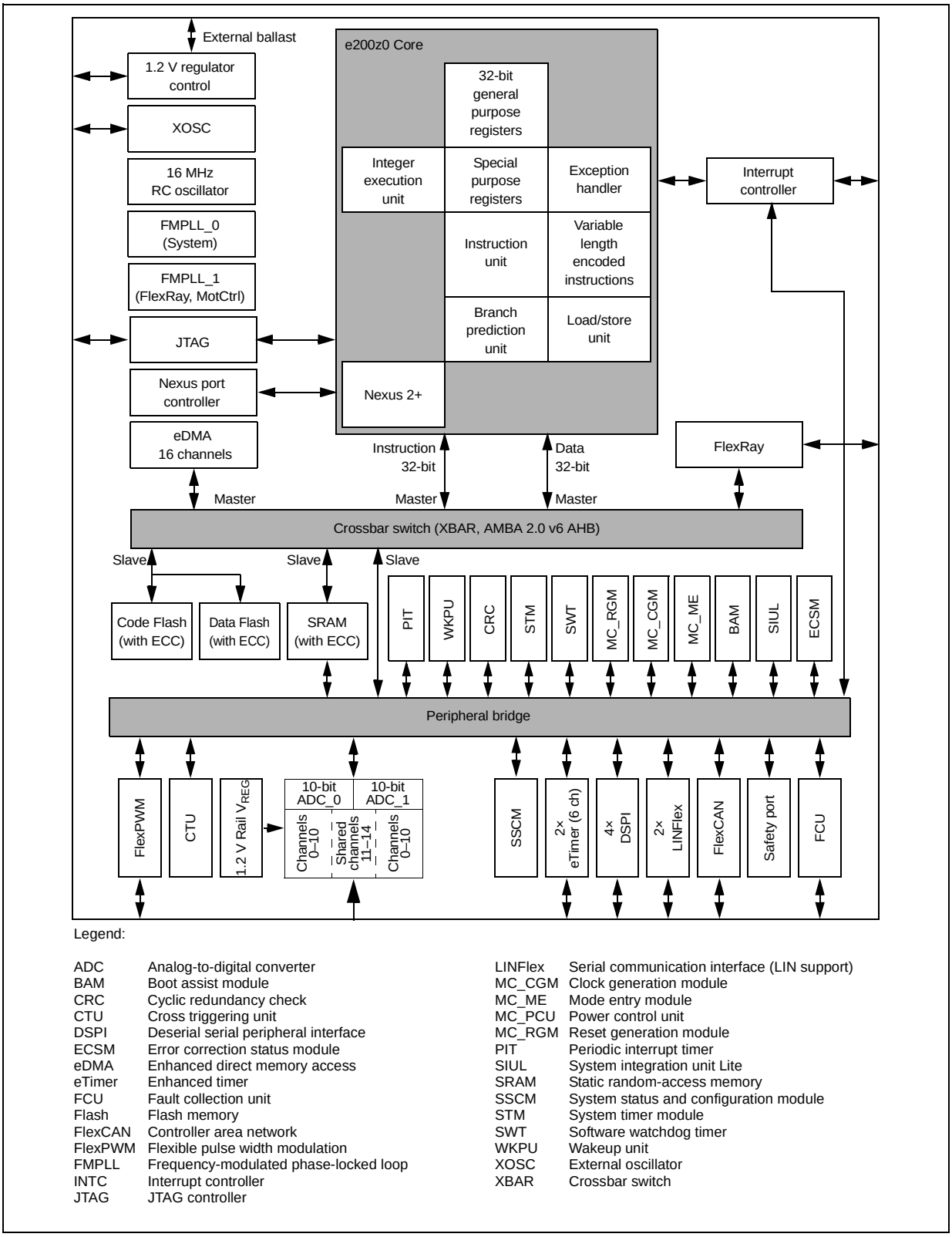


Legend:

ADC	Analog-to-digital converter
BAM	Boot assist module
CRC	Cyclic redundancy check
CTU	Cross triggering unit
DSPI	Deserial serial peripheral interface
ECSM	Error correction status module
eDMA	Enhanced direct memory access
eTimer	Enhanced timer
FCU	Fault collection unit
Flash	Flash memory
FlexCAN	Controller area network
FlexPWM	Flexible pulse width modulation
FMPLL	Frequency-modulated phase-locked loop
INTC	Interrupt controller
JTAG	JTAG controller
LINFlex	Serial communication interface (LIN support)
MC_CGM	Clock generation module
MC_ME	Mode entry module
MC_PCU	Power control unit
MC_RGM	Reset generation module
PIT	Periodic interrupt timer
SIUL	System integration unit Lite
SRAM	Static random-access memory
SSCM	System status and configuration module
STM	System timer module
SWT	Software watchdog timer
WKPU	Wakeup unit
XOSC	External oscillator
XBAR	Crossbar switch

Figure 1. SPC560P44Lx, SPC560P50Lx block diagram

The SIU provides the following features:

- Centralized general purpose input output (GPIO) control of as many as 80 input/output pins and 26 analog input-only pads (package dependent)
- All GPIO pins can be independently configured to support pull-up, pull down, or no pull
- Reading and writing to GPIO supported both as individual pins and 16-bit wide ports
- All peripheral pins (except ADC channels) can be alternatively configured as both general purpose input or output pins
- ADC channels support alternative configuration as general purpose inputs
- Direct readback of the pin value is supported on all pins through the SIUL
- Configurable digital input filter that can be applied to some general purpose input pins for noise elimination: as many as 4 internal functions can be multiplexed onto 1 pin

1.5.17 Boot and censorship

Different booting modes are available in the SPC560P44Lx, SPC560P50Lx: booting from internal flash memory and booting via a serial link.

The default booting scheme uses the internal flash memory (an internal pull-down is used to select this mode). Optionally, the user can boot via FlexCAN or LINFlex (using the boot assist module software).

A censorship scheme is provided to protect the content of the flash memory and offer increased security for the entire device.

A password mechanism is designed to grant the legitimate user access to the non-volatile memory.

Boot assist module (BAM)

The BAM is a block of read-only one-time programmed memory and is identical for all SPC560Pxx devices that are based on the e200z0h core. The BAM program is executed every time the device is powered on if the alternate boot mode has been selected by the user.

The BAM provides the following features:

- Serial bootloading via FlexCAN or LINFlex
- Ability to accept a password via the used serial communication channel to grant the legitimate user access to the non-volatile memory

1.5.18 Error correction status module (ECSM)

The ECSM provides a myriad of miscellaneous control functions regarding program-visible information about the platform configuration and revision levels, a reset status register, a software watchdog timer, wakeup control for exiting sleep modes, and information on platform memory errors reported by error-correcting codes and/or generic access error information for certain processor cores.

The Error Correction Status Module supports a number of miscellaneous control functions for the platform. The ECSM includes these features:

- Registers for capturing information on platform memory errors if error-correcting codes (ECC) are implemented
- For test purposes, optional registers to specify the generation of double-bit memory errors are enabled on the SPC560P44Lx, SPC560P50Lx.

block is an integration of several individual Nexus blocks that are selected to provide the development support interface for this device. The NDI block interfaces to the host processor and internal busses to provide development support as per the IEEE-ISTO 5001-2003 Class 2+ standard. The development support provided includes access to the MCU's internal memory map and access to the processor's internal registers during run time.

The Nexus Interface provides the following features:

- Configured via the IEEE 1149.1
- All Nexus port pins operate at V_{DDIO} (no dedicated power supply)
- Nexus 2+ features supported
  - Static debug
  - Watchpoint messaging
  - Ownership trace messaging
  - Program trace messaging
  - Real time read/write of any internally memory mapped resources through JTAG pins
  - Overrun control, which selects whether to stall before Nexus overruns or keep executing and allow overwrite of information
  - Watchpoint triggering, watchpoint triggers program tracing
- Auxiliary Output Port
  - 4 MDO (Message Data Out) pins
  - MCKO (Message Clock Out) pin
  - 2 $\overline{\text{MSEO}}$ (Message Start/End Out) pins
  - $\overline{\text{EVTO}}$ (Event Out) pin
- Auxiliary Input Port
  - $\overline{\text{EVTI}}$ (Event In) pin

1.5.30 Cyclic redundancy check (CRC)

The CRC computing unit is dedicated to the computation of CRC off-loading the CPU. The CRC module features:

- Support for CRC-16-CCITT (*x*25 protocol):
  - $x^{16} + x^{12} + x^5 + 1$
- Support for CRC-32 (Ethernet protocol):
  - $x^{32} + x^{26} + x^{23} + x^{22} + x^{16} + x^{12} + x^{11} + x^{10} + x^8 + x^7 + x^5 + x^4 + x^2 + x + 1$
- Zero wait states for each write/read operations to the CRC_CFG and CRC_INP registers at the maximum frequency

1.5.31 IEEE 1149.1 JTAG controller

The JTAG controller (JTAGC) block provides the means to test chip functionality and connectivity while remaining transparent to system logic when not in test mode. All data input to and output from the JTAGC block is communicated in serial format. The JTAGC block is compliant with the IEEE standard.

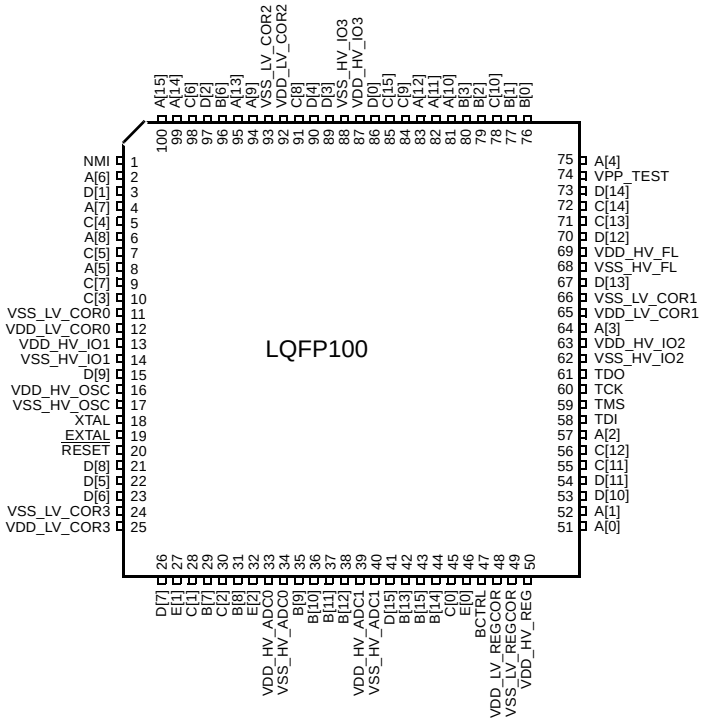
The JTAG controller provides the following features:

- IEEE Test Access Port (TAP) interface with 4 pins (TDI, TMS, TCK, TDO)
- Selectable modes of operation include JTAGC/debug or normal system operation.
- A 5-bit instruction register that supports the following IEEE 1149.1-2001 defined instructions:
  - BYPASS, IDCODE, EXTEST, SAMPLE, SAMPLE/PRELOAD
- A 5-bit instruction register that supports the additional following public instructions:
  - ACCESS_AUX_TAP_NPC, ACCESS_AUX_TAP_ONCE
- 3 test data registers: a bypass register, a boundary scan register, and a device identification register.
- A TAP controller state machine that controls the operation of the data registers, instruction register and associated circuitry.

1.5.32 On-chip voltage regulator (VREG)

The on-chip voltage regulator module provides the following features:

- Uses external NPN (negative-positive-negative) transistor
- Regulates external 3.3 V /5.0 V down to 1.2 V for the core logic
- Low voltage detection on the internal 1.2 V and I/O voltage 3.3 V



Note: Availability of port pin alternate functions depends on product selection.

Figure 3. 100-pin LQFP pinout – Airbag configuration (top view)

Table 7. Pin muxing (continued)

Port pin	Pad configuration register (PCR)	Alternate function[1], [2]	Functions	Peripheral[3]	I/O direction [4]	Pad speed[5]		Pin No.	
						SRC = 0	SRC = 1	100-pin	144-pin
A[14]	PCR[14]	ALT0 ALT1 ALT2 ALT3 —	GPIO[14] TXD ETC[4] — EIRQ[13]	SIUL Safety Port_0 eTimer_1 — SIUL	I/O O I/O — I	Slow	Medium	99	143
A[15]	PCR[15]	ALT0 ALT1 ALT2 ALT3 — —	GPIO[15] — ETC[5] — RXD EIRQ[14]	SIUL — eTimer_1 — Safety Port_0 SIUL	I/O — I/O — I I	Slow	Medium	100	144
Port B (16-bit)									
B[0]	PCR[16]	ALT0 ALT1 ALT2 ALT3 —	GPIO[16] TXD ETC[2] DEBUG[0] EIRQ[15]	SIUL FlexCAN_0 eTimer_1 SSCM SIUL	I/O O I/O — I	Slow	Medium	76	109
B[1]	PCR[17]	ALT0 ALT1 ALT2 ALT3 — —	GPIO[17] — ETC[3] DEBUG[1] RXD EIRQ[16]	SIUL — eTimer_1 SSCM FlexCAN_0 SIUL	I/O — I/O — I I	Slow	Medium	77	110
B[2]	PCR[18]	ALT0 ALT1 ALT2 ALT3 —	GPIO[18] TXD — DEBUG[2] EIRQ[17]	SIUL LIN_0 — SSCM SIUL	I/O O — — I	Slow	Medium	79	114
B[3]	PCR[19]	ALT0 ALT1 ALT2 ALT3 —	GPIO[19] — — DEBUG[3] RXD	SIUL — — SSCM LIN_0	I/O — — — I	Slow	Medium	80	116
B[6]	PCR[22]	ALT0 ALT1 ALT2 ALT3 —	GPIO[22] CLKOUT CS2 — EIRQ[18]	SIUL MC_CGL DSPI_2 — SIUL	I/O O O — I	Slow	Medium	96	138

Table 7. Pin muxing (continued)

Port pin	Pad configuration register (PCR)	Alternate function[1],[2]	Functions	Peripheral[3]	I/O direction[4]	Pad speed[5]		Pin No.	
						SRC = 0	SRC = 1	100-pin	144-pin
B[14]	PCR[30]	ALT0 ALT1 ALT2 ALT3 — — —	GPIO[30] — — — AN[1] ETC[4] EIRQ[19]	SIUL — — — ADC_1 eTimer_0 SIUL	Input only	—	—	44	64
B[15]	PCR[31]	ALT0 ALT1 ALT2 ALT3 — —	GPIO[31] — — — AN[2] EIRQ[20]	SIUL — — — ADC_1 SIUL	Input only	—	—	43	62
Port C (16-bit)									
C[0]	PCR[32]	ALT0 ALT1 ALT2 ALT3 —	GPIO[32] — — — AN[3]	SIUL — — — ADC_1	Input only	—	—	45	66
C[1]	PCR[33]	ALT0 ALT1 ALT2 ALT3 —	GPIO[33] — — — AN[2]	SIUL — — — ADC_0	Input only	—	—	28	41
C[2]	PCR[34]	ALT0 ALT1 ALT2 ALT3 —	GPIO[34] — — — AN[3]	SIUL — — — ADC_0	Input only	—	—	30	45
C[3]	PCR[35]	ALT0 ALT1 ALT2 ALT3 —	GPIO[35] CS1 ETC[4] TXD EIRQ[21]	SIUL DSPI_0 eTimer_1 LIN_1 SIUL	I/O O I/O O I	Slow	Medium	10	16
C[4]	PCR[36]	ALT0 ALT1 ALT2 ALT3 —	GPIO[36] CS0 X[1] DEBUG[4] EIRQ[22]	SIUL DSPI_0 FlexPWM_0 SSCM SIUL	I/O I/O I/O — I	Slow	Medium	5	11

Table 7. Pin muxing (continued)

Port pin	Pad configuration register (PCR)	Alternate function[1], [2]	Functions	Peripheral[3]	I/O direction [4]	Pad speed[5]		Pin No.	
						SRC = 0	SRC = 1	100-pin	144-pin
F[5]	PCR[85]	ALT0 ALT1 ALT2 ALT3	GPIO[85] MDO[2] — —	SIUL NEXUS_0 — —	I/O O — —	Slow	Fast	—	5
F[6]	PCR[86]	ALT0 ALT1 ALT2 ALT3	GPIO[86] MDO[1] — —	SIUL NEXUS_0 — —	I/O O — —	Slow	Fast	—	8
F[7]	PCR[87]	ALT0 ALT1 ALT2 ALT3	GPIO[87] MCKO — —	SIUL NEXUS_0 — —	I/O O — —	Slow	Fast	—	19
F[8]	PCR[88]	ALT0 ALT1 ALT2 ALT3	GPIO[88] MSEO1 — —	SIUL NEXUS_0 — —	I/O O — —	Slow	Fast	—	20
F[9]	PCR[89]	ALT0 ALT1 ALT2 ALT3	GPIO[89] MSEO0 — —	SIUL NEXUS_0 — —	I/O O — —	Slow	Fast	—	23
F[10]	PCR[90]	ALT0 ALT1 ALT2 ALT3	GPIO[90] EVTO — —	SIUL NEXUS_0 — —	I/O O — —	Slow	Fast	—	24
F[11]	PCR[91]	ALT0 ALT1 ALT2 ALT3 —	GPIO[91] — — — EVTI	SIUL — — — NEXUS_0	I/O — — — I	Slow	Medium	—	25
F[12]	PCR[92]	ALT0 ALT1 ALT2 ALT3	GPIO[92] ETC[3] — —	SIUL eTimer_1 — —	I/O I/O — —	Slow	Medium	—	106
F[13]	PCR[93]	ALT0 ALT1 ALT2 ALT3	GPIO[92] ETC[4] — —	SIUL eTimer_1 — —	I/O I/O — —	Slow	Medium	—	112

Table 9. Absolute maximum ratings(1) (continued)

Symbol		Parameter	Conditions	Value		Unit
				Min	Max(2)	
V_{INAN0}	SR	ADC0 and shared ADC0/1 analog input voltage(6)	$V_{DD\_HV\_REG}$ > 2.7 V	$V_{SS\_HV\_ADV0}$ – 0.3	$V_{DD\_HV\_ADV0}$ + 0.3	V
			$V_{DD\_HV\_REG}$ < 2.7 V	$V_{SS\_HV\_ADV0}$	$V_{DD\_HV\_ADV0}$	V
V_{INAN1}	SR	ADC1 analog input voltage(7)	$V_{DD\_HV\_REG}$ > 2.7 V	$V_{SS\_HV\_ADV1}$ – 0.3	$V_{DD\_HV\_ADV1}$ + 0.3	V
			$V_{DD\_HV\_REG}$ < 2.7 V	$V_{SS\_HV\_ADV1}$	$V_{DD\_HV\_ADV1}$	V
I_{INJPAD}	SR	Injected input current on any pin during overload condition	—	–10	10	mA
I_{INJSUM}	SR	Absolute sum of all injected input currents during overload condition	—	–50	50	mA
I_{VDD_LV}	SR	Low voltage static current sink through V_{DD_LV}	—	—	155	mA
T_{STG}	SR	Storage temperature	—	–55	150	°C
T_J	SR	Junction temperature under bias	—	–40	150	°C

1. Functional operating conditions are given in the DC electrical characteristics. Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the listed maxima may affect device reliability or cause permanent damage to the device.
2. Absolute maximum voltages are currently maximum burn-in voltages. Absolute maximum specifications for device stress have not yet been determined.
3. The difference between each couple of voltage supplies must be less than 300 mV, $|V_{DD\_HV\_IOy} – V_{DD\_HV\_IOx}| < 300$ mV.
4. The difference between ADC voltage supplies must be less than 100 mV, $|V_{DD\_HV\_ADC1} – V_{DD\_HV\_ADC0}| < 100$ mV.
5. Guaranteed by device validation
6. Not allowed to refer this voltage to $V_{DD\_HV\_ADV1}$, $V_{SS\_HV\_ADV1}$
7. Not allowed to refer this voltage to $V_{DD\_HV\_ADV0}$, $V_{SS\_HV\_ADV0}$

Figure 5 shows the constraints of the different power supplies.

3. The difference between ADC voltage supplies must be less than 100 mV, $|V_{DD\_HV\_ADC1} - V_{DD\_HV\_ADC0}| < 100$ mV.
4. To be connected to emitter of external NPN. Low voltage supplies are not under user control—they are produced by an on-chip voltage regulator—but for the device to function properly the low voltage grounds ($V_{SS\_LV\_xxx}$) must be shorted to high voltage grounds ($V_{SS\_HV\_xxx}$) and the low voltage supply pins ($V_{DD\_LV\_xxx}$) must be connected to the external ballast emitter.
5. The low voltage supplies ($V_{DD\_LV\_xxx}$) are not all independent.

$V_{DD\_LV\_COR1}$ and $V_{DD\_LV\_COR2}$ are shorted internally via double bonding connections with lines that provide the low voltage supply to the data flash module. Similarly, $V_{SS\_LV\_COR1}$ and $V_{SS\_LV\_COR2}$ are internally shorted.

$V_{DD\_LV\_REGCOR}$ and $V_{DD\_LV\_REGCORx}$ are physically shorted internally, as are $V_{SS\_LV\_REGCOR}$ and $V_{SS\_LV\_CORx}$.

Table 11. Recommended operating conditions (3.3 V)

Symbol		Parameter	Conditions	Value		Unit
				Min	Max(1)	
V_{SS}	SR	Device ground	—	0	0	V
$V_{DD\_HV\_IOx}$(2)	SR	3.3 V input/output supply voltage	—	3.0	3.6	V
$V_{SS\_HV\_IOx}$	SR	Input/output ground voltage	—	0	0	V
$V_{DD\_HV\_FL}$	SR	3.3 V code and data flash supply voltage	—	3.0	3.6	V
			Relative to $V_{DD\_HV\_IOx}$	$V_{DD\_HV\_IOx} - 0.1$	$V_{DD\_HV\_IOx} + 0.1$	
$V_{SS\_HV\_FL}$	SR	Code and data flash ground	—	0	0	V
$V_{DD\_HV\_OSC}$	SR	3.3 V crystal oscillator amplifier supply voltage	—	3.0	3.6	V
			Relative to $V_{DD\_HV\_IOx}$	$V_{DD\_HV\_IOx} - 0.1$	$V_{DD\_HV\_IOx} + 0.1$	
$V_{SS\_HV\_OSC}$	SR	3.3 V crystal oscillator amplifier reference voltage	—	0	0	V
$V_{DD\_HV\_REG}$	SR	3.3 V voltage regulator supply voltage	—	3.0	3.6	V
			Relative to $V_{DD\_HV\_IOx}$	$V_{DD\_HV\_IOx} - 0.1$	$V_{DD\_HV\_IOx} + 0.1$	
$V_{DD\_HV\_ADC0}$(3)	SR	3.3 V ADC_0 supply and high reference voltage	—	3.0	5.5	V
			Relative to $V_{DD\_HV\_REG}$	$V_{DD\_HV\_REG} - 0.1$	5.5	
$V_{SS\_HV\_ADC0}$	SR	ADC_0 ground and low reference voltage	—	0	0	V
$V_{DD\_HV\_ADC1}$(3)	SR	3.3 V ADC_1 supply and high reference voltage	—	3.0	5.5	V
			Relative to $V_{DD\_HV\_REG}$	$V_{DD\_HV\_REG} - 0.1$	5.5	
$V_{SS\_HV\_ADC1}$	SR	ADC_1 ground and low reference voltage	—	0	0	V
$V_{DD\_LV\_REGCOR}$(4),(5)	CC	Internal supply voltage	—	—	—	V
$V_{SS\_LV\_REGCOR}$(4)	SR	Internal reference voltage	—	0	0	V
$V_{DD\_LV\_CORx}$(4),(5)	CC	Internal supply voltage	—	—	—	V

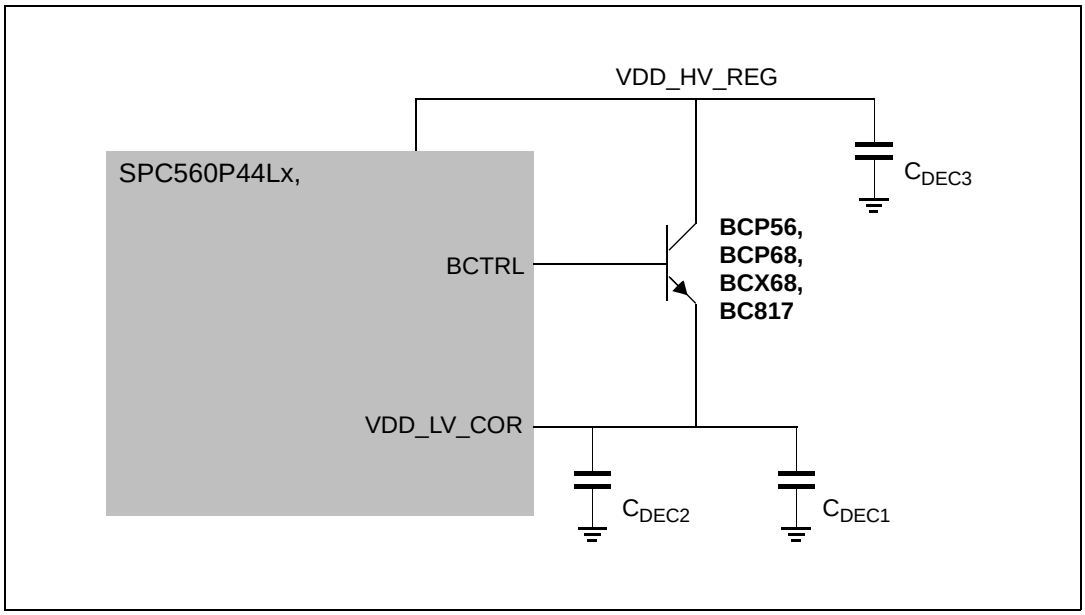


Figure 10. Configuration without resistor on base

Table 18. Voltage regulator electrical characteristics (configuration without resistor on base)

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
$V_{DD\_LV\_REGCOR}$	CC	P	Output voltage under maximum load run supply current configuration	Post-trimming	1.15	—	1.32	V
C_{DEC1}	SR	—	External decoupling/stability ceramic capacitor	4 capacitances	40	56	—	µF
R_{REG}	SR	—	Resulting ESR of all four C_{DEC1}	Absolute maximum value between 100 kHz and 10 MHz	—	—	45	mΩ
C_{DEC2}	SR	—	External decoupling/stability ceramic capacitor	4 capacitances of 100 nF each	400	—	—	nF
C_{DEC3}	SR	—	External decoupling/stability ceramic capacitor on VDD_HV_REG	—	40	—	—	µF
L_{Reg}	SR	—	Resulting ESL of $V_{DD\_HV\_REG}$, BCTRL and $V_{DD\_LV\_CORx}$ pins	—	—	—	15	nH

Table 22. Supply current (5.0 V, NVUSRO[PAD3V5V] = 0)

Symbol	C	Parameter		Conditions		Value		Unit
						Typ	Max	
$I_{DD\_LV\_CORx}$	T	Supply current	RUN—Maximum mode(1)	$V_{DD\_LV\_CORx}$ externally forced at 1.3 V	40 MHz	62	77	mA
					64 MHz	71	88	
			RUN—Typical mode(2)		40 MHz	45	56	
					64 MHz	52	65	
	P		RUN—Maximum mode(3)	$V_{DD\_LV\_CORx}$ externally forced at 1.3 V	64 MHz	60	75	
			HALT mode(4)	$V_{DD\_LV\_CORx}$ externally forced at 1.3 V	—	1.5	10	
			STOP mode(5)	$V_{DD\_LV\_CORx}$ externally forced at 1.3 V	—	1	10	
I_{DD_FLASH}	T		Flash during read	$V_{DD\_HV\_FL}$ at 5.0 V	—	10	12	
			Flash during erase operation on 1 flash module	$V_{DD\_HV\_FL}$ at 5.0 V	—	15	19	
I_{DD_ADC}	T		ADC—Maximum mode(1)	$V_{DD\_HV\_ADC0}$ at 5.0 V $V_{DD\_HV\_ADC1}$ at 5.0 V f_{ADC} = 16 MHz	ADC_1	3.5	5	
					ADC_0	3	4	
			ADC—Typical mode(2)		ADC_1	0.8	1	
					ADC_0	0.005	0.006	
I_{DD_OSC}	T		Oscillator	V_{DD_OSC} at 5.0 V	8 MHz	2.6	3.2	

1. Maximum mode: FlexPWM, ADCs, CTU, DSPI, LINFlex, FlexCAN, 15 output pins, 1st and 2nd PLL enabled. I/O supply current excluded.
2. Typical mode configurations: DSPI, LINFlex, FlexCAN, 15 output pins, 1st PLL only. I/O supply current excluded.
3. Code fetched from RAM, PLL_0: 64 MHz system clock (x4 multiplier with 16 MHz XTAL), PLL_1 is ON at PHI_div2 = 120 MHz and PHI_div3 = 80 MHz, auxiliary clock sources set that all peripherals receive maximum frequency, all peripherals enabled.
4. Halt mode configurations: code fetched from RAM, code and data flash memories in low power mode, OSC/PLL_0/PLL_1 are OFF, core clock frozen, all peripherals are disabled.
5. STOP “P” mode Device Under Test (DUT) configuration: code fetched from RAM, code and data flash memories OFF, OSC/PLL_0/PLL_1 are OFF, core clock frozen, all peripherals are disabled.

3.10.3 DC electrical characteristics (3.3 V)

Table 23 gives the DC electrical characteristics at 3.3 V ($3.0\ V < V_{DD\_HV\_IOx} < 3.6\ V$, NVUSRO[PAD3V5V] = 1); see *Figure 14*.

Table 23. DC electrical characteristics (3.3 V, NVUSRO[PAD3V5V] = 1)(1)

Symbol	C	Parameter	Conditions	Value		Unit
				Min	Max	
V_{IL}	D	Low level input voltage	—	–0.1(2)	—	V
	P		—	—	0.35 $V_{DD\_HV\_IOx}$	V

Calling f_0 the bandwidth of the source signal (and as a consequence the cut-off frequency of the anti-aliasing filter, f_F), according to the Nyquist theorem the conversion rate f_C must be at least $2f_0$; it means that the constant time of the filter is greater than or at least equal to twice the conversion period (T_C). Again the conversion period T_C is longer than the sampling time T_S, which is just a portion of it, even when fixed channel continuous conversion mode is selected (fastest conversion rate at a specific channel): in conclusion it is evident that the time constant of the filter R_FC_F is definitively much higher than the sampling time T_S, so the charge level on C_S cannot be modified by the analog signal source during the time in which the sampling switch is closed.

The considerations above lead to impose new constraints on the external circuit, to reduce the accuracy error due to the voltage drop on C_S; from the two charge balance equations above, it is simple to derive *Equation 11* between the ideal and real sampled voltage on C_S:

Equation 11

$$\frac{V_A}{V_{A2}} = \frac{C_{P1} + C_{P2} + C_F}{C_{P1} + C_{P2} + C_F + C_S}$$

From this formula, in the worst case (when V_A is maximum, that is for instance 5 V), assuming to accept a maximum error of half a count, a constraint is evident on C_F value:

Equation 12

$$C_F > 2048 \bullet C_S$$

3.14.2 ADC conversion characteristics

Table 33. ADC conversion characteristics

Symbol		C	Parameter	Conditions(1)	Value			Unit
					Min	Typ	Max	
V_{INAN0}	SR		ADC0 and shared ADC0/1 analog input voltage(2), (3)	—	$V_{SS\_HV\_ADV0}$ – 0.3	—	$V_{DD\_HV\_ADV0}$ + 0.3	V
V_{INAN1}	SR		ADC1 analog input voltage(2), (4)	—	$V_{SS\_HV\_ADV1}$ – 0.3	—	$V_{DD\_HV\_ADV1}$ + 0.3	V
f_{CK}	SR	—	ADC clock frequency (depends on ADC configuration) (The duty cycle depends on AD_clk(5) frequency)	—	3(6)	—	60	MHz
f_s	SR	—	Sampling frequency	—	—	—	1.53	MHz
t_{ADC_S}	—	D	Sample time(7)	f_{ADC} = 20 MHz, INPSAMP = 3	125	—	—	ns
				f_{ADC} = 9 MHz, INPSAMP = 255	—	—	28.2	µs
t_{ADC_C}	—	P	Conversion time(8)	f_{ADC} = 20 MHz(9), INPCMP = 1	0.650	—	—	µs

Table 40. Nexus debug port timing(1) (continued)

No.	Symbol		C	Parameter	Value			Unit
					Min	Typ	Max	
6	t_{NTDIS}	CC	D	TDI data setup time	6	—	—	ns
	t_{NTMSS}	CC	D	TMS data setup time	6	—	—	ns
7	t_{NTDIH}	CC	D	TDI data hold time	10	—	—	ns
	t_{NTMSH}	CC	D	TMS data hold time	10	—	—	ns
8	t_{TDOV}	CC	D	TCK low to TDO data valid	—	—	35	ns
9	t_{TDOI}	CC	D	TCK low to TDO data invalid	6	—	—	ns

1. All Nexus timing relative to MCKO is measured from 50% of MCKO and 50% of the respective signal.
2. MDO, $\overline{\text{MSEO}}$, and $\overline{\text{EVTO}}$ data is held valid until next MCKO low cycle.
3. Lower frequency is required to be fully compliant to standard.

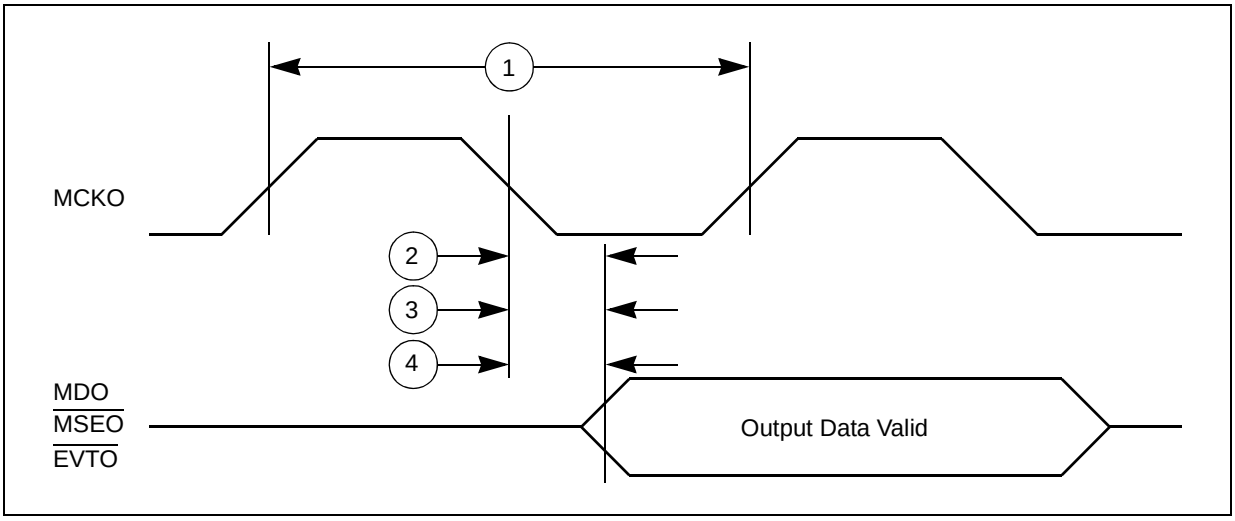


Figure 25. Nexus output timing

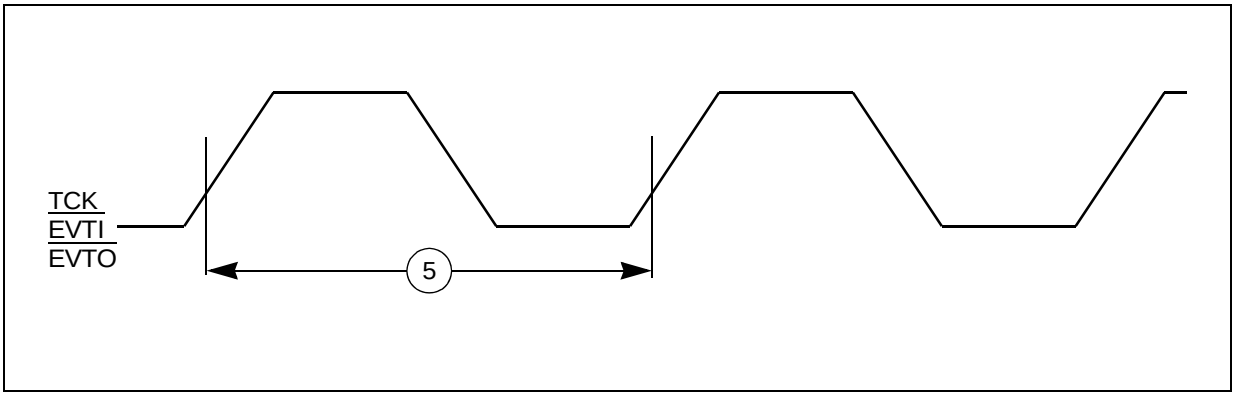
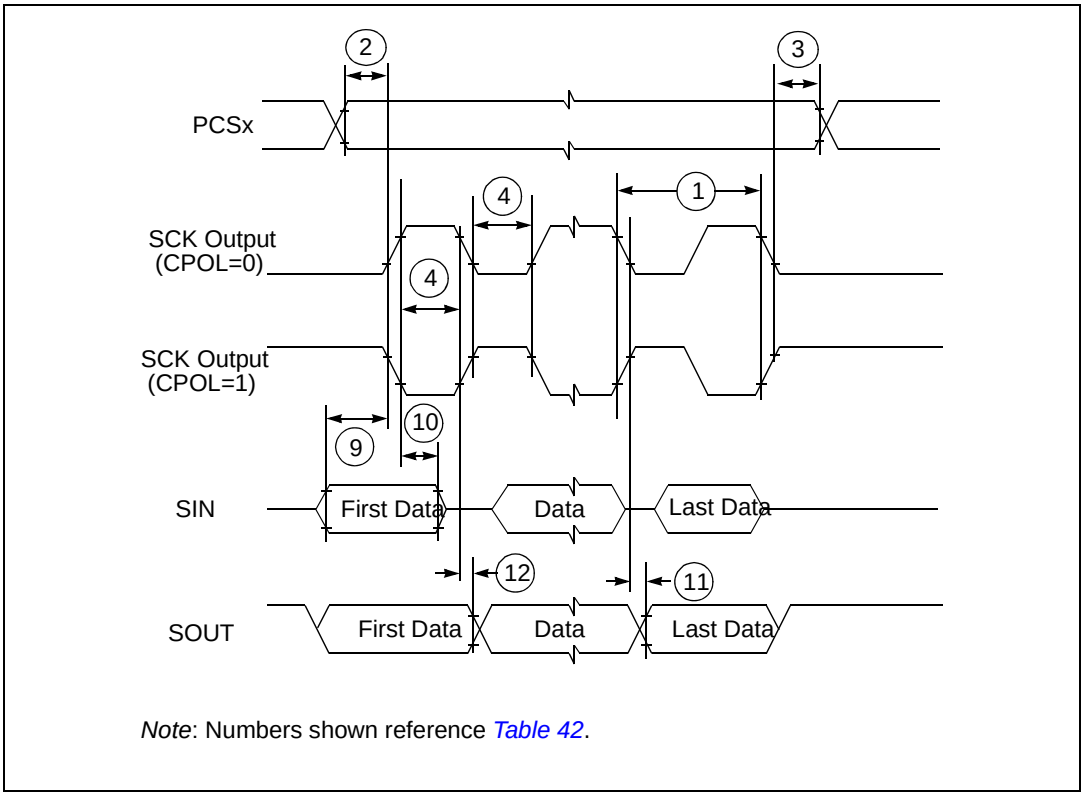


Figure 26. Nexus event trigger and test clock timings

Table 42. DSPI timing(1) (continued)

No.	Symbol		C	Parameter	Conditions	Value		Unit
						Min	Max	
11	t_{SUO}	CC	D	Data valid (after SCK edge)	Master (MTFE = 0)	—	12	ns
					Slave	—	36	
					Master (MTFE = 1, CPHA = 0)	—	12	
					Master (MTFE = 1, CPHA = 1)	—	12	
12	t_{HO}	CC	D	Data hold time for outputs	Master (MTFE = 0)	–2	—	ns
					Slave	6	—	
					Master (MTFE = 1, CPHA = 0)	6	—	
					Master (MTFE = 1, CPHA = 1)	–2	—	

1. All timing is provided with 50 pF capacitance on output, 1 ns transition time on input signal.



Note: Numbers shown reference *Table 42*.

Figure 29. DSPI classic SPI timing – Master, CPHA = 0

Table 44. LQFP100 package mechanical data

Symbol	Dimensions					
	mm			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	—	—	1.600	—	—	0.0630
A1	0.050	—	0.150	0.0020	—	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	—	0.200	0.0035	—	0.0079
D	15.800	16.000	16.200	0.6220	0.6299	0.6378
D1	13.800	14.000	14.200	0.5433	0.5512	0.5591
D3	—	12.000	—	—	0.4724	—
E	15.800	16.000	16.200	0.6220	0.6299	0.6378
E1	13.800	14.000	14.200	0.5433	0.5512	0.5591
E3	—	12.000	—	—	0.4724	—
e	—	0.500	—	—	0.0197	—
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	—	1.000	—	—	0.0394	—
k	0.0°	3.5°	7.0°	0.0°	3.5°	7.0°
ccc[2]	0.08			0.0031		

1. Values in inches are converted from millimeters (mm) and rounded to four decimal digits.
2. Tolerance

Table 46. Revision history (continued)

Date	Revision	Changes
27-Oct-2009	5	- Added “Full Feature“ and “Airbag“ customization. - Removed B[4] and B[5] rows from “Pin muxing” table and inserted them on “System pins” table. - Updated package pinout. - Rewrote entirely section “Power Up/dpwn Sequencing“ section. - Renamend “$V_{DD\_LV\_PLL}$“ and “$V_{SS\_LV\_PLL}$“ supply pins with respectively “$V_{DD\_LV\_COR3}$“ and “$V_{SS\_LV\_COR3}$”. - Added explicative figures on “Electrical characteristics” section. - Updated “Thermal characteristics“ for 100-pin. - Proposed two different configuration of “voltage regulator. - Inserted Power Up/Down sequence. - Added explicative figures on “DC Electrical characteristics”. - Added “I/O pad current specification” section. - Renamed the “Airbag mode” with “Typical mode“and updated the values on “supply current” tables. - Added more order code.
06-Apr-2010	6	Inserted label of Y-axis in the “Independent ADC supply“ figure. “Recommended Operating Conditions” tables: Moved the T_J row to “Absolute Maximum Ratings“ table. Rewrite note 1 and 3 Inverted Min a Typ value of C_{DEC2} on ”Voltage Regulator Electrical Characteristics” table. Removed an useless duplicate of “Voltage Regulator Electrical Characteristics“ table. Inserted the name of C_S into “Input Equivalent Circuit“ figure. Removed leakage Ivpp from datasheet. Updated “Supply Current” tables. Added note on “Output pin transition times“ table. Updated ”Temperature Sensor Electrical Characteristics” table. Updated “16 MHz RC Oscillator Electrical Characteristics” table. Removed the note about the condition from “Flash read access timing“ table. Removed the notes that assert the values need to be confirmed before validation.
07-Apr-2011	7	Formatting and editorial changes throughout Removed all content referencing Junction Temperature Sensor Cover page Features: – CPU core—specified 64 MHz frequency – updated memory features – eTimer units: changed “up/down capabilities” to “up/down count capabilities” – ADC—changed “2 × 13 input channels” to “2 × 11 input channels, + 4 shared channels” – replaced “On-chip CAN/UART/FlexRay bootstrap loader” with “On-chip CAN/UART bootstrap loader” *Section 1: Introduction*: changed title (was: Overview); reorganized contents SPC560P44Lx, SPC560P50Lx device comparison: – ADC feature: changed “16 channels” to “15-channel”; added footnote to to indicate that four channels are shared between the two ADCs – removed SPC560P40 column – changed “dual channel” to “selectable single or dual channel support” in FlexRay footnote – updated “eTimer” feature – updated footnote relative to “Digital power supply” feature

Table 46. Revision history (continued)

Date	Revision	Changes
18-Jul-2012	8	Updated *Table 1 (Device summary)* *Section 1.5.4, Flash memory*: Changed “Data flash memory: 32-bit ECC” to “Data flash memory: 64-bit ECC” *Figure 40 (Commercial product code structure)*, replaced "C = 60 MHz, 5 V" and "D = 60 MHz, 3.3 V" with respectively "C = 40 MHz, 5 V" and "D = 40 MHz, 3.3 V" *Table 9 (Absolute maximum ratings)*, updated TV_{DD} parameter, the minimum value to 3.0 V/s and the maximum value to 0.5 V/µs *Table 7 (Pin muxing)*, changed the description in the column "I/O direction" from "I/O" to "O" for the following port pins: A[10] with function B[0] A[11] with function A[0] A[11] with function A[2] A[12] with function A[2] A[12] with function B[2] A[13] with function B[2] C[7] with function A[1] C[10] with function A[3] C[15] with function A[1] D[0] with function B[1] D[10] with function A[0] D[11] with function B[0] D[13] with function A[1] D[14] with function B[1] Updated *Section 3.8.1, Voltage regulator electrical characteristics* Added *Table 27 (I/O consumption)* *Section 3.10, DC electrical characteristics*: deleted references to “oscillator margin” deleted subsection “NVUSRO[OSCILLATOR_MARGIN] field description” *Table 21 (DC electrical characteristics (5.0 V, NVUSRO[PAD3V5V] = 0))*, added IPU row for $\overline{\text{RESET}}$ pin *Table 23 (DC electrical characteristics (3.3 V, NVUSRO[PAD3V5V] = 1))*, added IPU row for $\overline{\text{RESET}}$ pin *Table 33 (ADC conversion characteristics)*, added V_{INAN} entry Removed “Order codes” table *Figure 40 (Commercial product code structure)*: added a footnote updated “E = Data flash memory”
18-Sep-2013	9	Updated Disclaimer