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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Not For New Designs
Core Processor	e200z0h
Core Size	32-Bit Single-Core
Speed	64MHz
Connectivity	CANbus, LINbus, SPI, UART/USART
Peripherals	DMA, POR, PWM, WDT
Number of I/O	67
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	40K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 26x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/spc560p50l3b1aby

1.5.29	Nexus development interface (NDI)	26
1.5.30	Cyclic redundancy check (CRC)	27
1.5.31	IEEE 1149.1 JTAG controller	27
1.5.32	On-chip voltage regulator (VREG)	28
2	Package pinouts and signal descriptions	29
2.1	Package pinouts	29
2.2	Pin description	31
2.2.1	Power supply and reference voltage pins	31
2.2.2	System pins	33
2.2.3	Pin muxing	34
3	Electrical characteristics	49
3.1	Introduction	49
3.2	Parameter classification	49
3.3	Absolute maximum ratings	50
3.4	Recommended operating conditions	53
3.5	Thermal characteristics	56
3.5.1	Package thermal characteristics	56
3.5.2	General notes for specifications at maximum junction temperature . . .	57
3.6	Electromagnetic interference (EMI) characteristics	59
3.7	Electrostatic discharge (ESD) characteristics	59
3.8	Power management electrical characteristics	59
3.8.1	Voltage regulator electrical characteristics	59
3.8.2	Voltage monitor electrical characteristics	63
3.9	Power up/down sequencing	63
3.10	DC electrical characteristics	65
3.10.1	NVUSRO register	65
3.10.2	DC electrical characteristics (5 V)	66
3.10.3	DC electrical characteristics (3.3 V)	67
3.10.4	Input DC electrical characteristics definition	69
3.10.5	I/O pad current specification	70
3.11	Main oscillator electrical characteristics	75
3.12	FMPLL electrical characteristics	76
3.13	16 MHz RC oscillator electrical characteristics	78

1 Introduction

1.1 Document overview

This document provides electrical specifications, pin assignments, and package diagrams for the SPC560P44/50 series of microcontroller units (MCUs). It also describes the device features and highlights important electrical and physical characteristics. For functional characteristics, refer to the device reference manual.

1.2 Description

This 32-bit system-on-chip (SoC) automotive microcontroller family is the latest achievement in integrated automotive application controllers. It belongs to an expanding range of automotive-focused products designed to address chassis applications—specifically, electrical hydraulic power steering (EHPS) and electric power steering (EPS)—as well as airbag applications.

This family is one of a series of next-generation integrated automotive microcontrollers based on the Power Architecture technology.

The advanced and cost-efficient host processor core of this automotive controller family complies with the Power Architecture embedded category. It operates at speeds of up to 64 MHz and offers high performance processing optimized for low power consumption. It capitalizes on the available development infrastructure of current Power Architecture devices and is supported with software drivers, operating systems and configuration code to assist with users implementations.

1.3 Device comparison

[Table 2](#) provides a summary of different members of the SPC560P44Lx, SPC560P50Lx family and their features—relative to full-featured version—to enable a comparison among the family members and an understanding of the range of functionality offered within this family.

Table 2. SPC560P44Lx, SPC560P50Lx device comparison

Feature	SPC560P44	SPC560P50
Code flash memory (with ECC)	384 KB	512 KB
Data flash memory / EE option (with ECC)	64 KB	
SRAM (with ECC)	36 KB	40 KB
Processor core	32-bit e200z0h	
Instruction set	VLE (variable length encoding)	
CPU performance	0–64 MHz	
FMPLL (frequency-modulated phase-locked loop) module	2	
INTC (interrupt controller) channels	147	
PIT (periodic interrupt timer)	1 (includes four 32-bit timers)	

Table 3. SPC560P44Lx, SPC560P50Lx device configuration differences (continued)

Feature	Full-featured	Airbag
FlexRay	Yes	No
FMPLL (frequency-modulated phase-locked loop) module	2 (one FMPLL, one for FlexRay)	1 (only FMPLL)

1.4 Block diagram

[Figure 1](#) shows a top-level block diagram of the SPC560P44Lx, SPC560P50Lx MCU.

1.5 Feature details

1.5.1 High performance e200z0 core processor

The e200z0 Power Architecture core provides the following features:

- High performance e200z0 core processor for managing peripherals and interrupts
- Single issue 4-stage pipeline in-order execution 32-bit Power Architecture CPU
- Harvard architecture
- Variable length encoding (VLE), allowing mixed 16-bit and 32-bit instructions
 - Results in smaller code size footprint
 - Minimizes impact on performance
- Branch processing acceleration using lookahead instruction buffer
- Load/store unit
 - 1 cycle load latency
 - Misaligned access support
 - No load-to-use pipeline bubbles
- Thirty-two 32-bit general purpose registers (GPRs)
- Separate instruction bus and load/store bus Harvard architecture
- Hardware vectored interrupt support
- Reservation instructions for implementing read-modify-write constructs
- Long cycle time instructions, except for guarded loads, do not increase interrupt latency
- Extensive system development support through Nexus debug port
- Non-maskable interrupt support

1.5.2 Crossbar switch (XBAR)

The XBAR multi-port crossbar switch supports simultaneous connections between four master ports and three slave ports. The crossbar supports a 32-bit address bus width and a 32-bit data bus width.

The crossbar allows for two concurrent transactions to occur from any master port to any slave port; but one of those transfers must be an instruction fetch from internal flash memory. If a slave port is simultaneously requested by more than one master port, arbitration logic will select the higher priority master and grant it ownership of the slave port. All other masters requesting that slave port will be stalled until the higher priority master completes its transactions. Requesting masters will be treated with equal priority and will be granted access to a slave port in round-robin fashion, based upon the ID of the last master to be granted access.

The SIU provides the following features:

- Centralized general purpose input output (GPIO) control of as many as 80 input/output pins and 26 analog input-only pads (package dependent)
- All GPIO pins can be independently configured to support pull-up, pull down, or no pull
- Reading and writing to GPIO supported both as individual pins and 16-bit wide ports
- All peripheral pins (except ADC channels) can be alternatively configured as both general purpose input or output pins
- ADC channels support alternative configuration as general purpose inputs
- Direct readback of the pin value is supported on all pins through the SIUL
- Configurable digital input filter that can be applied to some general purpose input pins for noise elimination: as many as 4 internal functions can be multiplexed onto 1 pin

1.5.17 Boot and censorship

Different booting modes are available in the SPC560P44Lx, SPC560P50Lx: booting from internal flash memory and booting via a serial link.

The default booting scheme uses the internal flash memory (an internal pull-down is used to select this mode). Optionally, the user can boot via FlexCAN or LINFlex (using the boot assist module software).

A censorship scheme is provided to protect the content of the flash memory and offer increased security for the entire device.

A password mechanism is designed to grant the legitimate user access to the non-volatile memory.

Boot assist module (BAM)

The BAM is a block of read-only one-time programmed memory and is identical for all SPC560Pxx devices that are based on the e200z0h core. The BAM program is executed every time the device is powered on if the alternate boot mode has been selected by the user.

The BAM provides the following features:

- Serial bootloading via FlexCAN or LINFlex
- Ability to accept a password via the used serial communication channel to grant the legitimate user access to the non-volatile memory

1.5.18 Error correction status module (ECSM)

The ECSM provides a myriad of miscellaneous control functions regarding program-visible information about the platform configuration and revision levels, a reset status register, a software watchdog timer, wakeup control for exiting sleep modes, and information on platform memory errors reported by error-correcting codes and/or generic access error information for certain processor cores.

The Error Correction Status Module supports a number of miscellaneous control functions for the platform. The ECSM includes these features:

- Registers for capturing information on platform memory errors if error-correcting codes (ECC) are implemented
- For test purposes, optional registers to specify the generation of double-bit memory errors are enabled on the SPC560P44Lx, SPC560P50Lx.

Digital part:

- 2 × 13 input channels including 4 channels shared between the 2 converters
- 4 analog watchdogs comparing ADC results against predefined levels (low, high, range) before results are stored in the appropriate ADC result location,
- 2 modes of operation: Normal mode or CTU control mode
- Normal mode features
 - Register-based interface with the CPU: control register, status register, 1 result register per channel
 - ADC state machine managing 3 request flows: regular command, hardware injected command, software injected command
 - Selectable priority between software and hardware injected commands
 - 4 analog watchdogs comparing ADC results against predefined levels (low, high, range)
 - DMA compatible interface
- CTU control mode features
 - Triggered mode only
 - 4 independent result queues (2 × 16 entries, 2 × 4 entries)
 - Result alignment circuitry (left justified; right justified)
 - 32-bit read mode allows to have channel ID on one of the 16-bit part
 - DMA compatible interfaces

1.5.28 Cross triggering unit (CTU)

The cross triggering unit allows automatic generation of ADC conversion requests on user selected conditions without CPU load during the PWM period and with minimized CPU load for dynamic configuration.

It implements the following features:

- Double buffered trigger generation unit with as many as eight independent triggers generated from external triggers
- Trigger generation unit configurable in sequential mode or in triggered mode
- Each Trigger can be appropriately delayed to compensate the delay of external low pass filter
- Double buffered global trigger unit allowing eTimer synchronization and/or ADC command generation
- Double buffered ADC command list pointers to minimize ADC-trigger unit update
- Double buffered ADC conversion command list with as many as 24 ADC commands
- Each trigger has the capability to generate consecutive commands
- ADC conversion command allows to control ADC channel from each ADC, single or synchronous sampling, independent result queue selection

1.5.29 Nexus development interface (NDI)

The NDI (Nexus Development Interface) block provides real-time development support capabilities for the SPC560P44Lx, SPC560P50Lx Power Architecture based MCU in compliance with the IEEE-ISTO 5001-2003 standard. This development support is supplied for MCUs without requiring external address and data pins for internal visibility. The NDI

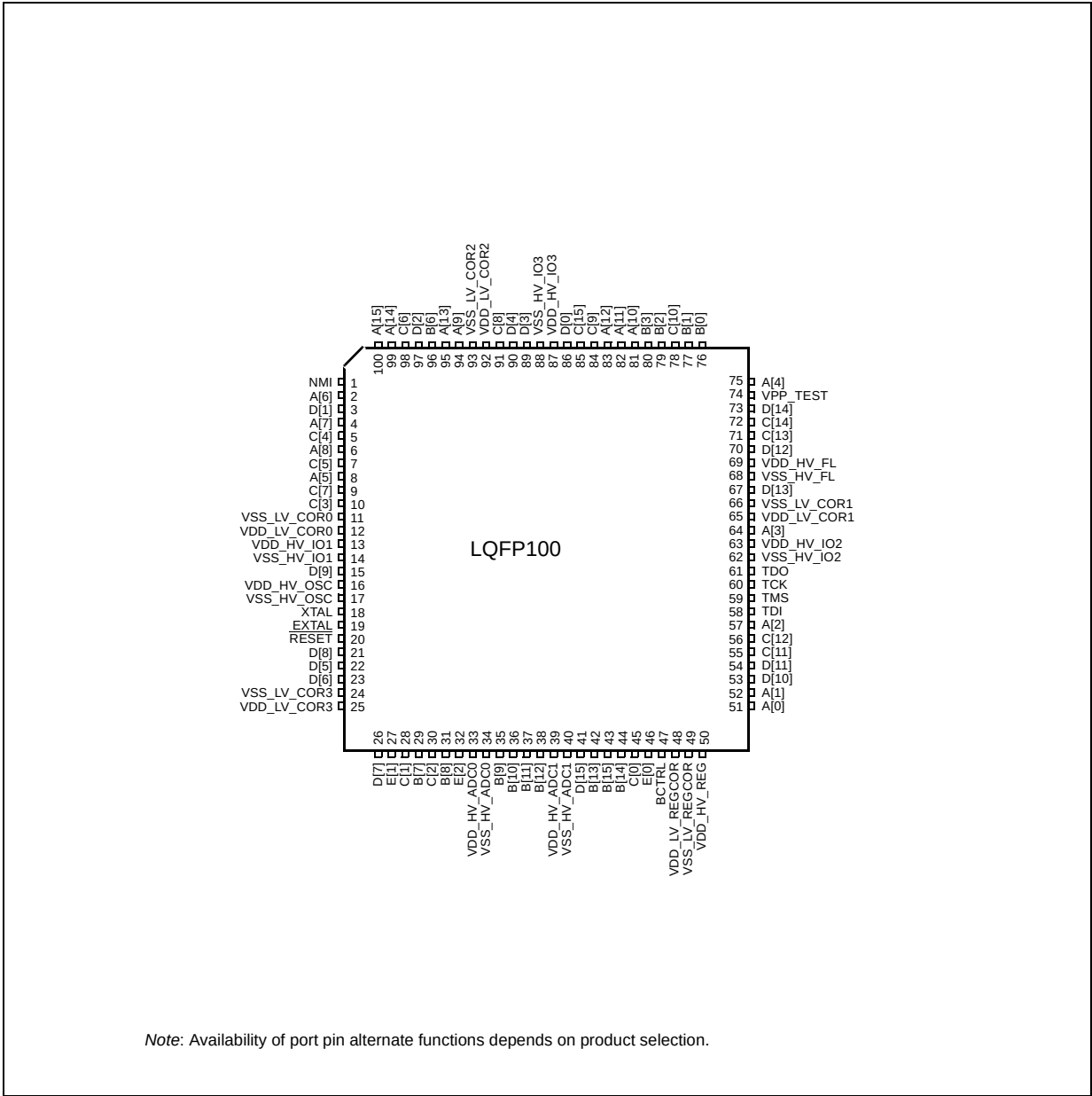


Figure 3. 100-pin LQFP pinout – Airbag configuration (top view)

Table 7. Pin muxing (continued)

Port pin	Pad configuration register (PCR)	Alternate function ⁽¹⁾ , (2)	Functions	Peripheral ⁽³⁾	I/O direction ⁽⁴⁾	Pad speed ⁽⁵⁾		Pin No.	
						SRC = 0	SRC = 1	100-pin	144-pin
C[5]	PCR[37]	ALT0 ALT1 ALT2 ALT3 — —	GPIO[37] SCK — DEBUG[5] FAULT[3] EIRQ[23]	SIUL DSPI_0 — SSCM FlexPWM_0 SIUL	I/O I/O — — I I	Slow	Medium	7	13
C[6]	PCR[38]	ALT0 ALT1 ALT2 ALT3 —	GPIO[38] SOUT B[1] DEBUG[6] EIRQ[24]	SIUL DSPI_0 FlexPWM_0 SSCM SIUL	I/O I/O O — I	Slow	Medium	98	142
C[7]	PCR[39]	ALT0 ALT1 ALT2 ALT3 —	GPIO[39] — A[1] DEBUG[7] SIN	SIUL — FlexPWM_0 SSCM DSPI_0	I/O — O — I	Slow	Medium	9	15
C[8]	PCR[40]	ALT0 ALT1 ALT2 ALT3 —	GPIO[40] CS1 — CS6 FAULT[2]	SIUL DSPI_1 — DSPI_0 FlexPWM_0	I/O O — O I	Slow	Medium	91	130
C[9]	PCR[41]	ALT0 ALT1 ALT2 ALT3 —	GPIO[41] CS3 — X[3] FAULT[2]	SIUL DSPI_2 — FlexPWM_0 FlexPWM_0	I/O O — I/O I	Slow	Medium	84	123
C[10]	PCR[42]	ALT0 ALT1 ALT2 ALT3 —	GPIO[42] CS2 — A[3] FAULT[1]	SIUL DSPI_2 — FlexPWM_0 FlexPWM_0	I/O O — O I	Slow	Medium	78	111
C[11]	PCR[43]	ALT0 ALT1 ALT2 ALT3	GPIO[43] ETC[4] CS2 CS0	SIUL eTimer_0 DSPI_2 DSPI_3	I/O I/O O I/O	Slow	Medium	55	80
C[12]	PCR[44]	ALT0 ALT1 ALT2 ALT3	GPIO[44] ETC[5] CS3 CS1	SIUL eTimer_0 DSPI_2 DSPI_3	I/O I/O O O	Slow	Medium	56	82

Table 7. Pin muxing (continued)

Port pin	Pad configuration register (PCR)	Alternate function ⁽¹⁾ , (2)	Functions	Peripheral ⁽³⁾	I/O direction ⁽⁴⁾	Pad speed ⁽⁵⁾		Pin No.	
						SRC = 0	SRC = 1	100-pin	144-pin
E[13]	PCR[77]	ALT0 ALT1 ALT2 ALT3 —	GPIO[77] SCK — — EIRQ[25]	SIUL DSPI_3 — — SIUL	I/O I/O — — I	Slow	Medium	—	117
E[14]	PCR[78]	ALT0 ALT1 ALT2 ALT3 —	GPIO[78] SOUT — — EIRQ[26]	SIUL DSPI_3 — — SIUL	I/O O — — I	Slow	Medium	—	119
E[15]	PCR[79]	ALT0 ALT1 ALT2 ALT3 — —	GPIO[79] — — — SIN EIRQ[27]	SIUL — — — DSPI_3 SIUL	I/O — — — I I	Slow	Medium	—	121
Port F (16-bit)									
F[0]	PCR[80]	ALT0 ALT1 ALT2 ALT3 —	GPIO[80] DBG0 CS3 — EIRQ[28]	SIUL FlexRay_0 DSPI_3 — SIUL	I/O O O — I	Slow	Medium	—	133
F[1]	PCR[81]	ALT0 ALT1 ALT2 ALT3 —	GPIO[81] DBG1 CS2 — EIRQ[29]	SIUL FlexRay_0 DSPI_3 — SIUL	I/O O O — I	Slow	Medium	—	135
F[2]	PCR[82]	ALT0 ALT1 ALT2 ALT3	GPIO[82] DBG2 CS1 —	SIUL FlexRay_0 DSPI_3 —	I/O O O —	Slow	Medium	—	137
F[3]	PCR[83]	ALT0 ALT1 ALT2 ALT3	GPIO[83] DBG3 CS0 —	SIUL FlexRay_0 DSPI_3 —	I/O O I/O —	Slow	Medium	—	139
F[4]	PCR[84]	ALT0 ALT1 ALT2 ALT3	GPIO[84] MDO[3] — —	SIUL NEXUS_0 — —	I/O O — —	Slow	Fast	—	4

Table 7. Pin muxing (continued)

Port pin	Pad configuration register (PCR)	Alternate function ⁽¹⁾ , (2)	Functions	Peripheral ⁽³⁾	I/O direction ⁽⁴⁾	Pad speed ⁽⁵⁾		Pin No.	
						SRC = 0	SRC = 1	100-pin	144-pin
F[5]	PCR[85]	ALT0 ALT1 ALT2 ALT3	GPIO[85] MDO[2] — —	SIUL NEXUS_0 — —	I/O O — —	Slow	Fast	—	5
F[6]	PCR[86]	ALT0 ALT1 ALT2 ALT3	GPIO[86] MDO[1] — —	SIUL NEXUS_0 — —	I/O O — —	Slow	Fast	—	8
F[7]	PCR[87]	ALT0 ALT1 ALT2 ALT3	GPIO[87] MCKO — —	SIUL NEXUS_0 — —	I/O O — —	Slow	Fast	—	19
F[8]	PCR[88]	ALT0 ALT1 ALT2 ALT3	GPIO[88] MSEO1 — —	SIUL NEXUS_0 — —	I/O O — —	Slow	Fast	—	20
F[9]	PCR[89]	ALT0 ALT1 ALT2 ALT3	GPIO[89] MSEO0 — —	SIUL NEXUS_0 — —	I/O O — —	Slow	Fast	—	23
F[10]	PCR[90]	ALT0 ALT1 ALT2 ALT3	GPIO[90] EVTO — —	SIUL NEXUS_0 — —	I/O O — —	Slow	Fast	—	24
F[11]	PCR[91]	ALT0 ALT1 ALT2 ALT3 —	GPIO[91] — — — EVTI	SIUL — — — NEXUS_0	I/O — — — I	Slow	Medium	—	25
F[12]	PCR[92]	ALT0 ALT1 ALT2 ALT3	GPIO[92] ETC[3] — —	SIUL eTimer_1 — —	I/O I/O — —	Slow	Medium	—	106
F[13]	PCR[93]	ALT0 ALT1 ALT2 ALT3	GPIO[92] ETC[4] — —	SIUL eTimer_1 — —	I/O I/O — —	Slow	Medium	—	112

Table 9. Absolute maximum ratings⁽¹⁾ (continued)

Symbol		Parameter	Conditions	Value		Unit
				Min	Max ⁽²⁾	
V _{INAN0}	SR	ADC0 and shared ADC0/1 analog input voltage ⁽⁶⁾	$V_{DD_HV_REG} > 2.7\text{ V}$	$V_{SS_HV_ADV0} - 0.3$	$V_{DD_HV_ADV0} + 0.3$	V
			$V_{DD_HV_REG} < 2.7\text{ V}$	$V_{SS_HV_ADV0}$	$V_{DD_HV_ADV0}$	V
V _{INAN1}	SR	ADC1 analog input voltage ⁽⁷⁾	$V_{DD_HV_REG} > 2.7\text{ V}$	$V_{SS_HV_ADV1} - 0.3$	$V_{DD_HV_ADV1} + 0.3$	V
			$V_{DD_HV_REG} < 2.7\text{ V}$	$V_{SS_HV_ADV1}$	$V_{DD_HV_ADV1}$	V
I _{INJPAD}	SR	Injected input current on any pin during overload condition	—	−10	10	mA
I _{INJSUM}	SR	Absolute sum of all injected input currents during overload condition	—	−50	50	mA
I _{VDD_LV}	SR	Low voltage static current sink through V _{DD_LV}	—	—	155	mA
T _{STG}	SR	Storage temperature	—	−55	150	°C
T _J	SR	Junction temperature under bias	—	−40	150	°C

- Functional operating conditions are given in the DC electrical characteristics. Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the listed maxima may affect device reliability or cause permanent damage to the device.
- Absolute maximum voltages are currently maximum burn-in voltages. Absolute maximum specifications for device stress have not yet been determined.
- The difference between each couple of voltage supplies must be less than 300 mV, $|V_{DD_HV_IOy} - V_{DD_HV_IOx}| < 300\text{ mV}$.
- The difference between ADC voltage supplies must be less than 100 mV, $|V_{DD_HV_ADC1} - V_{DD_HV_ADC0}| < 100\text{ mV}$.
- Guaranteed by device validation
- Not allowed to refer this voltage to V_{DD_HV_ADV1}, V_{SS_HV_ADV1}
- Not allowed to refer this voltage to V_{DD_HV_ADV0}, V_{SS_HV_ADV0}

Figure 5 shows the constraints of the different power supplies.

3.4 Recommended operating conditions

Table 10. Recommended operating conditions (5.0 V)

Symbol		Parameter	Conditions	Value		Unit
				Min	Max ⁽¹⁾	
V _{SS}	SR	Device ground	—	0	0	V
V _{DD_HV_IOx} ⁽²⁾	SR	5.0 V input/output supply voltage	—	4.5	5.5	V
V _{SS_HV_IOx}	SR	Input/output ground voltage	—	0	0	V
V _{DD_HV_FL}	SR	5.0 V code and data flash supply voltage	—	4.5	5.5	V
			Relative to V _{DD_HV_IOx}	V _{DD_HV_IOx} - 0.1	V _{DD_HV_IOx} + 0.1	
V _{SS_HV_FL}	SR	Code and data flash ground	—	0	0	V
V _{DD_HV_OSC}	SR	5.0 V crystal oscillator amplifier supply voltage	—	4.5	5.5	V
			Relative to V _{DD_HV_IOx}	V _{DD_HV_IOx} - 0.1	V _{DD_HV_IOx} + 0.1	
V _{SS_HV_OSC}	SR	5.0 V crystal oscillator amplifier reference voltage	—	0	0	V
V _{DD_HV_REG}	SR	5.0 V voltage regulator supply voltage	—	4.5	5.5	V
			Relative to V _{DD_HV_IOx}	V _{DD_HV_IOx} - 0.1	V _{DD_HV_IOx} + 0.1	
V _{DD_HV_ADC0} ⁽³⁾	SR	5.0 V ADC_0 supply and high reference voltage	—	4.5	5.5	V
			Relative to V _{DD_HV_REG}	V _{DD_HV_REG} - 0.1	—	
V _{SS_HV_ADC0}	SR	ADC_0 ground and low reference voltage	—	0	0	V
V _{DD_HV_ADC1} ⁽³⁾	SR	5.0 V ADC_1 supply and high reference voltage	—	4.5	5.5	V
			Relative to V _{DD_HV_REG}	V _{DD_HV_REG} - 0.1	—	
V _{SS_HV_ADC1}	SR	ADC_1 ground and low reference voltage	—	0	0	V
V _{DD_LV_REGCOR} ^{(4),(5)}	CC	Internal supply voltage	—	—	—	V
V _{SS_LV_REGCOR} ⁽⁴⁾	SR	Internal reference voltage	—	0	0	V
V _{DD_LV_CORx} ^{(4),(5)}	CC	Internal supply voltage	—	—	—	V
V _{SS_LV_CORx} ⁽⁴⁾	SR	Internal reference voltage	—	0	0	V
T _A	SR	Ambient temperature under bias	f _{CPU} = 64 MHz	-40	105	°C
			f _{CPU} = 60 MHz	-40	125	

1. Parametric figures can be out of specification when voltage drops below 4.5 V, however, guaranteeing the full functionality. In particular, ADC electrical characteristics and I/Os DC electrical specification may not be guaranteed.

2. The difference between each couple of voltage supplies must be less than 100 mV, $|V_{DD_HV_IOy} - V_{DD_HV_IOx}| < 100 \text{ mV}$.

2. Junction-to-board thermal resistance determined per JEDEC JESD51-8. Thermal test board meets JEDEC specification for the specified package.
3. Junction-to-case at the top of the package determined using MIL-STD 883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer.
4. Thermal characterization parameter indicating the temperature difference between the board and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JB.
5. Thermal characterization parameter indicating the temperature difference between the case and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JC.

Table 13. Thermal characteristics for 100-pin LQFP

Symbol	Parameter	Conditions	Typical value	Unit
$R_{\theta JA}$	Thermal resistance junction-to-ambient, natural convection ⁽¹⁾	Single layer board—1s	47.3	°C/W
		Four layer board—2s2p	35.3	°C/W
$R_{\theta JB}$	Thermal resistance junction-to-board ⁽²⁾	Four layer board—2s2p	19.1	°C/W
$R_{\theta JCtop}$	Thermal resistance junction-to-case (top) ⁽³⁾	Single layer board—1s	9.7	°C/W
Ψ_{JB}	Junction-to-board, natural convection ⁽⁴⁾	Operating conditions	19.1	°C/W
Ψ_{JC}	Junction-to-case, natural convection ⁽⁵⁾	Operating conditions	0.8	°C/W

1. Junction-to-ambient thermal resistance determined per JEDEC JESD51-7. Thermal test board meets JEDEC specification for this package.
2. Junction-to-board thermal resistance determined per JEDEC JESD51-8. Thermal test board meets JEDEC specification for the specified package.
3. Junction-to-case at the top of the package determined using MIL-STD 883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer.
4. Thermal characterization parameter indicating the temperature difference between the board and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JB.
5. Thermal characterization parameter indicating the temperature difference between the case and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JC.

3.5.2 General notes for specifications at maximum junction temperature

An estimation of the chip junction temperature, T_J , can be obtained from [Equation 1](#):

$$\text{Equation 1 } T_J = T_A + (R_{\theta JA} * P_D)$$

where:

T_A = ambient temperature for the package (°C)

$R_{\theta JA}$ = junction to ambient thermal resistance (°C/W)

P_D = power dissipation in the package (W)

The junction to ambient thermal resistance is an industry standard value that provides a quick and easy estimation of thermal performance. Unfortunately, there are two values in

3.8.2 Voltage monitor electrical characteristics

The device implements a Power-on Reset module to ensure correct power-up initialization, as well as three low voltage detectors to monitor the V_{DD} and the V_{DD_LV} voltage while device is supplied:

- POR monitors V_{DD} during the power-up phase to ensure device is maintained in a safe reset state
- LVDHV3 monitors V_{DD} to ensure device reset below minimum functional supply
- LVDHV5 monitors V_{DD} when application uses device in the $5.0\text{ V} \pm 10\%$ range
- LVDLVCOR monitors low voltage digital power domain

Table 19. Low voltage monitor electrical characteristics

Symbol	C	Parameter	Conditions (1)	Value		Unit
				Min	Max	
V_{PORH}	T	Power-on reset threshold	—	1.5	2.7	V
V_{PORUP}	P	Supply for functional POR module	$T_A = 25\text{ °C}$	1.0	—	V
$V_{REGLVDMOK_H}$	P	Regulator low voltage detector high threshold	—	—	2.95	V
$V_{REGLVDMOK_L}$	P	Regulator low voltage detector low threshold	—	2.6	—	V
$V_{FLLVDMOK_H}$	P	Flash low voltage detector high threshold	—	—	2.95	V
$V_{FLLVDMOK_L}$	P	Flash low voltage detector low threshold	—	2.6	—	V
$V_{IOLVDMOK_H}$	P	I/O low voltage detector high threshold	—	—	2.95	V
$V_{IOLVDMOK_L}$	P	I/O low voltage detector low threshold	—	2.6	—	V
$V_{IOLVDM5OK_H}$	P	I/O 5V low voltage detector high threshold	—	—	4.4	V
$V_{IOLVDM5OK_L}$	P	I/O 5V low voltage detector low threshold	—	3.8	—	V
$V_{MLVDDOK_H}$	P	Digital supply low voltage detector high	—	—	1.145	V
$V_{MLVDDOK_L}$	P	Digital supply low voltage detector low	—	1.08	—	V

1. $V_{DD} = 3.3\text{ V} \pm 10\% / 5.0\text{ V} \pm 10\%$, $T_A = -40\text{ °C}$ to $T_{A\text{ MAX}}$, unless otherwise specified

3.9 Power up/down sequencing

To prevent an overstress event or a malfunction within and outside the device, the SPC560P44Lx, SPC560P50Lx implements the following sequence to ensure each module is started only when all conditions for switching it ON are available:

- A POWER_ON module working on voltage regulator supply controls the correct start-up of the regulator. This is a key module ensuring safe configuration for all voltage regulator functionality when supply is below 1.5V. Associated POWER_ON (or POR) signal is active low.
- Several low voltage detectors, working on voltage regulator supply monitor the voltage of the critical modules (voltage regulator, I/Os, flash memory and low voltage domain). LVDs are gated low when POWER_ON is active.
- A POWER_OK signal is generated when all critical supplies monitored by the LVD are available. This signal is active high and released to all modules including I/Os, flash

Table 23. DC electrical characteristics (3.3 V, NVUSRO[PAD3V5V] = 1)⁽¹⁾ (continued)

Symbol	C	Parameter	Conditions	Value		Unit
				Min	Max	
V _{IH}	P	High level input voltage	—	0.65 V _{DD_HV_IOx}	—	V
	D		—	—	V _{DD_HV_IOx} + 0.1 ⁽²⁾	V
V _{HYS}	T	Schmitt trigger hysteresis	—	0.1 V _{DD_HV_IOx}	—	V
V _{OL_S}	P	Slow, low level output voltage	I _{OL} = 1.5 mA	—	0.5	V
V _{OH_S}	P	Slow, high level output voltage	I _{OH} = -1.5 mA	V _{DD_HV_IOx} - 0.8	—	V
V _{OL_M}	P	Medium, low level output voltage	I _{OL} = 2 mA	—	0.5	V
V _{OH_M}	P	Medium, high level output voltage	I _{OH} = -2 mA	V _{DD_HV_IOx} - 0.8	—	V
V _{OL_F}	P	Fast, low level output voltage	I _{OL} = 1.5 mA	—	0.5	V
V _{OH_F}	P	Fast, high level output voltage	I _{OH} = -1.5 mA	V _{DD_HV_IOx} - 0.8	—	V
V _{OL_SYM}	P	Symmetric, low level output voltage	I _{OL} = 1.5 mA	—	0.5	V
V _{OH_SYM}	P	Symmetric, high level output voltage	I _{OH} = -1.5 mA	V _{DD_HV_IOx} - 0.8	—	V
I _{PU}	P	Equivalent pull-up current	V _{IN} = V _{IL}	-130	—	μA
			V _{IN} = V _{IH}	—	-10	
I _{PD}	P	Equivalent pull-down current	V _{IN} = V _{IL}	10	—	μA
			V _{IN} = V _{IH}	—	130	
I _{IL}	P	Input leakage current (all bidirectional ports)	T _A = -40 to 125 °C	—	1	μA
I _{IL}	P	Input leakage current (all ADC input-only ports)	T _A = -40 to 125 °C	—	0.5	μA
C _{IN}	D	Input capacitance	—	—	10	pF
I _{PU}	D	$\overline{\text{RESET}}$, equivalent pull-up current	V _{IN} = V _{IL}	-130	—	μA
			V _{IN} = V _{IH}	—	-10	

1. These specifications are design targets and subject to change per device characterization.

2. "SR" parameter values must not exceed the absolute maximum ratings shown in [Table 9](#).

Table 26. I/O weight (continued)

Pad	LQFP144		LQFP100	
	Weight 5V	Weight 3.3V	Weight 5V	Weight 3.3V
PAD[86]	9%	6%	—	—
MODO[0]	12%	8%	—	—
PAD[7]	4%	4%	11%	10%
PAD[36]	5%	4%	11%	9%
PAD[8]	5%	4%	10%	9%
PAD[37]	5%	4%	10%	9%
PAD[5]	5%	4%	9%	8%
PAD[39]	5%	4%	9%	8%
PAD[35]	5%	4%	8%	7%
PAD[87]	12%	9%	—	—
PAD[88]	9%	6%	—	—
PAD[89]	10%	7%	—	—
PAD[90]	15%	11%	—	—
PAD[91]	6%	5%	—	—
PAD[57]	8%	7%	8%	7%
PAD[56]	13%	11%	13%	11%
PAD[53]	14%	12%	14%	12%
PAD[54]	15%	13%	15%	13%
PAD[55]	25%	22%	25%	22%
PAD[96]	27%	24%	—	—
PAD[65]	1%	1%	1%	1%
PAD[67]	1%	1%	—	—
PAD[33]	1%	1%	1%	1%
PAD[68]	1%	1%	—	—
PAD[23]	1%	1%	1%	1%
PAD[69]	1%	1%	—	—
PAD[34]	1%	1%	1%	1%
PAD[70]	1%	1%	—	—
PAD[24]	1%	1%	1%	1%
PAD[71]	1%	1%	—	—
PAD[66]	1%	1%	1%	1%
PAD[25]	1%	1%	1%	1%
PAD[26]	1%	1%	1%	1%

Table 26. I/O weight (continued)

Pad	LQFP144		LQFP100	
	Weight 5V	Weight 3.3V	Weight 5V	Weight 3.3V
PAD[60]	11%	10%	11%	10%
PAD[100]	12%	10%	—	—
PAD[45]	12%	10%	12%	10%
PAD[98]	12%	11%	—	—
PAD[46]	12%	11%	12%	11%
PAD[99]	13%	11%	—	—
PAD[62]	13%	11%	13%	11%
PAD[92]	13%	12%	—	—
VPP_TEST	1%	1%	1%	1%
PAD[4]	14%	12%	14%	12%
PAD[16]	13%	12%	13%	12%
PAD[17]	13%	11%	13%	11%
PAD[42]	13%	11%	13%	11%
PAD[93]	12%	11%	—	—
PAD[95]	12%	11%	—	—
PAD[18]	12%	10%	12%	10%
PAD[94]	11%	10%	—	—
PAD[19]	11%	10%	11%	10%
PAD[77]	10%	9%	—	—
PAD[10]	10%	9%	10%	9%
PAD[78]	9%	8%	—	—
PAD[11]	9%	8%	9%	8%
PAD[79]	8%	7%	—	—
PAD[12]	7%	7%	7%	7%
PAD[41]	7%	6%	7%	6%
PAD[47]	5%	4%	5%	4%
PAD[48]	4%	4%	4%	4%
PAD[51]	4%	4%	4%	4%
PAD[52]	5%	4%	5%	4%
PAD[40]	5%	5%	6%	5%
PAD[80]	9%	8%	—	—
PAD[9]	10%	9%	11%	10%
PAD[81]	10%	9%	—	—

Table 36. Flash memory read access timing

Symbol	C	Parameter	Conditions ⁽¹⁾	Max value	Unit
$f_{\max}$	C	Maximum working frequency at given number of wait states in worst conditions	2 wait states	66	MHz
			0 wait states	18	

1. $V_{DD} = 3.3 \text{ V} \pm 10\% / 5.0 \text{ V} \pm 10\%$, $T_A = -40$ to 125°C , unless otherwise specified

3.16 AC specifications

3.16.1 Pad AC specifications

Table 37. Output pin transition times

Symbol	C	Parameter	Conditions ⁽¹⁾	Value			Unit
				Min	Typ	Max	
t_{tr}	CC	Output transition time output pin ⁽²⁾ SLOW configuration	$C_L = 25 \text{ pF}$	—	—	50	ns
			$C_L = 50 \text{ pF}$	—	—	100	
			$C_L = 100 \text{ pF}$	—	—	125	
			$C_L = 25 \text{ pF}$	—	—	40	
			$C_L = 50 \text{ pF}$	—	—	50	
			$C_L = 100 \text{ pF}$	—	—	75	
t_{tr}	CC	Output transition time output pin ⁽²⁾ MEDIUM configuration	$C_L = 25 \text{ pF}$	—	—	10	ns
			$C_L = 50 \text{ pF}$	—	—	20	
			$C_L = 100 \text{ pF}$	—	—	40	
			$C_L = 25 \text{ pF}$	—	—	12	
			$C_L = 50 \text{ pF}$	—	—	25	
			$C_L = 100 \text{ pF}$	—	—	40	
t_{tr}	CC	Output transition time output pin ⁽²⁾ FAST configuration	$C_L = 25 \text{ pF}$	—	—	4	ns
			$C_L = 50 \text{ pF}$	—	—	6	
			$C_L = 100 \text{ pF}$	—	—	12	
			$C_L = 25 \text{ pF}$	—	—	4	
			$C_L = 50 \text{ pF}$	—	—	7	
			$C_L = 100 \text{ pF}$	—	—	12	
$t_{SYM}^{(3)}$	CC	Symmetric transition time, same drive strength between N and P transistor	$V_{DD} = 5.0 \text{ V} \pm 10\%$, $PAD3V5V = 0$	—	—	4	ns
			$V_{DD} = 3.3 \text{ V} \pm 10\%$, $PAD3V5V = 1$	—	—	5	

1. $V_{DD} = 3.3 \text{ V} \pm 10\% / 5.0 \text{ V} \pm 10\%$, $T_A = -40^\circ\text{C}$ to $T_{A \text{ MAX}}$, unless otherwise specified

2. C_L includes device and package capacitances ($C_{PKG} < 5 \text{ pF}$).

3. Transition timing of both positive and negative slopes will differ maximum 50%

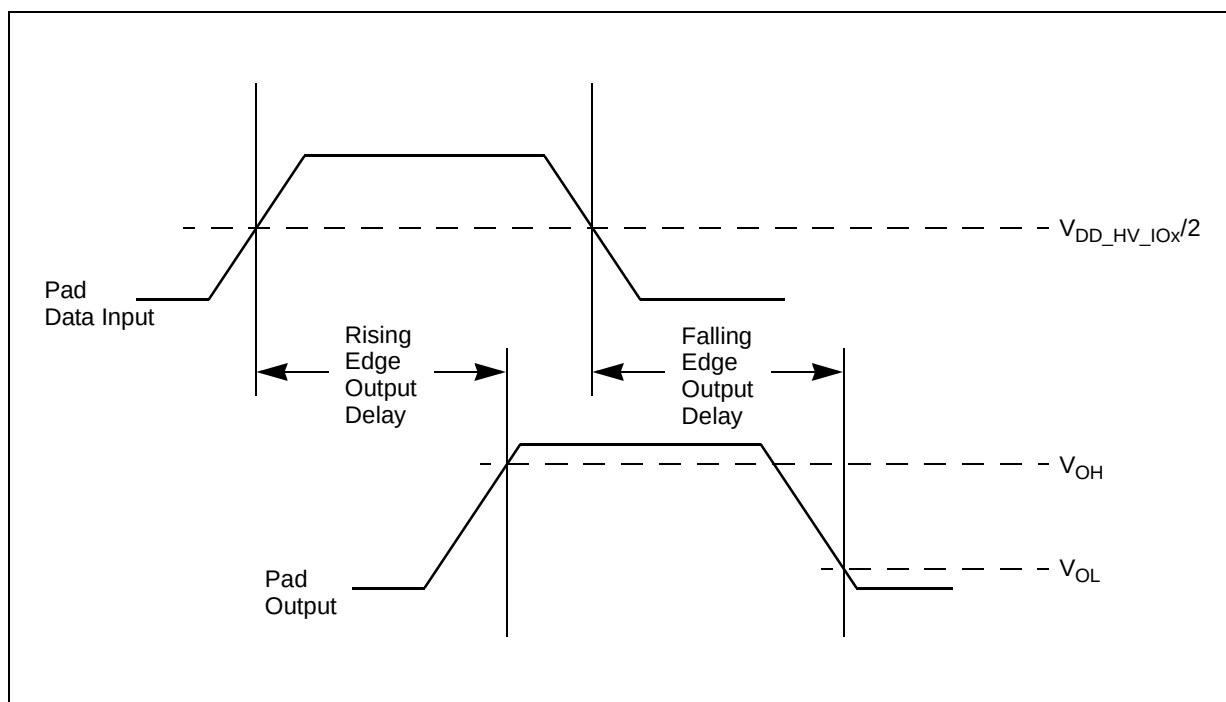


Figure 19. Pad output delay

3.17 AC timing characteristics

3.17.1 $\overline{\text{RESET}}$ pin characteristics

The SPC560P44Lx, SPC560P50Lx implements a dedicated bidirectional $\overline{\text{RESET}}$ pin.

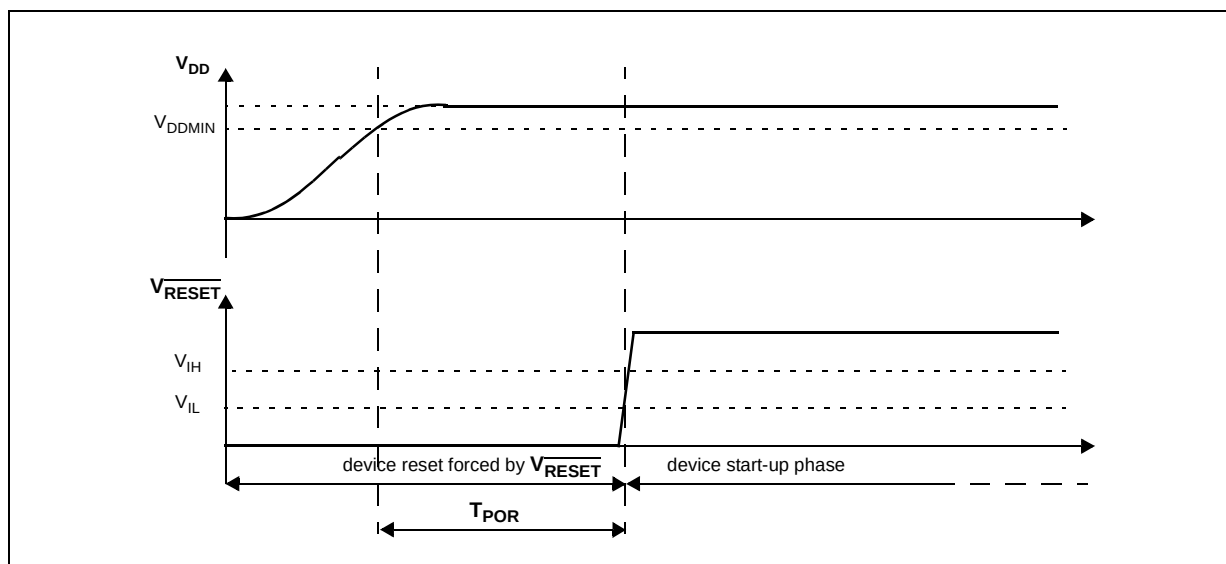


Figure 20. Start-up reset requirements

Table 44. LQFP100 package mechanical data

Symbol	Dimensions					
	mm			inches ⁽¹⁾		
	Min	Typ	Max	Min	Typ	Max
A	—	—	1.600	—	—	0.0630
A1	0.050	—	0.150	0.0020	—	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	—	0.200	0.0035	—	0.0079
D	15.800	16.000	16.200	0.6220	0.6299	0.6378
D1	13.800	14.000	14.200	0.5433	0.5512	0.5591
D3	—	12.000	—	—	0.4724	—
E	15.800	16.000	16.200	0.6220	0.6299	0.6378
E1	13.800	14.000	14.200	0.5433	0.5512	0.5591
E3	—	12.000	—	—	0.4724	—
e	—	0.500	—	—	0.0197	—
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	—	1.000	—	—	0.0394	—
k	0.0°	3.5°	7.0°	0.0°	3.5°	7.0°
ccc ⁽²⁾	0.08			0.0031		

1. Values in inches are converted from millimeters (mm) and rounded to four decimal digits.

2. Tolerance