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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	e200z0h
Core Size	32-Bit Single-Core
Speed	64MHz
Connectivity	CANbus, LINbus, SPI, UART/USART
Peripherals	DMA, POR, PWM, WDT
Number of I/O	67
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	40K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 26x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/spc560p50l3befar

Table 2. SPC560P44Lx, SPC560P50Lx device comparison (continued)

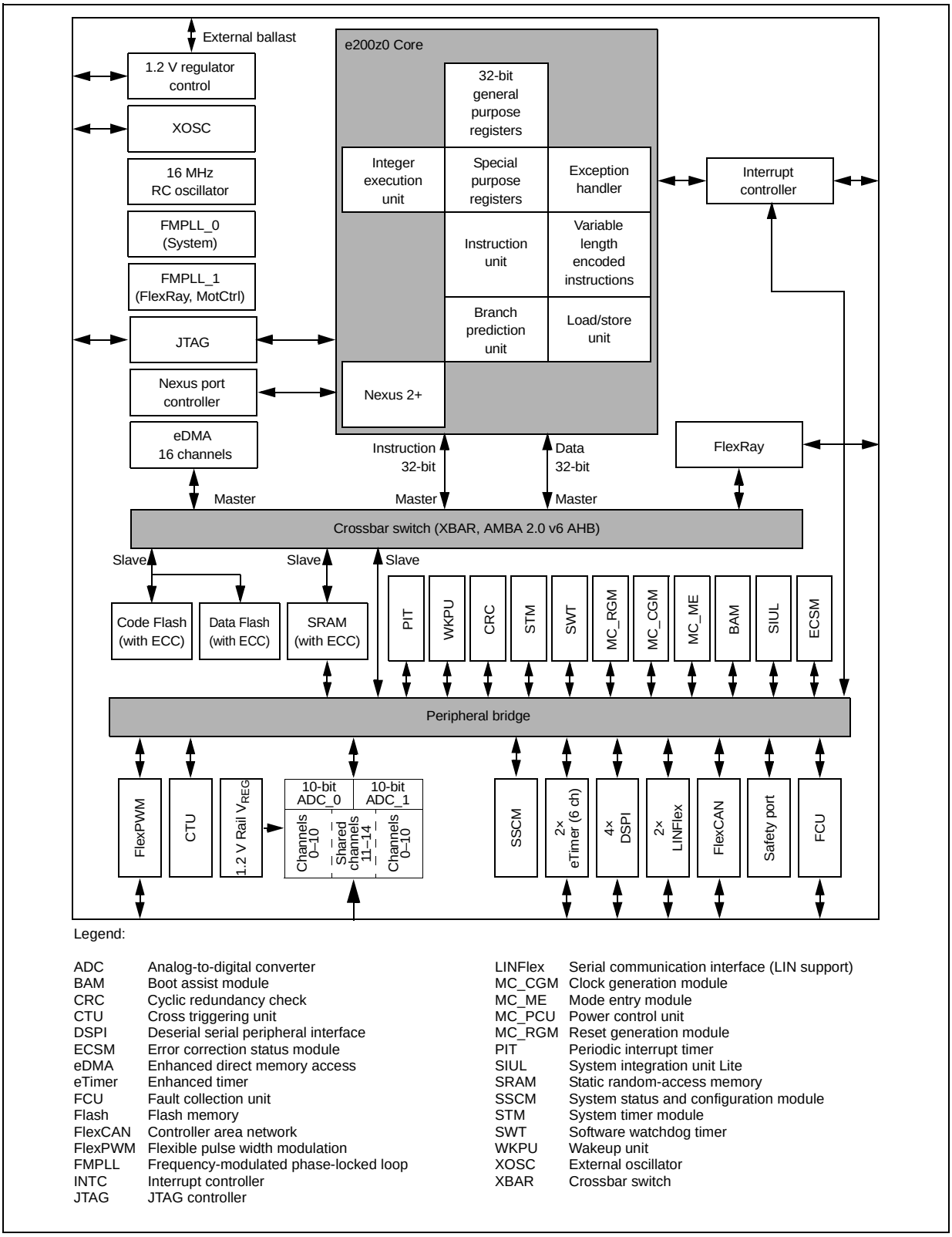
Feature		SPC560P44	SPC560P50
eDMA (enhanced direct memory access) channels		16	
FlexRay		Yes(1)	
FlexCAN (controller area network)		2(2),(3)	
Safety port		Yes (via second FlexCAN module)	
FCU (fault collection unit)		Yes	
CTU (cross triggering unit)		Yes	
eTimer		2 (16-bit, 6 channels)	
FlexPWM (pulse-width modulation) channels		8 (capturing on X-channels)	
ADC (analog-to-digital converter)		2 (10-bit, 15-channel(4))	
LINFlex		2	
DSPI (deserial serial peripheral interface)		4	
CRC (cyclic redundancy check) unit		Yes	
JTAG controller		Yes	
Nexus port controller (NPC)		Yes (Level 2+)	
Supply	Digital power supply(5)	3.3 V or 5 V single supply with external transistor	
	Analog power supply	3.3 V or 5 V	
	Internal RC oscillator	16 MHz	
	External crystal oscillator	4–40 MHz	
Packages		LQFP100 LQFP144	
Temperature	Standard ambient temperature	–40 to 125 °C	

1. 32 message buffers, selectable single or dual channel support
2. Each FlexCAN module has 32 message buffers.
3. One FlexCAN module can act as a Safety Port with a bit rate as high as 7.5 Mbit/s.
4. Four channels shared between the two ADCs
5. The different supply voltages vary according to the part number ordered.

SPC560P44Lx, SPC560P50Lx is available in two configurations having different features: full-featured and airbag. *Table 3* shows the main differences between the two versions.

Table 3. SPC560P44Lx, SPC560P50Lx device configuration differences

Feature	Full-featured	Airbag
CTU (cross triggering unit)	Yes	No
FlexPWM	Yes	No



Legend:

ADC	Analog-to-digital converter
BAM	Boot assist module
CRC	Cyclic redundancy check
CTU	Cross triggering unit
DSPI	Deserial serial peripheral interface
ECSM	Error correction status module
eDMA	Enhanced direct memory access
eTimer	Enhanced timer
FCU	Fault collection unit
Flash	Flash memory
FlexCAN	Controller area network
FlexPWM	Flexible pulse width modulation
FMPLL	Frequency-modulated phase-locked loop
INTC	Interrupt controller
JTAG	JTAG controller
LINFlex	Serial communication interface (LIN support)
MC_CGM	Clock generation module
MC_ME	Mode entry module
MC_PCU	Power control unit
MC_RGM	Reset generation module
PIT	Periodic interrupt timer
SIUL	System integration unit Lite
SRAM	Static random-access memory
SSCM	System status and configuration module
STM	System timer module
SWT	Software watchdog timer
WKPU	Wakeup unit
XOSC	External oscillator
XBAR	Crossbar switch

Figure 1. SPC560P44Lx, SPC560P50Lx block diagram

Table 4. SPC560P44Lx, SPC560P50Lx series block summary (continued)

Block	Function
Pulse width modulator (FlexPWM)	Contains four PWM submodules, each of which is capable of controlling a single half-bridge power stage and two fault input channels
Reset generation module (MC_RGM)	Centralizes reset sources and manages the device reset sequence of the device
Static random-access memory (SRAM)	Provides storage for program code, constants, and variables
System integration unit lite (SIUL)	Provides control over all the electrical pad controls and up 32 ports with 16 bits of bidirectional, general-purpose input and output signals and supports up to 32 external interrupts with trigger event configuration
System status and configuration module (SSCM)	Provides system configuration and status data (such as memory size and status, device mode and security status), device identification data, debug status port enable and selection, and bus and peripheral abort enable/disable
System timer module (STM)	Provides a set of output compare events to support AUTOSAR(1) and operating system tasks
System watchdog timer (SWT)	Provides protection from runaway code
Wakeup unit (WKPU)	Supports up to 18 external sources that can generate interrupts or wakeup events, 1 of which can cause non-maskable interrupt requests or wakeup events

1. AUTOSAR: AUTomotive Open System ARchitecture (see www.autosar.org)

1.5.24 Deserial serial peripheral interface (DSPI)

The deserial serial peripheral interface (DSPI) module provides a synchronous serial interface for communication between the SPC560P44Lx, SPC560P50Lx MCU and external devices.

The DSPI modules provide these features:

- Full duplex, synchronous transfers
- Master or slave operation
- Programmable master bit rates
- Programmable clock polarity and phase
- End-of-transmission interrupt flag
- Programmable transfer baud rate
- Programmable data frames from 4 to 16 bits
- Up to 20 chip select lines available
  - 8 on DSPI_0
  - 4 each on DSPI_1, DSPI_2 and DSPI_3
- 8 clock and transfer attributes registers
- Chip select strobe available as alternate function on one of the chip select pins for deglitching
- FIFOs for buffering as many as 5 transfers on the transmit and receive side
- Queueing operation possible through use of the eDMA
- General purpose I/O functionality on pins when not used for SPI

1.5.25 Pulse width modulator (FlexPWM)

The pulse width modulator module (PWM) contains four PWM submodules, each capable of controlling a single half-bridge power stage. There are also four fault channels.

This PWM is capable of controlling most motor types: AC induction motors (ACIM), permanent magnet AC motors (PMAC), both brushless (BLDC) and brush DC motors (BDC), switched (SRM) and variable reluctance motors (VRM), and stepper motors.

block is an integration of several individual Nexus blocks that are selected to provide the development support interface for this device. The NDI block interfaces to the host processor and internal busses to provide development support as per the IEEE-ISTO 5001-2003 Class 2+ standard. The development support provided includes access to the MCU's internal memory map and access to the processor's internal registers during run time.

The Nexus Interface provides the following features:

- Configured via the IEEE 1149.1
- All Nexus port pins operate at V_{DDIO} (no dedicated power supply)
- Nexus 2+ features supported
  - Static debug
  - Watchpoint messaging
  - Ownership trace messaging
  - Program trace messaging
  - Real time read/write of any internally memory mapped resources through JTAG pins
  - Overrun control, which selects whether to stall before Nexus overruns or keep executing and allow overwrite of information
  - Watchpoint triggering, watchpoint triggers program tracing
- Auxiliary Output Port
  - 4 MDO (Message Data Out) pins
  - MCKO (Message Clock Out) pin
  - 2 $\overline{\text{MSEO}}$ (Message Start/End Out) pins
  - $\overline{\text{EVTO}}$ (Event Out) pin
- Auxiliary Input Port
  - $\overline{\text{EVTI}}$ (Event In) pin

1.5.30 Cyclic redundancy check (CRC)

The CRC computing unit is dedicated to the computation of CRC off-loading the CPU. The CRC module features:

- Support for CRC-16-CCITT (*x*25 protocol):
  - $x^{16} + x^{12} + x^5 + 1$
- Support for CRC-32 (Ethernet protocol):
  - $x^{32} + x^{26} + x^{23} + x^{22} + x^{16} + x^{12} + x^{11} + x^{10} + x^8 + x^7 + x^5 + x^4 + x^2 + x + 1$
- Zero wait states for each write/read operations to the CRC_CFG and CRC_INP registers at the maximum frequency

1.5.31 IEEE 1149.1 JTAG controller

The JTAG controller (JTAGC) block provides the means to test chip functionality and connectivity while remaining transparent to system logic when not in test mode. All data input to and output from the JTAGC block is communicated in serial format. The JTAGC block is compliant with the IEEE standard.

Table 5. Supply pins

Supply		Pin	
Symbol	**Description**	**100-pin**	**144-pin**
VREG control and power supply pins. Pins available on 100-pin and 144-pin package.			
BCTRL	Voltage regulator external NPN ballast base control pin	47	69
$V_{DD\_HV\_REG}$ (3.3 V or 5.0 V)	Voltage regulator supply voltage	50	72
$V_{DD\_LV\_REGCOR}$	1.2 V decoupling pins for core logic and regulator feedback. Decoupling capacitor must be connected between this pins and $V_{SS\_LV\_REGCOR}$.	48	70
$V_{SS\_LV\_REGCOR}$	1.2 V decoupling pins for core logic and regulator feedback. Decoupling capacitor must be connected between this pins and $V_{DD\_LV\_REGCOR}$.	49	71
ADC_0/ADC_1 reference and supply voltage. Pins available on 100-pin and 144-pin package.			
$V_{DD\_HV\_ADC0}$ (1)	ADC_0 supply and high reference voltage	33	50
$V_{SS\_HV\_ADC0}$	ADC_0 ground and low reference voltage	34	51
$V_{DD\_HV\_ADC1}$	ADC_1 supply and high reference voltage	39	56
$V_{SS\_HV\_ADC1}$	ADC_1 ground and low reference voltage	40	57
Power supply pins (3.3 V or 5.0 V). All pins available on 144-pin package. Five pairs (V_{DD}; V_{SS}) available on 100-pin package.			
$V_{DD\_HV\_IO0}$ (2)	Input/Output supply voltage	—	6
$V_{SS\_HV\_IO0}$ (2)	Input/Output ground	—	7
$V_{DD\_HV\_IO1}$	Input/Output supply voltage	13	21
$V_{SS\_HV\_IO1}$	Input/Output ground	14	22
$V_{DD\_HV\_IO2}$	Input/Output supply voltage	63	91
$V_{SS\_HV\_IO2}$	Input/Output ground	62	90
$V_{DD\_HV\_IO3}$	Input/Output supply voltage	87	126
$V_{SS\_HV\_IO3}$	Input/Output ground	88	127
$V_{DD\_HV\_FL}$	Code and data flash supply voltage	69	97
$V_{SS\_HV\_FL}$	Code and data flash supply ground	68	96
$V_{DD\_HV\_OSC}$	Crystal oscillator amplifier supply voltage	16	27
$V_{SS\_HV\_OSC}$	Crystal oscillator amplifier ground	17	28
Power supply pins (1.2 V). All pins available on 100-pin and 144-pin package.			
$V_{DD\_LV\_COR0}$	1.2 V Decoupling pins for core logic. Decoupling capacitor must be connected between these pins and the nearest $V_{SS\_LV\_COR}$ pin.	12	18
$V_{SS\_LV\_COR0}$	1.2 V Decoupling pins for core logic. Decoupling capacitor must be connected between these pins and the nearest $V_{DD\_LV\_COR}$ pin.	11	17

Table 5. Supply pins (continued)

Supply		Pin	
Symbol	**Description**	**100-pin**	**144-pin**
$V_{DD\_LV\_COR1}$	1.2 V Decoupling pins for core logic. Decoupling capacitor must be connected between these pins and the nearest $V_{SS\_LV\_COR}$ pin.	65	93
$V_{SS\_LV\_COR1}$	1.2 V Decoupling pins for core logic. Decoupling capacitor must be connected between these pins and the nearest $V_{DD\_LV\_COR}$ pin.	66	94
$V_{DD\_LV\_COR2}$	1.2 V Decoupling pins for core logic. Decoupling capacitor must be connected between these pins and the nearest $V_{SS\_LV\_COR}$ pin.	92	131
$V_{SS\_LV\_COR2}$	1.2 V Decoupling pins for core logic. Decoupling capacitor must be connected between these pins and the nearest $V_{DD\_LV\_COR}$ pin.	93	132
$V_{DD\_LV\_COR3}$	1.2 V Decoupling pins for on-chip PLL modules. Decoupling capacitor must be connected between this pin and $V_{SS\_LV\_COR3}$.	25	36
$V_{SS\_LV\_COR3}$	1.2 V Decoupling pins for on-chip PLL modules. Decoupling capacitor must be connected between this pin and $V_{DD\_LV\_COR3}$.	24	35

1. Analog supply/ground and high/low reference lines are internally physically separate, but are shorted via a double-bonding connection on $V_{DD\_HV\_ADCx}$/$V_{SS\_HV\_ADCx}$ pins.
2. Not available on 100-pin package.

2.2.2 System pins

Table 5 and *Table 6* contain information on pin functions for the SPC560P44Lx, SPC560P50Lx devices. The pins listed in *Table 6* are single-function pins. The pins shown in *Table 7* are multi-function pins, programmable via their respective Pad Configuration Register (PCR) values.

Table 6. System pins

Symbol	Description	Direction	Pad speed(1)		Pin	
			SRC = 0	SRC = 1	100-pin	144-pin
Dedicated pins. Available on 100-pin and 144-pin package.						
MDO[0]	Nexus Message Data Output—line 0	Output only	Fast		—	9
NMI	Non-Maskable Interrupt	Input only	Slow	—	1	1
XTAL	Analog output of the oscillator amplifier circuit; needs to be grounded if oscillator is used in bypass mode	—	—	—	18	29
EXTAL	– Analog input of oscillator amplifier circuit, when oscillator not in bypass mode – Analog input for clock generator when oscillator in bypass mode	—	—	—	19	30

Table 7. Pin muxing

Port pin	Pad configuration register (PCR)	Alternate function[1], [2]	Functions	Peripheral[3]	I/O direction [4]	Pad speed[5]		Pin No.	
						SRC = 0	SRC = 1	100-pin	144-pin
Port A (16-bit)									
A[0]	PCR[0]	ALT0 ALT1 ALT2 ALT3 —	GPIO[0] ETC[0] SCK F[0] EIRQ[0]	SIUL eTimer_0 DSPI_2 FCU_0 SIUL	I/O I/O O O I	Slow	Medium	51	73
A[1]	PCR[1]	ALT0 ALT1 ALT2 ALT3 —	GPIO[1] ETC[1] SOUT F[1] EIRQ[1]	SIUL eTimer_0 DSPI_2 FCU_0 SIUL	I/O I/O O O I	Slow	Medium	52	74
A[2][6]	PCR[2]	ALT0 ALT1 ALT2 ALT3 — — —	GPIO[2] ETC[2] — A[3] SIN ABS[0] EIRQ[2]	SIUL eTimer_0 — FlexPWM_0 DSPI_2 MC_RGM SIUL	I/O I/O — O I I I	Slow	Medium	57	84
A[3][6]	PCR[3]	ALT0 ALT1 ALT2 ALT3 — —	GPIO[3] ETC[3] CS0 B[3] ABS[2] EIRQ[3]	SIUL eTimer_0 DSPI_2 FlexPWM_0 MC_RGM SIUL	I/O I/O I/O O I I	Slow	Medium	64	92
A[4][6]	PCR[4]	ALT0 ALT1 ALT2 ALT3 — —	GPIO[4] ETC[0] CS1 ETC[4] FAB EIRQ[4]	SIUL eTimer_1 DSPI_2 eTimer_0 MC_RGM SIUL	I/O I/O O I/O I I	Slow	Medium	75	108
A[5]	PCR[5]	ALT0 ALT1 ALT2 ALT3 —	GPIO[5] CS0 ETC[5] CS7 EIRQ[5]	SIUL DSPI_1 eTimer_1 DSPI_0 SIUL	I/O I/O I/O O I	Slow	Medium	8	14
A[6]	PCR[6]	ALT0 ALT1 ALT2 ALT3 —	GPIO[6] SCK — — EIRQ[6]	SIUL DSPI_1 — — SIUL	I/O I/O — — I	Slow	Medium	2	2

Table 7. Pin muxing (continued)

Port pin	Pad configuration register (PCR)	Alternate function[1],[2]	Functions	Peripheral[3]	I/O direction[4]	Pad speed[5]		Pin No.	
						SRC = 0	SRC = 1	100-pin	144-pin
D[5]	PCR[53]	ALT0 ALT1 ALT2 ALT3	GPIO[53] CS3 F[0] SOUT	SIUL DSPI_0 FCU_0 DSPI_3	I/O O O O	Slow	Medium	22	33
D[6]	PCR[54]	ALT0 ALT1 ALT2 ALT3 —	GPIO[54] CS2 SCK — FAULT[1]	SIUL DSPI_0 DSPI_3 — FlexPWM_0	I/O O I/O — I	Slow	Medium	23	34
D[7]	PCR[55]	ALT0 ALT1 ALT2 ALT3 —	GPIO[55] CS3 F[1] CS4 SIN	SIUL DSPI_1 FCU_0 DSPI_0 DSPI_3	I/O O O O I	Slow	Medium	26	37
D[8]	PCR[56]	ALT0 ALT1 ALT2 ALT3 —	GPIO[56] CS2 — CS5 FAULT[3]	SIUL DSPI_1 — DSPI_0 FlexPWM_0	I/O O — O I	Slow	Medium	21	32
D[9]	PCR[57]	ALT0 ALT1 ALT2 ALT3	GPIO[57] X[0] TXD —	SIUL FlexPWM_0 LIN_1 —	I/O I/O O —	Slow	Medium	15	26
D[10]	PCR[58]	ALT0 ALT1 ALT2 ALT3	GPIO[58] A[0] CS0 —	SIUL FlexPWM_0 DSPI_3 —	I/O O I/O —	Slow	Medium	53	76
D[11]	PCR[59]	ALT0 ALT1 ALT2 ALT3	GPIO[59] B[0] CS1 SCK	SIUL FlexPWM_0 DSPI_3 DSPI_3	I/O O O I/O	Slow	Medium	54	78
D[12]	PCR[60]	ALT0 ALT1 ALT2 ALT3 —	GPIO[60] X[1] — — RXD	SIUL FlexPWM_0 — — LIN_1	I/O I/O — — I	Slow	Medium	70	99
D[13]	PCR[61]	ALT0 ALT1 ALT2 ALT3	GPIO[61] A[1] CS2 SOUT	SIUL FlexPWM_0 DSPI_3 DSPI_3	I/O O O O	Slow	Medium	67	95

Table 7. Pin muxing (continued)

Port pin	Pad configuration register (PCR)	Alternate function[1], [2]	Functions	Peripheral[3]	I/O direction [4]	Pad speed[5]		Pin No.	
						SRC = 0	SRC = 1	100-pin	144-pin
F[5]	PCR[85]	ALT0 ALT1 ALT2 ALT3	GPIO[85] MDO[2] — —	SIUL NEXUS_0 — —	I/O O — —	Slow	Fast	—	5
F[6]	PCR[86]	ALT0 ALT1 ALT2 ALT3	GPIO[86] MDO[1] — —	SIUL NEXUS_0 — —	I/O O — —	Slow	Fast	—	8
F[7]	PCR[87]	ALT0 ALT1 ALT2 ALT3	GPIO[87] MCKO — —	SIUL NEXUS_0 — —	I/O O — —	Slow	Fast	—	19
F[8]	PCR[88]	ALT0 ALT1 ALT2 ALT3	GPIO[88] MSEO1 — —	SIUL NEXUS_0 — —	I/O O — —	Slow	Fast	—	20
F[9]	PCR[89]	ALT0 ALT1 ALT2 ALT3	GPIO[89] MSEO0 — —	SIUL NEXUS_0 — —	I/O O — —	Slow	Fast	—	23
F[10]	PCR[90]	ALT0 ALT1 ALT2 ALT3	GPIO[90] EVTO — —	SIUL NEXUS_0 — —	I/O O — —	Slow	Fast	—	24
F[11]	PCR[91]	ALT0 ALT1 ALT2 ALT3 —	GPIO[91] — — — EVTI	SIUL — — — NEXUS_0	I/O — — — I	Slow	Medium	—	25
F[12]	PCR[92]	ALT0 ALT1 ALT2 ALT3	GPIO[92] ETC[3] — —	SIUL eTimer_1 — —	I/O I/O — —	Slow	Medium	—	106
F[13]	PCR[93]	ALT0 ALT1 ALT2 ALT3	GPIO[92] ETC[4] — —	SIUL eTimer_1 — —	I/O I/O — —	Slow	Medium	—	112

2. Junction-to-board thermal resistance determined per JEDEC JESD51-8. Thermal test board meets JEDEC specification for the specified package.
3. Junction-to-case at the top of the package determined using MIL-STD 883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer.
4. Thermal characterization parameter indicating the temperature difference between the board and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JB.
5. Thermal characterization parameter indicating the temperature difference between the case and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JC.

Table 13. Thermal characteristics for 100-pin LQFP

Symbol	Parameter	Conditions	Typical value	Unit
$R_{\theta JA}$	Thermal resistance junction-to-ambient, natural convection(1)	Single layer board—1s	47.3	°C/W
		Four layer board—2s2p	35.3	°C/W
$R_{\theta JB}$	Thermal resistance junction-to-board(2)	Four layer board—2s2p	19.1	°C/W
$R_{\theta JCtop}$	Thermal resistance junction-to-case (top)(3)	Single layer board—1s	9.7	°C/W
Ψ_{JB}	Junction-to-board, natural convection(4)	Operating conditions	19.1	°C/W
Ψ_{JC}	Junction-to-case, natural convection(5)	Operating conditions	0.8	°C/W

1. Junction-to-ambient thermal resistance determined per JEDEC JESD51-7. Thermal test board meets JEDEC specification for this package.
2. Junction-to-board thermal resistance determined per JEDEC JESD51-8. Thermal test board meets JEDEC specification for the specified package.
3. Junction-to-case at the top of the package determined using MIL-STD 883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer.
4. Thermal characterization parameter indicating the temperature difference between the board and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JB.
5. Thermal characterization parameter indicating the temperature difference between the case and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JC.

3.5.2 General notes for specifications at maximum junction temperature

An estimation of the chip junction temperature, T_J, can be obtained from *Equation 1*:

Equation 1 $T_J = T_A + (R_{\theta JA} * P_D)$

where:

T_A = ambient temperature for the package (°C)

$R_{\theta JA}$ = junction to ambient thermal resistance (°C/W)

P_D = power dissipation in the package (W)

The junction to ambient thermal resistance is an industry standard value that provides a quick and easy estimation of thermal performance. Unfortunately, there are two values in

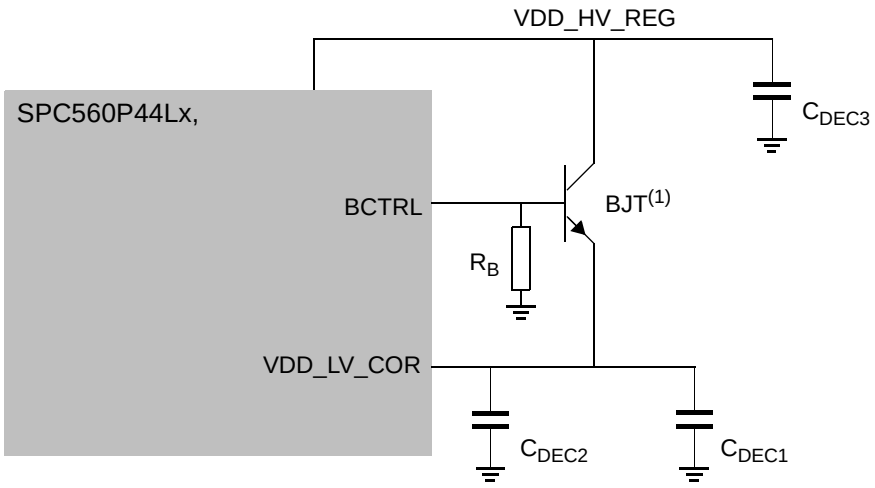
L_{Reg}, see *Table 17*.

Note: The voltage regulator output cannot be used to drive external circuits. Output pins are used only for decoupling capacitances.

$V_{DD\_LV\_COR}$ must be generated using internal regulator and external NPN transistor. It is not possible to provide $V_{DD\_LV\_COR}$ through external regulator.

For the SPC560P44Lx, SPC560P50Lx microcontroller, capacitors, with total values not below C_{DEC1}, should be placed between $V_{DD\_LV\_CORx}/V_{SS\_LV\_CORx}$ close to external ballast transistor emitter. 4 capacitors, with total values not below C_{DEC2}, should be placed close to microcontroller pins between each $V_{DD\_LV\_CORx}/V_{SS\_LV\_CORx}$ supply pairs and the $V_{DD\_LV\_REGCOR}/V_{SS\_LV\_REGCOR}$ pair . Additionally, capacitors with total values not below C_{DEC3}, should be placed between the $V_{DD\_HV\_REG}/V_{SS\_HV\_REG}$ pins close to ballast collector. Capacitors values have to take into account capacitor accuracy, aging and variation versus temperature.

All reported information are valid for voltage and temperature ranges described in recommended operating condition, *Table 10* and *Table 11*.



1. Refer to *Table 16*.

Figure 9. Configuration with resistor on base

Table 16. Approved NPN ballast components (configuration with resistor on base)

Part	Manufacturer	Approved derivatives(1)
BCP68	ON Semi	BCP68
	NXP	BCP68-25
	Infineon	BCP68-25
BCX68	Infineon	BCX68-10;BCX68-16;BCX68-25
BC868	NXP	BC868

memory and RC16 oscillator needed during power-up phase and reset phase. When POWER_OK is low the associated module are set into a safe state.

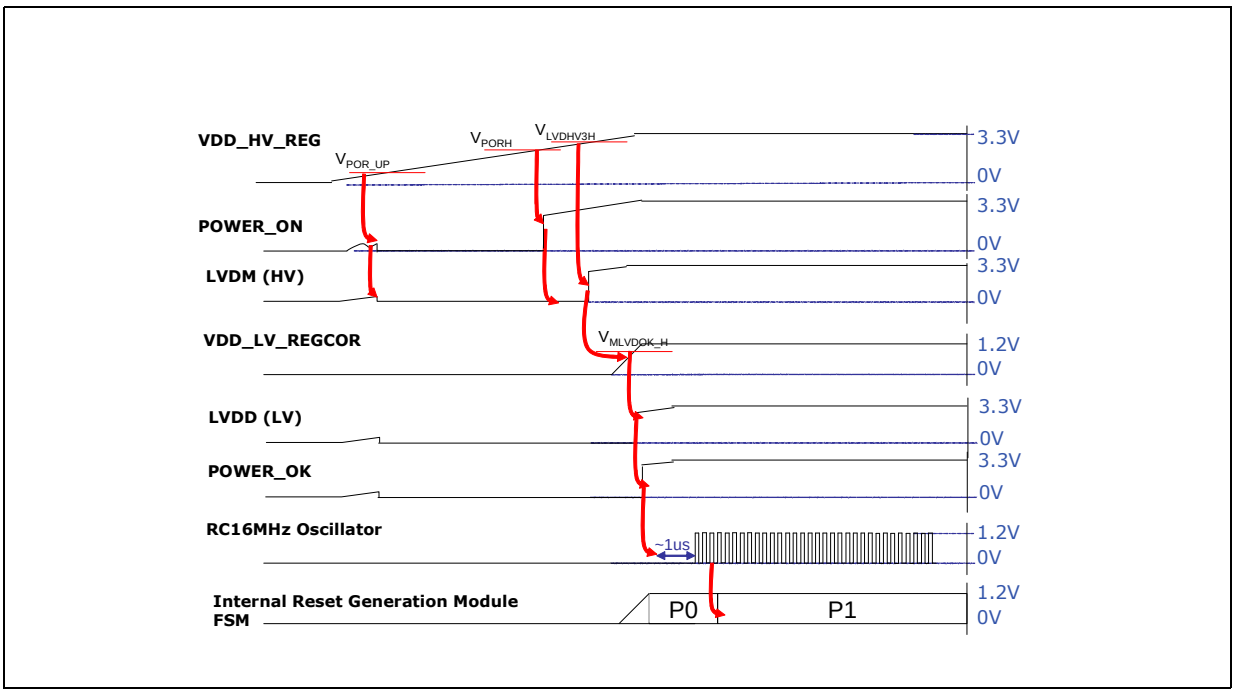


Figure 11. Power-up typical sequence

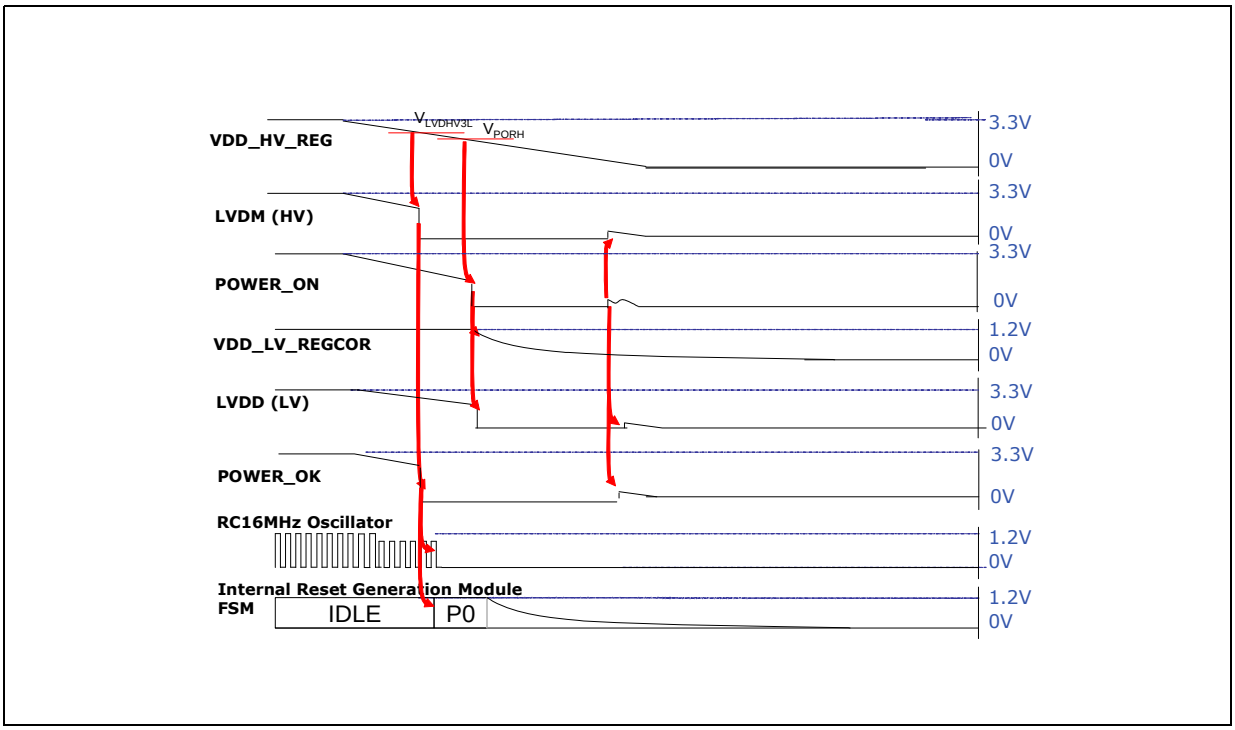


Figure 12. Power-down typical sequence

3.10.2 DC electrical characteristics (5 V)

Table 21 gives the DC electrical characteristics at 5 V (4.5 V < $V_{DD\_HV\_IOx}$ < 5.5 V, NVUSRO[PAD3V5V] = 0); see *Figure 14*.

Table 21. DC electrical characteristics (5.0 V, NVUSRO[PAD3V5V] = 0)

Symbol	C	Parameter	Conditions	Value		Unit
				Min	Max	
V_{IL}	D	Low level input voltage	—	–0.1(1)	—	V
	P		—	—	0.35 $V_{DD\_HV\_IOx}$	V
V_{IH}	P	High level input voltage	—	0.65 $V_{DD\_HV\_IOx}$	—	V
	D		—	—	$V_{DD\_HV\_IOx}$ + 0.1(1)	V
V_{HYS}	T	Schmitt trigger hysteresis	—	0.1 $V_{DD\_HV\_IOx}$	—	V
V_{OL_S}	P	Slow, low level output voltage	I_{OL} = 3 mA	—	0.1 $V_{DD\_HV\_IOx}$	V
V_{OH_S}	P	Slow, high level output voltage	I_{OH} = –3 mA	0.8 $V_{DD\_HV\_IOx}$	—	V
V_{OL_M}	P	Medium, low level output voltage	I_{OL} = 3 mA	—	0.1 $V_{DD\_HV\_IOx}$	V
V_{OH_M}	P	Medium, high level output voltage	I_{OH} = –3 mA	0.8 $V_{DD\_HV\_IOx}$	—	V
V_{OL_F}	P	Fast, low level output voltage	I_{OL} = 3 mA	—	0.1 $V_{DD\_HV\_IOx}$	V
V_{OH_F}	P	Fast, high level output voltage	I_{OH} = –3 mA	0.8 $V_{DD\_HV\_IOx}$	—	V
V_{OL_SYM}	P	Symmetric, low level output voltage	I_{OL} = 3 mA	—	0.1 $V_{DD\_HV\_IOx}$	V
V_{OH_SYM}	P	Symmetric, high level output voltage	I_{OH} = –3 mA	0.8 $V_{DD\_HV\_IOx}$	—	V
I_{PU}	P	Equivalent pull-up current	V_{IN} = V_{IL}	–130	—	µA
			V_{IN} = V_{IH}	—	–10	
I_{PD}	P	Equivalent pull-down current	V_{IN} = V_{IL}	10	—	µA
			V_{IN} = V_{IH}	—	130	
I_{IL}	P	Input leakage current (all bidirectional ports)	T_A = –40 to 125 °C	–1	1	µA
I_{IL}	P	Input leakage current (all ADC input-only ports)	T_A = –40 to 125 °C	–0.5	0.5	µA
C_{IN}	D	Input capacitance	—	—	10	pF
I_{PU}	D	$\overline{\text{RESET}}$, equivalent pull-up current	V_{IN} = V_{IL}	–130	—	µA
			V_{IN} = V_{IH}	—	–10	

1. “SR” parameter values must not exceed the absolute maximum ratings shown in *Table 9*.

Table 26. I/O weight (continued)

Pad	LQFP144		LQFP100	
	Weight 5V	Weight 3.3V	Weight 5V	Weight 3.3V
PAD[27]	1%	1%	1%	1%
PAD[28]	1%	1%	1%	1%
PAD[63]	1%	1%	1%	1%
PAD[72]	1%	1%	—	—
PAD[29]	1%	1%	1%	1%
PAD[73]	1%	1%	—	—
PAD[31]	1%	1%	1%	1%
PAD[74]	1%	1%	—	—
PAD[30]	1%	1%	1%	1%
PAD[75]	1%	1%	—	—
PAD[32]	1%	1%	1%	1%
PAD[76]	1%	1%	—	—
PAD[64]	1%	1%	1%	1%
PAD[0]	23%	20%	23%	20%
PAD[1]	21%	18%	21%	18%
PAD[107]	20%	17%	—	—
PAD[58]	19%	16%	19%	16%
PAD[106]	18%	16%	—	—
PAD[59]	17%	15%	17%	15%
PAD[105]	16%	14%	—	—
PAD[43]	15%	13%	15%	13%
PAD[104]	14%	13%	—	—
PAD[44]	13%	12%	13%	12%
PAD[103]	12%	11%	—	—
PAD[2]	11%	10%	11%	10%
PAD[101]	11%	9%	—	—
PAD[21]	10%	8%	10%	8%
TMS	1%	1%	1%	1%
TCK	1%	1%	1%	1%
PAD[20]	16%	11%	16%	11%
PAD[3]	4%	3%	4%	3%
PAD[61]	9%	8%	9%	8%
PAD[102]	11%	10%	—	—

Table 29. Main oscillator output electrical characteristics (3.3 V, NVUSRO[PAD3V5V] = 1)

Symbol		C	Parameter	Value		Unit
				Min	Max	
f_{OSC}	SR	—	Oscillator frequency	4	40	MHz
g_m	—	P	Transconductance	4	20	mA/V
V_{OSC}	—	T	Oscillation amplitude on XTAL pin	1	—	V
t_{OSCSU}	—	T	Start-up time(1),(2)	8	—	ms

1. The start-up time is dependent upon crystal characteristics, board leakage, etc., high ESR and excessive capacitive loads can cause long start-up time.
2. Value captured when amplitude reaches 90% of XTAL

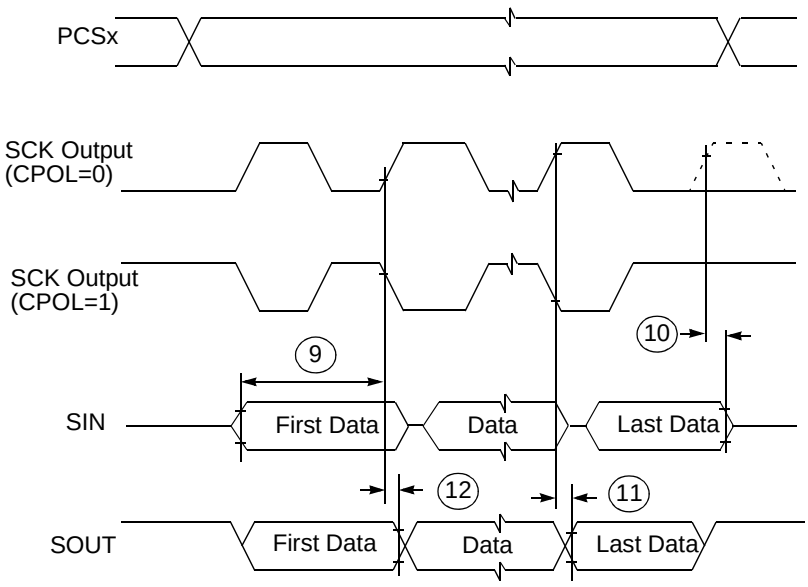
Table 30. Input clock characteristics

Symbol		Parameter	Value			Unit
			Min	Typ	Max	
f_{OSC}	SR	Oscillator frequency	4	—	40	MHz
f_{CLK}	SR	Frequency in bypass	—	—	64	MHz
t_{rCLK}	SR	Rise/fall time in bypass	—	—	1	ns
t_{DC}	SR	Duty cycle	47.5	50	52.5	%

3.12 FMPLL electrical characteristics

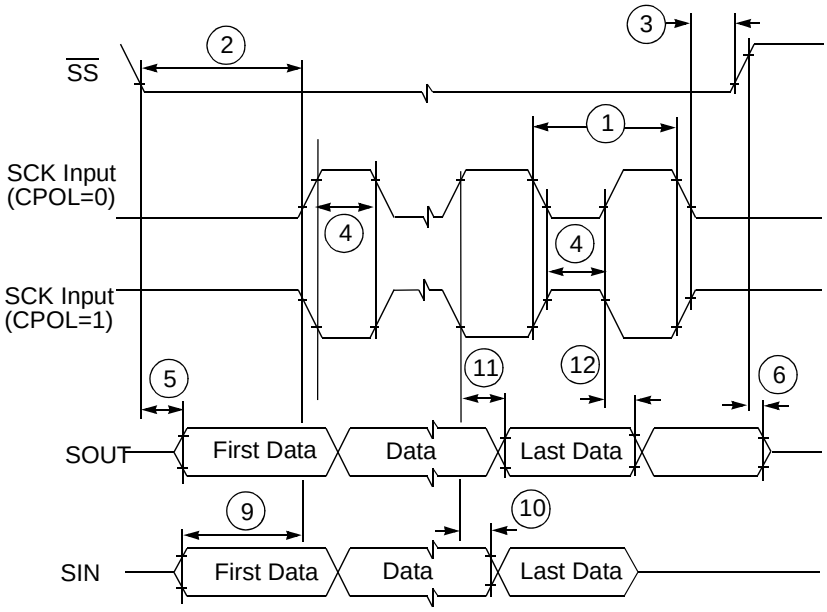
Table 31. FMPLL electrical characteristics

Symbol	C	Parameter	Conditions(1)	Value		Unit
				Min	Max	
$f_{ref\_crystal}$ f_{ref_ext}	D	PLL reference frequency range(2)	Crystal reference	4	40	MHz
f_{PLLIN}	D	Phase detector input frequency range (after pre-divider)	—	4	16	MHz
$f_{FMPLLOUT}$	D	Clock frequency range in normal mode	—	16	120	MHz
f_{FREE}	P	Free-running frequency	Measured using clock division — typically /16	20	150	MHz
t_{CYC}	D	System clock period	—	—	1 / f_{SYS}	ns
f_{LORL} f_{LORH}	D	Loss of reference frequency window(3)	Lower limit	1.6	3.7	MHz
			Upper limit	24	56	
f_{SCM}	D	Self-clocked mode frequency(4),(5)	—	20	150	MHz



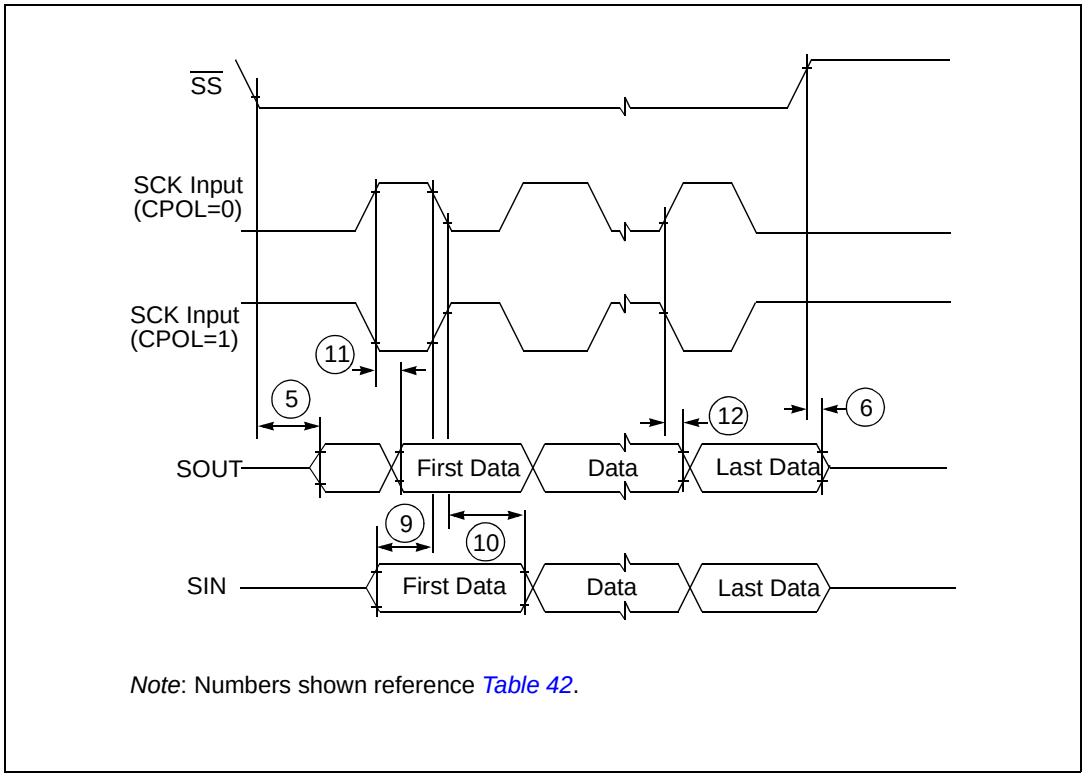
Note: Numbers shown reference *Table 42*.

Figure 34. DSPI modified transfer format timing – Master, CPHA = 1



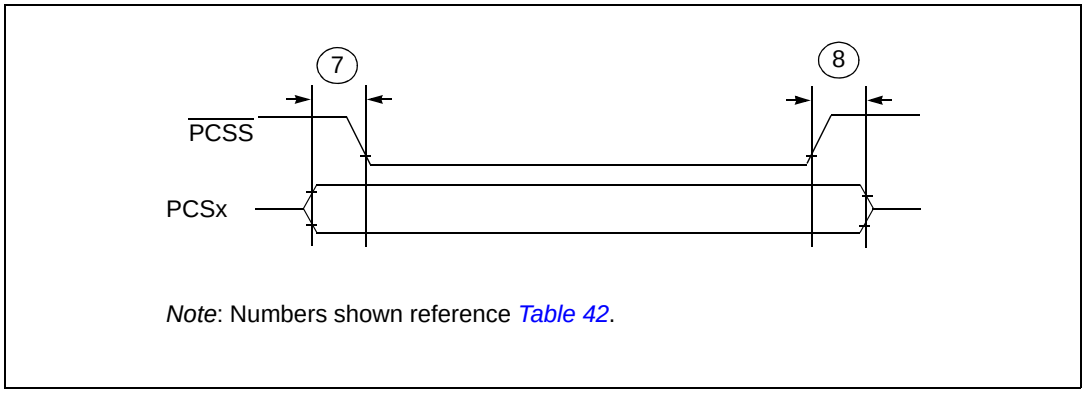
Note: Numbers shown reference *Table 42*.

Figure 35. DSPI modified transfer format timing – Slave, CPHA = 0



Note: Numbers shown reference *Table 42*.

Figure 36. DSPI modified transfer format timing – Slave, CPHA = 1



Note: Numbers shown reference *Table 42*.

Figure 37. DSPI PCS strobe ($\overline{\text{PCSS}}$) timing

Appendix A Abbreviations

Table 45 lists abbreviations used in this document.

Table 45. Abbreviations

Abbreviation	Meaning
CMOS	Complementary metal–oxide–semiconductor
CPHA	Clock phase
CPOL	Clock polarity
CS	Peripheral chip select
DUT	Device under test
ECC	Error code correction
EVTO	Event out
GPIO	General purpose input/output
MC	Modulus counter
MCKO	Message clock out
MCU	Microcontroller unit
MDO	Message data out
MSEO	Message start/end out
MTFE	Modified timing format enable
NPN	Negative-positive-negative
NVUSRO	Non-volatile user options register
PTF	Post trimming frequency
PWM	Pulse width modulation
RBW	Resolution bandwidth
SCK	Serial communications clock
SOUT	Serial data out
TCK	Test clock input
TDI	Test data input
TDO	Test data output
TMS	Test mode select

Table 46. Revision history (continued)

Date	Revision	Changes
07-Jul-2009	4	Through all document: – Replaced all “RESET_B” occurrences with “$\overline{\text{RESET}}$” through all document. – AC Timings: 1149.1 (JTAG) Timing, Nexus Timing, External Interrupt Timing, and DSPI Timing sections inserted again. – Electrical parameters updated. *Section , Features*: – Specified LIN 2.1 in communications interfaces feature. *Table 2* – Added row for Data Flash. *Table 4* – Added a footnote regarding the decoupling capacitors. *Table 6* – Removed the “other function“ column. – Rearranged the contents. *Table 14* – Updated definition of Condition column. *Table 19* – merged in an unique Table the power consumption data related to "Maximum mode" and "Airbag mode". *Table 21* – merged in an unique Table the power consumption data related to "Maximum mode" and "Airbag mode". *Table 29* – Updated the parameter definition of ΔRCMVAR. – Removed the condition definition of ΔRCMVAR. *Table 29* – Added t_{ADC_C} and TUE rows. *Table 30* – Added t_{ADC_C} and TUE rows. – Removed $R_{sw2.}$ *Table 33* – Added. *Table 29* – Updated and added footnotes. *Section 3.16.1 RESET Pin Characteristics* – Replaces whole section. *Table 38* – Renamed the “Flash (KB)“ heading column in “Code Flash / Data Flash (EE) (KB)“ – Replaced the value of RAM from 32 to 36KB in the last four rows.