Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	e200z0h
Core Size	32-Bit Single-Core
Speed	64MHz
Connectivity	CANbus, LINbus, SPI, UART/USART
Peripherals	DMA, POR, PWM, WDT
Number of I/O	67
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	40K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 26x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/spc560p50l3befay

The sources of the ECC errors are:

- Flash memory
- SRAM

1.5.19 Peripheral bridge (PBRIDGE)

The PBRIDGE implements the following features:

- Duplicated periphery
- Master access privilege level per peripheral (per master: read access enable; write access enable)
- Write buffering for peripherals
- Checker applied on PBRIDGE output toward periphery
- Byte endianess swap capability

1.5.20 Controller area network (FlexCAN)

The SPC560P44Lx, SPC560P50Lx MCU contains one controller area network (FlexCAN) module. This module is a communication controller implementing the CAN protocol according to Bosch Specification version 2.0B. The CAN protocol was designed to be used primarily as a vehicle serial data bus, meeting the specific requirements of this field: real-time processing, reliable operation in the EMI environment of a vehicle, cost-effectiveness and required bandwidth. The FlexCAN module contains 32 message buffers.

block is an integration of several individual Nexus blocks that are selected to provide the development support interface for this device. The NDI block interfaces to the host processor and internal busses to provide development support as per the IEEE-ISTO 5001-2003 Class 2+ standard. The development support provided includes access to the MCU's internal memory map and access to the processor's internal registers during run time.

The Nexus Interface provides the following features:

- Configured via the IEEE 1149.1
- All Nexus port pins operate at V_{DDIO} (no dedicated power supply)
- Nexus 2+ features supported
  - Static debug
  - Watchpoint messaging
  - Ownership trace messaging
  - Program trace messaging
  - Real time read/write of any internally memory mapped resources through JTAG pins
  - Overrun control, which selects whether to stall before Nexus overruns or keep executing and allow overwrite of information
  - Watchpoint triggering, watchpoint triggers program tracing
- Auxiliary Output Port
  - 4 MDO (Message Data Out) pins
  - MCKO (Message Clock Out) pin
  - 2 $\overline{\text{MSEO}}$ (Message Start/End Out) pins
  - $\overline{\text{EVTO}}$ (Event Out) pin
- Auxiliary Input Port
  - $\overline{\text{EVTI}}$ (Event In) pin

1.5.30 Cyclic redundancy check (CRC)

The CRC computing unit is dedicated to the computation of CRC off-loading the CPU. The CRC module features:

- Support for CRC-16-CCITT (*x*25 protocol):
  - $x^{16} + x^{12} + x^5 + 1$
- Support for CRC-32 (Ethernet protocol):
  - $x^{32} + x^{26} + x^{23} + x^{22} + x^{16} + x^{12} + x^{11} + x^{10} + x^8 + x^7 + x^5 + x^4 + x^2 + x + 1$
- Zero wait states for each write/read operations to the CRC_CFG and CRC_INP registers at the maximum frequency

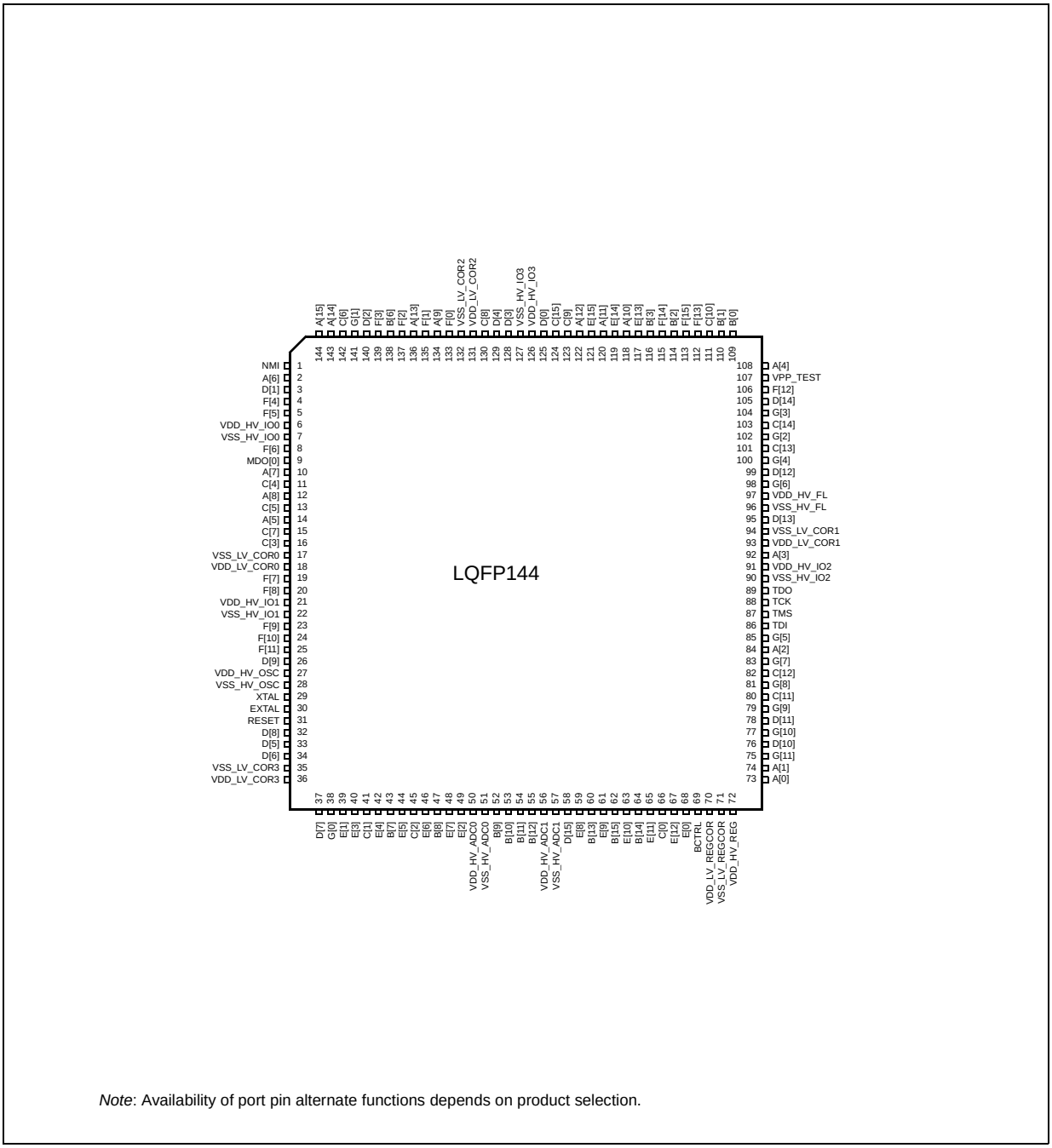
1.5.31 IEEE 1149.1 JTAG controller

The JTAG controller (JTAGC) block provides the means to test chip functionality and connectivity while remaining transparent to system logic when not in test mode. All data input to and output from the JTAGC block is communicated in serial format. The JTAGC block is compliant with the IEEE standard.

2 Package pinouts and signal descriptions

2.1 Package pinouts

The LQFP pinouts are shown in the following figures.



Note: Availability of port pin alternate functions depends on product selection.

Figure 2. 144-pin LQFP pinout – Full featured configuration (top view)

Table 5. Supply pins

Supply		Pin	
Symbol	**Description**	**100-pin**	**144-pin**
VREG control and power supply pins. Pins available on 100-pin and 144-pin package.			
BCTRL	Voltage regulator external NPN ballast base control pin	47	69
$V_{DD\_HV\_REG}$ (3.3 V or 5.0 V)	Voltage regulator supply voltage	50	72
$V_{DD\_LV\_REGCOR}$	1.2 V decoupling pins for core logic and regulator feedback. Decoupling capacitor must be connected between this pins and $V_{SS\_LV\_REGCOR}$.	48	70
$V_{SS\_LV\_REGCOR}$	1.2 V decoupling pins for core logic and regulator feedback. Decoupling capacitor must be connected between this pins and $V_{DD\_LV\_REGCOR}$.	49	71
ADC_0/ADC_1 reference and supply voltage. Pins available on 100-pin and 144-pin package.			
$V_{DD\_HV\_ADC0}$ (1)	ADC_0 supply and high reference voltage	33	50
$V_{SS\_HV\_ADC0}$	ADC_0 ground and low reference voltage	34	51
$V_{DD\_HV\_ADC1}$	ADC_1 supply and high reference voltage	39	56
$V_{SS\_HV\_ADC1}$	ADC_1 ground and low reference voltage	40	57
Power supply pins (3.3 V or 5.0 V). All pins available on 144-pin package. Five pairs (V_{DD}; V_{SS}) available on 100-pin package.			
$V_{DD\_HV\_IO0}$ (2)	Input/Output supply voltage	—	6
$V_{SS\_HV\_IO0}$ (2)	Input/Output ground	—	7
$V_{DD\_HV\_IO1}$	Input/Output supply voltage	13	21
$V_{SS\_HV\_IO1}$	Input/Output ground	14	22
$V_{DD\_HV\_IO2}$	Input/Output supply voltage	63	91
$V_{SS\_HV\_IO2}$	Input/Output ground	62	90
$V_{DD\_HV\_IO3}$	Input/Output supply voltage	87	126
$V_{SS\_HV\_IO3}$	Input/Output ground	88	127
$V_{DD\_HV\_FL}$	Code and data flash supply voltage	69	97
$V_{SS\_HV\_FL}$	Code and data flash supply ground	68	96
$V_{DD\_HV\_OSC}$	Crystal oscillator amplifier supply voltage	16	27
$V_{SS\_HV\_OSC}$	Crystal oscillator amplifier ground	17	28
Power supply pins (1.2 V). All pins available on 100-pin and 144-pin package.			
$V_{DD\_LV\_COR0}$	1.2 V Decoupling pins for core logic. Decoupling capacitor must be connected between these pins and the nearest $V_{SS\_LV\_COR}$ pin.	12	18
$V_{SS\_LV\_COR0}$	1.2 V Decoupling pins for core logic. Decoupling capacitor must be connected between these pins and the nearest $V_{DD\_LV\_COR}$ pin.	11	17

Table 7. Pin muxing

Port pin	Pad configuration register (PCR)	Alternate function[1], [2]	Functions	Peripheral[3]	I/O direction [4]	Pad speed[5]		Pin No.	
						SRC = 0	SRC = 1	100-pin	144-pin
Port A (16-bit)									
A[0]	PCR[0]	ALT0 ALT1 ALT2 ALT3 —	GPIO[0] ETC[0] SCK F[0] EIRQ[0]	SIUL eTimer_0 DSPI_2 FCU_0 SIUL	I/O I/O O O I	Slow	Medium	51	73
A[1]	PCR[1]	ALT0 ALT1 ALT2 ALT3 —	GPIO[1] ETC[1] SOUT F[1] EIRQ[1]	SIUL eTimer_0 DSPI_2 FCU_0 SIUL	I/O I/O O O I	Slow	Medium	52	74
A[2][6]	PCR[2]	ALT0 ALT1 ALT2 ALT3 — — —	GPIO[2] ETC[2] — A[3] SIN ABS[0] EIRQ[2]	SIUL eTimer_0 — FlexPWM_0 DSPI_2 MC_RGM SIUL	I/O I/O — O I I I	Slow	Medium	57	84
A[3][6]	PCR[3]	ALT0 ALT1 ALT2 ALT3 — —	GPIO[3] ETC[3] CS0 B[3] ABS[2] EIRQ[3]	SIUL eTimer_0 DSPI_2 FlexPWM_0 MC_RGM SIUL	I/O I/O I/O O I I	Slow	Medium	64	92
A[4][6]	PCR[4]	ALT0 ALT1 ALT2 ALT3 — —	GPIO[4] ETC[0] CS1 ETC[4] FAB EIRQ[4]	SIUL eTimer_1 DSPI_2 eTimer_0 MC_RGM SIUL	I/O I/O O I/O I I	Slow	Medium	75	108
A[5]	PCR[5]	ALT0 ALT1 ALT2 ALT3 —	GPIO[5] CS0 ETC[5] CS7 EIRQ[5]	SIUL DSPI_1 eTimer_1 DSPI_0 SIUL	I/O I/O I/O O I	Slow	Medium	8	14
A[6]	PCR[6]	ALT0 ALT1 ALT2 ALT3 —	GPIO[6] SCK — — EIRQ[6]	SIUL DSPI_1 — — SIUL	I/O I/O — — I	Slow	Medium	2	2

Table 7. Pin muxing (continued)

Port pin	Pad configuration register (PCR)	Alternate function[1],[2]	Functions	Peripheral[3]	I/O direction[4]	Pad speed[5]		Pin No.	
						SRC = 0	SRC = 1	100-pin	144-pin
C[13]	PCR[45]	ALT0 ALT1 ALT2 ALT3 — —	GPIO[45] ETC[1] — — EXT_IN EXT_SYNC	SIUL eTimer_1 — — CTU_0 FlexPWM_0	I/O I/O — — I I	Slow	Medium	71	101
C[14]	PCR[46]	ALT0 ALT1 ALT2 ALT3	GPIO[46] ETC[2] EXT_TGR —	SIUL eTimer_1 CTU_0 —	I/O I/O O —	Slow	Medium	72	103
C[15]	PCR[47]	ALT0 ALT1 ALT2 ALT3 — —	GPIO[47] CA_TR_EN ETC[0] A[1] EXT_IN EXT_SYNC	SIUL FlexRay_0 eTimer_1 FlexPWM_0 CTU_0 FlexPWM_0	I/O O I/O O I I	Slow	Symmetric	85	124
Port D (16-bit)									
D[0]	PCR[48]	ALT0 ALT1 ALT2 ALT3	GPIO[48] CA_TX ETC[1] B[1]	SIUL FlexRay_0 eTimer_1 FlexPWM_0	I/O O I/O O	Slow	Symmetric	86	125
D[1]	PCR[49]	ALT0 ALT1 ALT2 ALT3 —	GPIO[49] — ETC[2] EXT_TRG CA_RX	SIUL — eTimer_1 CTU_0 FlexRay_0	I/O — I/O O I	Slow	Medium	3	3
D[2]	PCR[50]	ALT0 ALT1 ALT2 ALT3 —	GPIO[50] — ETC[3] X[3] CB_RX	SIUL — eTimer_1 FlexPWM_0 FlexRay_0	I/O — I/O I/O I	Slow	Medium	97	140
D[3]	PCR[51]	ALT0 ALT1 ALT2 ALT3	GPIO[51] CB_TX ETC[4] A[3]	SIUL FlexRay_0 eTimer_1 FlexPWM_0	I/O O I/O O	Slow	Symmetric	89	128
D[4]	PCR[52]	ALT0 ALT1 ALT2 ALT3	GPIO[52] CB_TR_EN ETC[5] B[3]	SIUL FlexRay_0 eTimer_1 FlexPWM_0	I/O O I/O O	Slow	Symmetric	90	129

Table 7. Pin muxing (continued)

Port pin	Pad configuration register (PCR)	Alternate function[1],[2]	Functions	Peripheral[3]	I/O direction[4]	Pad speed[5]		Pin No.	
						SRC = 0	SRC = 1	100-pin	144-pin
D[5]	PCR[53]	ALT0 ALT1 ALT2 ALT3	GPIO[53] CS3 F[0] SOUT	SIUL DSPI_0 FCU_0 DSPI_3	I/O O O O	Slow	Medium	22	33
D[6]	PCR[54]	ALT0 ALT1 ALT2 ALT3 —	GPIO[54] CS2 SCK — FAULT[1]	SIUL DSPI_0 DSPI_3 — FlexPWM_0	I/O O I/O — I	Slow	Medium	23	34
D[7]	PCR[55]	ALT0 ALT1 ALT2 ALT3 —	GPIO[55] CS3 F[1] CS4 SIN	SIUL DSPI_1 FCU_0 DSPI_0 DSPI_3	I/O O O O I	Slow	Medium	26	37
D[8]	PCR[56]	ALT0 ALT1 ALT2 ALT3 —	GPIO[56] CS2 — CS5 FAULT[3]	SIUL DSPI_1 — DSPI_0 FlexPWM_0	I/O O — O I	Slow	Medium	21	32
D[9]	PCR[57]	ALT0 ALT1 ALT2 ALT3	GPIO[57] X[0] TXD —	SIUL FlexPWM_0 LIN_1 —	I/O I/O O —	Slow	Medium	15	26
D[10]	PCR[58]	ALT0 ALT1 ALT2 ALT3	GPIO[58] A[0] CS0 —	SIUL FlexPWM_0 DSPI_3 —	I/O O I/O —	Slow	Medium	53	76
D[11]	PCR[59]	ALT0 ALT1 ALT2 ALT3	GPIO[59] B[0] CS1 SCK	SIUL FlexPWM_0 DSPI_3 DSPI_3	I/O O O I/O	Slow	Medium	54	78
D[12]	PCR[60]	ALT0 ALT1 ALT2 ALT3 —	GPIO[60] X[1] — — RXD	SIUL FlexPWM_0 — — LIN_1	I/O I/O — — I	Slow	Medium	70	99
D[13]	PCR[61]	ALT0 ALT1 ALT2 ALT3	GPIO[61] A[1] CS2 SOUT	SIUL FlexPWM_0 DSPI_3 DSPI_3	I/O O O O	Slow	Medium	67	95

Table 7. Pin muxing (continued)

Port pin	Pad configuration register (PCR)	Alternate function[1], [2]	Functions	Peripheral[3]	I/O direction [4]	Pad speed[5]		Pin No.	
						SRC = 0	SRC = 1	100-pin	144-pin
E[5]	PCR[69]	ALT0 ALT1 ALT2 ALT3 —	GPIO[69] — — — AN[8]	SIUL — — — ADC_0	Input only	—	—	—	44
E[6]	PCR[70]	ALT0 ALT1 ALT2 ALT3 —	GPIO[70] — — — AN[9]	SIUL — — — ADC_0	Input only	—	—	—	46
E[7]	PCR[71]	ALT0 ALT1 ALT2 ALT3 —	GPIO[71] — — — AN[10]	SIUL — — — ADC_0	Input only	—	—	—	48
E[8]	PCR[72]	ALT0 ALT1 ALT2 ALT3 —	GPIO[72] — — — AN[6]	SIUL — — — ADC_1	Input only	—	—	—	59
E[9]	PCR[73]	ALT0 ALT1 ALT2 ALT3 —	GPIO[73] — — — AN[7]	SIUL — — — ADC_1	Input only	—	—	—	61
E[10]	PCR[74]	ALT0 ALT1 ALT2 ALT3 —	GPIO[74] — — — AN[8]	SIUL — — — ADC_1	Input only	—	—	—	63
E[11]	PCR[75]	ALT0 ALT1 ALT2 ALT3 —	GPIO[75] — — — AN[9]	SIUL — — — ADC_1	Input only	—	—	—	65
E[12]	PCR[76]	ALT0 ALT1 ALT2 ALT3 —	GPIO[76] — — — AN[10]	SIUL — — — ADC_1	Input only	—	—	—	67

3 Electrical characteristics

3.1 Introduction

This section contains device electrical characteristics as well as temperature and power considerations.

This microcontroller contains input protection against damage due to high static voltages. However, it is advisable to take precautions to avoid application of any voltage higher than the specified maximum rated voltages.

To enhance reliability, unused inputs can be driven to an appropriate logic voltage level (V_{DD} or V_{SS}). This can be done by the internal pull-up or pull-down resistors, which are provided by the device for most general purpose pins.

The following tables provide the device characteristics and its demands on the system.

In the tables where the device logic provides signals with their respective timing characteristics, the symbol “CC” for Controller Characteristics is included in the Symbol column.

In the tables where the external system must provide signals with their respective timing characteristics to the device, the symbol “SR” for System Requirement is included in the Symbol column.

Caution: All of the following parameter values can vary depending on the application and must be confirmed during silicon characterization or silicon reliability trial.

3.2 Parameter classification

The electrical parameters are guaranteed by various methods. To give the customer a better understanding, the classifications listed in *Table 8* are used and the parameters are tagged accordingly in the tables where appropriate.

Table 8. Parameter classifications

Classification tag	Tag description
P	Those parameters are guaranteed during production testing on each individual device.
C	Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.
T	Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.
D	Those parameters are derived mainly from simulations.

Note: The classification is shown in the column labeled “C” in the parameter tables where appropriate.

Table 11. Recommended operating conditions (3.3 V) (continued)

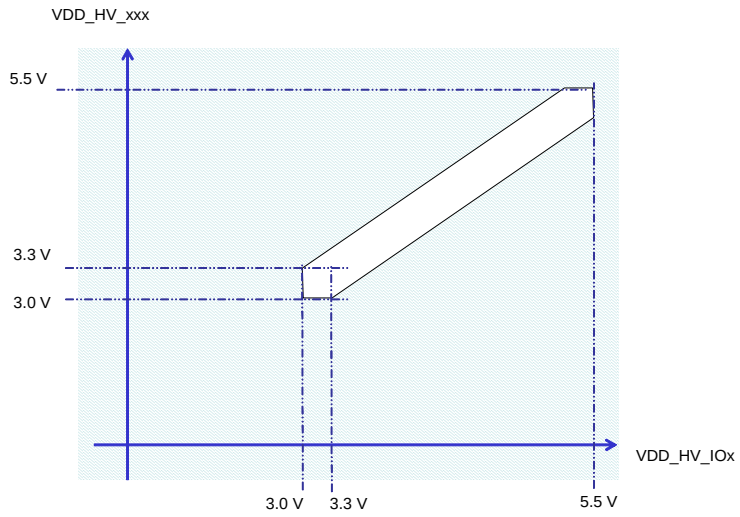
Symbol		Parameter	Conditions	Value		Unit
				Min	Max(1)	
$V_{SS\_LV\_CORx}$(4)	SR	Internal reference voltage	—	0	0	V
T_A	SR	Ambient temperature under bias	f_{CPU} = 64 MHz	–40	105	°C
			f_{CPU} = 60 MHz	–40	125	

1. Parametric figures can be out of specification when voltage drops below 4.5 V, however, guaranteeing the full functionality. In particular, ADC electrical characteristics and I/Os DC electrical specification may not be guaranteed.
2. The difference between each couple of voltage supplies must be less than 100 mV, $|V_{DD\_HV\_IOy} - V_{DD\_HV\_IOx}| < 100$ mV.
3. The difference between each couple of voltage supplies must be less than 100 mV, $|V_{DD\_HV\_ADC1} - V_{DD\_HV\_ADC0}| < 100$ mV. As long as that condition is met, ADC_0 and ADC_1 can be operated at 5 V with the rest of the device operating at 3.3 V.
4. To be connected to emitter of external NPN. Low voltage supplies are not under user control—they are produced by an on-chip voltage regulator—but for the device to function properly the low voltage grounds ($V_{SS\_LV\_xxx}$) must be shorted to high voltage grounds ($V_{SS\_HV\_xxx}$) and the low voltage supply pins ($V_{DD\_LV\_xxx}$) must be connected to the external ballast emitter.
5. The low voltage supplies ($V_{DD\_LV\_xxx}$) are not all independent.

$V_{DD\_LV\_COR1}$ and $V_{DD\_LV\_COR2}$ are shorted internally via double bonding connections with lines that provide the low voltage supply to the data flash module. Similarly, $V_{SS\_LV\_COR1}$ and $V_{SS\_LV\_COR2}$ are internally shorted.

$V_{DD\_LV\_REGCOR}$ and $V_{DD\_LV\_REGCORx}$ are physically shorted internally, as are $V_{SS\_LV\_REGCOR}$ and $V_{SS\_LV\_CORx}$.

Figure 7 shows the constraints of the different power supplies.



Note: IO AC and DC characteristics are guaranteed only in the range of 3.0–3.6 V when PAD3V5V is low, and in the range of 4.5–5.5 V when PAD3V5V is high.

Figure 7. Power supplies constraints (3.0 V ≤ $V_{DD\_HV\_IOx}$ ≤ 5.5 V)

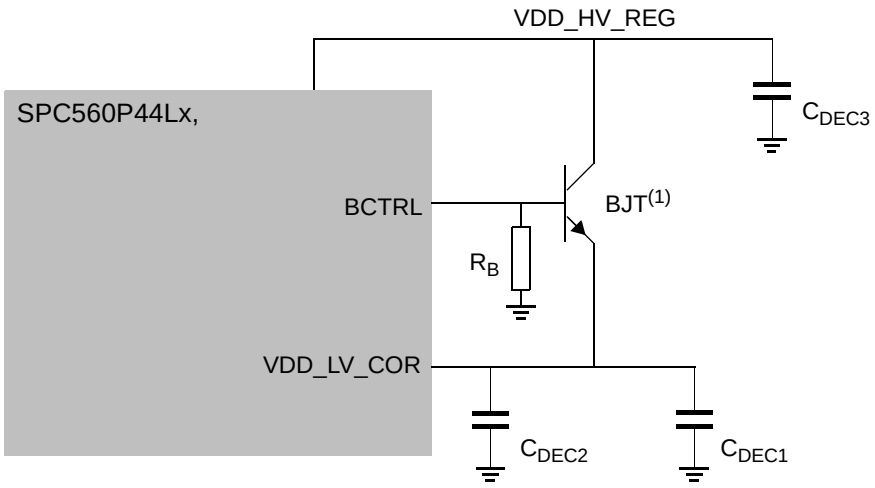
L_{Reg}, see *Table 17*.

Note: The voltage regulator output cannot be used to drive external circuits. Output pins are used only for decoupling capacitances.

$V_{DD\_LV\_COR}$ must be generated using internal regulator and external NPN transistor. It is not possible to provide $V_{DD\_LV\_COR}$ through external regulator.

For the SPC560P44Lx, SPC560P50Lx microcontroller, capacitors, with total values not below C_{DEC1}, should be placed between $V_{DD\_LV\_CORx}/V_{SS\_LV\_CORx}$ close to external ballast transistor emitter. 4 capacitors, with total values not below C_{DEC2}, should be placed close to microcontroller pins between each $V_{DD\_LV\_CORx}/V_{SS\_LV\_CORx}$ supply pairs and the $V_{DD\_LV\_REGCOR}/V_{SS\_LV\_REGCOR}$ pair . Additionally, capacitors with total values not below C_{DEC3}, should be placed between the $V_{DD\_HV\_REG}/V_{SS\_HV\_REG}$ pins close to ballast collector. Capacitors values have to take into account capacitor accuracy, aging and variation versus temperature.

All reported information are valid for voltage and temperature ranges described in recommended operating condition, *Table 10* and *Table 11*.



1. Refer to *Table 16*.

Figure 9. Configuration with resistor on base

Table 16. Approved NPN ballast components (configuration with resistor on base)

Part	Manufacturer	Approved derivatives(1)
BCP68	ON Semi	BCP68
	NXP	BCP68-25
	Infineon	BCP68-25
BCX68	Infineon	BCX68-10;BCX68-16;BCX68-25
BC868	NXP	BC868

3.8.2 Voltage monitor electrical characteristics

The device implements a Power-on Reset module to ensure correct power-up initialization, as well as three low voltage detectors to monitor the V_{DD} and the V_{DD_LV} voltage while device is supplied:

- POR monitors V_{DD} during the power-up phase to ensure device is maintained in a safe reset state
- LVDHV3 monitors V_{DD} to ensure device reset below minimum functional supply
- LVDHV5 monitors V_{DD} when application uses device in the 5.0 V ± 10 % range
- LVDLVCOR monitors low voltage digital power domain

Table 19. Low voltage monitor electrical characteristics

Symbol	C	Parameter	Conditions (1)	Value		Unit
				Min	Max	
V_{PORH}	T	Power-on reset threshold	—	1.5	2.7	V
V_{PORUP}	P	Supply for functional POR module	T_A = 25 °C	1.0	—	V
$V_{REGLVDMOK\_H}$	P	Regulator low voltage detector high threshold	—	—	2.95	V
$V_{REGLVDMOK\_L}$	P	Regulator low voltage detector low threshold	—	2.6	—	V
$V_{FLLVDMOK\_H}$	P	Flash low voltage detector high threshold	—	—	2.95	V
$V_{FLLVDMOK\_L}$	P	Flash low voltage detector low threshold	—	2.6	—	V
$V_{IOLVDMOK\_H}$	P	I/O low voltage detector high threshold	—	—	2.95	V
$V_{IOLVDMOK\_L}$	P	I/O low voltage detector low threshold	—	2.6	—	V
$V_{IOLVDM5OK\_H}$	P	I/O 5V low voltage detector high threshold	—	—	4.4	V
$V_{IOLVDM5OK\_L}$	P	I/O 5V low voltage detector low threshold	—	3.8	—	V
$V_{MLVDDOK\_H}$	P	Digital supply low voltage detector high	—	—	1.145	V
$V_{MLVDDOK\_L}$	P	Digital supply low voltage detector low	—	1.08	—	V

1. V_{DD} = 3.3V ± 10% / 5.0V ± 10%, T_A = –40 °C to $T_{A\ MAX}$, unless otherwise specified

3.9 Power up/down sequencing

To prevent an overstress event or a malfunction within and outside the device, the SPC560P44Lx, SPC560P50Lx implements the following sequence to ensure each module is started only when all conditions for switching it ON are available:

- A POWER_ON module working on voltage regulator supply controls the correct start-up of the regulator. This is a key module ensuring safe configuration for all voltage regulator functionality when supply is below 1.5V. Associated POWER_ON (or POR) signal is active low.
- Several low voltage detectors, working on voltage regulator supply monitor the voltage of the critical modules (voltage regulator, I/Os, flash memory and low voltage domain). LVDs are gated low when POWER_ON is active.
- A POWER_OK signal is generated when all critical supplies monitored by the LVD are available. This signal is active high and released to all modules including I/Os, flash

Table 27. I/O consumption (continued)

Symbol		C	Parameter	Conditions[1]		Value			Unit
						Min	Typ	Max	
I_{RMSMED}	CC	D	Root medium square I/O current for MEDIUM configuration	C_L = 25 pF, 13 MHz	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	6.6	mA
				C_L = 25 pF, 40 MHz		—	—	13.4	
				C_L = 100 pF, 13 MHz		—	—	18.3	
				C_L = 25 pF, 13 MHz	V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	5	
				C_L = 25 pF, 40 MHz		—	—	8.5	
				C_L = 100 pF, 13 MHz		—	—	11	
I_{RMSFST}	CC	D	Root medium square I/O current for FAST configuration	C_L = 25 pF, 40 MHz	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	22	mA
				C_L = 25 pF, 64 MHz		—	—	33	
				C_L = 100 pF, 40 MHz		—	—	56	
				C_L = 25 pF, 40 MHz	V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	14	
				C_L = 25 pF, 64 MHz		—	—	20	
				C_L = 100 pF, 40 MHz		—	—	35	
I_{AVGSEG}	SR	D	Sum of all the static I/O current within a supply segment	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0		—	—	70	mA
				V_{DD} = 3.3 V ± 10%, PAD3V5V = 1		—	—	65	

1. V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified
2. Stated maximum values represent peak consumption that lasts only a few ns during I/O transition.

3.11 Main oscillator electrical characteristics

The SPC560P44Lx, SPC560P50Lx provides an oscillator/resonator driver.

Table 28. Main oscillator output electrical characteristics (5.0 V, NVUSRO[PAD3V5V] = 0)

Symbol		C	Parameter	Value		Unit
				Min	Max	
f_{OSC}	SR	—	Oscillator frequency	4	40	MHz
g_m	—	P	Transconductance	6.5	25	mA/V
V_{OSC}	—	T	Oscillation amplitude on XTAL pin	1	—	V
t_{OSCSU}	—	T	Start-up time[1],[2]	8	—	ms

1. The start-up time is dependent upon crystal characteristics, board leakage, etc., high ESR and excessive capacitive loads can cause long start-up time.
2. Value captured when amplitude reaches 90% of XTAL

3.13 16 MHz RC oscillator electrical characteristics

Table 32. 16 MHz RC oscillator electrical characteristics

Symbol	C	Parameter	Conditions	Value			Unit
				Min	Typ	Max	
f_{RC}	P	RC oscillator frequency	T_A = 25 °C	—	16	—	MHz
Δ_{RCMVAR}	P	Fast internal RC oscillator variation over temperature and supply with respect to f_{RC} at T_A = 25 °C in high-frequency configuration	—	–5	—	5	%
$\Delta_{RCMTRIM}$	T	Post Trim Accuracy: The variation of the PTF(1) from the 16 MHz	T_A = 25 °C	–1	—	1	%
$\Delta_{RCMSTEP}$	T	Fast internal RC oscillator trimming step	T_A = 25 °C	—	1.6	—	%

1. PTF = Post Trimming Frequency: The frequency of the output clock after trimming at typical supply voltage and temperature

3.14 Analog-to-digital converter (ADC) electrical characteristics

The device provides a 10-bit successive approximation register (SAR) analog-to-digital converter.

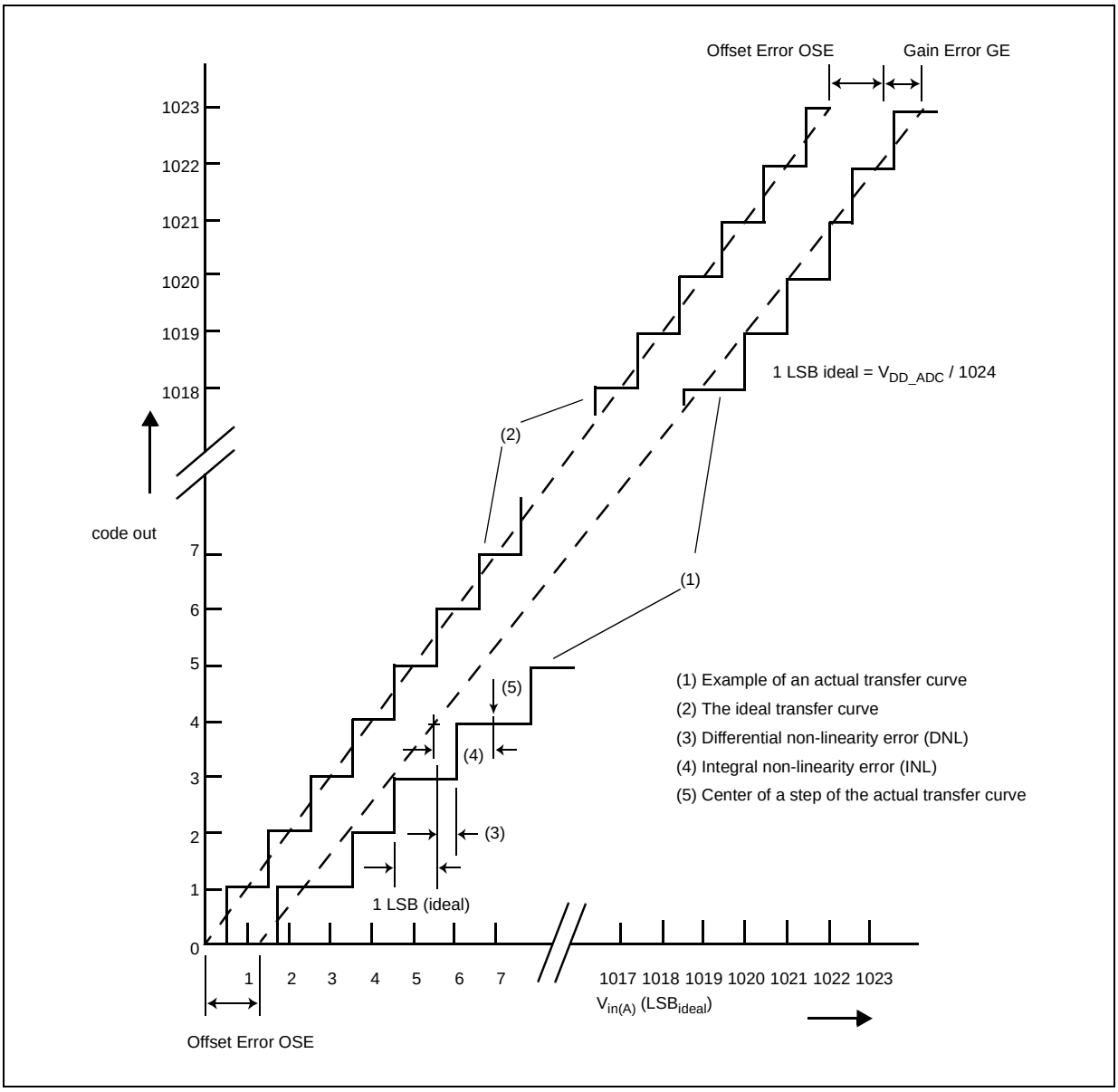


Figure 15. ADC characteristics and error definitions

3.14.1 Input impedance and ADC accuracy

To preserve the accuracy of the A/D converter, it is necessary that analog input pins have low AC impedance. Placing a capacitor with good high frequency characteristics at the input pin of the device can be effective: the capacitor should be as large as possible, ideally infinite. This capacitor contributes to attenuating the noise present on the input pin; further, it sources charge during the sampling phase, when the analog signal source is a high-impedance source.

A real filter can typically be obtained by using a series resistance with a capacitor on the input pin (simple RC filter). The RC filtering may be limited according to the source impedance value of the transducer or circuit supplying the analog signal to be measured.

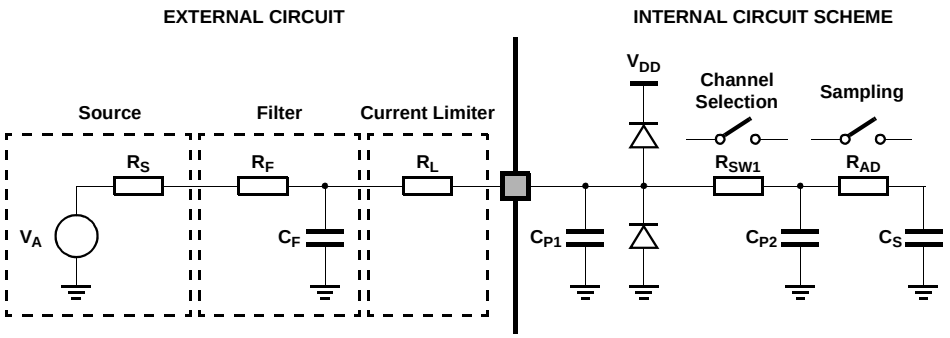
The filter at the input pins must be designed taking into account the dynamic characteristics of the input signal (bandwidth) and the equivalent input impedance of the ADC itself.

In fact a current sink contributor is represented by the charge sharing effects with the sampling capacitance: C_S and C_{P2} being substantially two switched capacitances, with a frequency equal to the ADC conversion rate, it can be seen as a resistive path to ground. For instance, assuming a conversion rate of 1 MHz, with C_S+C_{P2} equal to 3 pF, a resistance of 330 kΩ is obtained (R_{EQ} = 1 / (fc × (C_S+C_{P2})), where fc represents the conversion rate at the considered channel). To minimize the error induced by the voltage partitioning between this resistance (sampled voltage on C_S+C_{P2}) and the sum of R_S + R_F, the external circuit must be designed to respect the *Equation 4*:

Equation 4

$$V_A \bullet \frac{R_S + R_F}{R_{EQ}} < \frac{1}{2} LSB$$

Equation 4 generates a constraint for external network design, in particular on resistive path.



R_S: Source impedance
R_F: Filter resistance
C_F: Filter capacitance
R_L: Current limiter resistance
R_{SW1}: Channel selection switch impedance
R_{AD}: Sampling switch impedance
C_P: Pin capacitance (two contributions, C_{P1} and C_{P2})
C_S: Sampling capacitance

Figure 16. Input equivalent circuit

Table 38. $\overline{\text{RESET}}$ electrical characteristics (continued)

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
t_{tr}	CC	D	Output transition time output pin[3] MEDIUM configuration	C_L = 25pF, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	10	ns
				C_L = 50pF, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	20	
				C_L = 100pF, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	40	
				C_L = 25pF, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	12	
				C_L = 50pF, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	25	
				C_L = 100pF, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	40	
W_{FRST}	SR	P	$\overline{\text{RESET}}$ input filtered pulse	—	—	—	40	ns
W_{NFRST}	SR	P	$\overline{\text{RESET}}$ input not filtered pulse	—	500	—	—	ns
t_{POR}	CC	D	Maximum delay before internal reset is released after all V_{DD_HV} reach nominal supply	Monotonic V_{DD_HV} supply ramp	—	—	1	ms
$\lvert I_{WPU} \rvert$	CC	P	Weak pull-up current absolute value	V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	10	—	150	µA
				V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	10	—	150	
				V_{DD} = 5.0 V ± 10%, PAD3V5V = 1[4]	10	—	250	

1. V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 °C to $T_{A\ MAX}$, unless otherwise specified
2. This is a transient configuration during power-up, up to the end of reset PHASE2 (refer to RGM module section of device reference manual).
3. C_L includes device and package capacitance (C_{PKG} < 5 pF).
4. The configuration PAD3V5 = 1 when V_{DD} = 5 V is only transient configuration during power-up. All pads but RESET and Nexus output (MDOx, EVTO, MCKO) are configured in input or in high impedance state.

3.17.2 IEEE 1149.1 interface timing

Table 39. JTAG pin AC electrical characteristics

No.	Symbol		C	Parameter	Conditions	Value		Unit
						Min	Max	
1	t_{JCYC}	CC	D	TCK cycle time	—	100	—	ns
2	t_{JDC}	CC	D	TCK clock pulse width (measured at $V_{DD\_HV\_IOx}$/2)	—	40	60	ns
3	$t_{TCKRISE}$	CC	D	TCK rise and fall times (40% – 70%)	—	—	3	ns
4	t_{TMSS}, t_{TDIS}	CC	D	TMS, TDI data setup time	—	5	—	ns

Table 39. JTAG pin AC electrical characteristics (continued)

No.	Symbol		C	Parameter	Conditions	Value		Unit
						Min	Max	
5	t_{TMSH}, t_{TDIH}	CC	D	TMS, TDI data hold time	—	25	—	ns
6	t_{TDOV}	CC	D	TCK low to TDO data valid	—	—	40	ns
7	t_{TDOI}	CC	D	TCK low to TDO data invalid	—	0	—	ns
8	t_{TDOHZ}	CC	D	TCK low to TDO high impedance	—	40	—	ns
11	t_{BSDV}	CC	D	TCK falling edge to output valid	—	—	50	ns
12	t_{BSDVZ}	CC	D	TCK falling edge to output valid out of high impedance	—	—	50	ns
13	t_{BSDHZ}	CC	D	TCK falling edge to output high impedance	—	—	50	ns
14	t_{BSDST}	CC	D	Boundary scan input valid to TCK rising edge	—	50	—	ns
15	t_{BSDHT}	CC	D	TCK rising edge to boundary scan input invalid	—	50	—	ns

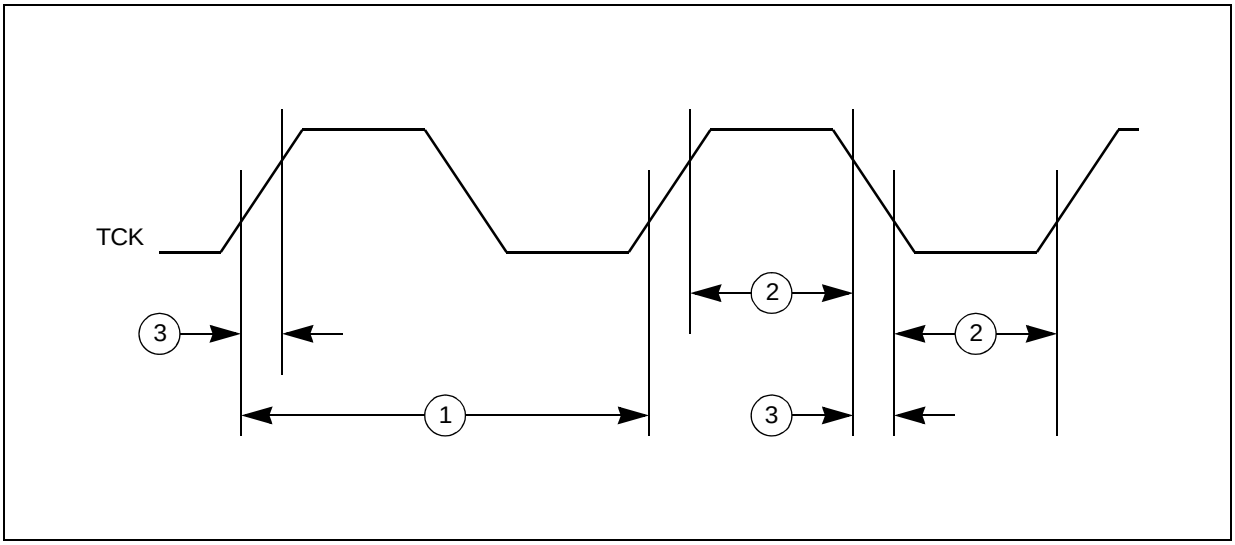


Figure 22. JTAG test clock input timing

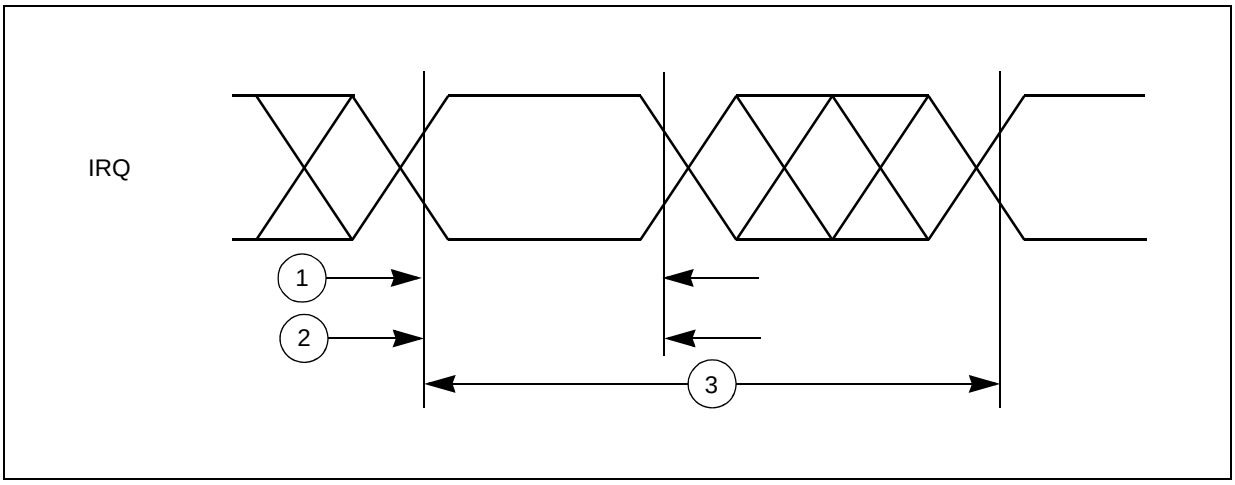


Figure 28. External interrupt timing

3.17.5 DSPI timing

Table 42. DSPI timing(1)

No.	Symbol		C	Parameter	Conditions	Value		Unit
						Min	Max	
1	t_{SCK}	CC	D	DSPI cycle time	Master (MTFE = 0)	60	—	ns
					Slave (MTFE = 0)	60	—	
2	t_{CSC}	CC	D	CS to SCK delay	—	16	—	ns
3	t_{ASC}	CC	D	After SCK delay	—	26	—	ns
4	t_{SDC}	CC	D	SCK duty cycle	—	0.4 * t_{SCK}	0.6 * t_{SCK}	ns
5	t_A	CC	D	Slave access time	$\overline{SS}$ active to SOUT valid	—	30	ns
6	t_{DIS}	CC	D	Slave SOUT disable time	$\overline{SS}$ inactive to SOUT high impedance or invalid	—	16	ns
7	t_{PCSC}	CC	D	PCSx to $\overline{PCSS}$ time	—	13	—	ns
8	t_{PASC}	CC	D	$\overline{PCSS}$ to PCSx time	—	13	—	ns
9	t_{SUI}	CC	D	Data setup time for inputs	Master (MTFE = 0)	35	—	ns
					Slave	4	—	
					Master (MTFE = 1, CPHA = 0)	35	—	
					Master (MTFE = 1, CPHA = 1)	35	—	
10	t_{HI}	CC	D	Data hold time for inputs	Master (MTFE = 0)	–5	—	ns
					Slave	4	—	
					Master (MTFE = 1, CPHA = 0)	11	—	
					Master (MTFE = 1, CPHA = 1)	–5	—	

Table 46. Revision history (continued)

Date	Revision	Changes
27-Oct-2009	5	- Added “Full Feature“ and “Airbag“ customization. - Removed B[4] and B[5] rows from “Pin muxing” table and inserted them on “System pins” table. - Updated package pinout. - Rewrote entirely section “Power Up/dpwn Sequencing“ section. - Renamend “$V_{DD\_LV\_PLL}$“ and “$V_{SS\_LV\_PLL}$“ supply pins with respectively “$V_{DD\_LV\_COR3}$“ and “$V_{SS\_LV\_COR3}$”. - Added explicative figures on “Electrical characteristics” section. - Updated “Thermal characteristics“ for 100-pin. - Proposed two different configuration of “voltage regulator. - Inserted Power Up/Down sequence. - Added explicative figures on “DC Electrical characteristics”. - Added “I/O pad current specification” section. - Renamed the “Airbag mode” with “Typical mode“and updated the values on “supply current” tables. - Added more order code.
06-Apr-2010	6	Inserted label of Y-axis in the “Independent ADC supply“ figure. “Recommended Operating Conditions” tables: Moved the T_J row to “Absolute Maximum Ratings“ table. Rewrite note 1 and 3 Inverted Min a Typ value of C_{DEC2} on ”Voltage Regulator Electrical Characteristics” table. Removed an useless duplicate of “Voltage Regulator Electrical Characteristics“ table. Inserted the name of C_S into “Input Equivalent Circuit“ figure. Removed leakage Ivpp from datasheet. Updated “Supply Current” tables. Added note on “Output pin transition times“ table. Updated ”Temperature Sensor Electrical Characteristics” table. Updated “16 MHz RC Oscillator Electrical Characteristics” table. Removed the note about the condition from “Flash read access timing“ table. Removed the notes that assert the values need to be confirmed before validation.
07-Apr-2011	7	Formatting and editorial changes throughout Removed all content referencing Junction Temperature Sensor Cover page Features: – CPU core—specified 64 MHz frequency – updated memory features – eTimer units: changed “up/down capabilities” to “up/down count capabilities” – ADC—changed “2 × 13 input channels” to “2 × 11 input channels, + 4 shared channels” – replaced “On-chip CAN/UART/FlexRay bootstrap loader” with “On-chip CAN/UART bootstrap loader” *Section 1: Introduction*: changed title (was: Overview); reorganized contents SPC560P44Lx, SPC560P50Lx device comparison: – ADC feature: changed “16 channels” to “15-channel”; added footnote to to indicate that four channels are shared between the two ADCs – removed SPC560P40 column – changed “dual channel” to “selectable single or dual channel support” in FlexRay footnote – updated “eTimer” feature – updated footnote relative to “Digital power supply” feature