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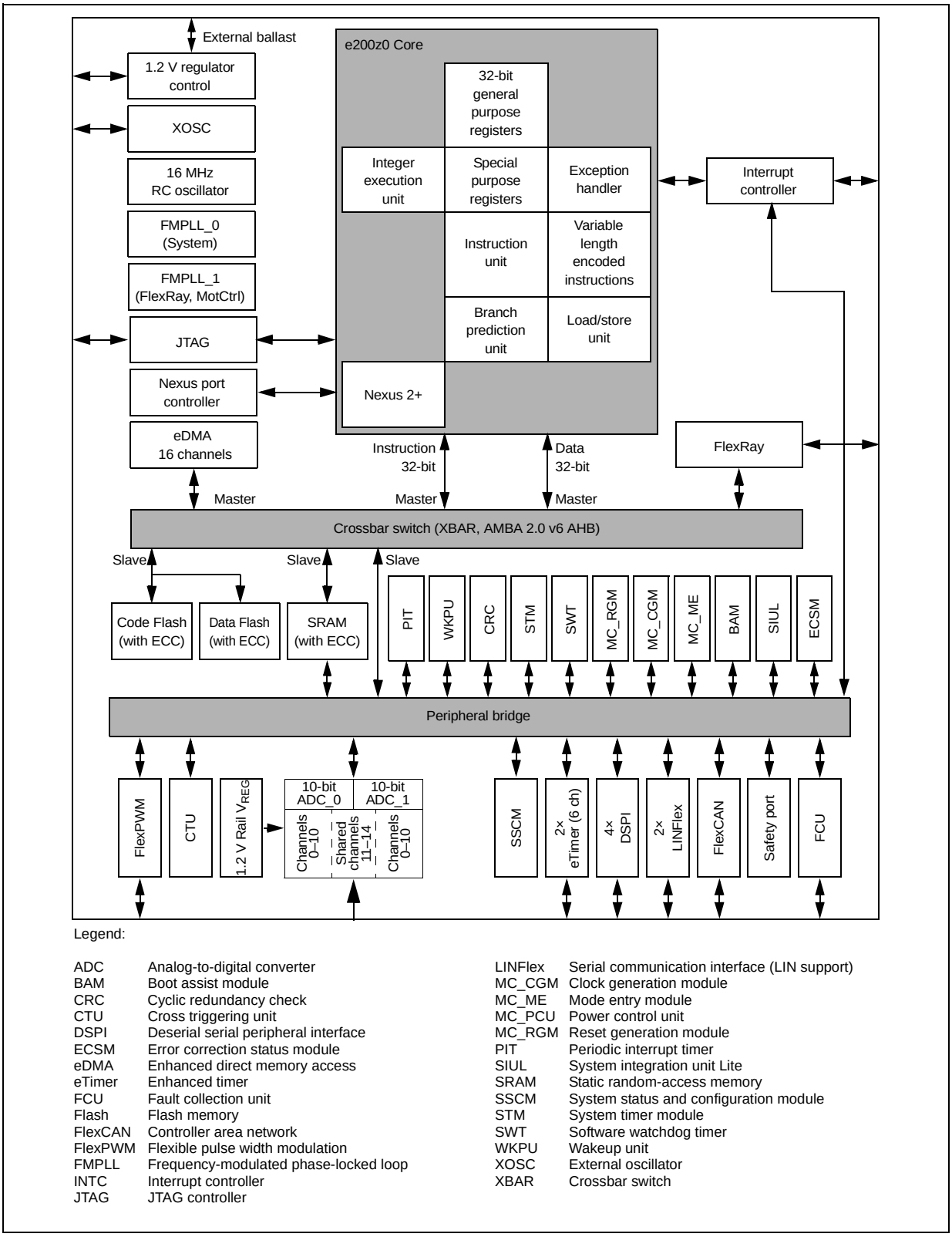
What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z0h
Core Size	32-Bit Single-Core
Speed	64MHz
Connectivity	CANbus, LINbus, SPI, UART/USART
Peripherals	DMA, POR, PWM, WDT
Number of I/O	67
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	40K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 26x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/spc560p50l3cefar

List of figures



Legend:

ADC	Analog-to-digital converter
BAM	Boot assist module
CRC	Cyclic redundancy check
CTU	Cross triggering unit
DSPI	Deserial serial peripheral interface
ECSM	Error correction status module
eDMA	Enhanced direct memory access
eTimer	Enhanced timer
FCU	Fault collection unit
Flash	Flash memory
FlexCAN	Controller area network
FlexPWM	Flexible pulse width modulation
FMPLL	Frequency-modulated phase-locked loop
INTC	Interrupt controller
JTAG	JTAG controller
LINFlex	Serial communication interface (LIN support)
MC_CGM	Clock generation module
MC_ME	Mode entry module
MC_PCU	Power control unit
MC_RGM	Reset generation module
PIT	Periodic interrupt timer
SIUL	System integration unit Lite
SRAM	Static random-access memory
SSCM	System status and configuration module
STM	System timer module
SWT	Software watchdog timer
WKPU	Wakeup unit
XOSC	External oscillator
XBAR	Crossbar switch

Figure 1. SPC560P44Lx, SPC560P50Lx block diagram

1.5.9 Frequency-modulated phase-locked loop (FMPLL)

The FMPLL allows the user to generate high speed system clocks from a 4–40 MHz input clock. Further, the FMPLL supports programmable frequency modulation of the system clock. The PLL multiplication factor, output clock divider ratio are all software configurable.

The PLL has the following major features:

- Input clock frequency: 4–40 MHz
- Maximum output frequency: 64 MHz
- Voltage controlled oscillator (VCO)—frequency 256–512 MHz
- Reduced frequency divider (RFD) for reduced frequency operation without forcing the PLL to relock
- Frequency-modulated PLL
  - Modulation enabled/disabled through software
  - Triangle wave modulation
- Programmable modulation depth (±0.25% to ±4% deviation from center frequency): programmable modulation frequency dependent on reference frequency
- Self-clocked mode (SCM) operation

1.5.10 Main oscillator

The main oscillator provides these features:

- Input frequency range: 4–40 MHz
- Crystal input mode or oscillator input mode
- PLL reference

1.5.11 Internal RC oscillator

This device has an RC ladder phase-shift oscillator. The architecture uses constant current charging of a capacitor. The voltage at the capacitor is compared by the stable bandgap reference voltage.

The RC oscillator provides these features:

- Nominal frequency 16 MHz
- ±5% variation over voltage and temperature after process trim
- Clock output of the RC oscillator serves as system clock source in case loss of lock or loss of clock is detected by the PLL
- RC oscillator is used as the default system clock during startup

1.5.12 Periodic interrupt timer (PIT)

The PIT module implements these features:

- 4 general purpose interrupt timers
- 32-bit counter resolution
- Clocked by system clock frequency
- Each channel can be used as trigger for a DMA request

The sources of the ECC errors are:

- Flash memory
- SRAM

1.5.19 Peripheral bridge (PBRIDGE)

The PBRIDGE implements the following features:

- Duplicated periphery
- Master access privilege level per peripheral (per master: read access enable; write access enable)
- Write buffering for peripherals
- Checker applied on PBRIDGE output toward periphery
- Byte endianess swap capability

1.5.20 Controller area network (FlexCAN)

The SPC560P44Lx, SPC560P50Lx MCU contains one controller area network (FlexCAN) module. This module is a communication controller implementing the CAN protocol according to Bosch Specification version 2.0B. The CAN protocol was designed to be used primarily as a vehicle serial data bus, meeting the specific requirements of this field: real-time processing, reliable operation in the EMI environment of a vehicle, cost-effectiveness and required bandwidth. The FlexCAN module contains 32 message buffers.

The FlexPWM block implements the following features:

- 16-bit resolution for center, edge-aligned, and asymmetrical PWMs
- Maximum operating clock frequency of 120 MHz
- PWM outputs can operate as complementary pairs or independent channels
- Can accept signed numbers for PWM generation
- Independent control of both edges of each PWM output
- Synchronization to external hardware or other PWM supported
- Double buffered PWM registers
  - Integral reload rates from 1 to 16
  - Half cycle reload capability
- Multiple ADC trigger events can be generated per PWM cycle via hardware
- Write protection for critical registers
- Fault inputs can be assigned to control multiple PWM outputs
- Programmable filters for fault inputs
- Independently programmable PWM output polarity
- Independent top and bottom deadtime insertion
- Each complementary pair can operate with its own PWM frequency and deadtime values
- Individual software-control for each PWM output
- All outputs can be programmed to change simultaneously via a “Force Out” event
- PWMX pin can optionally output a third PWM signal from each submodule
- Channels not used for PWM generation can be used for buffered output compare functions
- Channels not used for PWM generation can be used for input capture functions
- Enhanced dual-edge capture functionality
- eDMA support with automatic reload
- 2 fault inputs
- Capture capability for PWMA, PWMB, and PWMX channels not supported

The JTAG controller provides the following features:

- IEEE Test Access Port (TAP) interface with 4 pins (TDI, TMS, TCK, TDO)
- Selectable modes of operation include JTAGC/debug or normal system operation.
- A 5-bit instruction register that supports the following IEEE 1149.1-2001 defined instructions:
  - BYPASS, IDCODE, EXTEST, SAMPLE, SAMPLE/PRELOAD
- A 5-bit instruction register that supports the additional following public instructions:
  - ACCESS_AUX_TAP_NPC, ACCESS_AUX_TAP_ONCE
- 3 test data registers: a bypass register, a boundary scan register, and a device identification register.
- A TAP controller state machine that controls the operation of the data registers, instruction register and associated circuitry.

1.5.32 On-chip voltage regulator (VREG)

The on-chip voltage regulator module provides the following features:

- Uses external NPN (negative-positive-negative) transistor
- Regulates external 3.3 V /5.0 V down to 1.2 V for the core logic
- Low voltage detection on the internal 1.2 V and I/O voltage 3.3 V

Table 6. System pins (continued)

Symbol	Description	Direction	Pad speed(1)		Pin	
			SRC = 0	SRC = 1	100-pin	144-pin
TMS	JTAG state machine control	Bidirectional	Slow	Fast	59	87
TCK	JTAG clock	Input only	Slow	—	60	88
TDI	Test Data In	Input only	Slow	Medium	58	86
TDO	Test Data Out	Output only	Slow	Fast	61	89
Reset pin, available on 100-pin and 144-pin package.						
$\overline{\text{RESET}}$	Bidirectional reset with Schmitt trigger characteristics and noise filter	Bidirectional	Medium	—	20	31
Test pin, available on 100-pin and 144-pin package.						
VPP_TEST	Pin for testing purpose only. To be tied to ground in normal operating mode.	—	—	—	74	107

1. SCR values refer to the value assigned to the Slew Rate Control bits of the pad configuration register.

2.2.3 Pin muxing

Table 7 defines the pin list and muxing for the SPC560P44Lx, SPC560P50Lx devices.

Each row of *Table 7* shows all the possible ways of configuring each pin, via alternate functions. The default function assigned to each pin after reset is the ALT0 function.

SPC560P44Lx, SPC560P50Lx devices provide four main I/O pad types, depending on the associated functions:

- *Slow pads* are the most common, providing a compromise between transition time and low electromagnetic emission.
- *Medium pads* provide fast enough transition for serial communication channels with controlled current to reduce electromagnetic emission.
- *Fast pads* provide maximum speed. They are used for improved NEXUS debugging capability.
- *Symmetric pads* are designed to meet FlexRay requirements.

Medium and Fast pads can use slow configuration to reduce electromagnetic emission, at the cost of reducing AC performance. For more information, see the datasheet's "Pad AC Specifications" section.

Table 7. Pin muxing (continued)

Port pin	Pad configuration register (PCR)	Alternate function[1], [2]	Functions	Peripheral[3]	I/O direction [4]	Pad speed[5]		Pin No.	
						SRC = 0	SRC = 1	100-pin	144-pin
F[14]	PCR[94]	ALT0 ALT1 ALT2 ALT3	GPIO[94] TXD — —	SIUL LIN_1 — —	I/O O — —	Slow	Medium	—	115
F[15]	PCR[95]	ALT0 ALT1 ALT2 ALT3 —	GPIO[95] — — — RXD	SIUL — — — LIN_1	I/O — — — I	Slow	Medium	—	113
Port G (12-bit)									
G[0]	PCR[96]	ALT0 ALT1 ALT2 ALT3 —	GPIO[96] F[0] — — EIRQ[30]	SIUL FCU_0 — — SIUL	I/O O — — I	Slow	Medium	—	38
G[1]	PCR[97]	ALT0 ALT1 ALT2 ALT3 —	GPIO[97] F[1] — — EIRQ[31]	SIUL FCU_0 — — SIUL	I/O O — — I	Slow	Medium	—	141
G[2]	PCR[98]	ALT0 ALT1 ALT2 ALT3	GPIO[98] X[2] — —	SIUL FlexPWM_0 — —	I/O I/O — —	Slow	Medium	—	102
G[3]	PCR[99]	ALT0 ALT1 ALT2 ALT3	GPIO[99] A[2] — —	SIUL FlexPWM_0 — —	I/O O — —	Slow	Medium	—	104
G[4]	PCR[100]	ALT0 ALT1 ALT2 ALT3	GPIO[100] B[2] — —	SIUL FlexPWM_0 — —	I/O O — —	Slow	Medium	—	100
G[5]	PCR[101]	ALT0 ALT1 ALT2 ALT3	GPIO[101] X[3] — —	SIUL FlexPWM_0 — —	I/O I/O — —	Slow	Medium	—	85
G[6]	PCR[102]	ALT0 ALT1 ALT2 ALT3	GPIO[102] A[3] — —	SIUL FlexPWM_0 — —	I/O O — —	Slow	Medium	—	98

3.3 Absolute maximum ratings

Table 9. Absolute maximum ratings(1)

Symbol		Parameter	Conditions	Value		Unit
				Min	Max(2)	
V_{SS}	SR	Device ground	—	0	0	V
$V_{DD\_HV\_IOx}$(3)	SR	3.3 V / 5.0 V input/output supply voltage with respect to ground (V_{SS})	—	–0.3	6.0	V
$V_{SS\_HV\_IOx}$	SR	Input/output ground voltage with respect to ground (V_{SS})	—	–0.1	0.1	V
$V_{DD\_HV\_FL}$	SR	3.3 V / 5.0 V code and data flash supply voltage with respect to ground (V_{SS})	—	–0.3	6.0	V
			Relative to $V_{DD\_HV\_IOx}$		$V_{DD\_HV\_IOx}$ + 0.3	
$V_{SS\_HV\_FL}$	SR	Code and data flash ground with respect to ground (V_{SS})	—	–0.1	0.1	V
$V_{DD\_HV\_OSC}$	SR	3.3 V / 5.0 V crystal oscillator amplifier supply voltage with respect to ground (V_{SS})	—	–0.3	6.0	V
			Relative to $V_{DD\_HV\_IOx}$		$V_{DD\_HV\_IOx}$ + 0.3	
$V_{SS\_HV\_OSC}$	SR	3.3 V / 5.0 V crystal oscillator amplifier reference voltage with respect to ground (V_{SS})	—	–0.1	0.1	V
$V_{DD\_HV\_REG}$	SR	3.3 V / 5.0 V voltage regulator supply voltage with respect to ground (V_{SS})	—	–0.3	6.0	V
			Relative to $V_{DD\_HV\_IOx}$		$V_{DD\_HV\_IOx}$ + 0.3	
$V_{DD\_HV\_ADC0}$(4)	SR	3.3 V / 5.0 V ADC_0 supply and high reference voltage with respect to ground (V_{SS})	$V_{DD\_HV\_REG}$ < 2.7 V	–0.3	$V_{DD\_HV\_REG}$ + 0.3	V
			$V_{DD\_HV\_REG}$ > 2.7 V		6.0	
$V_{SS\_HV\_ADC0}$	SR	ADC_0 ground and low reference voltage with respect to ground (V_{SS})	—	–0.1	0.1	V
$V_{DD\_HV\_ADC1}$(4)	SR	3.3 V / 5.0 V ADC_0 supply and high reference voltage with respect to ground (V_{SS})	$V_{DD\_HV\_REG}$ < 2.7 V	–0.3	$V_{DD\_HV\_REG}$ + 0.3	V
			$V_{DD\_HV\_REG}$ > 2.7 V		6.0	
$V_{SS\_HV\_ADC1}$	SR	ADC_1 ground and low reference voltage with respect to ground (V_{SS})	—	–0.1	0.1	V
TV_{DD}	SR	Slope characteristics on all V_{DD} during power up(5) with respect to ground (V_{SS})	—	3.0	500 x 10^3 (0.5 [V/µs])	V/s
V_{IN}	SR	Voltage on any pin with respect to ground ($V_{SS\_HV\_IOx}$) with respect to ground (V_{SS})	—	–0.3	6.0	V
			Relative to $V_{DD\_HV\_IOx}$		$V_{DD\_HV\_IOx}$ + 0.3	

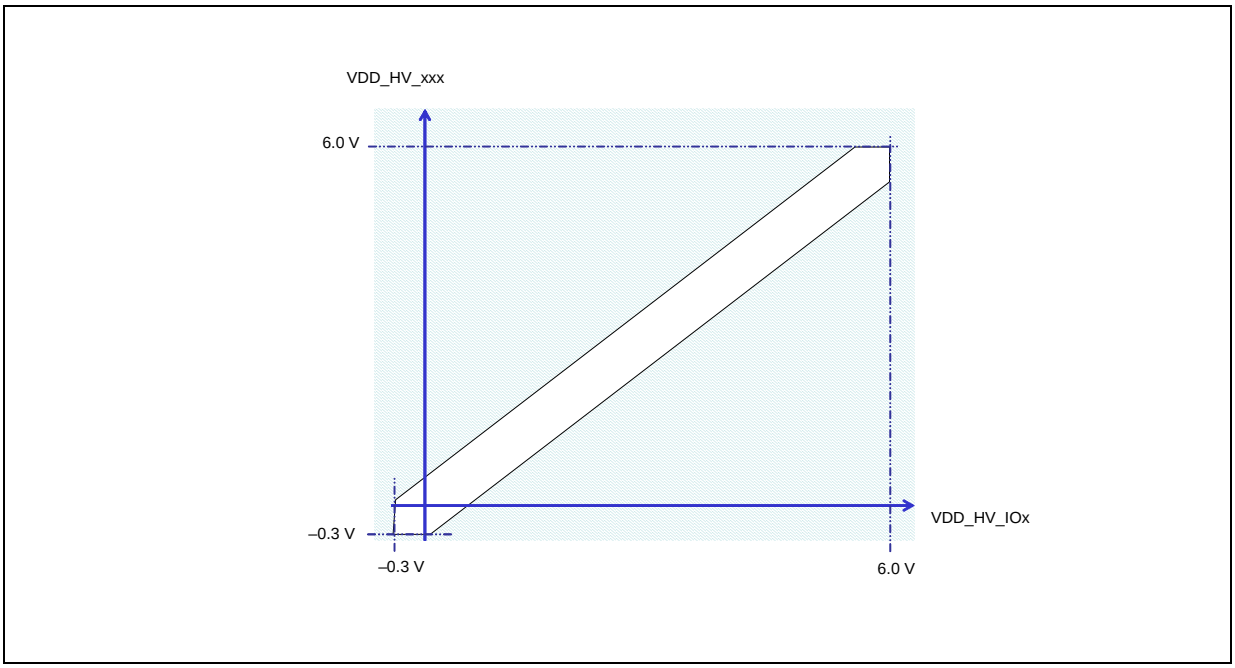


Figure 5. Power supplies constraints (–0.3 V ≤ $V_{DD\_HV\_IOx}$ ≤ 6.0 V)

The SPC560P44Lx, SPC560P50Lx supply architecture allows of having ADC supply managed independently from standard V_{DD_HV} supply. *Figure 6* shows the constraints of the ADC power supply.

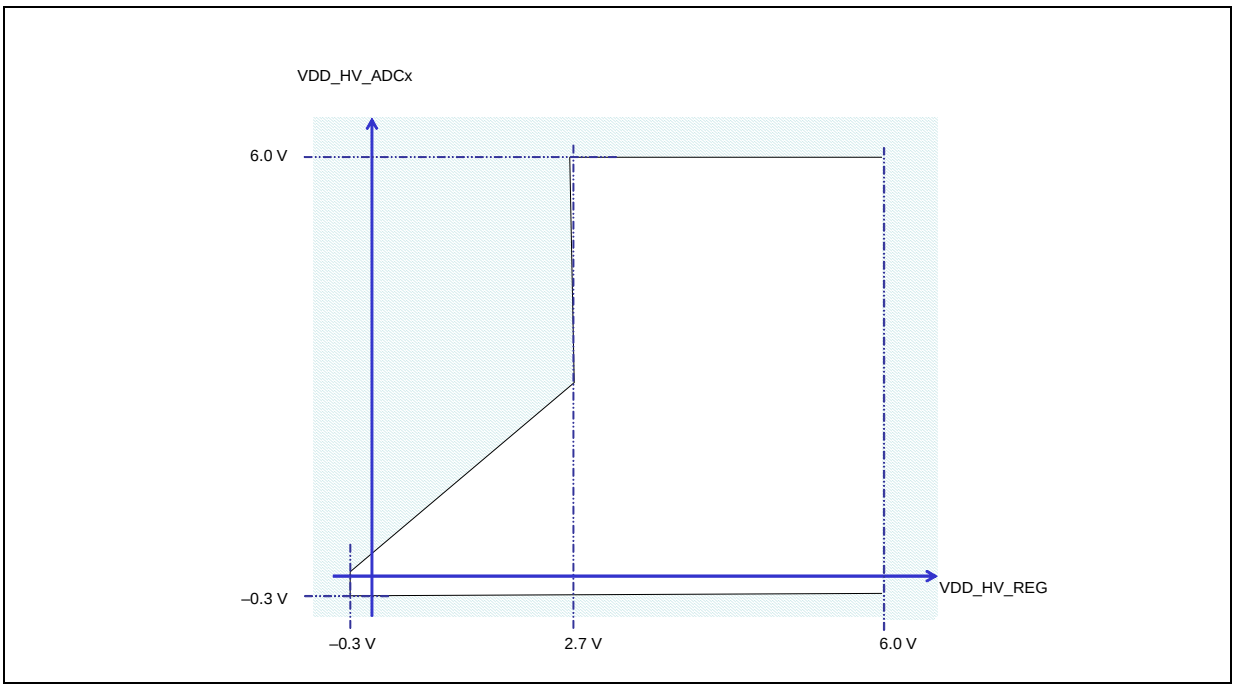


Figure 6. Independent ADC supply (–0.3 V ≤ $V_{DD\_HV\_REG}$ ≤ 6.0 V)

Table 16. Approved NPN ballast components (configuration with resistor on base)

Part	Manufacturer	Approved derivatives(1)
BC817	Infineon	BC817-16;BC817-25;BC817SU;
	NXP	BC817-16;BC817-25
BCP56	ST	BCP56-16
	Infineon	BCP56-10;BCP56-16
	ON Semi	BCP56-10
	NXP	BCP56-10;BCP56-16

1. For automotive applications please check with the appropriate transistor vendor for automotive grade certification

Table 17. Voltage regulator electrical characteristics (configuration with resistor on base)

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
$V_{DD\_LV\_REGCOR}$	CC	P	Output voltage under maximum load run supply current configuration	Post-trimming	1.15	—	1.32	V
R_B	SR	—	External resistance on bipolar junction transistor (BJT) base	—	18	—	22	kΩ
C_{DEC1}	SR	—	External decoupling/stability ceramic capacitor	BJT from *Table 16*. 3 capacitances (i.e. X7R or X8R capacitors) with nominal value of 10 µF	19.5	30	—	µF
				BJT BC817, one capacitance of 22 µF	14.3	22		µF
R_{REG}	SR	—	Resulting ESR of all three capacitors of C_{DEC1}	BJT from *Table 16*. 3x10 µF. Absolute maximum value between 100 kHz and 10 MHz	—	—	50	mΩ
			Resulting ESR of the unique capacitor C_{DEC1}	BJT BC817, 1x 22 µF. Absolute maximum value between 100 kHz and 10 MHz	10	—	40	mΩ
C_{DEC2}	SR	—	External decoupling/stability ceramic capacitor	4 capacitances (i.e. X7R or X8R capacitors) with nominal value of 440 nF	1200	1760	—	nF
C_{DEC3}	SR	—	External decoupling/stability ceramic capacitor on $V_{DD\_HV\_REG}$	3 capacitances (i.e. X7R or X8R capacitors) with nominal value of 10 µF; C_{DEC3} has to be equal or greater than C_{DEC1}	19.5	30	—	µF
L_{Reg}	SR	—	Resulting ESL of $V_{DD\_HV\_REG}$, BCTRL and $V_{DD\_LV\_CORx}$ pins	—	—	—	15	nH

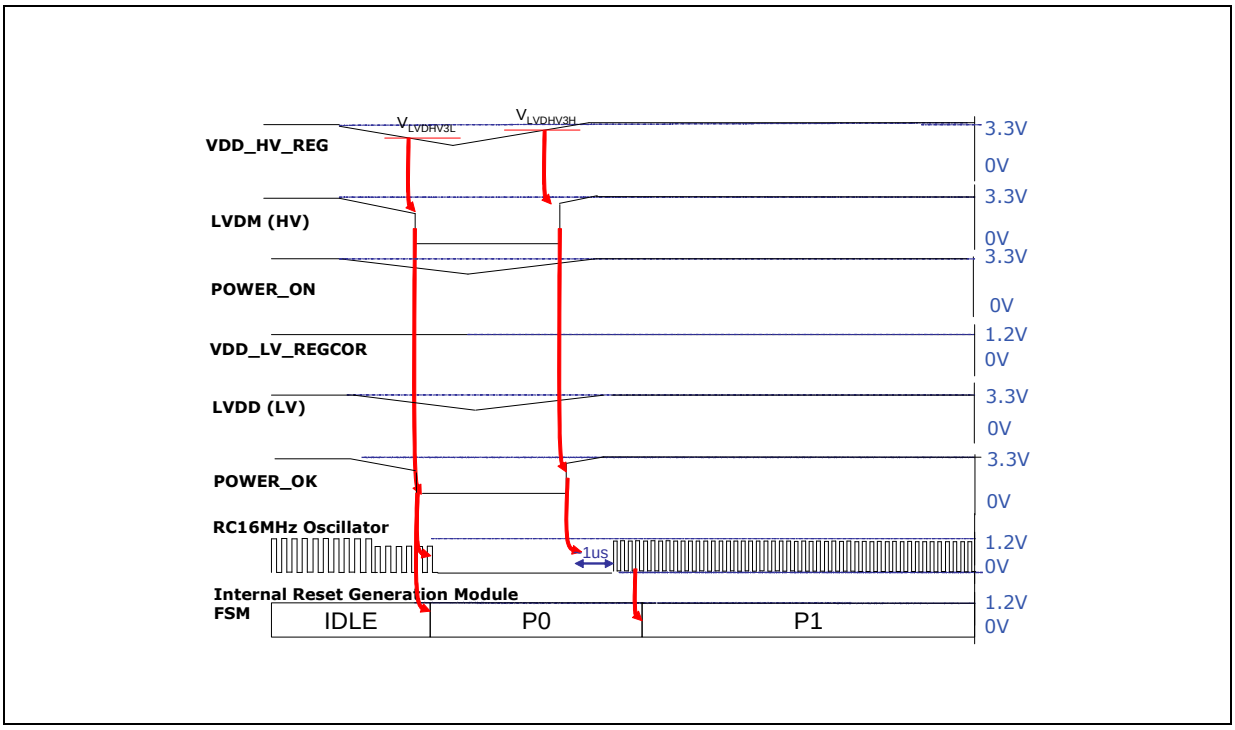


Figure 13. Brown-out typical sequence

3.10 DC electrical characteristics

3.10.1 NVUSRO register

Portions of the device configuration, such as high voltage supply, and watchdog enable/disable after reset are controlled via bit values in the non-volatile user options (NVUSRO) register.

For a detailed description of the NVUSRO register, please refer to the device reference manual.

NVUSRO[PAD3V5V] field description

The DC electrical characteristics are dependent on the PAD3V5V bit value. *Table 20* shows how NVUSRO[PAD3V5V] controls the device configuration.

Table 20. PAD3V5V field description

Value(1)	Description
0	High voltage supply is 5.0 V
1	High voltage supply is 3.3 V

1. Default manufacturing value before flash initialization is ‘1’ (3.3 V).

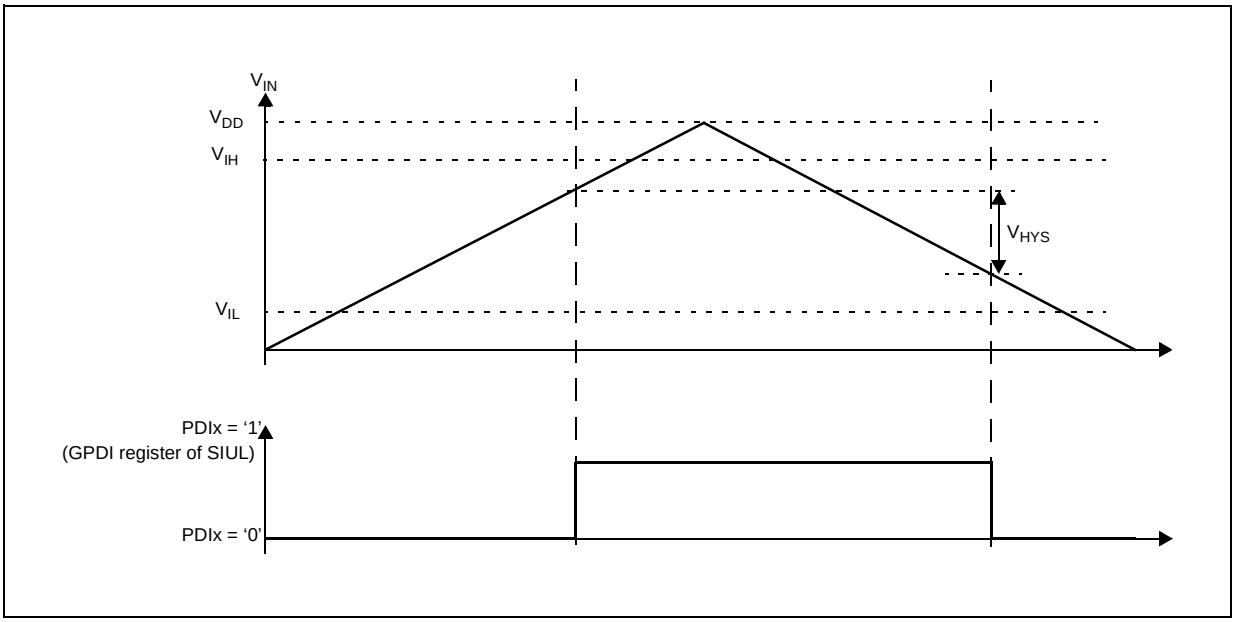


Figure 14. Input DC electrical characteristics definition

3.10.5 I/O pad current specification

The I/O pads are distributed across the I/O supply segment. Each I/O supply segment is associated to a V_{DD}/V_{SS} supply pair as described in *Table 25*.

Table 25. I/O supply segment

Package	Supply segment						
	1	2	3	4	5	6	7
LQFP144	pin8 – pin20	pin23 – pin38	pin39 – pin55	pin58 – pin68	pin73 – pin89	pin92 – pin125	pin128 – pin5
LQFP100	pin15 – pin26	pin27 – pin38	pin41 – pin46	pin51 – pin61	pin64 – pin86	pin89 – pin10	—

Table 26 provides the weight of concurrent switching I/Os.

In order to ensure device functionality, the sum of the weight of concurrent switching I/Os on a single segment should remain below 100%.

Table 26. I/O weight

Pad	LQFP144		LQFP100	
	Weight 5V	Weight 3.3V	Weight 5V	Weight 3.3V
NMI	1%	1%	1%	1%
PAD[6]	6%	5%	14%	13%
PAD[49]	5%	4%	14%	12%
PAD[84]	14%	10%	—	—
PAD[85]	9%	7%	—	—

Table 26. I/O weight (continued)

Pad	LQFP144		LQFP100	
	Weight 5V	Weight 3.3V	Weight 5V	Weight 3.3V
PAD[60]	11%	10%	11%	10%
PAD[100]	12%	10%	—	—
PAD[45]	12%	10%	12%	10%
PAD[98]	12%	11%	—	—
PAD[46]	12%	11%	12%	11%
PAD[99]	13%	11%	—	—
PAD[62]	13%	11%	13%	11%
PAD[92]	13%	12%	—	—
VPP_TEST	1%	1%	1%	1%
PAD[4]	14%	12%	14%	12%
PAD[16]	13%	12%	13%	12%
PAD[17]	13%	11%	13%	11%
PAD[42]	13%	11%	13%	11%
PAD[93]	12%	11%	—	—
PAD[95]	12%	11%	—	—
PAD[18]	12%	10%	12%	10%
PAD[94]	11%	10%	—	—
PAD[19]	11%	10%	11%	10%
PAD[77]	10%	9%	—	—
PAD[10]	10%	9%	10%	9%
PAD[78]	9%	8%	—	—
PAD[11]	9%	8%	9%	8%
PAD[79]	8%	7%	—	—
PAD[12]	7%	7%	7%	7%
PAD[41]	7%	6%	7%	6%
PAD[47]	5%	4%	5%	4%
PAD[48]	4%	4%	4%	4%
PAD[51]	4%	4%	4%	4%
PAD[52]	5%	4%	5%	4%
PAD[40]	5%	5%	6%	5%
PAD[80]	9%	8%	—	—
PAD[9]	10%	9%	11%	10%
PAD[81]	10%	9%	—	—

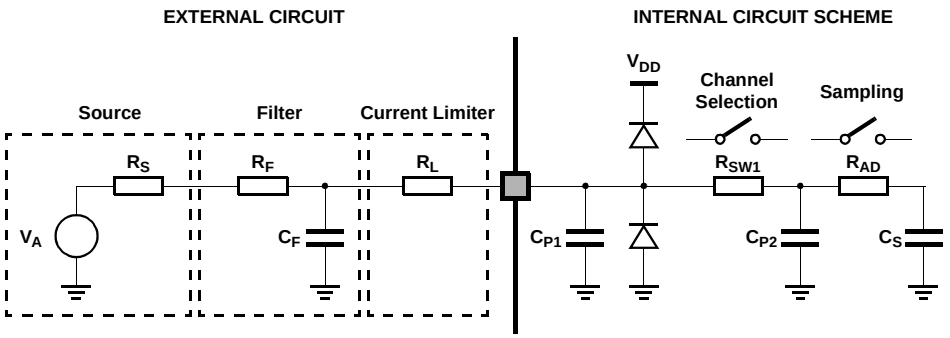
The filter at the input pins must be designed taking into account the dynamic characteristics of the input signal (bandwidth) and the equivalent input impedance of the ADC itself.

In fact a current sink contributor is represented by the charge sharing effects with the sampling capacitance: C_S and C_{P2} being substantially two switched capacitances, with a frequency equal to the ADC conversion rate, it can be seen as a resistive path to ground. For instance, assuming a conversion rate of 1 MHz, with C_S+C_{P2} equal to 3 pF, a resistance of 330 kΩ is obtained (R_{EQ} = 1 / (fc × (C_S+C_{P2})), where fc represents the conversion rate at the considered channel). To minimize the error induced by the voltage partitioning between this resistance (sampled voltage on C_S+C_{P2}) and the sum of R_S + R_F, the external circuit must be designed to respect the *Equation 4*:

Equation 4

$$V_A \bullet \frac{R_S + R_F}{R_{EQ}} < \frac{1}{2} LSB$$

Equation 4 generates a constraint for external network design, in particular on resistive path.



R_S: Source impedance
R_F: Filter resistance
C_F: Filter capacitance
R_L: Current limiter resistance
R_{SW1}: Channel selection switch impedance
R_{AD}: Sampling switch impedance
C_P: Pin capacitance (two contributions, C_{P1} and C_{P2})
C_S: Sampling capacitance

Figure 16. Input equivalent circuit

Calling f_0 the bandwidth of the source signal (and as a consequence the cut-off frequency of the anti-aliasing filter, f_F), according to the Nyquist theorem the conversion rate f_C must be at least $2f_0$; it means that the constant time of the filter is greater than or at least equal to twice the conversion period (T_C). Again the conversion period T_C is longer than the sampling time T_S, which is just a portion of it, even when fixed channel continuous conversion mode is selected (fastest conversion rate at a specific channel): in conclusion it is evident that the time constant of the filter R_FC_F is definitively much higher than the sampling time T_S, so the charge level on C_S cannot be modified by the analog signal source during the time in which the sampling switch is closed.

The considerations above lead to impose new constraints on the external circuit, to reduce the accuracy error due to the voltage drop on C_S; from the two charge balance equations above, it is simple to derive *Equation 11* between the ideal and real sampled voltage on C_S:

Equation 11

$$\frac{V_A}{V_{A2}} = \frac{C_{P1} + C_{P2} + C_F}{C_{P1} + C_{P2} + C_F + C_S}$$

From this formula, in the worst case (when V_A is maximum, that is for instance 5 V), assuming to accept a maximum error of half a count, a constraint is evident on C_F value:

Equation 12

$$C_F > 2048 \bullet C_S$$

3.14.2 ADC conversion characteristics

Table 33. ADC conversion characteristics

Symbol		C	Parameter	Conditions(1)	Value			Unit
					Min	Typ	Max	
V_{INAN0}	SR		ADC0 and shared ADC0/1 analog input voltage(2), (3)	—	$V_{SS\_HV\_ADV0}$ – 0.3	—	$V_{DD\_HV\_ADV0}$ + 0.3	V
V_{INAN1}	SR		ADC1 analog input voltage(2), (4)	—	$V_{SS\_HV\_ADV1}$ – 0.3	—	$V_{DD\_HV\_ADV1}$ + 0.3	V
f_{CK}	SR	—	ADC clock frequency (depends on ADC configuration) (The duty cycle depends on AD_clk(5) frequency)	—	3(6)	—	60	MHz
f_s	SR	—	Sampling frequency	—	—	—	1.53	MHz
t_{ADC_S}	—	D	Sample time(7)	f_{ADC} = 20 MHz, INPSAMP = 3	125	—	—	ns
				f_{ADC} = 9 MHz, INPSAMP = 255	—	—	28.2	µs
t_{ADC_C}	—	P	Conversion time(8)	f_{ADC} = 20 MHz(9), INPCMP = 1	0.650	—	—	µs

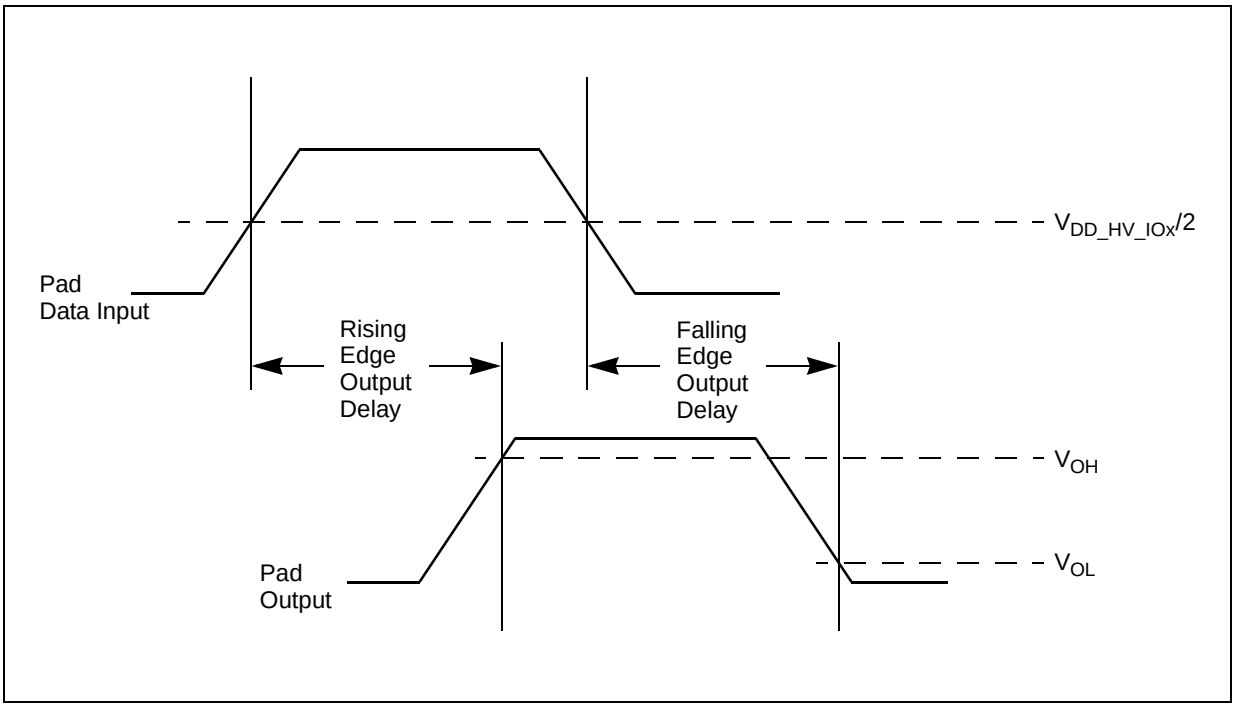


Figure 19. Pad output delay

3.17 AC timing characteristics

3.17.1 $\overline{\text{RESET}}$ pin characteristics

The SPC560P44Lx, SPC560P50Lx implements a dedicated bidirectional $\overline{\text{RESET}}$ pin.

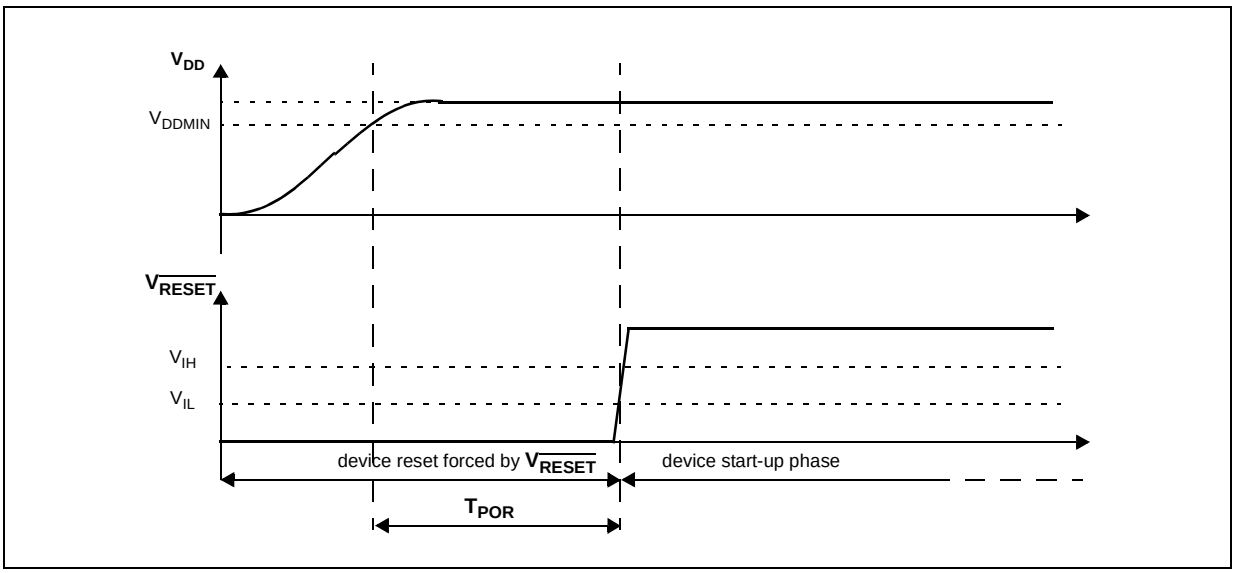


Figure 20. Start-up reset requirements

Table 38. $\overline{\text{RESET}}$ electrical characteristics (continued)

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
t_{tr}	CC	D	Output transition time output pin[3] MEDIUM configuration	C_L = 25pF, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	10	ns
				C_L = 50pF, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	20	
				C_L = 100pF, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	40	
				C_L = 25pF, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	12	
				C_L = 50pF, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	25	
				C_L = 100pF, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	40	
W_{FRST}	SR	P	$\overline{\text{RESET}}$ input filtered pulse	—	—	—	40	ns
W_{NFRST}	SR	P	$\overline{\text{RESET}}$ input not filtered pulse	—	500	—	—	ns
t_{POR}	CC	D	Maximum delay before internal reset is released after all V_{DD_HV} reach nominal supply	Monotonic V_{DD_HV} supply ramp	—	—	1	ms
$\lvert I_{WPU} \rvert$	CC	P	Weak pull-up current absolute value	V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	10	—	150	µA
				V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	10	—	150	
				V_{DD} = 5.0 V ± 10%, PAD3V5V = 1[4]	10	—	250	

1. V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 °C to $T_{A\ MAX}$, unless otherwise specified
2. This is a transient configuration during power-up, up to the end of reset PHASE2 (refer to RGM module section of device reference manual).
3. C_L includes device and package capacitance (C_{PKG} < 5 pF).
4. The configuration PAD3V5 = 1 when V_{DD} = 5 V is only transient configuration during power-up. All pads but RESET and Nexus output (MDOx, EVTO, MCKO) are configured in input or in high impedance state.

3.17.2 IEEE 1149.1 interface timing

Table 39. JTAG pin AC electrical characteristics

No.	Symbol		C	Parameter	Conditions	Value		Unit
						Min	Max	
1	t_{JCYC}	CC	D	TCK cycle time	—	100	—	ns
2	t_{JDC}	CC	D	TCK clock pulse width (measured at $V_{DD\_HV\_IOx}$/2)	—	40	60	ns
3	$t_{TCKRISE}$	CC	D	TCK rise and fall times (40% – 70%)	—	—	3	ns
4	t_{TMSS}, t_{TDIS}	CC	D	TMS, TDI data setup time	—	5	—	ns

Table 44. LQFP100 package mechanical data

Symbol	Dimensions					
	mm			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	—	—	1.600	—	—	0.0630
A1	0.050	—	0.150	0.0020	—	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	—	0.200	0.0035	—	0.0079
D	15.800	16.000	16.200	0.6220	0.6299	0.6378
D1	13.800	14.000	14.200	0.5433	0.5512	0.5591
D3	—	12.000	—	—	0.4724	—
E	15.800	16.000	16.200	0.6220	0.6299	0.6378
E1	13.800	14.000	14.200	0.5433	0.5512	0.5591
E3	—	12.000	—	—	0.4724	—
e	—	0.500	—	—	0.0197	—
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	—	1.000	—	—	0.0394	—
k	0.0°	3.5°	7.0°	0.0°	3.5°	7.0°
ccc[2]	0.08			0.0031		

1. Values in inches are converted from millimeters (mm) and rounded to four decimal digits.
2. Tolerance

Table 46. Revision history (continued)

Date	Revision	Changes
07-Apr-2011	7 (cont'd)	SPC560P44Lx, SPC560P50Lx device configuration differences: Removed "temperature" row (temperature information is provided in Order codes) Updated SPC560P44Lx, SPC560P50Lx block diagram Added SPC560P44Lx, SPC560P50Lx series block summary Added *Section 1.5 Feature details* *Section 2.1, Package pinouts*: removed alternate functions from pinout diagrams Supply pins: updated descriptions of power supply pins (1.2 V) System pins: updated table Pin muxing: added rows "B[4]" and "B[5] *Section 3.3, Absolute maximum ratings*: added voltage specifications to titles of *Figure 5* and *Figure 6*; in *Table 9*, changed row "V_{SS_HV} / Digital Ground" to "V_{SS} / Device Ground"; updated symbols *Section 3.4, Recommended operating conditions*: added voltage specifications to titles of *Figure 7* and *Figure 8* Recommended operating conditions (5.0 V), and Recommended operating conditions (3.3 V): changed row "V_{SS_HV} / Digital Ground" to "V_{SS} / Device Ground"; updated symbols Updated *Section 3.5.1, Package thermal characteristics* Updated *Section 3.6, Electromagnetic interference (EMI) characteristics* *Section 3.8.1, Voltage regulator electrical characteristics*: amended titles of *Table 16* and *Table 19* Voltage regulator electrical characteristics (configuration without resistor on base) and Voltage regulator electrical characteristics (configuration with resistor on base): updated symbol and values for $V_{DD\_LV\_REGCOR}$ Low voltage monitor electrical characteristics: Updated $V_{MLVDDOK\_H}$ max value—was 1.15 V; is 1.145 V *Section 3.10, DC electrical characteristics*: reorganized contents Updated *Section 3.10.1, NVUSRO register* (includes adding *Section NVUSRO[OSCILLATOR_MARGIN] field description*) Supply current (5.0 V, NVUSRO[PAD3V5V] = 0): updated symbols Corrected parameter descriptions in DC electrical characteristics (3.3 V, NVUSRO[PAD3V5V] = 1): – V_{OL_F}—was "Fast, high level output voltage"; is "Fast, low level output voltage" – V_{OL_SYM}—was "Symmetric, high level output voltage"; is "Symmetric, low level output voltage" Supply current (3.3 V, NVUSRO[PAD3V5V] = 1): updated symbols Main oscillator output electrical characteristics (5.0 V, NVUSRO[PAD3V5V] = 0): replaced instances of EXTAL with XTAL Main oscillator output electrical characteristics (3.3 V, NVUSRO[PAD3V5V] = 1): replaced instances of EXTAL with XTAL FMPLL electrical characteristics: replaced "PLLMRFM" with "FMPLL" in table title; updated conditions; removed f_{sys} row; updated $f_{FMPLLOUT}$ min value ADC conversion characteristics: updated symbols; added row t_{ADC_PU} Flash memory read access timing: added footnote to "Conditions" column *Section 3.16.1, Pad AC specifications*: added Pad output delay diagram In the range of figures "DSPI Classic SPI Timing — Master, CPHA = 0" to "DSPI PCS Strobe (PCSS) Timing": added note Updated Order codes Updated "Commercial product code structure" figure *Table 45*: Added abbreviations "DUT", "NPN", and "RBW"