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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	e200z0h
Core Size	32-Bit Single-Core
Speed	64MHz
Connectivity	CANbus, LINbus, SPI, UART/USART
Peripherals	DMA, POR, PWM, WDT
Number of I/O	67
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	40K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 26x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/spc560p50l3cefay

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Table 3. SPC560P44Lx, SPC560P50Lx device configuration differences (continued)

Feature	Full-featured	Airbag
FlexRay	Yes	No
FMPLL (frequency-modulated phase-locked loop) module	2 (one FMPLL, one for FlexRay)	1 (only FMPLL)

1.4 Block diagram

Figure 1 shows a top-level block diagram of the SPC560P44Lx, SPC560P50Lx MCU.

For high priority interrupt requests, the time from the assertion of the interrupt request from the peripheral to when the processor is executing the interrupt service routine (ISR) has been minimized. The INTC provides a unique vector for each interrupt request source for quick determination of which ISR has to be executed. It also provides a wide number of priorities so that lower priority ISRs do not delay the execution of higher priority ISRs. To allow the appropriate priorities for each source of interrupt request, the priority of each interrupt request is software configurable.

When multiple tasks share a resource, coherent accesses to that resource need to be supported. The INTC supports the priority ceiling protocol (PCP) for coherent accesses. By providing a modifiable priority mask, the priority can be raised temporarily so that all tasks which share the same resource can not preempt each other.

The INTC provides the following features:

- Unique 9-bit vector for each separate interrupt source
- 8 software triggerable interrupt sources
- 16 priority levels with fixed hardware arbitration within priority levels for each interrupt source
- Ability to modify the ISR or task priority: modifying the priority can be used to implement the Priority Ceiling Protocol for accessing shared resources.
- 2 external high priority interrupts directly accessing the main core and I/O processor (IOP) critical interrupt mechanism

1.5.7 System status and configuration module (SSCM)

The system status and configuration module (SSCM) provides central device functionality.

The SSCM includes these features:

- System configuration and status
  - Memory sizes/status
  - Device mode and security status
  - Determine boot vector
  - Search code flash for bootable sector
  - DMA status
- Debug status port enable and selection
- Bus and peripheral abort enable/disable

1.5.8 System clocks and clock generation

The following list summarizes the system clock and clock generation on the SPC560P44Lx, SPC560P50Lx:

- Lock detect circuitry continuously monitors lock status
- Loss of clock (LOC) detection for PLL outputs
- Programmable output clock divider (÷1, ÷2, ÷4, ÷8)
- FlexPWM module and eTimer module can run on an independent clock source
- On-chip oscillator with automatic level control
- Internal 16 MHz RC oscillator for rapid start-up and safe mode: supports frequency trimming by user application

The sources of the ECC errors are:

- Flash memory
- SRAM

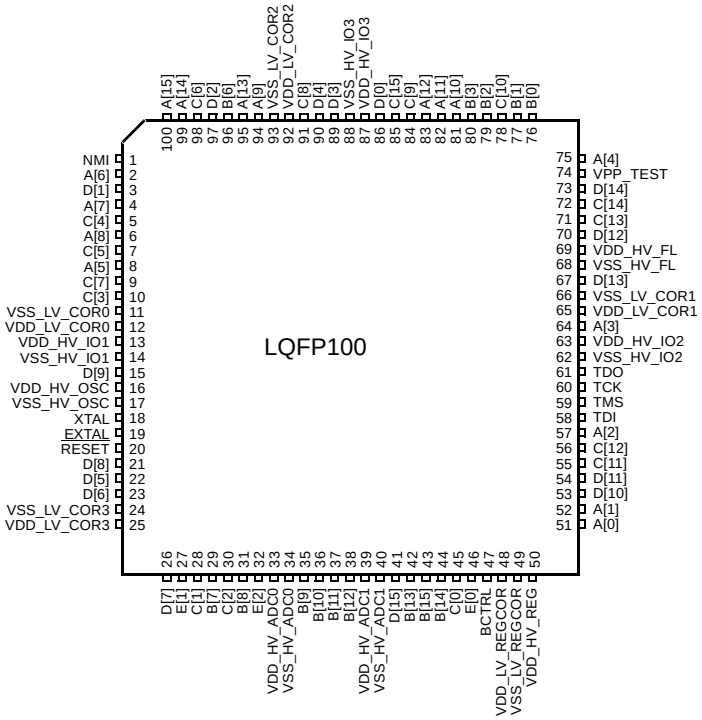
1.5.19 Peripheral bridge (PBRIDGE)

The PBRIDGE implements the following features:

- Duplicated periphery
- Master access privilege level per peripheral (per master: read access enable; write access enable)
- Write buffering for peripherals
- Checker applied on PBRIDGE output toward periphery
- Byte endianess swap capability

1.5.20 Controller area network (FlexCAN)

The SPC560P44Lx, SPC560P50Lx MCU contains one controller area network (FlexCAN) module. This module is a communication controller implementing the CAN protocol according to Bosch Specification version 2.0B. The CAN protocol was designed to be used primarily as a vehicle serial data bus, meeting the specific requirements of this field: real-time processing, reliable operation in the EMI environment of a vehicle, cost-effectiveness and required bandwidth. The FlexCAN module contains 32 message buffers.



Note: Availability of port pin alternate functions depends on product selection.

Figure 4. 100-pin LQFP pinout – Full featured configuration (top view)

2.2 Pin description

The following sections provide signal descriptions and related information about the functionality and configuration of the SPC560P44Lx, SPC560P50Lx devices.

2.2.1 Power supply and reference voltage pins

Table 5 lists the power supply and reference voltage for the SPC560P44Lx, SPC560P50Lx devices.

Table 5. Supply pins (continued)

Supply		Pin	
Symbol	**Description**	**100-pin**	**144-pin**
$V_{DD\_LV\_COR1}$	1.2 V Decoupling pins for core logic. Decoupling capacitor must be connected between these pins and the nearest $V_{SS\_LV\_COR}$ pin.	65	93
$V_{SS\_LV\_COR1}$	1.2 V Decoupling pins for core logic. Decoupling capacitor must be connected between these pins and the nearest $V_{DD\_LV\_COR}$ pin.	66	94
$V_{DD\_LV\_COR2}$	1.2 V Decoupling pins for core logic. Decoupling capacitor must be connected between these pins and the nearest $V_{SS\_LV\_COR}$ pin.	92	131
$V_{SS\_LV\_COR2}$	1.2 V Decoupling pins for core logic. Decoupling capacitor must be connected between these pins and the nearest $V_{DD\_LV\_COR}$ pin.	93	132
$V_{DD\_LV\_COR3}$	1.2 V Decoupling pins for on-chip PLL modules. Decoupling capacitor must be connected between this pin and $V_{SS\_LV\_COR3}$.	25	36
$V_{SS\_LV\_COR3}$	1.2 V Decoupling pins for on-chip PLL modules. Decoupling capacitor must be connected between this pin and $V_{DD\_LV\_COR3}$.	24	35

1. Analog supply/ground and high/low reference lines are internally physically separate, but are shorted via a double-bonding connection on $V_{DD\_HV\_ADCx}$/$V_{SS\_HV\_ADCx}$ pins.
2. Not available on 100-pin package.

2.2.2 System pins

Table 5 and *Table 6* contain information on pin functions for the SPC560P44Lx, SPC560P50Lx devices. The pins listed in *Table 6* are single-function pins. The pins shown in *Table 7* are multi-function pins, programmable via their respective Pad Configuration Register (PCR) values.

Table 6. System pins

Symbol	Description	Direction	Pad speed(1)		Pin	
			SRC = 0	SRC = 1	100-pin	144-pin
Dedicated pins. Available on 100-pin and 144-pin package.						
MDO[0]	Nexus Message Data Output—line 0	Output only	Fast		—	9
NMI	Non-Maskable Interrupt	Input only	Slow	—	1	1
XTAL	Analog output of the oscillator amplifier circuit; needs to be grounded if oscillator is used in bypass mode	—	—	—	18	29
EXTAL	– Analog input of oscillator amplifier circuit, when oscillator not in bypass mode – Analog input for clock generator when oscillator in bypass mode	—	—	—	19	30

Table 7. Pin muxing

Port pin	Pad configuration register (PCR)	Alternate function[1], [2]	Functions	Peripheral[3]	I/O direction [4]	Pad speed[5]		Pin No.	
						SRC = 0	SRC = 1	100-pin	144-pin
Port A (16-bit)									
A[0]	PCR[0]	ALT0 ALT1 ALT2 ALT3 —	GPIO[0] ETC[0] SCK F[0] EIRQ[0]	SIUL eTimer_0 DSPI_2 FCU_0 SIUL	I/O I/O O O I	Slow	Medium	51	73
A[1]	PCR[1]	ALT0 ALT1 ALT2 ALT3 —	GPIO[1] ETC[1] SOUT F[1] EIRQ[1]	SIUL eTimer_0 DSPI_2 FCU_0 SIUL	I/O I/O O O I	Slow	Medium	52	74
A[2][6]	PCR[2]	ALT0 ALT1 ALT2 ALT3 — — —	GPIO[2] ETC[2] — A[3] SIN ABS[0] EIRQ[2]	SIUL eTimer_0 — FlexPWM_0 DSPI_2 MC_RGM SIUL	I/O I/O — O I I I	Slow	Medium	57	84
A[3][6]	PCR[3]	ALT0 ALT1 ALT2 ALT3 — —	GPIO[3] ETC[3] CS0 B[3] ABS[2] EIRQ[3]	SIUL eTimer_0 DSPI_2 FlexPWM_0 MC_RGM SIUL	I/O I/O I/O O I I	Slow	Medium	64	92
A[4][6]	PCR[4]	ALT0 ALT1 ALT2 ALT3 — —	GPIO[4] ETC[0] CS1 ETC[4] FAB EIRQ[4]	SIUL eTimer_1 DSPI_2 eTimer_0 MC_RGM SIUL	I/O I/O O I/O I I	Slow	Medium	75	108
A[5]	PCR[5]	ALT0 ALT1 ALT2 ALT3 —	GPIO[5] CS0 ETC[5] CS7 EIRQ[5]	SIUL DSPI_1 eTimer_1 DSPI_0 SIUL	I/O I/O I/O O I	Slow	Medium	8	14
A[6]	PCR[6]	ALT0 ALT1 ALT2 ALT3 —	GPIO[6] SCK — — EIRQ[6]	SIUL DSPI_1 — — SIUL	I/O I/O — — I	Slow	Medium	2	2

Table 7. Pin muxing (continued)

Port pin	Pad configuration register (PCR)	Alternate function[1],[2]	Functions	Peripheral[3]	I/O direction[4]	Pad speed[5]		Pin No.	
						SRC = 0	SRC = 1	100-pin	144-pin
B[7]	PCR[23]	ALT0 ALT1 ALT2 ALT3 — —	GPIO[23] — — — AN[0] RXD	SIUL — — — ADC_0 LIN_0	Input only	—	—	29	43
B[8]	PCR[24]	ALT0 ALT1 ALT2 ALT3 — —	GPIO[24] — — — AN[1] ETC[5]	SIUL — — — ADC_0 eTimer_0	Input only	—	—	31	47
B[9]	PCR[25]	ALT0 ALT1 ALT2 ALT3 —	GPIO[25] — — — AN[11]	SIUL — — — ADC_0 / ADC_1	Input only	—	—	35	52
B[10]	PCR[26]	ALT0 ALT1 ALT2 ALT3 —	GPIO[26] — — — AN[12]	SIUL — — — ADC_0 / ADC_1	Input only	—	—	36	53
B[11]	PCR[27]	ALT0 ALT1 ALT2 ALT3 —	GPIO[27] — — — AN[13]	SIUL — — — ADC_0 / ADC_1	Input only	—	—	37	54
B[12]	PCR[28]	ALT0 ALT1 ALT2 ALT3 —	GPIO[28] — — — AN[14]	SIUL — — — ADC_0 / ADC_1	Input only	—	—	38	55
B[13]	PCR[29]	ALT0 ALT1 ALT2 ALT3 — —	GPIO[29] — — — AN[0] RXD	SIUL — — — ADC_1 LIN_1	Input only	—	—	42	60

Table 7. Pin muxing (continued)

Port pin	Pad configuration register (PCR)	Alternate function[1],[2]	Functions	Peripheral[3]	I/O direction[4]	Pad speed[5]		Pin No.	
						SRC = 0	SRC = 1	100-pin	144-pin
B[14]	PCR[30]	ALT0 ALT1 ALT2 ALT3 — — —	GPIO[30] — — — AN[1] ETC[4] EIRQ[19]	SIUL — — — ADC_1 eTimer_0 SIUL	Input only	—	—	44	64
B[15]	PCR[31]	ALT0 ALT1 ALT2 ALT3 — —	GPIO[31] — — — AN[2] EIRQ[20]	SIUL — — — ADC_1 SIUL	Input only	—	—	43	62
Port C (16-bit)									
C[0]	PCR[32]	ALT0 ALT1 ALT2 ALT3 —	GPIO[32] — — — AN[3]	SIUL — — — ADC_1	Input only	—	—	45	66
C[1]	PCR[33]	ALT0 ALT1 ALT2 ALT3 —	GPIO[33] — — — AN[2]	SIUL — — — ADC_0	Input only	—	—	28	41
C[2]	PCR[34]	ALT0 ALT1 ALT2 ALT3 —	GPIO[34] — — — AN[3]	SIUL — — — ADC_0	Input only	—	—	30	45
C[3]	PCR[35]	ALT0 ALT1 ALT2 ALT3 —	GPIO[35] CS1 ETC[4] TXD EIRQ[21]	SIUL DSPI_0 eTimer_1 LIN_1 SIUL	I/O O I/O O I	Slow	Medium	10	16
C[4]	PCR[36]	ALT0 ALT1 ALT2 ALT3 —	GPIO[36] CS0 X[1] DEBUG[4] EIRQ[22]	SIUL DSPI_0 FlexPWM_0 SSCM SIUL	I/O I/O I/O — I	Slow	Medium	5	11

Table 7. Pin muxing (continued)

Port pin	Pad configuration register (PCR)	Alternate function[1], [2]	Functions	Peripheral[3]	I/O direction [4]	Pad speed[5]		Pin No.	
						SRC = 0	SRC = 1	100-pin	144-pin
F[14]	PCR[94]	ALT0 ALT1 ALT2 ALT3	GPIO[94] TXD — —	SIUL LIN_1 — —	I/O O — —	Slow	Medium	—	115
F[15]	PCR[95]	ALT0 ALT1 ALT2 ALT3 —	GPIO[95] — — — RXD	SIUL — — — LIN_1	I/O — — — I	Slow	Medium	—	113
Port G (12-bit)									
G[0]	PCR[96]	ALT0 ALT1 ALT2 ALT3 —	GPIO[96] F[0] — — EIRQ[30]	SIUL FCU_0 — — SIUL	I/O O — — I	Slow	Medium	—	38
G[1]	PCR[97]	ALT0 ALT1 ALT2 ALT3 —	GPIO[97] F[1] — — EIRQ[31]	SIUL FCU_0 — — SIUL	I/O O — — I	Slow	Medium	—	141
G[2]	PCR[98]	ALT0 ALT1 ALT2 ALT3	GPIO[98] X[2] — —	SIUL FlexPWM_0 — —	I/O I/O — —	Slow	Medium	—	102
G[3]	PCR[99]	ALT0 ALT1 ALT2 ALT3	GPIO[99] A[2] — —	SIUL FlexPWM_0 — —	I/O O — —	Slow	Medium	—	104
G[4]	PCR[100]	ALT0 ALT1 ALT2 ALT3	GPIO[100] B[2] — —	SIUL FlexPWM_0 — —	I/O O — —	Slow	Medium	—	100
G[5]	PCR[101]	ALT0 ALT1 ALT2 ALT3	GPIO[101] X[3] — —	SIUL FlexPWM_0 — —	I/O I/O — —	Slow	Medium	—	85
G[6]	PCR[102]	ALT0 ALT1 ALT2 ALT3	GPIO[102] A[3] — —	SIUL FlexPWM_0 — —	I/O O — —	Slow	Medium	—	98

2. Junction-to-board thermal resistance determined per JEDEC JESD51-8. Thermal test board meets JEDEC specification for the specified package.
3. Junction-to-case at the top of the package determined using MIL-STD 883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer.
4. Thermal characterization parameter indicating the temperature difference between the board and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JB.
5. Thermal characterization parameter indicating the temperature difference between the case and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JC.

Table 13. Thermal characteristics for 100-pin LQFP

Symbol	Parameter	Conditions	Typical value	Unit
$R_{\theta JA}$	Thermal resistance junction-to-ambient, natural convection(1)	Single layer board—1s	47.3	°C/W
		Four layer board—2s2p	35.3	°C/W
$R_{\theta JB}$	Thermal resistance junction-to-board(2)	Four layer board—2s2p	19.1	°C/W
$R_{\theta JCtop}$	Thermal resistance junction-to-case (top)(3)	Single layer board—1s	9.7	°C/W
Ψ_{JB}	Junction-to-board, natural convection(4)	Operating conditions	19.1	°C/W
Ψ_{JC}	Junction-to-case, natural convection(5)	Operating conditions	0.8	°C/W

1. Junction-to-ambient thermal resistance determined per JEDEC JESD51-7. Thermal test board meets JEDEC specification for this package.
2. Junction-to-board thermal resistance determined per JEDEC JESD51-8. Thermal test board meets JEDEC specification for the specified package.
3. Junction-to-case at the top of the package determined using MIL-STD 883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer.
4. Thermal characterization parameter indicating the temperature difference between the board and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JB.
5. Thermal characterization parameter indicating the temperature difference between the case and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JC.

3.5.2 General notes for specifications at maximum junction temperature

An estimation of the chip junction temperature, T_J, can be obtained from *Equation 1*:

Equation 1 $T_J = T_A + (R_{\theta JA} * P_D)$

where:

T_A = ambient temperature for the package (°C)

$R_{\theta JA}$ = junction to ambient thermal resistance (°C/W)

P_D = power dissipation in the package (W)

The junction to ambient thermal resistance is an industry standard value that provides a quick and easy estimation of thermal performance. Unfortunately, there are two values in

common usage: the value determined on a single layer board and the value obtained on a board with two planes. For packages such as the PBGA, these values can be different by a factor of two. Which value is closer to the application depends on the power dissipated by other components on the board. The value obtained on a single layer board is appropriate for the tightly packed printed circuit board. The value obtained on the board with the internal planes is usually appropriate if the board has low power dissipation and the components are well separated.

When a heat sink is used, the thermal resistance is expressed in *Equation 2* as the sum of a junction to case thermal resistance and a case to ambient thermal resistance:

Equation 2 $R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$

where:

$R_{\theta JA}$ = junction to ambient thermal resistance (°C/W)

$R_{\theta JC}$ = junction to case thermal resistance (°C/W)

$R_{\theta CA}$ = case to ambient thermal resistance (°C/W)

$R_{\theta JC}$ is device related and cannot be influenced by the user. The user controls the thermal environment to change the case to ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the size of the heat sink, the air flow around the device, the interface material, the mounting arrangement on printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the device.

To determine the junction temperature of the device in the application when heat sinks are not used, the Thermal Characterization Parameter (Ψ_{JT}) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using *Equation 3*:

Equation 3 $T_J = T_T + (\Psi_{JT} \times P_D)$

where:

T_T = thermocouple temperature on top of the package (°C)

Ψ_{JT} = thermal characterization parameter (°C/W)

P_D = power dissipation in the package (W)

The thermal characterization parameter is measured per JESD51-2 specification using a 40 gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

References:

Semiconductor Equipment and Materials International

3081 Zanker Road

San Jose, CA 95134 U.S.A.

(408) 943-6900

MIL-SPEC and EIA/JESD (JEDEC) specifications are available from Global Engineering Documents at 800-854-7179 or 303-397-7956.

JEDEC specifications are available on the WEB at http://www.jedec.org.

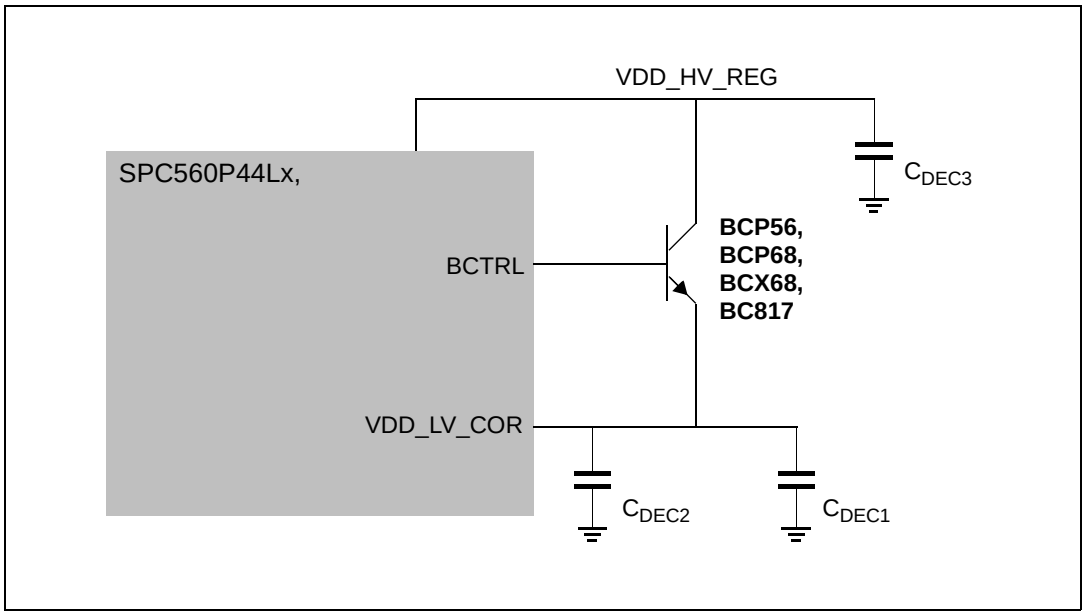


Figure 10. Configuration without resistor on base

Table 18. Voltage regulator electrical characteristics (configuration without resistor on base)

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
$V_{DD\_LV\_REGCOR}$	CC	P	Output voltage under maximum load run supply current configuration	Post-trimming	1.15	—	1.32	V
C_{DEC1}	SR	—	External decoupling/stability ceramic capacitor	4 capacitances	40	56	—	µF
R_{REG}	SR	—	Resulting ESR of all four C_{DEC1}	Absolute maximum value between 100 kHz and 10 MHz	—	—	45	mΩ
C_{DEC2}	SR	—	External decoupling/stability ceramic capacitor	4 capacitances of 100 nF each	400	—	—	nF
C_{DEC3}	SR	—	External decoupling/stability ceramic capacitor on VDD_HV_REG	—	40	—	—	µF
L_{Reg}	SR	—	Resulting ESL of $V_{DD\_HV\_REG}$, BCTRL and $V_{DD\_LV\_CORx}$ pins	—	—	—	15	nH

Table 24. Supply current (3.3 V, NVUSRO[PAD3V5V] = 1)

Symbol	C	Parameter		Conditions		Value		Unit
						Typ	Max	
$I_{DD\_LV\_CORx}$	T	Supply current	RUN—Maximum mode(1)	$V_{DD\_LV\_CORx}$ externally forced at 1.3 V	40 MHz	62	77	mA
					64 MHz	71	89	
			RUN—Typical mode(2)		40 MHz	45	56	
					64 MHz	53	66	
	P		RUN—Maximum mode(3)	$V_{DD\_LV\_CORx}$ externally forced at 1.3 V	64 MHz	60	75	
			HALT mode(4)	$V_{DD\_LV\_CORx}$ externally forced at 1.3 V	—	1.5	10	
			STOP mode(5)	$V_{DD\_LV\_CORx}$ externally forced at 1.3 V	—	1	10	
I_{DD_FLASH}	T		Flash during read on single mode	$V_{DD\_HV\_FL}$ at 3.3 V	—	8	10	
			Flash during erase operation on single mode	$V_{DD\_HV\_FL}$ at 3.3 V	—	10	12	
I_{DD_ADC}	T		ADC—Maximum mode(1)	$V_{DD\_HV\_ADC0}$ at 3.3 V $V_{DD\_HV\_ADC1}$ at 3.3 V f_{ADC} = 16 MHz	ADC_1	2.5	4	
					ADC_0	2	4	
			ADC—Typical mode(2)		ADC_1	0.8	1	
					ADC_0	0.005	0.006	
I_{DD_OSC}	T		Oscillator	V_{DD_OSC} at 3.3 V	8 MHz	2.4	3	

1. Maximum mode: FlexPWM, ADCs, CTU, DSPI, LINFlex, FlexCAN, 15 output pins, 1st and 2nd PLL enabled. I/O supply current excluded.
2. Typical mode: DSPI, LINFlex, FlexCAN, 15 output pins, 1st PLL only. I/O supply current excluded.
3. Code fetched from RAM, PLL_0: 64 MHz system clock (x4 multiplier with 16 MHz XTAL), PLL_1 is ON at PHI_div2 = 120 MHz and PHI_div3 = 80 MHz, auxiliary clock sources set that all peripherals receive maximum frequency, all peripherals enabled.
4. Halt mode configurations: code fetched from RAM, code and data flash memories in low power mode, OSC/PLL_0/PLL_1 are OFF, core clock frozen, all peripherals are disabled.
5. STOP “P” mode Device Under Test (DUT) configuration: code fetched from RAM, code and data flash memories OFF, OSC/PLL_0/PLL_1 are OFF, core clock frozen, all peripherals are disabled.

3.10.4 Input DC electrical characteristics definition

Figure 14 shows the DC electrical characteristics behavior as function of time.

Table 26. I/O weight (continued)

Pad	LQFP144		LQFP100	
	Weight 5V	Weight 3.3V	Weight 5V	Weight 3.3V
PAD[27]	1%	1%	1%	1%
PAD[28]	1%	1%	1%	1%
PAD[63]	1%	1%	1%	1%
PAD[72]	1%	1%	—	—
PAD[29]	1%	1%	1%	1%
PAD[73]	1%	1%	—	—
PAD[31]	1%	1%	1%	1%
PAD[74]	1%	1%	—	—
PAD[30]	1%	1%	1%	1%
PAD[75]	1%	1%	—	—
PAD[32]	1%	1%	1%	1%
PAD[76]	1%	1%	—	—
PAD[64]	1%	1%	1%	1%
PAD[0]	23%	20%	23%	20%
PAD[1]	21%	18%	21%	18%
PAD[107]	20%	17%	—	—
PAD[58]	19%	16%	19%	16%
PAD[106]	18%	16%	—	—
PAD[59]	17%	15%	17%	15%
PAD[105]	16%	14%	—	—
PAD[43]	15%	13%	15%	13%
PAD[104]	14%	13%	—	—
PAD[44]	13%	12%	13%	12%
PAD[103]	12%	11%	—	—
PAD[2]	11%	10%	11%	10%
PAD[101]	11%	9%	—	—
PAD[21]	10%	8%	10%	8%
TMS	1%	1%	1%	1%
TCK	1%	1%	1%	1%
PAD[20]	16%	11%	16%	11%
PAD[3]	4%	3%	4%	3%
PAD[61]	9%	8%	9%	8%
PAD[102]	11%	10%	—	—

Equation 7

$$V_{A1} \bullet (C_S + C_{P1} + C_{P2}) = V_A \bullet (C_{P1} + C_{P2})$$

- A second charge transfer involves also C_F (that is typically bigger than the on-chip capacitance) through the resistance R_L: again considering the worst case in which C_{P2} and C_S were in parallel to C_{P1} (since the time constant in reality would be faster), the time constant is:

Equation 8

$$\tau_2 < R_L \bullet (C_S + C_{P1} + C_{P2})$$

In this case, the time constant depends on the external circuit: in particular imposing that the transient is completed well before the end of sampling time T_S, a constraints on R_L sizing is obtained:

Equation 9

$$8.5 \bullet \tau_2 = 8.5 \bullet R_L \bullet (C_S + C_{P1} + C_{P2}) < T_S$$

Of course, R_L shall be sized also according to the current limitation constraints, in combination with R_S (source impedance) and R_F (filter resistance). Being C_F definitively bigger than C_{P1}, C_{P2} and C_S, then the final voltage V_{A2} (at the end of the charge transfer transient) will be much higher than V_{A1}. *Equation 10* must be respected (charge balance assuming now C_S already charged at V_{A1}):

Equation 10

$$V_{A2} \bullet (C_S + C_{P1} + C_{P2} + C_F) = V_A \bullet C_F + V_{A1} \bullet (C_{P1} + C_{P2} + C_S)$$

The two transients above are not influenced by the voltage source that, due to the presence of the $R_F C_F$ filter, is not able to provide the extra charge to compensate the voltage drop on C_S with respect to the ideal source V_A; the time constant $R_F C_F$ of the filter is very high with respect to the sampling time (T_S). The filter is typically designed to act as anti-aliasing.

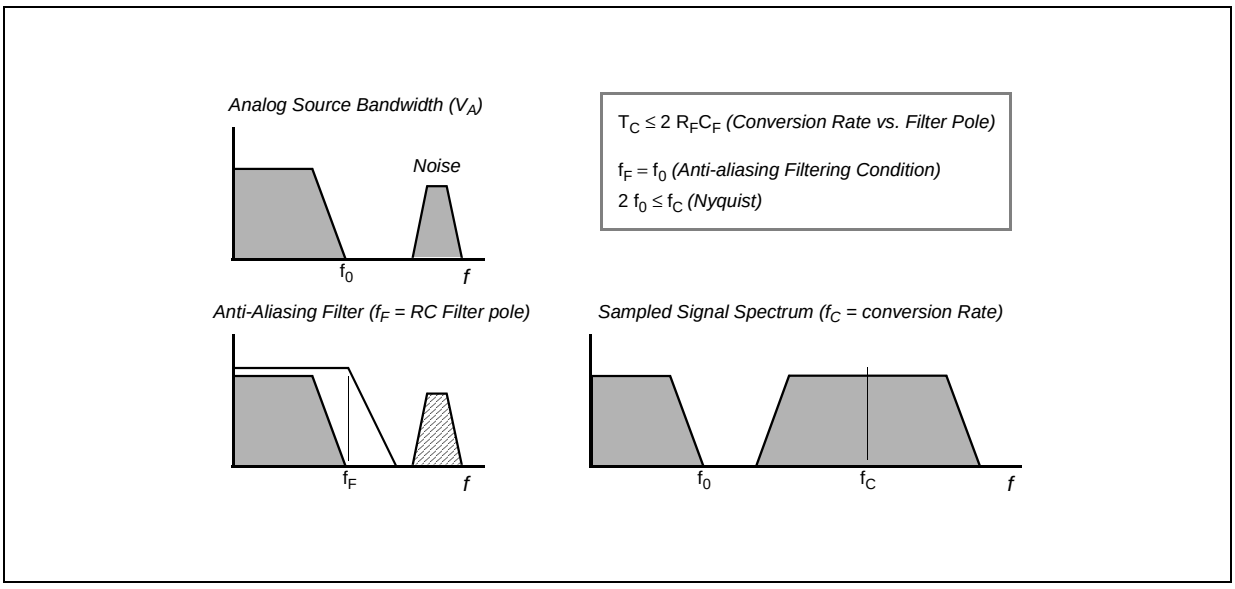


Figure 18. Spectral representation of input signal

Table 46. Revision history (continued)

Date	Revision	Changes
27-Oct-2009	5	- Added “Full Feature“ and “Airbag“ customization. - Removed B[4] and B[5] rows from “Pin muxing” table and inserted them on “System pins” table. - Updated package pinout. - Rewrote entirely section “Power Up/dpwn Sequencing“ section. - Renamend “$V_{DD\_LV\_PLL}$“ and “$V_{SS\_LV\_PLL}$“ supply pins with respectively “$V_{DD\_LV\_COR3}$“ and “$V_{SS\_LV\_COR3}$”. - Added explicative figures on “Electrical characteristics” section. - Updated “Thermal characteristics“ for 100-pin. - Proposed two different configuration of “voltage regulator. - Inserted Power Up/Down sequence. - Added explicative figures on “DC Electrical characteristics”. - Added “I/O pad current specification” section. - Renamed the “Airbag mode” with “Typical mode“and updated the values on “supply current” tables. - Added more order code.
06-Apr-2010	6	Inserted label of Y-axis in the “Independent ADC supply“ figure. “Recommended Operating Conditions” tables: Moved the T_J row to “Absolute Maximum Ratings“ table. Rewrite note 1 and 3 Inverted Min a Typ value of C_{DEC2} on ”Voltage Regulator Electrical Characteristics” table. Removed an useless duplicate of “Voltage Regulator Electrical Characteristics“ table. Inserted the name of C_S into “Input Equivalent Circuit“ figure. Removed leakage Ivpp from datasheet. Updated “Supply Current” tables. Added note on “Output pin transition times“ table. Updated ”Temperature Sensor Electrical Characteristics” table. Updated “16 MHz RC Oscillator Electrical Characteristics” table. Removed the note about the condition from “Flash read access timing“ table. Removed the notes that assert the values need to be confirmed before validation.
07-Apr-2011	7	Formatting and editorial changes throughout Removed all content referencing Junction Temperature Sensor Cover page Features: – CPU core—specified 64 MHz frequency – updated memory features – eTimer units: changed “up/down capabilities” to “up/down count capabilities” – ADC—changed “2 × 13 input channels” to “2 × 11 input channels, + 4 shared channels” – replaced “On-chip CAN/UART/FlexRay bootstrap loader” with “On-chip CAN/UART bootstrap loader” *Section 1: Introduction*: changed title (was: Overview); reorganized contents SPC560P44Lx, SPC560P50Lx device comparison: – ADC feature: changed “16 channels” to “15-channel”; added footnote to to indicate that four channels are shared between the two ADCs – removed SPC560P40 column – changed “dual channel” to “selectable single or dual channel support” in FlexRay footnote – updated “eTimer” feature – updated footnote relative to “Digital power supply” feature

Table 46. Revision history (continued)

Date	Revision	Changes
07-Apr-2011	7 (cont'd)	SPC560P44Lx, SPC560P50Lx device configuration differences: Removed "temperature" row (temperature information is provided in Order codes) Updated SPC560P44Lx, SPC560P50Lx block diagram Added SPC560P44Lx, SPC560P50Lx series block summary Added *Section 1.5 Feature details* *Section 2.1, Package pinouts*: removed alternate functions from pinout diagrams Supply pins: updated descriptions of power supply pins (1.2 V) System pins: updated table Pin muxing: added rows "B[4]" and "B[5] *Section 3.3, Absolute maximum ratings*: added voltage specifications to titles of *Figure 5* and *Figure 6*; in *Table 9*, changed row "V_{SS_HV} / Digital Ground" to "V_{SS} / Device Ground"; updated symbols *Section 3.4, Recommended operating conditions*: added voltage specifications to titles of *Figure 7* and *Figure 8* Recommended operating conditions (5.0 V), and Recommended operating conditions (3.3 V): changed row "V_{SS_HV} / Digital Ground" to "V_{SS} / Device Ground"; updated symbols Updated *Section 3.5.1, Package thermal characteristics* Updated *Section 3.6, Electromagnetic interference (EMI) characteristics* *Section 3.8.1, Voltage regulator electrical characteristics*: amended titles of *Table 16* and *Table 19* Voltage regulator electrical characteristics (configuration without resistor on base) and Voltage regulator electrical characteristics (configuration with resistor on base): updated symbol and values for $V_{DD\_LV\_REGCOR}$ Low voltage monitor electrical characteristics: Updated $V_{MLVDDOK\_H}$ max value—was 1.15 V; is 1.145 V *Section 3.10, DC electrical characteristics*: reorganized contents Updated *Section 3.10.1, NVUSRO register* (includes adding *Section NVUSRO[OSCILLATOR_MARGIN] field description*) Supply current (5.0 V, NVUSRO[PAD3V5V] = 0): updated symbols Corrected parameter descriptions in DC electrical characteristics (3.3 V, NVUSRO[PAD3V5V] = 1): – V_{OL_F}—was "Fast, high level output voltage"; is "Fast, low level output voltage" – V_{OL_SYM}—was "Symmetric, high level output voltage"; is "Symmetric, low level output voltage" Supply current (3.3 V, NVUSRO[PAD3V5V] = 1): updated symbols Main oscillator output electrical characteristics (5.0 V, NVUSRO[PAD3V5V] = 0): replaced instances of EXTAL with XTAL Main oscillator output electrical characteristics (3.3 V, NVUSRO[PAD3V5V] = 1): replaced instances of EXTAL with XTAL FMPLL electrical characteristics: replaced "PLLMRFM" with "FMPLL" in table title; updated conditions; removed f_{sys} row; updated $f_{FMPLLOUT}$ min value ADC conversion characteristics: updated symbols; added row t_{ADC_PU} Flash memory read access timing: added footnote to "Conditions" column *Section 3.16.1, Pad AC specifications*: added Pad output delay diagram In the range of figures "DSPI Classic SPI Timing — Master, CPHA = 0" to "DSPI PCS Strobe (PCSS) Timing": added note Updated Order codes Updated "Commercial product code structure" figure *Table 45*: Added abbreviations "DUT", "NPN", and "RBW"

Table 46. Revision history (continued)

Date	Revision	Changes
18-Jul-2012	8	Updated *Table 1 (Device summary)* *Section 1.5.4, Flash memory*: Changed “Data flash memory: 32-bit ECC” to “Data flash memory: 64-bit ECC” *Figure 40 (Commercial product code structure)*, replaced "C = 60 MHz, 5 V" and "D = 60 MHz, 3.3 V" with respectively "C = 40 MHz, 5 V" and "D = 40 MHz, 3.3 V" *Table 9 (Absolute maximum ratings)*, updated TV_{DD} parameter, the minimum value to 3.0 V/s and the maximum value to 0.5 V/µs *Table 7 (Pin muxing)*, changed the description in the column "I/O direction" from "I/O" to "O" for the following port pins: A[10] with function B[0] A[11] with function A[0] A[11] with function A[2] A[12] with function A[2] A[12] with function B[2] A[13] with function B[2] C[7] with function A[1] C[10] with function A[3] C[15] with function A[1] D[0] with function B[1] D[10] with function A[0] D[11] with function B[0] D[13] with function A[1] D[14] with function B[1] Updated *Section 3.8.1, Voltage regulator electrical characteristics* Added *Table 27 (I/O consumption)* *Section 3.10, DC electrical characteristics*: deleted references to “oscillator margin” deleted subsection “NVUSRO[OSCILLATOR_MARGIN] field description” *Table 21 (DC electrical characteristics (5.0 V, NVUSRO[PAD3V5V] = 0))*, added IPU row for $\overline{\text{RESET}}$ pin *Table 23 (DC electrical characteristics (3.3 V, NVUSRO[PAD3V5V] = 1))*, added IPU row for $\overline{\text{RESET}}$ pin *Table 33 (ADC conversion characteristics)*, added V_{INAN} entry Removed “Order codes” table *Figure 40 (Commercial product code structure)*: added a footnote updated “E = Data flash memory”
18-Sep-2013	9	Updated Disclaimer