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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z0h
Core Size	32-Bit Single-Core
Speed	64MHz
Connectivity	CANbus, LINbus, SPI, UART/USART
Peripherals	DMA, POR, PWM, WDT
Number of I/O	67
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	40K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 26x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/spc560p50l3cefbr

Table 4. SPC560P44Lx, SPC560P50Lx series block summary (continued)

Block	Function
Pulse width modulator (FlexPWM)	Contains four PWM submodules, each of which is capable of controlling a single half-bridge power stage and two fault input channels
Reset generation module (MC_RGM)	Centralizes reset sources and manages the device reset sequence of the device
Static random-access memory (SRAM)	Provides storage for program code, constants, and variables
System integration unit lite (SIUL)	Provides control over all the electrical pad controls and up 32 ports with 16 bits of bidirectional, general-purpose input and output signals and supports up to 32 external interrupts with trigger event configuration
System status and configuration module (SSCM)	Provides system configuration and status data (such as memory size and status, device mode and security status), device identification data, debug status port enable and selection, and bus and peripheral abort enable/disable
System timer module (STM)	Provides a set of output compare events to support AUTOSAR(1) and operating system tasks
System watchdog timer (SWT)	Provides protection from runaway code
Wakeup unit (WKPU)	Supports up to 18 external sources that can generate interrupts or wakeup events, 1 of which can cause non-maskable interrupt requests or wakeup events

1. AUTOSAR: AUTomotive Open System ARchitecture (see www.autosar.org)

For high priority interrupt requests, the time from the assertion of the interrupt request from the peripheral to when the processor is executing the interrupt service routine (ISR) has been minimized. The INTC provides a unique vector for each interrupt request source for quick determination of which ISR has to be executed. It also provides a wide number of priorities so that lower priority ISRs do not delay the execution of higher priority ISRs. To allow the appropriate priorities for each source of interrupt request, the priority of each interrupt request is software configurable.

When multiple tasks share a resource, coherent accesses to that resource need to be supported. The INTC supports the priority ceiling protocol (PCP) for coherent accesses. By providing a modifiable priority mask, the priority can be raised temporarily so that all tasks which share the same resource can not preempt each other.

The INTC provides the following features:

- Unique 9-bit vector for each separate interrupt source
- 8 software triggerable interrupt sources
- 16 priority levels with fixed hardware arbitration within priority levels for each interrupt source
- Ability to modify the ISR or task priority: modifying the priority can be used to implement the Priority Ceiling Protocol for accessing shared resources.
- 2 external high priority interrupts directly accessing the main core and I/O processor (IOP) critical interrupt mechanism

1.5.7 System status and configuration module (SSCM)

The system status and configuration module (SSCM) provides central device functionality.

The SSCM includes these features:

- System configuration and status
  - Memory sizes/status
  - Device mode and security status
  - Determine boot vector
  - Search code flash for bootable sector
  - DMA status
- Debug status port enable and selection
- Bus and peripheral abort enable/disable

1.5.8 System clocks and clock generation

The following list summarizes the system clock and clock generation on the SPC560P44Lx, SPC560P50Lx:

- Lock detect circuitry continuously monitors lock status
- Loss of clock (LOC) detection for PLL outputs
- Programmable output clock divider (÷1, ÷2, ÷4, ÷8)
- FlexPWM module and eTimer module can run on an independent clock source
- On-chip oscillator with automatic level control
- Internal 16 MHz RC oscillator for rapid start-up and safe mode: supports frequency trimming by user application

The FlexPWM block implements the following features:

- 16-bit resolution for center, edge-aligned, and asymmetrical PWMs
- Maximum operating clock frequency of 120 MHz
- PWM outputs can operate as complementary pairs or independent channels
- Can accept signed numbers for PWM generation
- Independent control of both edges of each PWM output
- Synchronization to external hardware or other PWM supported
- Double buffered PWM registers
  - Integral reload rates from 1 to 16
  - Half cycle reload capability
- Multiple ADC trigger events can be generated per PWM cycle via hardware
- Write protection for critical registers
- Fault inputs can be assigned to control multiple PWM outputs
- Programmable filters for fault inputs
- Independently programmable PWM output polarity
- Independent top and bottom deadtime insertion
- Each complementary pair can operate with its own PWM frequency and deadtime values
- Individual software-control for each PWM output
- All outputs can be programmed to change simultaneously via a “Force Out” event
- PWMX pin can optionally output a third PWM signal from each submodule
- Channels not used for PWM generation can be used for buffered output compare functions
- Channels not used for PWM generation can be used for input capture functions
- Enhanced dual-edge capture functionality
- eDMA support with automatic reload
- 2 fault inputs
- Capture capability for PWMA, PWMB, and PWMX channels not supported

Digital part:

- 2 × 13 input channels including 4 channels shared between the 2 converters
- 4 analog watchdogs comparing ADC results against predefined levels (low, high, range) before results are stored in the appropriate ADC result location,
- 2 modes of operation: Normal mode or CTU control mode
- Normal mode features
  - Register-based interface with the CPU: control register, status register, 1 result register per channel
  - ADC state machine managing 3 request flows: regular command, hardware injected command, software injected command
  - Selectable priority between software and hardware injected commands
  - 4 analog watchdogs comparing ADC results against predefined levels (low, high, range)
  - DMA compatible interface
- CTU control mode features
  - Triggered mode only
  - 4 independent result queues (2 × 16 entries, 2 × 4 entries)
  - Result alignment circuitry (left justified; right justified)
  - 32-bit read mode allows to have channel ID on one of the 16-bit part
  - DMA compatible interfaces

1.5.28 Cross triggering unit (CTU)

The cross triggering unit allows automatic generation of ADC conversion requests on user selected conditions without CPU load during the PWM period and with minimized CPU load for dynamic configuration.

It implements the following features:

- Double buffered trigger generation unit with as many as eight independent triggers generated from external triggers
- Trigger generation unit configurable in sequential mode or in triggered mode
- Each Trigger can be appropriately delayed to compensate the delay of external low pass filter
- Double buffered global trigger unit allowing eTimer synchronization and/or ADC command generation
- Double buffered ADC command list pointers to minimize ADC-trigger unit update
- Double buffered ADC conversion command list with as many as 24 ADC commands
- Each trigger has the capability to generate consecutive commands
- ADC conversion command allows to control ADC channel from each ADC, single or synchronous sampling, independent result queue selection

1.5.29 Nexus development interface (NDI)

The NDI (Nexus Development Interface) block provides real-time development support capabilities for the SPC560P44Lx, SPC560P50Lx Power Architecture based MCU in compliance with the IEEE-ISTO 5001-2003 standard. This development support is supplied for MCUs without requiring external address and data pins for internal visibility. The NDI

Table 5. Supply pins

Supply		Pin	
Symbol	**Description**	**100-pin**	**144-pin**
VREG control and power supply pins. Pins available on 100-pin and 144-pin package.			
BCTRL	Voltage regulator external NPN ballast base control pin	47	69
$V_{DD\_HV\_REG}$ (3.3 V or 5.0 V)	Voltage regulator supply voltage	50	72
$V_{DD\_LV\_REGCOR}$	1.2 V decoupling pins for core logic and regulator feedback. Decoupling capacitor must be connected between this pins and $V_{SS\_LV\_REGCOR}$.	48	70
$V_{SS\_LV\_REGCOR}$	1.2 V decoupling pins for core logic and regulator feedback. Decoupling capacitor must be connected between this pins and $V_{DD\_LV\_REGCOR}$.	49	71
ADC_0/ADC_1 reference and supply voltage. Pins available on 100-pin and 144-pin package.			
$V_{DD\_HV\_ADC0}$ (1)	ADC_0 supply and high reference voltage	33	50
$V_{SS\_HV\_ADC0}$	ADC_0 ground and low reference voltage	34	51
$V_{DD\_HV\_ADC1}$	ADC_1 supply and high reference voltage	39	56
$V_{SS\_HV\_ADC1}$	ADC_1 ground and low reference voltage	40	57
Power supply pins (3.3 V or 5.0 V). All pins available on 144-pin package. Five pairs (V_{DD}; V_{SS}) available on 100-pin package.			
$V_{DD\_HV\_IO0}$ (2)	Input/Output supply voltage	—	6
$V_{SS\_HV\_IO0}$ (2)	Input/Output ground	—	7
$V_{DD\_HV\_IO1}$	Input/Output supply voltage	13	21
$V_{SS\_HV\_IO1}$	Input/Output ground	14	22
$V_{DD\_HV\_IO2}$	Input/Output supply voltage	63	91
$V_{SS\_HV\_IO2}$	Input/Output ground	62	90
$V_{DD\_HV\_IO3}$	Input/Output supply voltage	87	126
$V_{SS\_HV\_IO3}$	Input/Output ground	88	127
$V_{DD\_HV\_FL}$	Code and data flash supply voltage	69	97
$V_{SS\_HV\_FL}$	Code and data flash supply ground	68	96
$V_{DD\_HV\_OSC}$	Crystal oscillator amplifier supply voltage	16	27
$V_{SS\_HV\_OSC}$	Crystal oscillator amplifier ground	17	28
Power supply pins (1.2 V). All pins available on 100-pin and 144-pin package.			
$V_{DD\_LV\_COR0}$	1.2 V Decoupling pins for core logic. Decoupling capacitor must be connected between these pins and the nearest $V_{SS\_LV\_COR}$ pin.	12	18
$V_{SS\_LV\_COR0}$	1.2 V Decoupling pins for core logic. Decoupling capacitor must be connected between these pins and the nearest $V_{DD\_LV\_COR}$ pin.	11	17

Table 6. System pins (continued)

Symbol	Description	Direction	Pad speed(1)		Pin	
			SRC = 0	SRC = 1	100-pin	144-pin
TMS	JTAG state machine control	Bidirectional	Slow	Fast	59	87
TCK	JTAG clock	Input only	Slow	—	60	88
TDI	Test Data In	Input only	Slow	Medium	58	86
TDO	Test Data Out	Output only	Slow	Fast	61	89
Reset pin, available on 100-pin and 144-pin package.						
$\overline{\text{RESET}}$	Bidirectional reset with Schmitt trigger characteristics and noise filter	Bidirectional	Medium	—	20	31
Test pin, available on 100-pin and 144-pin package.						
VPP_TEST	Pin for testing purpose only. To be tied to ground in normal operating mode.	—	—	—	74	107

1. SCR values refer to the value assigned to the Slew Rate Control bits of the pad configuration register.

2.2.3 Pin muxing

Table 7 defines the pin list and muxing for the SPC560P44Lx, SPC560P50Lx devices.

Each row of *Table 7* shows all the possible ways of configuring each pin, via alternate functions. The default function assigned to each pin after reset is the ALT0 function.

SPC560P44Lx, SPC560P50Lx devices provide four main I/O pad types, depending on the associated functions:

- *Slow pads* are the most common, providing a compromise between transition time and low electromagnetic emission.
- *Medium pads* provide fast enough transition for serial communication channels with controlled current to reduce electromagnetic emission.
- *Fast pads* provide maximum speed. They are used for improved NEXUS debugging capability.
- *Symmetric pads* are designed to meet FlexRay requirements.

Medium and Fast pads can use slow configuration to reduce electromagnetic emission, at the cost of reducing AC performance. For more information, see the datasheet's "Pad AC Specifications" section.

Table 7. Pin muxing (continued)

Port pin	Pad configuration register (PCR)	Alternate function[1],[2]	Functions	Peripheral[3]	I/O direction[4]	Pad speed[5]		Pin No.	
						SRC = 0	SRC = 1	100-pin	144-pin
B[7]	PCR[23]	ALT0 ALT1 ALT2 ALT3 — —	GPIO[23] — — — AN[0] RXD	SIUL — — — ADC_0 LIN_0	Input only	—	—	29	43
B[8]	PCR[24]	ALT0 ALT1 ALT2 ALT3 — —	GPIO[24] — — — AN[1] ETC[5]	SIUL — — — ADC_0 eTimer_0	Input only	—	—	31	47
B[9]	PCR[25]	ALT0 ALT1 ALT2 ALT3 —	GPIO[25] — — — AN[11]	SIUL — — — ADC_0 / ADC_1	Input only	—	—	35	52
B[10]	PCR[26]	ALT0 ALT1 ALT2 ALT3 —	GPIO[26] — — — AN[12]	SIUL — — — ADC_0 / ADC_1	Input only	—	—	36	53
B[11]	PCR[27]	ALT0 ALT1 ALT2 ALT3 —	GPIO[27] — — — AN[13]	SIUL — — — ADC_0 / ADC_1	Input only	—	—	37	54
B[12]	PCR[28]	ALT0 ALT1 ALT2 ALT3 —	GPIO[28] — — — AN[14]	SIUL — — — ADC_0 / ADC_1	Input only	—	—	38	55
B[13]	PCR[29]	ALT0 ALT1 ALT2 ALT3 — —	GPIO[29] — — — AN[0] RXD	SIUL — — — ADC_1 LIN_1	Input only	—	—	42	60

Table 7. Pin muxing (continued)

Port pin	Pad configuration register (PCR)	Alternate function[1], [2]	Functions	Peripheral[3]	I/O direction [4]	Pad speed[5]		Pin No.	
						SRC = 0	SRC = 1	100-pin	144-pin
E[5]	PCR[69]	ALT0 ALT1 ALT2 ALT3 —	GPIO[69] — — — AN[8]	SIUL — — — ADC_0	Input only	—	—	—	44
E[6]	PCR[70]	ALT0 ALT1 ALT2 ALT3 —	GPIO[70] — — — AN[9]	SIUL — — — ADC_0	Input only	—	—	—	46
E[7]	PCR[71]	ALT0 ALT1 ALT2 ALT3 —	GPIO[71] — — — AN[10]	SIUL — — — ADC_0	Input only	—	—	—	48
E[8]	PCR[72]	ALT0 ALT1 ALT2 ALT3 —	GPIO[72] — — — AN[6]	SIUL — — — ADC_1	Input only	—	—	—	59
E[9]	PCR[73]	ALT0 ALT1 ALT2 ALT3 —	GPIO[73] — — — AN[7]	SIUL — — — ADC_1	Input only	—	—	—	61
E[10]	PCR[74]	ALT0 ALT1 ALT2 ALT3 —	GPIO[74] — — — AN[8]	SIUL — — — ADC_1	Input only	—	—	—	63
E[11]	PCR[75]	ALT0 ALT1 ALT2 ALT3 —	GPIO[75] — — — AN[9]	SIUL — — — ADC_1	Input only	—	—	—	65
E[12]	PCR[76]	ALT0 ALT1 ALT2 ALT3 —	GPIO[76] — — — AN[10]	SIUL — — — ADC_1	Input only	—	—	—	67

Table 7. Pin muxing (continued)

Port pin	Pad configuration register (PCR)	Alternate function[1],[2]	Functions	Peripheral[3]	I/O direction[4]	Pad speed[5]		Pin No.	
						SRC = 0	SRC = 1	100-pin	144-pin
E[13]	PCR[77]	ALT0 ALT1 ALT2 ALT3 —	GPIO[77] SCK — — EIRQ[25]	SIUL DSPI_3 — — SIUL	I/O I/O — — I	Slow	Medium	—	117
E[14]	PCR[78]	ALT0 ALT1 ALT2 ALT3 —	GPIO[78] SOUT — — EIRQ[26]	SIUL DSPI_3 — — SIUL	I/O O — — I	Slow	Medium	—	119
E[15]	PCR[79]	ALT0 ALT1 ALT2 ALT3 — —	GPIO[79] — — — SIN EIRQ[27]	SIUL — — — DSPI_3 SIUL	I/O — — — I I	Slow	Medium	—	121
Port F (16-bit)									
F[0]	PCR[80]	ALT0 ALT1 ALT2 ALT3 —	GPIO[80] DBG0 CS3 — EIRQ[28]	SIUL FlexRay_0 DSPI_3 — SIUL	I/O O O — I	Slow	Medium	—	133
F[1]	PCR[81]	ALT0 ALT1 ALT2 ALT3 —	GPIO[81] DBG1 CS2 — EIRQ[29]	SIUL FlexRay_0 DSPI_3 — SIUL	I/O O O — I	Slow	Medium	—	135
F[2]	PCR[82]	ALT0 ALT1 ALT2 ALT3	GPIO[82] DBG2 CS1 —	SIUL FlexRay_0 DSPI_3 —	I/O O O —	Slow	Medium	—	137
F[3]	PCR[83]	ALT0 ALT1 ALT2 ALT3	GPIO[83] DBG3 CS0 —	SIUL FlexRay_0 DSPI_3 —	I/O O I/O —	Slow	Medium	—	139
F[4]	PCR[84]	ALT0 ALT1 ALT2 ALT3	GPIO[84] MDO[3] — —	SIUL NEXUS_0 — —	I/O O — —	Slow	Fast	—	4

Table 7. Pin muxing (continued)

Port pin	Pad configuration register (PCR)	Alternate function[1],[2]	Functions	Peripheral[3]	I/O direction[4]	Pad speed[5]		Pin No.	
						SRC = 0	SRC = 1	100-pin	144-pin
G[7]	PCR[103]	ALT0 ALT1 ALT2 ALT3	GPIO[103] B[3] — —	SIUL FlexPWM_0 — —	I/O O — —	Slow	Medium	—	83
G[8]	PCR[104]	ALT0 ALT1 ALT2 ALT3 —	GPIO[104] — — — FAULT[0]	SIUL — — — FlexPWM_0	I/O — — — I	Slow	Medium	—	81
G[9]	PCR[105]	ALT0 ALT1 ALT2 ALT3 —	GPIO[105] — — — FAULT[1]	SIUL — — — FlexPWM_0	I/O — — — I	Slow	Medium	—	79
G[10]	PCR[106]	ALT0 ALT1 ALT2 ALT3 —	GPIO[106] — — — FAULT[2]	SIUL — — — FlexPWM_0	I/O — — — I	Slow	Medium	—	77
G[11]	PCR[107]	ALT0 ALT1 ALT2 ALT3 —	GPIO[107] — — — FAULT[3]	SIUL — — — FlexPWM_0	I/O — — — I	Slow	Medium	—	75

1. ALT0 is the primary (default) function for each port after reset.
2. Alternate functions are chosen by setting the values of the PCR[PA] bitfields inside the SIU module. PCR[PA] = 00 → ALT0; PCR[PA] = 01 → ALT1; PCR[PA] = 10 → ALT2; PCR[PA] = 11 → ALT3. This is intended to select the output functions; to use one of the input-only functions, the PCR[IBE] bit must be written to '1', regardless of the values selected in the PCR[PA] bitfields. For this reason, the value corresponding to an input only function is reported as "—".
3. Module included on the MCU.
4. Multiple inputs are routed to all respective modules internally. The input of some modules must be configured by setting the values of the PSMI[PADSEL*x*] bitfields inside the SIUL module.
5. Programmable via the SRC (Slew Rate Control) bits in the respective Pad Configuration Register.
6. Weak pull down during reset.

3.4 Recommended operating conditions

Table 10. Recommended operating conditions (5.0 V)

Symbol		Parameter	Conditions	Value		Unit
				Min	Max(1)	
V_{SS}	SR	Device ground	—	0	0	V
$V_{DD\_HV\_IOx}$(2)	SR	5.0 V input/output supply voltage	—	4.5	5.5	V
$V_{SS\_HV\_IOx}$	SR	Input/output ground voltage	—	0	0	V
$V_{DD\_HV\_FL}$	SR	5.0 V code and data flash supply voltage	—	4.5	5.5	V
			Relative to $V_{DD\_HV\_IOx}$	$V_{DD\_HV\_IOx}$ – 0.1	$V_{DD\_HV\_IOx}$ + 0.1	
$V_{SS\_HV\_FL}$	SR	Code and data flash ground	—	0	0	V
$V_{DD\_HV\_OSC}$	SR	5.0 V crystal oscillator amplifier supply voltage	—	4.5	5.5	V
			Relative to $V_{DD\_HV\_IOx}$	$V_{DD\_HV\_IOx}$ – 0.1	$V_{DD\_HV\_IOx}$ + 0.1	
$V_{SS\_HV\_OSC}$	SR	5.0 V crystal oscillator amplifier reference voltage	—	0	0	V
$V_{DD\_HV\_REG}$	SR	5.0 V voltage regulator supply voltage	—	4.5	5.5	V
			Relative to $V_{DD\_HV\_IOx}$	$V_{DD\_HV\_IOx}$ – 0.1	$V_{DD\_HV\_IOx}$ + 0.1	
$V_{DD\_HV\_ADC0}$(3)	SR	5.0 V ADC_0 supply and high reference voltage	—	4.5	5.5	V
			Relative to $V_{DD\_HV\_REG}$	$V_{DD\_HV\_REG}$ – 0.1	—	
$V_{SS\_HV\_ADC0}$	SR	ADC_0 ground and low reference voltage	—	0	0	V
$V_{DD\_HV\_ADC1}$(3)	SR	5.0 V ADC_1 supply and high reference voltage	—	4.5	5.5	V
			Relative to $V_{DD\_HV\_REG}$	$V_{DD\_HV\_REG}$ – 0.1	—	
$V_{SS\_HV\_ADC1}$	SR	ADC_1 ground and low reference voltage	—	0	0	V
$V_{DD\_LV\_REGCOR}$(4),(5)	CC	Internal supply voltage	—	—	—	V
$V_{SS\_LV\_REGCOR}$(4)	SR	Internal reference voltage	—	0	0	V
$V_{DD\_LV\_CORx}$(4),(5)	CC	Internal supply voltage	—	—	—	V
$V_{SS\_LV\_CORx}$(4)	SR	Internal reference voltage	—	0	0	V
T_A	SR	Ambient temperature under bias	f_{CPU} = 64 MHz	–40	105	°C
			f_{CPU} = 60 MHz	–40	125	

1. Parametric figures can be out of specification when voltage drops below 4.5 V, however, guaranteeing the full functionality. In particular, ADC electrical characteristics and I/Os DC electrical specification may not be guaranteed.
2. The difference between each couple of voltage supplies must be less than 100 mV, $|V_{DD\_HV\_IOy} - V_{DD\_HV\_IOx}| < 100$ mV.

The SPC560P44Lx, SPC560P50Lx supply architecture allows the ADC supply to be managed independently from the standard V_{DD_HV} supply. *Figure 8* shows the constraints of the ADC power supply.

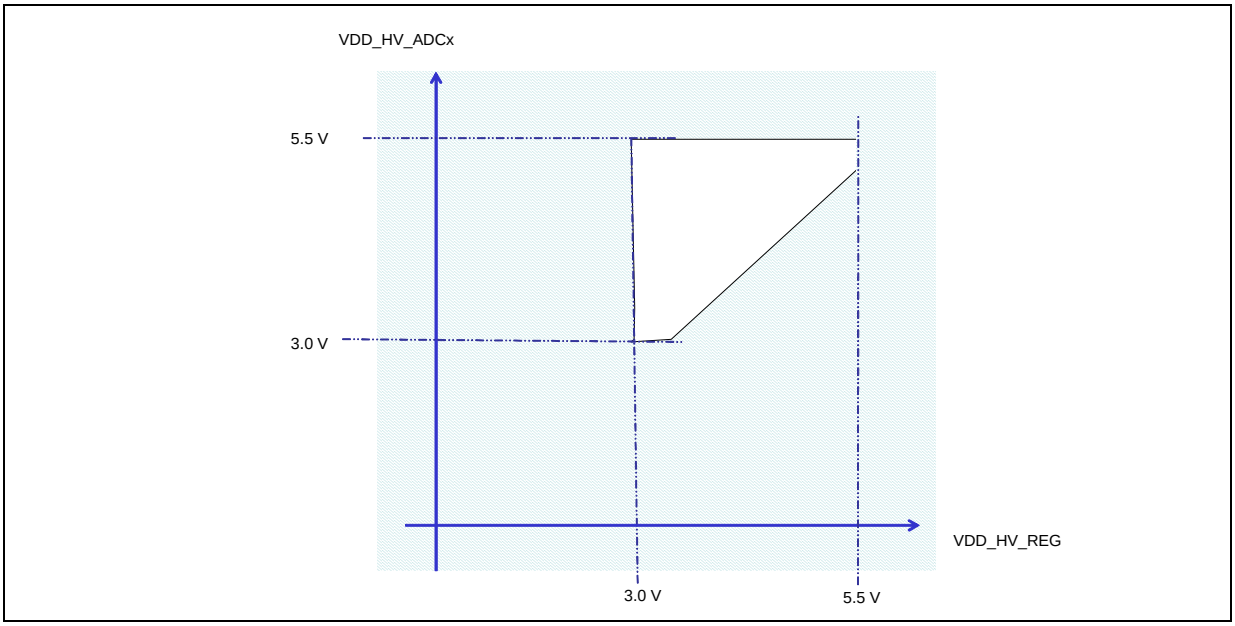


Figure 8. Independent ADC supply (3.0 V ≤ $V_{DD\_HV\_REG}$ ≤ 5.5 V)

3.5 Thermal characteristics

3.5.1 Package thermal characteristics

Table 12. Thermal characteristics for 144-pin LQFP

Symbol	Parameter	Conditions	Typical value	Unit
$R_{\theta JA}$	Thermal resistance junction-to-ambient, natural convection(1)	Single layer board—1s	54.2	°C/W
		Four layer board—2s2p	44.4	°C/W
$R_{\theta JB}$	Thermal resistance junction-to-board(2)	Four layer board—2s2p	29.9	°C/W
$R_{\theta JCtop}$	Thermal resistance junction-to-case (top)(3)	Single layer board—1s	9.3	°C/W
Ψ_{JB}	Junction-to-board, natural convection(4)	Operating conditions	30.2	°C/W
Ψ_{JC}	Junction-to-case, natural convection(5)	Operating conditions	0.8	°C/W

1. Junction-to-ambient thermal resistance determined per JEDEC JESD51-7. Thermal test board meets JEDEC specification for this package.

common usage: the value determined on a single layer board and the value obtained on a board with two planes. For packages such as the PBGA, these values can be different by a factor of two. Which value is closer to the application depends on the power dissipated by other components on the board. The value obtained on a single layer board is appropriate for the tightly packed printed circuit board. The value obtained on the board with the internal planes is usually appropriate if the board has low power dissipation and the components are well separated.

When a heat sink is used, the thermal resistance is expressed in *Equation 2* as the sum of a junction to case thermal resistance and a case to ambient thermal resistance:

Equation 2 $R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$

where:

$R_{\theta JA}$ = junction to ambient thermal resistance (°C/W)

$R_{\theta JC}$ = junction to case thermal resistance (°C/W)

$R_{\theta CA}$ = case to ambient thermal resistance (°C/W)

$R_{\theta JC}$ is device related and cannot be influenced by the user. The user controls the thermal environment to change the case to ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the size of the heat sink, the air flow around the device, the interface material, the mounting arrangement on printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the device.

To determine the junction temperature of the device in the application when heat sinks are not used, the Thermal Characterization Parameter (Ψ_{JT}) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using *Equation 3*:

Equation 3 $T_J = T_T + (\Psi_{JT} \times P_D)$

where:

T_T = thermocouple temperature on top of the package (°C)

Ψ_{JT} = thermal characterization parameter (°C/W)

P_D = power dissipation in the package (W)

The thermal characterization parameter is measured per JESD51-2 specification using a 40 gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

References:

Semiconductor Equipment and Materials International

3081 Zanker Road

San Jose, CA 95134 U.S.A.

(408) 943-6900

MIL-SPEC and EIA/JESD (JEDEC) specifications are available from Global Engineering Documents at 800-854-7179 or 303-397-7956.

JEDEC specifications are available on the WEB at http://www.jedec.org.

3.8.2 Voltage monitor electrical characteristics

The device implements a Power-on Reset module to ensure correct power-up initialization, as well as three low voltage detectors to monitor the V_{DD} and the V_{DD_LV} voltage while device is supplied:

- POR monitors V_{DD} during the power-up phase to ensure device is maintained in a safe reset state
- LVDHV3 monitors V_{DD} to ensure device reset below minimum functional supply
- LVDHV5 monitors V_{DD} when application uses device in the 5.0 V ± 10 % range
- LVDLVCOR monitors low voltage digital power domain

Table 19. Low voltage monitor electrical characteristics

Symbol	C	Parameter	Conditions (1)	Value		Unit
				Min	Max	
V_{PORH}	T	Power-on reset threshold	—	1.5	2.7	V
V_{PORUP}	P	Supply for functional POR module	T_A = 25 °C	1.0	—	V
$V_{REGLVDMOK\_H}$	P	Regulator low voltage detector high threshold	—	—	2.95	V
$V_{REGLVDMOK\_L}$	P	Regulator low voltage detector low threshold	—	2.6	—	V
$V_{FLLVDMOK\_H}$	P	Flash low voltage detector high threshold	—	—	2.95	V
$V_{FLLVDMOK\_L}$	P	Flash low voltage detector low threshold	—	2.6	—	V
$V_{IOLVDMOK\_H}$	P	I/O low voltage detector high threshold	—	—	2.95	V
$V_{IOLVDMOK\_L}$	P	I/O low voltage detector low threshold	—	2.6	—	V
$V_{IOLVDM5OK\_H}$	P	I/O 5V low voltage detector high threshold	—	—	4.4	V
$V_{IOLVDM5OK\_L}$	P	I/O 5V low voltage detector low threshold	—	3.8	—	V
$V_{MLVDDOK\_H}$	P	Digital supply low voltage detector high	—	—	1.145	V
$V_{MLVDDOK\_L}$	P	Digital supply low voltage detector low	—	1.08	—	V

1. V_{DD} = 3.3V ± 10% / 5.0V ± 10%, T_A = –40 °C to $T_{A\ MAX}$, unless otherwise specified

3.9 Power up/down sequencing

To prevent an overstress event or a malfunction within and outside the device, the SPC560P44Lx, SPC560P50Lx implements the following sequence to ensure each module is started only when all conditions for switching it ON are available:

- A POWER_ON module working on voltage regulator supply controls the correct start-up of the regulator. This is a key module ensuring safe configuration for all voltage regulator functionality when supply is below 1.5V. Associated POWER_ON (or POR) signal is active low.
- Several low voltage detectors, working on voltage regulator supply monitor the voltage of the critical modules (voltage regulator, I/Os, flash memory and low voltage domain). LVDs are gated low when POWER_ON is active.
- A POWER_OK signal is generated when all critical supplies monitored by the LVD are available. This signal is active high and released to all modules including I/Os, flash

3.10.2 DC electrical characteristics (5 V)

Table 21 gives the DC electrical characteristics at 5 V (4.5 V < $V_{DD\_HV\_IOx}$ < 5.5 V, NVUSRO[PAD3V5V] = 0); see *Figure 14*.

Table 21. DC electrical characteristics (5.0 V, NVUSRO[PAD3V5V] = 0)

Symbol	C	Parameter	Conditions	Value		Unit
				Min	Max	
V_{IL}	D	Low level input voltage	—	–0.1(1)	—	V
	P		—	—	0.35 $V_{DD\_HV\_IOx}$	V
V_{IH}	P	High level input voltage	—	0.65 $V_{DD\_HV\_IOx}$	—	V
	D		—	—	$V_{DD\_HV\_IOx}$ + 0.1(1)	V
V_{HYS}	T	Schmitt trigger hysteresis	—	0.1 $V_{DD\_HV\_IOx}$	—	V
V_{OL_S}	P	Slow, low level output voltage	I_{OL} = 3 mA	—	0.1 $V_{DD\_HV\_IOx}$	V
V_{OH_S}	P	Slow, high level output voltage	I_{OH} = –3 mA	0.8 $V_{DD\_HV\_IOx}$	—	V
V_{OL_M}	P	Medium, low level output voltage	I_{OL} = 3 mA	—	0.1 $V_{DD\_HV\_IOx}$	V
V_{OH_M}	P	Medium, high level output voltage	I_{OH} = –3 mA	0.8 $V_{DD\_HV\_IOx}$	—	V
V_{OL_F}	P	Fast, low level output voltage	I_{OL} = 3 mA	—	0.1 $V_{DD\_HV\_IOx}$	V
V_{OH_F}	P	Fast, high level output voltage	I_{OH} = –3 mA	0.8 $V_{DD\_HV\_IOx}$	—	V
V_{OL_SYM}	P	Symmetric, low level output voltage	I_{OL} = 3 mA	—	0.1 $V_{DD\_HV\_IOx}$	V
V_{OH_SYM}	P	Symmetric, high level output voltage	I_{OH} = –3 mA	0.8 $V_{DD\_HV\_IOx}$	—	V
I_{PU}	P	Equivalent pull-up current	V_{IN} = V_{IL}	–130	—	µA
			V_{IN} = V_{IH}	—	–10	
I_{PD}	P	Equivalent pull-down current	V_{IN} = V_{IL}	10	—	µA
			V_{IN} = V_{IH}	—	130	
I_{IL}	P	Input leakage current (all bidirectional ports)	T_A = –40 to 125 °C	–1	1	µA
I_{IL}	P	Input leakage current (all ADC input-only ports)	T_A = –40 to 125 °C	–0.5	0.5	µA
C_{IN}	D	Input capacitance	—	—	10	pF
I_{PU}	D	$\overline{\text{RESET}}$, equivalent pull-up current	V_{IN} = V_{IL}	–130	—	µA
			V_{IN} = V_{IH}	—	–10	

1. “SR” parameter values must not exceed the absolute maximum ratings shown in *Table 9*.

Table 24. Supply current (3.3 V, NVUSRO[PAD3V5V] = 1)

Symbol	C	Parameter		Conditions		Value		Unit
						Typ	Max	
$I_{DD\_LV\_CORx}$	T	Supply current	RUN—Maximum mode(1)	$V_{DD\_LV\_CORx}$ externally forced at 1.3 V	40 MHz	62	77	mA
					64 MHz	71	89	
			RUN—Typical mode(2)		40 MHz	45	56	
					64 MHz	53	66	
	P		RUN—Maximum mode(3)	$V_{DD\_LV\_CORx}$ externally forced at 1.3 V	64 MHz	60	75	
			HALT mode(4)	$V_{DD\_LV\_CORx}$ externally forced at 1.3 V	—	1.5	10	
			STOP mode(5)	$V_{DD\_LV\_CORx}$ externally forced at 1.3 V	—	1	10	
I_{DD_FLASH}	T		Flash during read on single mode	$V_{DD\_HV\_FL}$ at 3.3 V	—	8	10	
			Flash during erase operation on single mode	$V_{DD\_HV\_FL}$ at 3.3 V	—	10	12	
I_{DD_ADC}	T		ADC—Maximum mode(1)	$V_{DD\_HV\_ADC0}$ at 3.3 V $V_{DD\_HV\_ADC1}$ at 3.3 V f_{ADC} = 16 MHz	ADC_1	2.5	4	
					ADC_0	2	4	
			ADC—Typical mode(2)		ADC_1	0.8	1	
					ADC_0	0.005	0.006	
I_{DD_OSC}	T		Oscillator	V_{DD_OSC} at 3.3 V	8 MHz	2.4	3	

1. Maximum mode: FlexPWM, ADCs, CTU, DSPI, LINFlex, FlexCAN, 15 output pins, 1st and 2nd PLL enabled. I/O supply current excluded.
2. Typical mode: DSPI, LINFlex, FlexCAN, 15 output pins, 1st PLL only. I/O supply current excluded.
3. Code fetched from RAM, PLL_0: 64 MHz system clock (x4 multiplier with 16 MHz XTAL), PLL_1 is ON at PHI_div2 = 120 MHz and PHI_div3 = 80 MHz, auxiliary clock sources set that all peripherals receive maximum frequency, all peripherals enabled.
4. Halt mode configurations: code fetched from RAM, code and data flash memories in low power mode, OSC/PLL_0/PLL_1 are OFF, core clock frozen, all peripherals are disabled.
5. STOP “P” mode Device Under Test (DUT) configuration: code fetched from RAM, code and data flash memories OFF, OSC/PLL_0/PLL_1 are OFF, core clock frozen, all peripherals are disabled.

3.10.4 Input DC electrical characteristics definition

Figure 14 shows the DC electrical characteristics behavior as function of time.

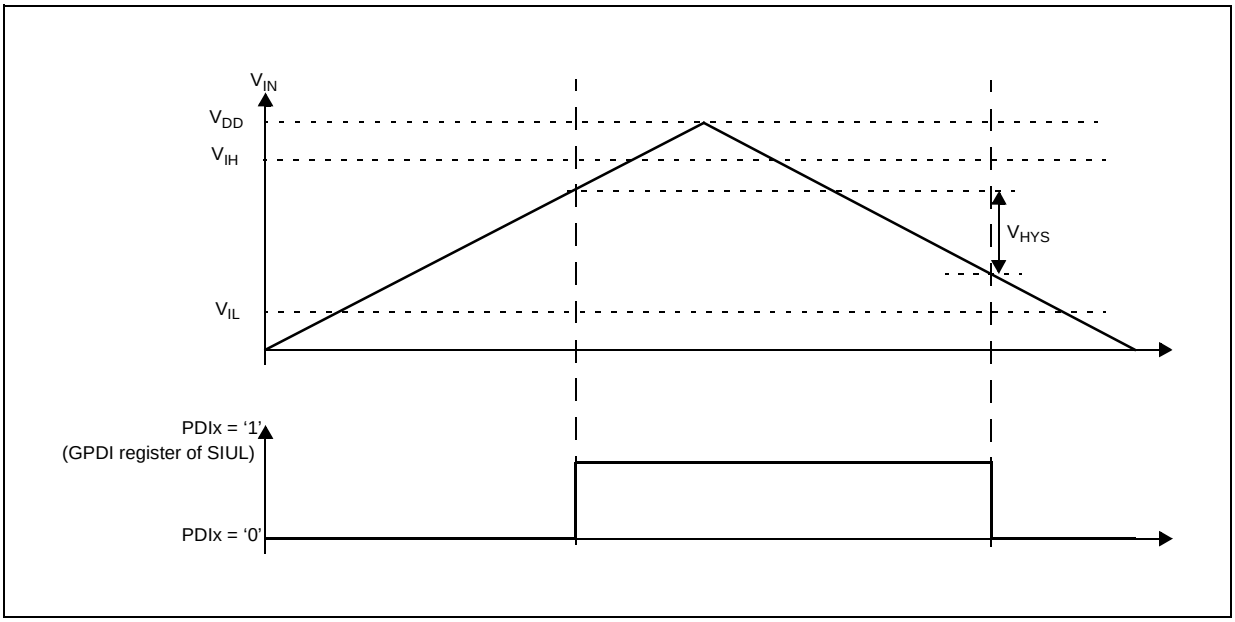


Figure 14. Input DC electrical characteristics definition

3.10.5 I/O pad current specification

The I/O pads are distributed across the I/O supply segment. Each I/O supply segment is associated to a V_{DD}/V_{SS} supply pair as described in *Table 25*.

Table 25. I/O supply segment

Package	Supply segment						
	1	2	3	4	5	6	7
LQFP144	pin8 – pin20	pin23 – pin38	pin39 – pin55	pin58 – pin68	pin73 – pin89	pin92 – pin125	pin128 – pin5
LQFP100	pin15 – pin26	pin27 – pin38	pin41 – pin46	pin51 – pin61	pin64 – pin86	pin89 – pin10	—

Table 26 provides the weight of concurrent switching I/Os.

In order to ensure device functionality, the sum of the weight of concurrent switching I/Os on a single segment should remain below 100%.

Table 26. I/O weight

Pad	LQFP144		LQFP100	
	Weight 5V	Weight 3.3V	Weight 5V	Weight 3.3V
NMI	1%	1%	1%	1%
PAD[6]	6%	5%	14%	13%
PAD[49]	5%	4%	14%	12%
PAD[84]	14%	10%	—	—
PAD[85]	9%	7%	—	—

A second aspect involving the capacitance network shall be considered. Assuming the three capacitances C_F, C_{P1} and C_{P2} are initially charged at the source voltage V_A (refer to the equivalent circuit reported in *Figure 16*): A charge sharing phenomenon is installed when the sampling phase is started (A/D switch closed).

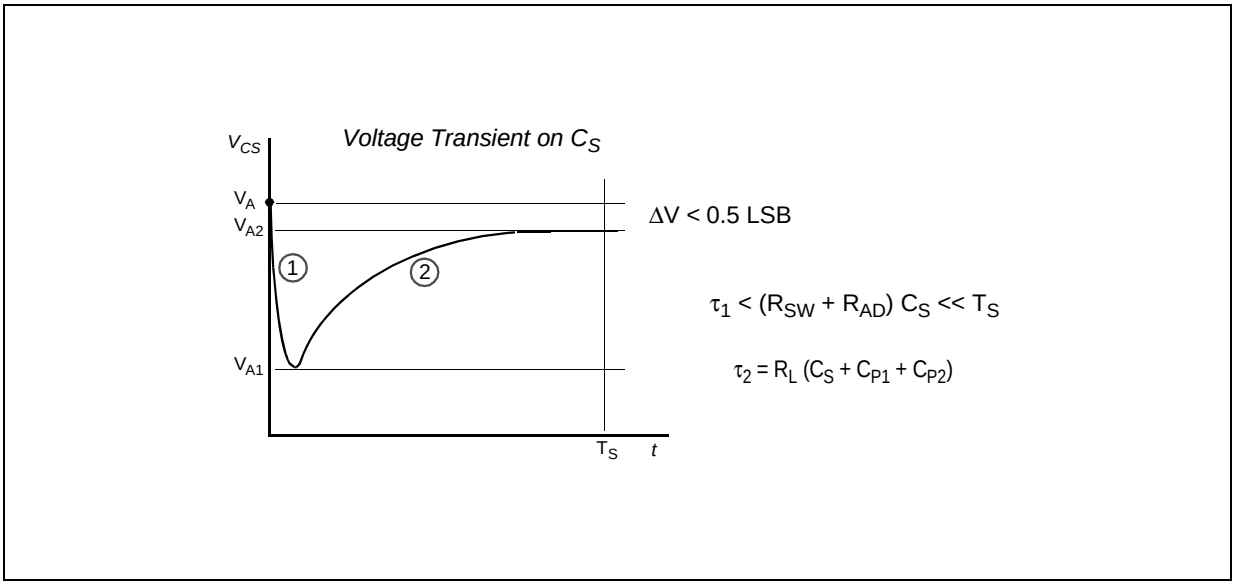


Figure 17. Transient behavior during sampling phase

In particular two different transient periods can be distinguished:

- A first and quick charge transfer from the internal capacitance C_{P1} and C_{P2} to the sampling capacitance C_S occurs (C_S is supposed initially completely discharged): considering a worst case (since the time constant in reality would be faster) in which C_{P2} is reported in parallel to C_{P1} (call $C_P = C_{P1} + C_{P2}$), the two capacitances C_P and C_S are in series, and the time constant is

Equation 5

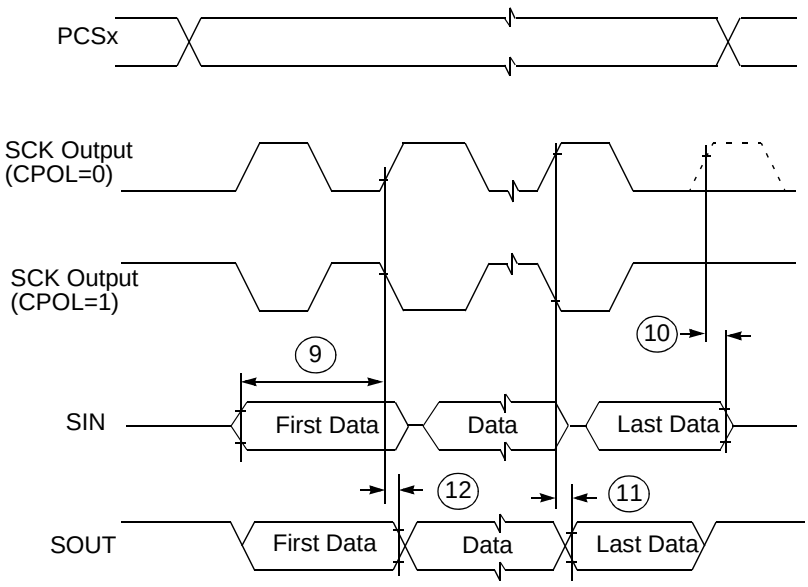
$$\tau_1 = (R_{SW} + R_{AD}) \bullet \frac{C_P \bullet C_S}{C_P + C_S}$$

Equation 5 can again be simplified considering only C_S as an additional worst condition. In reality, the transient is faster, but the A/D converter circuitry has been designed to be robust also in the very worst case: the sampling time T_S is always much longer than the internal time constant:

Equation 6

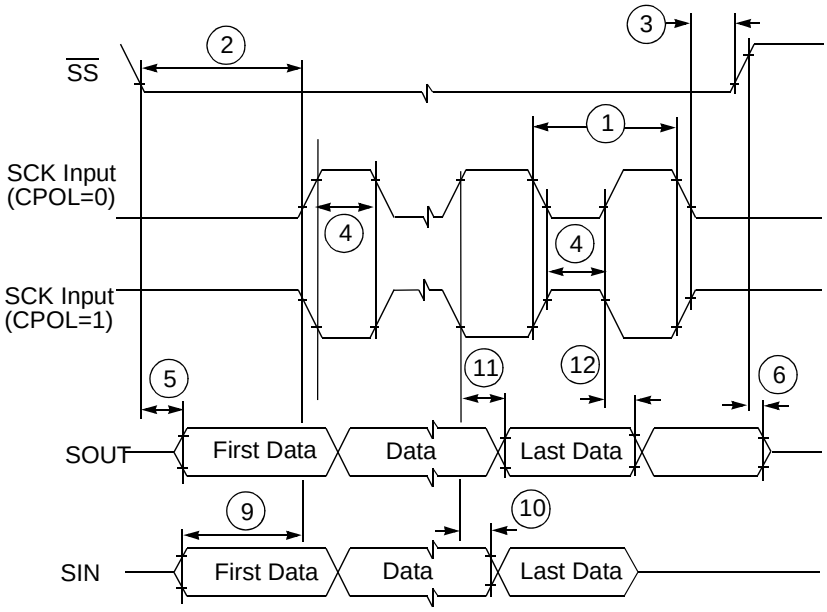
$$\tau_1 < (R_{SW} + R_{AD}) \bullet C_S \ll T_S$$

The charge of C_{P1} and C_{P2} is redistributed also on C_S, determining a new value of the voltage V_{A1} on the capacitance according to *Equation 7*:



Note: Numbers shown reference *Table 42*.

Figure 34. DSPI modified transfer format timing – Master, CPHA = 1



Note: Numbers shown reference *Table 42*.

Figure 35. DSPI modified transfer format timing – Slave, CPHA = 0

6 Revision history

Table 46 summarizes revisions to this document.

Table 46. Revision history

Date	Revision	Changes
28-Aug-2008	1	Initial release
25-Nov-2008	2	*Table 7*: TDO and TDI pins (Port pins B[4:5] are single function pins. *Table 12*, *Table 13*: Thermal characteristics added. *Table 11*, *Table 12*: EMI testing specifications split into separate tables for Normal mode and Airbag mode; data to be added in a later revision. *Table 16*, *Table 17*, *Table 19*, *Table 20*: Supply current specifications split into separate tables for Normal mode and Airbag mode; data to be added in a later revision. *Table 23*: ● Values for I_{OL} and I_{OH} (in Conditions column) changed. ● Max values for V_{OH_S}, V_{OH_M}, V_{OH_F} and V_{OH_SYM} deleted. ● V_{ILR} max value changed. ● I_{PUR} min and max values changed. *Table 27*: Sensitivity value changed. *Table 30*: Most values in table changed.
05-Mar-2009	3	● Description of system requirements, controller characteristics and how controller characteristics are guaranteed updated. ● Electrical parameters updated. ● EMI characteristics are now in one table; values have been updated. ● ESD characteristics are now in one table. ● Electrical parameters are identified as either system requirements or controller characteristics. Method used to guarantee each controller characteristic is noted in table. ● AC Timings: 1149.1 (JTAG) Timing, Nexus Timing, External Interrupt Timing, and DSPI Timing sections deleted