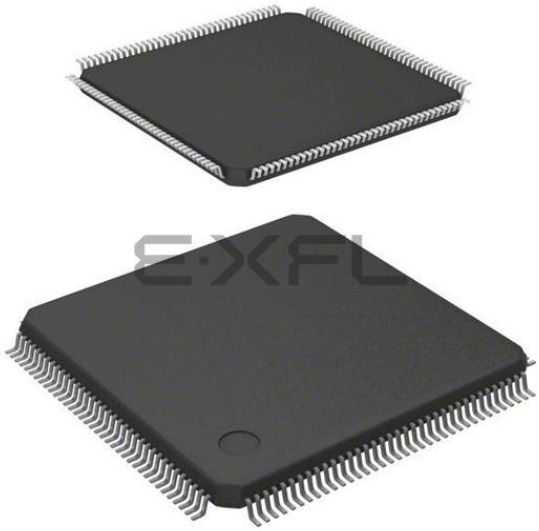

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What is "Embedded - Microcontrollers"?

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	e200z0h
Core Size	32-Bit Single-Core
Speed	64MHz
Connectivity	CANbus, LINbus, SPI, UART/USART
Peripherals	DMA, POR, PWM, WDT
Number of I/O	107
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	40K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 26x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/spc560p50l5beabr

List of tables

Table 2. SPC560P44Lx, SPC560P50Lx device comparison (continued)

Feature		SPC560P44	SPC560P50
eDMA (enhanced direct memory access) channels		16	
FlexRay		Yes(1)	
FlexCAN (controller area network)		2(2),(3)	
Safety port		Yes (via second FlexCAN module)	
FCU (fault collection unit)		Yes	
CTU (cross triggering unit)		Yes	
eTimer		2 (16-bit, 6 channels)	
FlexPWM (pulse-width modulation) channels		8 (capturing on X-channels)	
ADC (analog-to-digital converter)		2 (10-bit, 15-channel(4))	
LINFlex		2	
DSPI (deserial serial peripheral interface)		4	
CRC (cyclic redundancy check) unit		Yes	
JTAG controller		Yes	
Nexus port controller (NPC)		Yes (Level 2+)	
Supply	Digital power supply(5)	3.3 V or 5 V single supply with external transistor	
	Analog power supply	3.3 V or 5 V	
	Internal RC oscillator	16 MHz	
	External crystal oscillator	4–40 MHz	
Packages		LQFP100 LQFP144	
Temperature	Standard ambient temperature	–40 to 125 °C	

1. 32 message buffers, selectable single or dual channel support
2. Each FlexCAN module has 32 message buffers.
3. One FlexCAN module can act as a Safety Port with a bit rate as high as 7.5 Mbit/s.
4. Four channels shared between the two ADCs
5. The different supply voltages vary according to the part number ordered.

SPC560P44Lx, SPC560P50Lx is available in two configurations having different features: full-featured and airbag. *Table 3* shows the main differences between the two versions.

Table 3. SPC560P44Lx, SPC560P50Lx device configuration differences

Feature	Full-featured	Airbag
CTU (cross triggering unit)	Yes	No
FlexPWM	Yes	No

Table 3. SPC560P44Lx, SPC560P50Lx device configuration differences (continued)

Feature	Full-featured	Airbag
FlexRay	Yes	No
FMPLL (frequency-modulated phase-locked loop) module	2 (one FMPLL, one for FlexRay)	1 (only FMPLL)

1.4 Block diagram

Figure 1 shows a top-level block diagram of the SPC560P44Lx, SPC560P50Lx MCU.

The flash memory module provides the following features:

- As much as 576 KB flash memory
  - 8 blocks (32 KB + 2×16 KB + 32 KB + 32 KB + 3×128 KB) code flash
  - 4 blocks (16 KB + 16 KB + 16 KB + 16 KB) data flash
  - Full Read While Write (RWW) capability between code and data flash
- Four 128-bit wide prefetch buffers to provide single cycle in-line accesses (prefetch buffers can be configured to prefetch code or data or both)
- Typical flash memory access time: 0 wait states for buffer hits, 2 wait states for page buffer miss at 64 MHz
- Hardware managed flash memory writes handled by 32-bit RISC Krypton engine
- Hardware and software configurable read and write access protections on a per-master basis
- Configurable access timing allowing use in a wide range of system frequencies
- Multiple-mapping support and mapping-based block access timing (up to 31 additional cycles) allowing use for emulation of other memory types.
- Software programmable block program/erase restriction control
- Erase of selected block(s)
- Read page sizes
  - Code flash memory: 128 bits (4 words)
  - Data flash memory: 32 bits (1 word)
- ECC with single-bit correction, double-bit detection for data integrity
  - Code flash memory: 64-bit ECC
  - Data flash memory: 64-bit ECC
- Embedded hardware program and erase algorithm
- Erase suspend, program suspend and erase-suspended program
- Censorship protection scheme to prevent flash memory content visibility
- Hardware support for EEPROM emulation

1.5.5 Static random access memory (SRAM)

The SPC560P44Lx, SPC560P50Lx SRAM module provides up to 40 KB of general-purpose memory.

The SRAM module provides the following features:

- Supports read/write accesses mapped to the SRAM from any master
- Up to 40 KB general purpose SRAM
- Supports byte (8-bit), half word (16-bit), and word (32-bit) writes for optimal use of memory
- Typical SRAM access time: 0 wait-state for reads and 32-bit writes; 1 wait state for 8- and 16-bit writes if back to back with a read to same memory block

1.5.6 Interrupt controller (INTC)

The interrupt controller (INTC) provides priority-based preemptive scheduling of interrupt requests, suitable for statically scheduled hard real-time systems. The INTC handles 147 selectable-priority interrupt sources.

For high priority interrupt requests, the time from the assertion of the interrupt request from the peripheral to when the processor is executing the interrupt service routine (ISR) has been minimized. The INTC provides a unique vector for each interrupt request source for quick determination of which ISR has to be executed. It also provides a wide number of priorities so that lower priority ISRs do not delay the execution of higher priority ISRs. To allow the appropriate priorities for each source of interrupt request, the priority of each interrupt request is software configurable.

When multiple tasks share a resource, coherent accesses to that resource need to be supported. The INTC supports the priority ceiling protocol (PCP) for coherent accesses. By providing a modifiable priority mask, the priority can be raised temporarily so that all tasks which share the same resource can not preempt each other.

The INTC provides the following features:

- Unique 9-bit vector for each separate interrupt source
- 8 software triggerable interrupt sources
- 16 priority levels with fixed hardware arbitration within priority levels for each interrupt source
- Ability to modify the ISR or task priority: modifying the priority can be used to implement the Priority Ceiling Protocol for accessing shared resources.
- 2 external high priority interrupts directly accessing the main core and I/O processor (IOP) critical interrupt mechanism

1.5.7 System status and configuration module (SSCM)

The system status and configuration module (SSCM) provides central device functionality.

The SSCM includes these features:

- System configuration and status
  - Memory sizes/status
  - Device mode and security status
  - Determine boot vector
  - Search code flash for bootable sector
  - DMA status
- Debug status port enable and selection
- Bus and peripheral abort enable/disable

1.5.8 System clocks and clock generation

The following list summarizes the system clock and clock generation on the SPC560P44Lx, SPC560P50Lx:

- Lock detect circuitry continuously monitors lock status
- Loss of clock (LOC) detection for PLL outputs
- Programmable output clock divider (÷1, ÷2, ÷4, ÷8)
- FlexPWM module and eTimer module can run on an independent clock source
- On-chip oscillator with automatic level control
- Internal 16 MHz RC oscillator for rapid start-up and safe mode: supports frequency trimming by user application

The SIU provides the following features:

- Centralized general purpose input output (GPIO) control of as many as 80 input/output pins and 26 analog input-only pads (package dependent)
- All GPIO pins can be independently configured to support pull-up, pull down, or no pull
- Reading and writing to GPIO supported both as individual pins and 16-bit wide ports
- All peripheral pins (except ADC channels) can be alternatively configured as both general purpose input or output pins
- ADC channels support alternative configuration as general purpose inputs
- Direct readback of the pin value is supported on all pins through the SIUL
- Configurable digital input filter that can be applied to some general purpose input pins for noise elimination: as many as 4 internal functions can be multiplexed onto 1 pin

1.5.17 Boot and censorship

Different booting modes are available in the SPC560P44Lx, SPC560P50Lx: booting from internal flash memory and booting via a serial link.

The default booting scheme uses the internal flash memory (an internal pull-down is used to select this mode). Optionally, the user can boot via FlexCAN or LINFlex (using the boot assist module software).

A censorship scheme is provided to protect the content of the flash memory and offer increased security for the entire device.

A password mechanism is designed to grant the legitimate user access to the non-volatile memory.

Boot assist module (BAM)

The BAM is a block of read-only one-time programmed memory and is identical for all SPC560Pxx devices that are based on the e200z0h core. The BAM program is executed every time the device is powered on if the alternate boot mode has been selected by the user.

The BAM provides the following features:

- Serial bootloading via FlexCAN or LINFlex
- Ability to accept a password via the used serial communication channel to grant the legitimate user access to the non-volatile memory

1.5.18 Error correction status module (ECSM)

The ECSM provides a myriad of miscellaneous control functions regarding program-visible information about the platform configuration and revision levels, a reset status register, a software watchdog timer, wakeup control for exiting sleep modes, and information on platform memory errors reported by error-correcting codes and/or generic access error information for certain processor cores.

The Error Correction Status Module supports a number of miscellaneous control functions for the platform. The ECSM includes these features:

- Registers for capturing information on platform memory errors if error-correcting codes (ECC) are implemented
- For test purposes, optional registers to specify the generation of double-bit memory errors are enabled on the SPC560P44Lx, SPC560P50Lx.

The JTAG controller provides the following features:

- IEEE Test Access Port (TAP) interface with 4 pins (TDI, TMS, TCK, TDO)
- Selectable modes of operation include JTAGC/debug or normal system operation.
- A 5-bit instruction register that supports the following IEEE 1149.1-2001 defined instructions:
  - BYPASS, IDCODE, EXTEST, SAMPLE, SAMPLE/PRELOAD
- A 5-bit instruction register that supports the additional following public instructions:
  - ACCESS_AUX_TAP_NPC, ACCESS_AUX_TAP_ONCE
- 3 test data registers: a bypass register, a boundary scan register, and a device identification register.
- A TAP controller state machine that controls the operation of the data registers, instruction register and associated circuitry.

1.5.32 On-chip voltage regulator (VREG)

The on-chip voltage regulator module provides the following features:

- Uses external NPN (negative-positive-negative) transistor
- Regulates external 3.3 V /5.0 V down to 1.2 V for the core logic
- Low voltage detection on the internal 1.2 V and I/O voltage 3.3 V

Table 6. System pins (continued)

Symbol	Description	Direction	Pad speed(1)		Pin	
			SRC = 0	SRC = 1	100-pin	144-pin
TMS	JTAG state machine control	Bidirectional	Slow	Fast	59	87
TCK	JTAG clock	Input only	Slow	—	60	88
TDI	Test Data In	Input only	Slow	Medium	58	86
TDO	Test Data Out	Output only	Slow	Fast	61	89
Reset pin, available on 100-pin and 144-pin package.						
$\overline{\text{RESET}}$	Bidirectional reset with Schmitt trigger characteristics and noise filter	Bidirectional	Medium	—	20	31
Test pin, available on 100-pin and 144-pin package.						
VPP_TEST	Pin for testing purpose only. To be tied to ground in normal operating mode.	—	—	—	74	107

1. SCR values refer to the value assigned to the Slew Rate Control bits of the pad configuration register.

2.2.3 Pin muxing

Table 7 defines the pin list and muxing for the SPC560P44Lx, SPC560P50Lx devices.

Each row of *Table 7* shows all the possible ways of configuring each pin, via alternate functions. The default function assigned to each pin after reset is the ALT0 function.

SPC560P44Lx, SPC560P50Lx devices provide four main I/O pad types, depending on the associated functions:

- *Slow pads* are the most common, providing a compromise between transition time and low electromagnetic emission.
- *Medium pads* provide fast enough transition for serial communication channels with controlled current to reduce electromagnetic emission.
- *Fast pads* provide maximum speed. They are used for improved NEXUS debugging capability.
- *Symmetric pads* are designed to meet FlexRay requirements.

Medium and Fast pads can use slow configuration to reduce electromagnetic emission, at the cost of reducing AC performance. For more information, see the datasheet's "Pad AC Specifications" section.

Table 7. Pin muxing (continued)

Port pin	Pad configuration register (PCR)	Alternate function[1],[2]	Functions	Peripheral[3]	I/O direction[4]	Pad speed[5]		Pin No.	
						SRC = 0	SRC = 1	100-pin	144-pin
C[13]	PCR[45]	ALT0 ALT1 ALT2 ALT3 — —	GPIO[45] ETC[1] — — EXT_IN EXT_SYNC	SIUL eTimer_1 — — CTU_0 FlexPWM_0	I/O I/O — — I I	Slow	Medium	71	101
C[14]	PCR[46]	ALT0 ALT1 ALT2 ALT3	GPIO[46] ETC[2] EXT_TGR —	SIUL eTimer_1 CTU_0 —	I/O I/O O —	Slow	Medium	72	103
C[15]	PCR[47]	ALT0 ALT1 ALT2 ALT3 — —	GPIO[47] CA_TR_EN ETC[0] A[1] EXT_IN EXT_SYNC	SIUL FlexRay_0 eTimer_1 FlexPWM_0 CTU_0 FlexPWM_0	I/O O I/O O I I	Slow	Symmetric	85	124
Port D (16-bit)									
D[0]	PCR[48]	ALT0 ALT1 ALT2 ALT3	GPIO[48] CA_TX ETC[1] B[1]	SIUL FlexRay_0 eTimer_1 FlexPWM_0	I/O O I/O O	Slow	Symmetric	86	125
D[1]	PCR[49]	ALT0 ALT1 ALT2 ALT3 —	GPIO[49] — ETC[2] EXT_TRG CA_RX	SIUL — eTimer_1 CTU_0 FlexRay_0	I/O — I/O O I	Slow	Medium	3	3
D[2]	PCR[50]	ALT0 ALT1 ALT2 ALT3 —	GPIO[50] — ETC[3] X[3] CB_RX	SIUL — eTimer_1 FlexPWM_0 FlexRay_0	I/O — I/O I/O I	Slow	Medium	97	140
D[3]	PCR[51]	ALT0 ALT1 ALT2 ALT3	GPIO[51] CB_TX ETC[4] A[3]	SIUL FlexRay_0 eTimer_1 FlexPWM_0	I/O O I/O O	Slow	Symmetric	89	128
D[4]	PCR[52]	ALT0 ALT1 ALT2 ALT3	GPIO[52] CB_TR_EN ETC[5] B[3]	SIUL FlexRay_0 eTimer_1 FlexPWM_0	I/O O I/O O	Slow	Symmetric	90	129

Table 7. Pin muxing (continued)

Port pin	Pad configuration register (PCR)	Alternate function[1], [2]	Functions	Peripheral[3]	I/O direction [4]	Pad speed[5]		Pin No.	
						SRC = 0	SRC = 1	100-pin	144-pin
D[14]	PCR[62]	ALT0 ALT1 ALT2 ALT3 —	GPIO[62] B[1] CS3 — SIN	SIUL FlexPWM_0 DSPI_3 — DSPI_3	I/O O O — I	Slow	Medium	73	105
D[15]	PCR[63]	ALT0 ALT1 ALT2 ALT3 —	GPIO[63] — — — AN[4]	SIUL — — — ADC_1	Input only	—	—	41	58
Port E(16-bit)									
E[0]	PCR[64]	ALT0 ALT1 ALT2 ALT3 —	GPIO[64] — — — AN[5]	SIUL — — — ADC_1	Input only	—	—	46	68
E[1]	PCR[65]	ALT0 ALT1 ALT2 ALT3 —	GPIO[65] — — — AN[4]	SIUL — — — ADC_0	Input only	—	—	27	39
E[2]	PCR[66]	ALT0 ALT1 ALT2 ALT3 —	GPIO[66] — — — AN[5]	SIUL — — — ADC_0	Input only	—	—	32	49
E[3]	PCR[67]	ALT0 ALT1 ALT2 ALT3 —	GPIO[67] — — — AN[6]	SIUL — — — ADC_0	Input only	—	—	—	40
E[4]	PCR[68]	ALT0 ALT1 ALT2 ALT3 —	GPIO[68] — — — AN[7]	SIUL — — — ADC_0	Input only	—	—	—	42

Table 11. Recommended operating conditions (3.3 V) (continued)

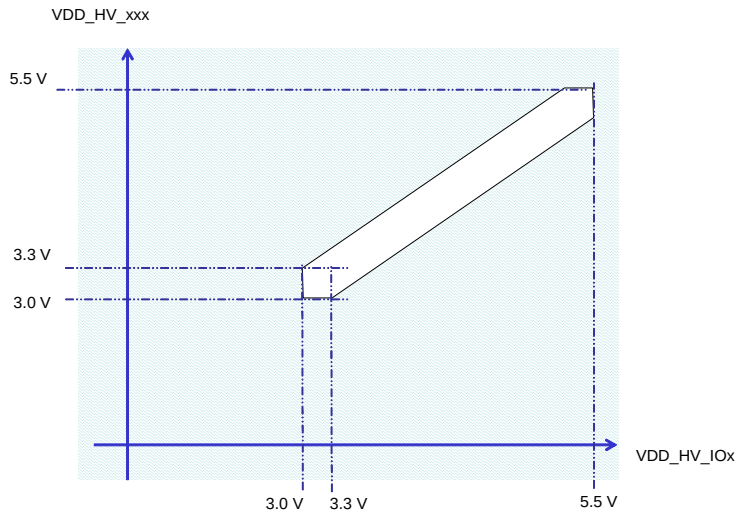
Symbol		Parameter	Conditions	Value		Unit
				Min	Max(1)	
$V_{SS\_LV\_CORx}$(4)	SR	Internal reference voltage	—	0	0	V
T_A	SR	Ambient temperature under bias	f_{CPU} = 64 MHz	–40	105	°C
			f_{CPU} = 60 MHz	–40	125	

1. Parametric figures can be out of specification when voltage drops below 4.5 V, however, guaranteeing the full functionality. In particular, ADC electrical characteristics and I/Os DC electrical specification may not be guaranteed.
2. The difference between each couple of voltage supplies must be less than 100 mV, $|V_{DD\_HV\_IOy} - V_{DD\_HV\_IOx}| < 100$ mV.
3. The difference between each couple of voltage supplies must be less than 100 mV, $|V_{DD\_HV\_ADC1} - V_{DD\_HV\_ADC0}| < 100$ mV. As long as that condition is met, ADC_0 and ADC_1 can be operated at 5 V with the rest of the device operating at 3.3 V.
4. To be connected to emitter of external NPN. Low voltage supplies are not under user control—they are produced by an on-chip voltage regulator—but for the device to function properly the low voltage grounds ($V_{SS\_LV\_xxx}$) must be shorted to high voltage grounds ($V_{SS\_HV\_xxx}$) and the low voltage supply pins ($V_{DD\_LV\_xxx}$) must be connected to the external ballast emitter.
5. The low voltage supplies ($V_{DD\_LV\_xxx}$) are not all independent.

$V_{DD\_LV\_COR1}$ and $V_{DD\_LV\_COR2}$ are shorted internally via double bonding connections with lines that provide the low voltage supply to the data flash module. Similarly, $V_{SS\_LV\_COR1}$ and $V_{SS\_LV\_COR2}$ are internally shorted.

$V_{DD\_LV\_REGCOR}$ and $V_{DD\_LV\_REGCORx}$ are physically shorted internally, as are $V_{SS\_LV\_REGCOR}$ and $V_{SS\_LV\_CORx}$.

Figure 7 shows the constraints of the different power supplies.



Note: IO AC and DC characteristics are guaranteed only in the range of 3.0–3.6 V when PAD3V5V is low, and in the range of 4.5–5.5 V when PAD3V5V is high.

Figure 7. Power supplies constraints (3.0 V ≤ $V_{DD\_HV\_IOx}$ ≤ 5.5 V)

3.10.2 DC electrical characteristics (5 V)

Table 21 gives the DC electrical characteristics at 5 V (4.5 V < $V_{DD\_HV\_IOx}$ < 5.5 V, NVUSRO[PAD3V5V] = 0); see *Figure 14*.

Table 21. DC electrical characteristics (5.0 V, NVUSRO[PAD3V5V] = 0)

Symbol	C	Parameter	Conditions	Value		Unit
				Min	Max	
V_{IL}	D	Low level input voltage	—	–0.1(1)	—	V
	P		—	—	0.35 $V_{DD\_HV\_IOx}$	V
V_{IH}	P	High level input voltage	—	0.65 $V_{DD\_HV\_IOx}$	—	V
	D		—	—	$V_{DD\_HV\_IOx}$ + 0.1(1)	V
V_{HYS}	T	Schmitt trigger hysteresis	—	0.1 $V_{DD\_HV\_IOx}$	—	V
V_{OL_S}	P	Slow, low level output voltage	I_{OL} = 3 mA	—	0.1 $V_{DD\_HV\_IOx}$	V
V_{OH_S}	P	Slow, high level output voltage	I_{OH} = –3 mA	0.8 $V_{DD\_HV\_IOx}$	—	V
V_{OL_M}	P	Medium, low level output voltage	I_{OL} = 3 mA	—	0.1 $V_{DD\_HV\_IOx}$	V
V_{OH_M}	P	Medium, high level output voltage	I_{OH} = –3 mA	0.8 $V_{DD\_HV\_IOx}$	—	V
V_{OL_F}	P	Fast, low level output voltage	I_{OL} = 3 mA	—	0.1 $V_{DD\_HV\_IOx}$	V
V_{OH_F}	P	Fast, high level output voltage	I_{OH} = –3 mA	0.8 $V_{DD\_HV\_IOx}$	—	V
V_{OL_SYM}	P	Symmetric, low level output voltage	I_{OL} = 3 mA	—	0.1 $V_{DD\_HV\_IOx}$	V
V_{OH_SYM}	P	Symmetric, high level output voltage	I_{OH} = –3 mA	0.8 $V_{DD\_HV\_IOx}$	—	V
I_{PU}	P	Equivalent pull-up current	V_{IN} = V_{IL}	–130	—	µA
			V_{IN} = V_{IH}	—	–10	
I_{PD}	P	Equivalent pull-down current	V_{IN} = V_{IL}	10	—	µA
			V_{IN} = V_{IH}	—	130	
I_{IL}	P	Input leakage current (all bidirectional ports)	T_A = –40 to 125 °C	–1	1	µA
I_{IL}	P	Input leakage current (all ADC input-only ports)	T_A = –40 to 125 °C	–0.5	0.5	µA
C_{IN}	D	Input capacitance	—	—	10	pF
I_{PU}	D	$\overline{\text{RESET}}$, equivalent pull-up current	V_{IN} = V_{IL}	–130	—	µA
			V_{IN} = V_{IH}	—	–10	

1. “SR” parameter values must not exceed the absolute maximum ratings shown in *Table 9*.

Table 26. I/O weight (continued)

Pad	LQFP144		LQFP100	
	Weight 5V	Weight 3.3V	Weight 5V	Weight 3.3V
PAD[86]	9%	6%	—	—
MODO[0]	12%	8%	—	—
PAD[7]	4%	4%	11%	10%
PAD[36]	5%	4%	11%	9%
PAD[8]	5%	4%	10%	9%
PAD[37]	5%	4%	10%	9%
PAD[5]	5%	4%	9%	8%
PAD[39]	5%	4%	9%	8%
PAD[35]	5%	4%	8%	7%
PAD[87]	12%	9%	—	—
PAD[88]	9%	6%	—	—
PAD[89]	10%	7%	—	—
PAD[90]	15%	11%	—	—
PAD[91]	6%	5%	—	—
PAD[57]	8%	7%	8%	7%
PAD[56]	13%	11%	13%	11%
PAD[53]	14%	12%	14%	12%
PAD[54]	15%	13%	15%	13%
PAD[55]	25%	22%	25%	22%
PAD[96]	27%	24%	—	—
PAD[65]	1%	1%	1%	1%
PAD[67]	1%	1%	—	—
PAD[33]	1%	1%	1%	1%
PAD[68]	1%	1%	—	—
PAD[23]	1%	1%	1%	1%
PAD[69]	1%	1%	—	—
PAD[34]	1%	1%	1%	1%
PAD[70]	1%	1%	—	—
PAD[24]	1%	1%	1%	1%
PAD[71]	1%	1%	—	—
PAD[66]	1%	1%	1%	1%
PAD[25]	1%	1%	1%	1%
PAD[26]	1%	1%	1%	1%

Table 31. FMPLL electrical characteristics (continued)

Symbol	C	Parameter		Conditions[1]	Value		Unit
					Min	Max	
C_{JITTER}	T	CLKOUT period jitter[6],[7],[8],[9]	Short-term jitter[10]	f_{SYS} maximum	–4	4	% f_{CLKOUT}
			Long-term jitter (avg. over 2 ms interval)	f_{PLLIN} = 16 MHz (resonator), f_{PLLCLK} at 64 MHz, 4000 cycles	—	10	ns
t_{lpll}	D	PLL lock time [11], [12]		—	—	200	µs
t_{dc}	D	Duty cycle of reference		—	40	60	%
f_{LCK}	D	Frequency LOCK range		—	–6	6	% f_{SYS}
f_{UL}	D	Frequency un-LOCK range		—	-18	18	% f_{SYS}
f_{CS} f_{DS}	D	Modulation depth		Center spread	±0.25	±4.0[13]	% f_{SYS}
				Down spread	–0.5	–8.0	
f_{MOD}	D	Modulation frequency[14]		—	—	70	kHz

1. $V_{DD\_LV\_CORx}$ = 1.2 V ±10%; V_{SS} = 0 V; T_A = –40 to 125 °C, unless otherwise specified
2. Considering operation with PLL not bypassed
3. “Loss of Reference Frequency” window is the reference frequency range outside of which the PLL is in self-clocked mode.
4. Self-clocked mode frequency is the frequency that the PLL operates at when the reference frequency falls outside the f_{LOR} window.
5. f_{VCO} self clock range is 20–150 MHz. f_{SCM} represents f_{SYS} after PLL output divider (ERFD) of 2 through 16 in enhanced mode.
6. This value is determined by the crystal manufacturer and board design.
7. Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{SYS}. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the PLL circuitry via V_{DDPLL} and V_{SSPLL} and variation in crystal oscillator frequency increase the C_{JITTER} percentage for a given interval.
8. Proper PC board layout procedures must be followed to achieve specifications.
9. Values are with frequency modulation disabled. If frequency modulation is enabled, jitter is the sum of C_{JITTER} and either f_{CS} or f_{DS} (depending on whether center spread or down spread modulation is enabled).
10. Short term jitter is measured on the clock rising edge at cycle n and cycle n+4.
11. This value is determined by the crystal manufacturer and board design. For 4 MHz to 20 MHz crystals specified for this PLL, load capacitors should not exceed these limits.
12. This specification applies to the period required for the PLL to relock after changing the MFD frequency control bits in the synthesizer control register (SYNCR).
13. This value is true when operating at frequencies above 60 MHz, otherwise f_{CS} is 2% (above 64 MHz).
14. Modulation depth will be attenuated from depth setting when operating at modulation frequencies above 50 kHz.

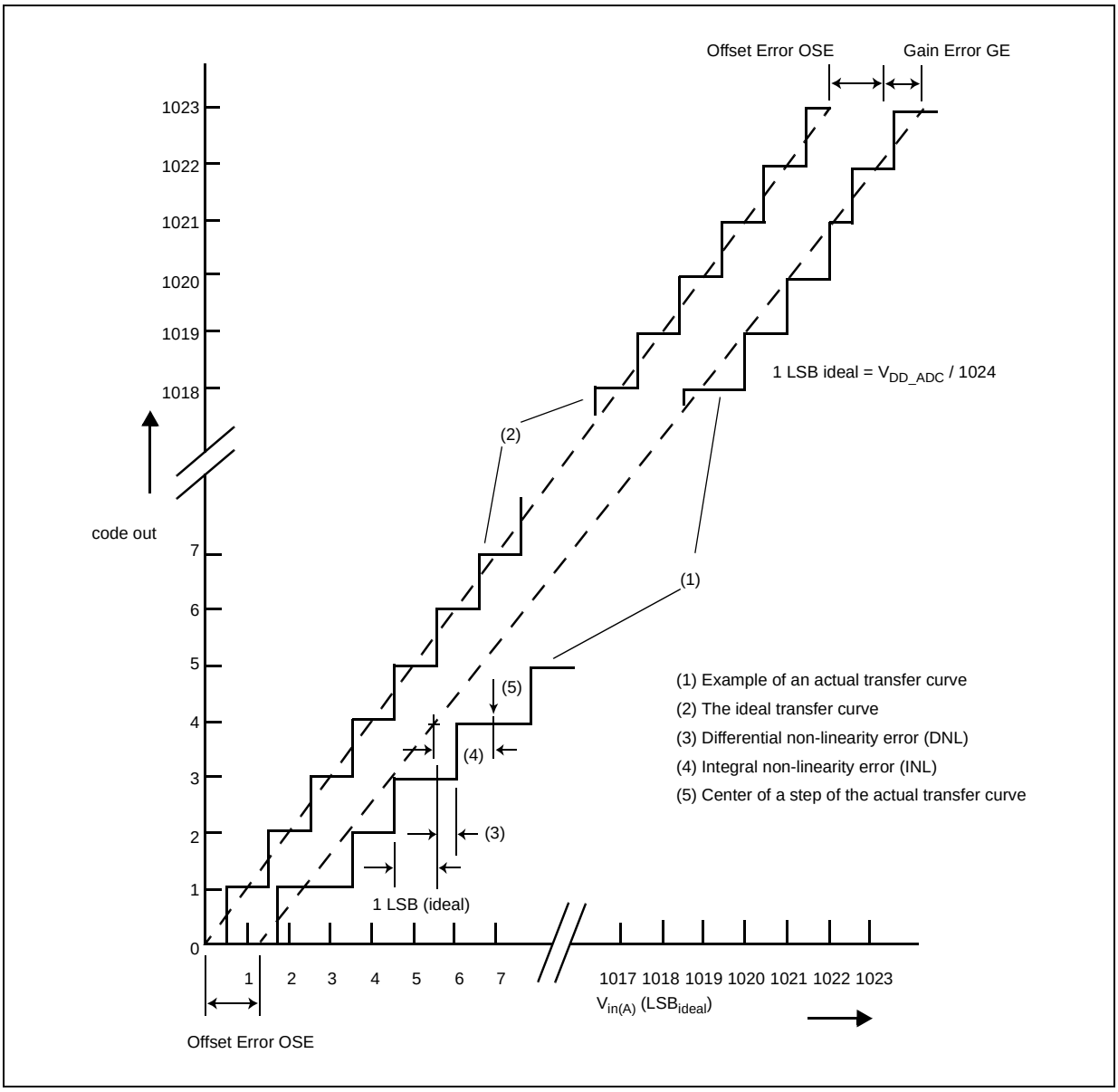


Figure 15. ADC characteristics and error definitions

3.14.1 Input impedance and ADC accuracy

To preserve the accuracy of the A/D converter, it is necessary that analog input pins have low AC impedance. Placing a capacitor with good high frequency characteristics at the input pin of the device can be effective: the capacitor should be as large as possible, ideally infinite. This capacitor contributes to attenuating the noise present on the input pin; further, it sources charge during the sampling phase, when the analog signal source is a high-impedance source.

A real filter can typically be obtained by using a series resistance with a capacitor on the input pin (simple RC filter). The RC filtering may be limited according to the source impedance value of the transducer or circuit supplying the analog signal to be measured.

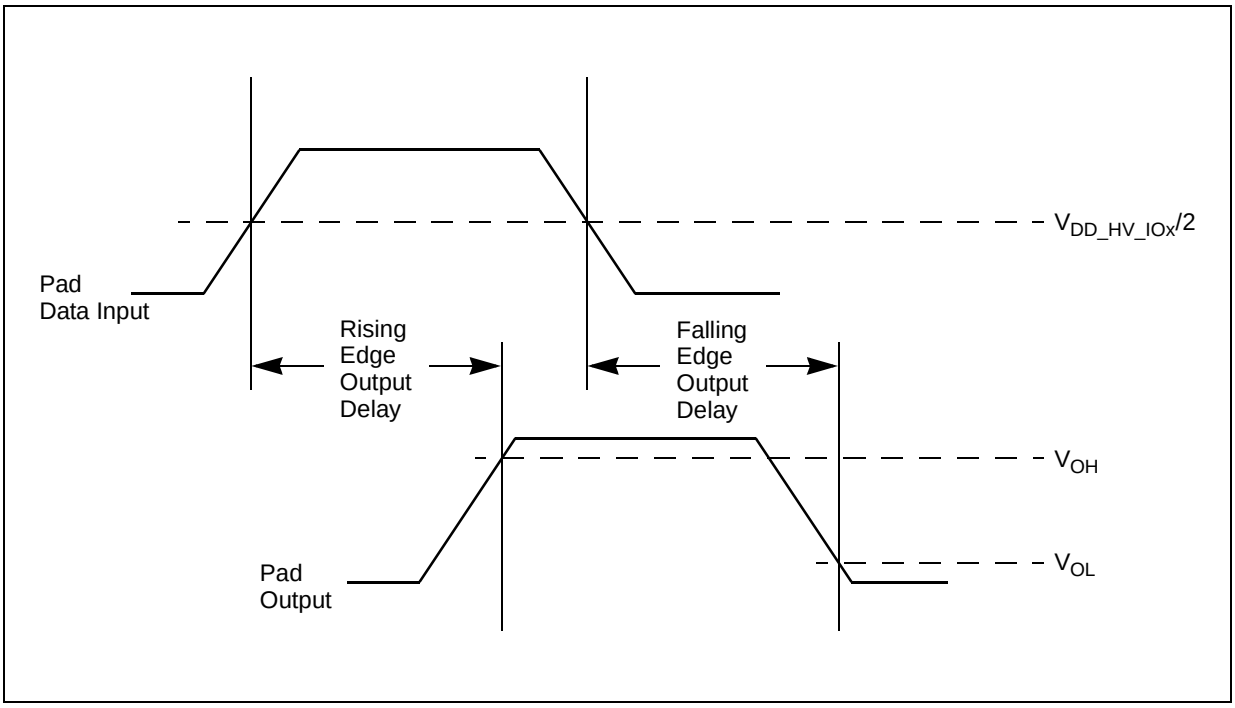


Figure 19. Pad output delay

3.17 AC timing characteristics

3.17.1 $\overline{\text{RESET}}$ pin characteristics

The SPC560P44Lx, SPC560P50Lx implements a dedicated bidirectional $\overline{\text{RESET}}$ pin.

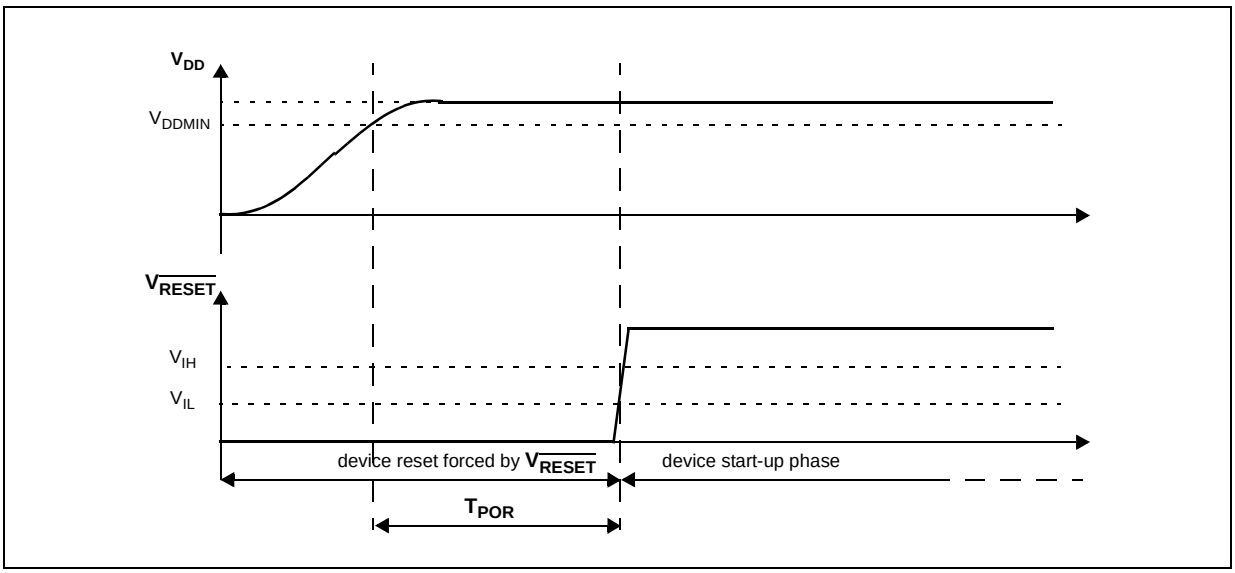


Figure 20. Start-up reset requirements

Table 38. $\overline{\text{RESET}}$ electrical characteristics (continued)

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
t_{tr}	CC	D	Output transition time output pin[3] MEDIUM configuration	C_L = 25pF, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	10	ns
				C_L = 50pF, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	20	
				C_L = 100pF, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	40	
				C_L = 25pF, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	12	
				C_L = 50pF, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	25	
				C_L = 100pF, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	40	
W_{FRST}	SR	P	$\overline{\text{RESET}}$ input filtered pulse	—	—	—	40	ns
W_{NFRST}	SR	P	$\overline{\text{RESET}}$ input not filtered pulse	—	500	—	—	ns
t_{POR}	CC	D	Maximum delay before internal reset is released after all V_{DD_HV} reach nominal supply	Monotonic V_{DD_HV} supply ramp	—	—	1	ms
$\lvert I_{WPU} \rvert$	CC	P	Weak pull-up current absolute value	V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	10	—	150	µA
				V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	10	—	150	
				V_{DD} = 5.0 V ± 10%, PAD3V5V = 1[4]	10	—	250	

1. V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 °C to $T_{A\ MAX}$, unless otherwise specified
2. This is a transient configuration during power-up, up to the end of reset PHASE2 (refer to RGM module section of device reference manual).
3. C_L includes device and package capacitance (C_{PKG} < 5 pF).
4. The configuration PAD3V5 = 1 when V_{DD} = 5 V is only transient configuration during power-up. All pads but RESET and Nexus output (MDOx, EVTO, MCKO) are configured in input or in high impedance state.

3.17.2 IEEE 1149.1 interface timing

Table 39. JTAG pin AC electrical characteristics

No.	Symbol		C	Parameter	Conditions	Value		Unit
						Min	Max	
1	t_{JCYC}	CC	D	TCK cycle time	—	100	—	ns
2	t_{JDC}	CC	D	TCK clock pulse width (measured at $V_{DD\_HV\_IOx}$/2)	—	40	60	ns
3	$t_{TCKRISE}$	CC	D	TCK rise and fall times (40% – 70%)	—	—	3	ns
4	t_{TMSS}, t_{TDIS}	CC	D	TMS, TDI data setup time	—	5	—	ns

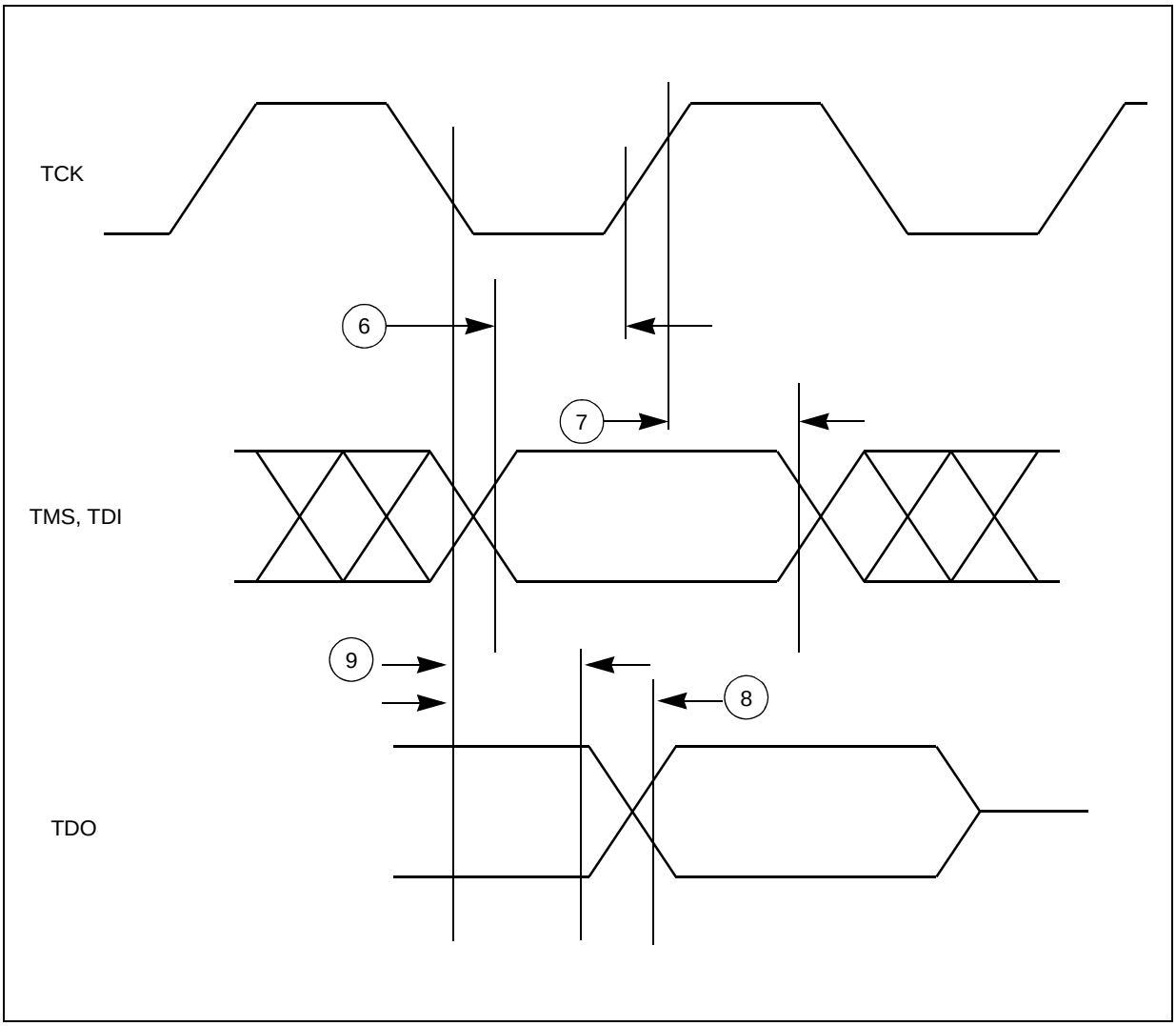


Figure 27. Nexus TDI, TMS, TDO timing

3.17.4 External interrupt timing (IRQ pin)

Table 41. External interrupt timing(1)

No.	Symbol		C	Parameter	Conditions	Value		Unit
						Min	Max	
1	t_{IPWL}	CC	D	IRQ pulse width low	—	4	—	t_{CYC}
2	t_{IPWH}	CC	D	IRQ pulse width high	—	4	—	t_{CYC}
3	t_{ICYC}	CC	D	IRQ edge to edge time(2)	—	4 + N (3)	—	t_{CYC}

1. IRQ timing specified at f_{SYS} = 64 MHz and $V_{DD\_HV\_IOx}$ = 3.0 V to 5.5 V, $T_A = T_L$ to T_H, and C_L = 200 pF with SRC = 0b00.
2. Applies when IRQ pins are configured for rising edge or falling edge events, but not both.
3. N = ISR time to clear the flag

Table 46. Revision history (continued)

Date	Revision	Changes
07-Apr-2011	7 (cont'd)	SPC560P44Lx, SPC560P50Lx device configuration differences: Removed "temperature" row (temperature information is provided in Order codes) Updated SPC560P44Lx, SPC560P50Lx block diagram Added SPC560P44Lx, SPC560P50Lx series block summary Added *Section 1.5 Feature details* *Section 2.1, Package pinouts*: removed alternate functions from pinout diagrams Supply pins: updated descriptions of power supply pins (1.2 V) System pins: updated table Pin muxing: added rows "B[4]" and "B[5] *Section 3.3, Absolute maximum ratings*: added voltage specifications to titles of *Figure 5* and *Figure 6*; in *Table 9*, changed row "V_{SS_HV} / Digital Ground" to "V_{SS} / Device Ground"; updated symbols *Section 3.4, Recommended operating conditions*: added voltage specifications to titles of *Figure 7* and *Figure 8* Recommended operating conditions (5.0 V), and Recommended operating conditions (3.3 V): changed row "V_{SS_HV} / Digital Ground" to "V_{SS} / Device Ground"; updated symbols Updated *Section 3.5.1, Package thermal characteristics* Updated *Section 3.6, Electromagnetic interference (EMI) characteristics* *Section 3.8.1, Voltage regulator electrical characteristics*: amended titles of *Table 16* and *Table 19* Voltage regulator electrical characteristics (configuration without resistor on base) and Voltage regulator electrical characteristics (configuration with resistor on base): updated symbol and values for $V_{DD\_LV\_REGCOR}$ Low voltage monitor electrical characteristics: Updated $V_{MLVDDOK\_H}$ max value—was 1.15 V; is 1.145 V *Section 3.10, DC electrical characteristics*: reorganized contents Updated *Section 3.10.1, NVUSRO register* (includes adding *Section NVUSRO[OSCILLATOR_MARGIN] field description*) Supply current (5.0 V, NVUSRO[PAD3V5V] = 0): updated symbols Corrected parameter descriptions in DC electrical characteristics (3.3 V, NVUSRO[PAD3V5V] = 1): – V_{OL_F}—was "Fast, high level output voltage"; is "Fast, low level output voltage" – V_{OL_SYM}—was "Symmetric, high level output voltage"; is "Symmetric, low level output voltage" Supply current (3.3 V, NVUSRO[PAD3V5V] = 1): updated symbols Main oscillator output electrical characteristics (5.0 V, NVUSRO[PAD3V5V] = 0): replaced instances of EXTAL with XTAL Main oscillator output electrical characteristics (3.3 V, NVUSRO[PAD3V5V] = 1): replaced instances of EXTAL with XTAL FMPLL electrical characteristics: replaced "PLLMRFM" with "FMPLL" in table title; updated conditions; removed f_{sys} row; updated $f_{FMPLLOUT}$ min value ADC conversion characteristics: updated symbols; added row t_{ADC_PU} Flash memory read access timing: added footnote to "Conditions" column *Section 3.16.1, Pad AC specifications*: added Pad output delay diagram In the range of figures "DSPI Classic SPI Timing — Master, CPHA = 0" to "DSPI PCS Strobe (PCSS) Timing": added note Updated Order codes Updated "Commercial product code structure" figure *Table 45*: Added abbreviations "DUT", "NPN", and "RBW"

Table 46. Revision history (continued)

Date	Revision	Changes
18-Jul-2012	8	Updated *Table 1 (Device summary)* *Section 1.5.4, Flash memory*: Changed “Data flash memory: 32-bit ECC” to “Data flash memory: 64-bit ECC” *Figure 40 (Commercial product code structure)*, replaced "C = 60 MHz, 5 V" and "D = 60 MHz, 3.3 V" with respectively "C = 40 MHz, 5 V" and "D = 40 MHz, 3.3 V" *Table 9 (Absolute maximum ratings)*, updated TV_{DD} parameter, the minimum value to 3.0 V/s and the maximum value to 0.5 V/µs *Table 7 (Pin muxing)*, changed the description in the column "I/O direction" from "I/O" to "O" for the following port pins: A[10] with function B[0] A[11] with function A[0] A[11] with function A[2] A[12] with function A[2] A[12] with function B[2] A[13] with function B[2] C[7] with function A[1] C[10] with function A[3] C[15] with function A[1] D[0] with function B[1] D[10] with function A[0] D[11] with function B[0] D[13] with function A[1] D[14] with function B[1] Updated *Section 3.8.1, Voltage regulator electrical characteristics* Added *Table 27 (I/O consumption)* *Section 3.10, DC electrical characteristics*: deleted references to “oscillator margin” deleted subsection “NVUSRO[OSCILLATOR_MARGIN] field description” *Table 21 (DC electrical characteristics (5.0 V, NVUSRO[PAD3V5V] = 0))*, added IPU row for $\overline{\text{RESET}}$ pin *Table 23 (DC electrical characteristics (3.3 V, NVUSRO[PAD3V5V] = 1))*, added IPU row for $\overline{\text{RESET}}$ pin *Table 33 (ADC conversion characteristics)*, added V_{INAN} entry Removed “Order codes” table *Figure 40 (Commercial product code structure)*: added a footnote updated “E = Data flash memory”
18-Sep-2013	9	Updated Disclaimer