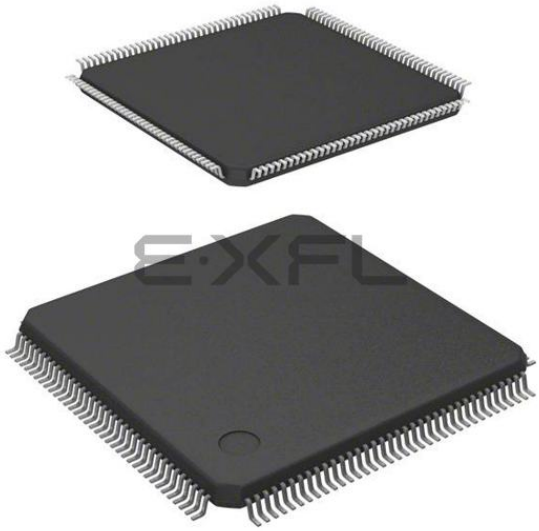

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	e200z0h
Core Size	32-Bit Single-Core
Speed	64MHz
Connectivity	CANbus, LINbus, SPI, UART/USART
Peripherals	DMA, POR, PWM, WDT
Number of I/O	107
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	40K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 26x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/spc560p50l5beaby

List of figures

1 Introduction

1.1 Document overview

This document provides electrical specifications, pin assignments, and package diagrams for the SPC560P44/50 series of microcontroller units (MCUs). It also describes the device features and highlights important electrical and physical characteristics. For functional characteristics, refer to the device reference manual.

1.2 Description

This 32-bit system-on-chip (SoC) automotive microcontroller family is the latest achievement in integrated automotive application controllers. It belongs to an expanding range of automotive-focused products designed to address chassis applications—specifically, electrical hydraulic power steering (EHPS) and electric power steering (EPS)—as well as airbag applications.

This family is one of a series of next-generation integrated automotive microcontrollers based on the Power Architecture technology.

The advanced and cost-efficient host processor core of this automotive controller family complies with the Power Architecture embedded category. It operates at speeds of up to 64 MHz and offers high performance processing optimized for low power consumption. It capitalizes on the available development infrastructure of current Power Architecture devices and is supported with software drivers, operating systems and configuration code to assist with users implementations.

1.3 Device comparison

Table 2 provides a summary of different members of the SPC560P44Lx, SPC560P50Lx family and their features—relative to full-featured version—to enable a comparison among the family members and an understanding of the range of functionality offered within this family.

Table 2. SPC560P44Lx, SPC560P50Lx device comparison

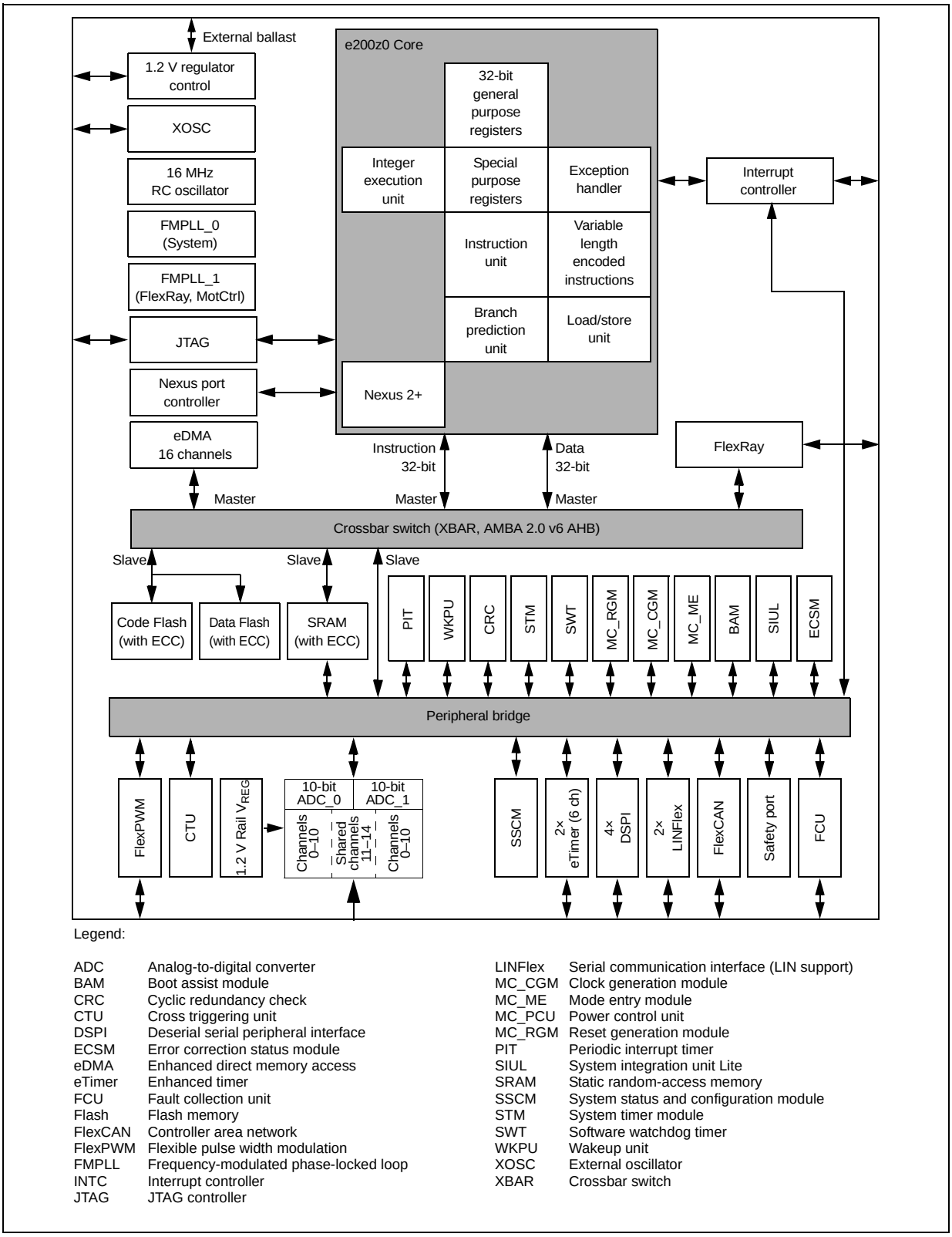
Feature	SPC560P44	SPC560P50
Code flash memory (with ECC)	384 KB	512 KB
Data flash memory / EE option (with ECC)	64 KB	
SRAM (with ECC)	36 KB	40 KB
Processor core	32-bit e200z0h	
Instruction set	VLE (variable length encoding)	
CPU performance	0–64 MHz	
FMPLL (frequency-modulated phase-locked loop) module	2	
INTC (interrupt controller) channels	147	
PIT (periodic interrupt timer)	1 (includes four 32-bit timers)	

Table 3. SPC560P44Lx, SPC560P50Lx device configuration differences (continued)

Feature	Full-featured	Airbag
FlexRay	Yes	No
FMPLL (frequency-modulated phase-locked loop) module	2 (one FMPLL, one for FlexRay)	1 (only FMPLL)

1.4 Block diagram

Figure 1 shows a top-level block diagram of the SPC560P44Lx, SPC560P50Lx MCU.



Legend:

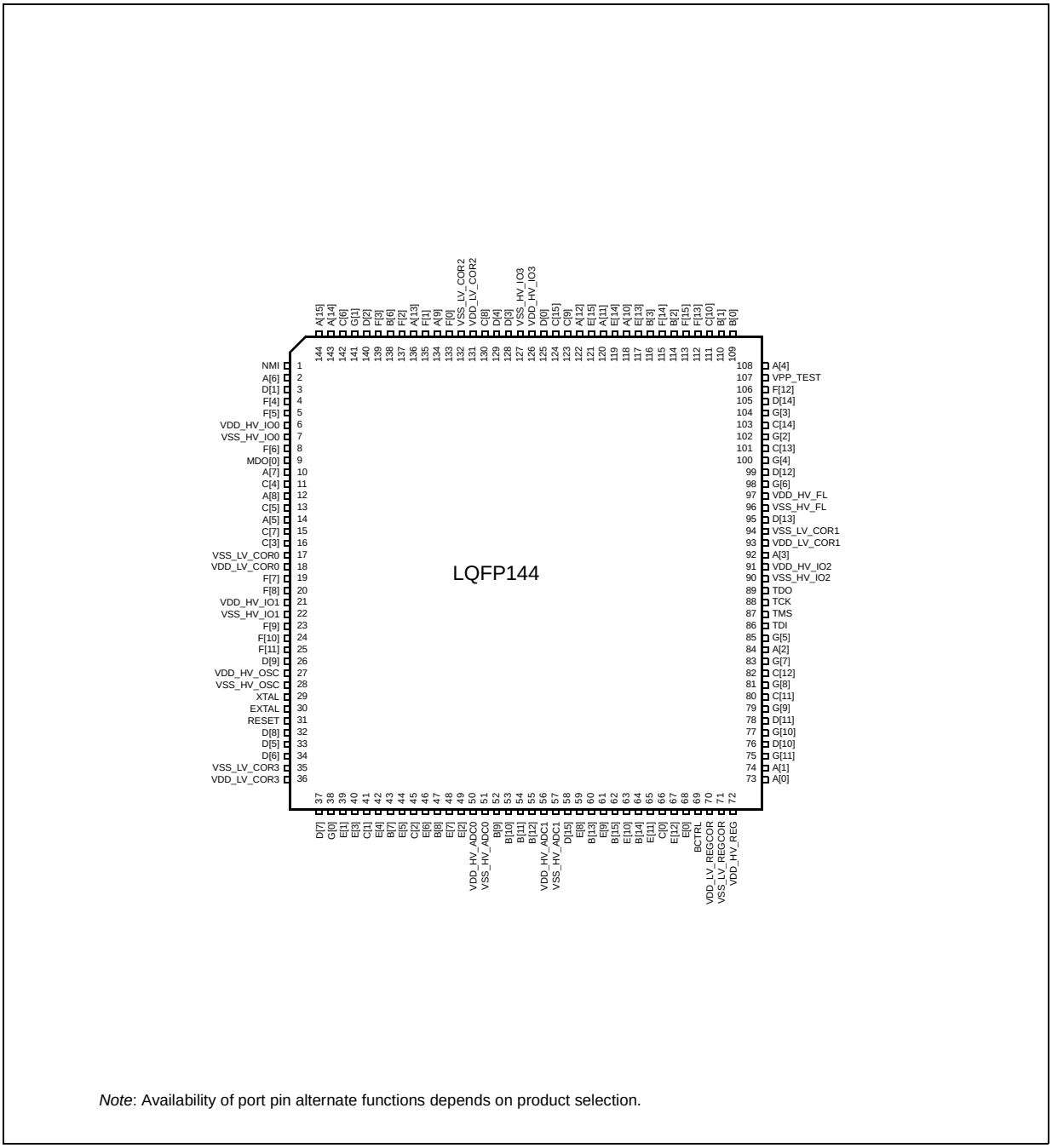
ADC	Analog-to-digital converter
BAM	Boot assist module
CRC	Cyclic redundancy check
CTU	Cross triggering unit
DSPI	Deserial serial peripheral interface
ECSM	Error correction status module
eDMA	Enhanced direct memory access
eTimer	Enhanced timer
FCU	Fault collection unit
Flash	Flash memory
FlexCAN	Controller area network
FlexPWM	Flexible pulse width modulation
FMPLL	Frequency-modulated phase-locked loop
INTC	Interrupt controller
JTAG	JTAG controller
LINFlex	Serial communication interface (LIN support)
MC_CGM	Clock generation module
MC_ME	Mode entry module
MC_PCU	Power control unit
MC_RGM	Reset generation module
PIT	Periodic interrupt timer
SIUL	System integration unit Lite
SRAM	Static random-access memory
SSCM	System status and configuration module
STM	System timer module
SWT	Software watchdog timer
WKPU	Wakeup unit
XOSC	External oscillator
XBAR	Crossbar switch

Figure 1. SPC560P44Lx, SPC560P50Lx block diagram

2 Package pinouts and signal descriptions

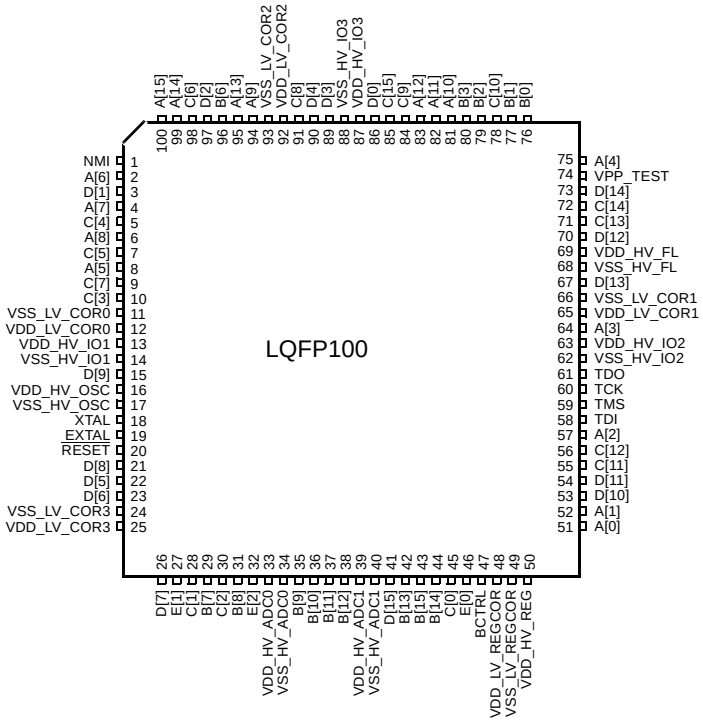
2.1 Package pinouts

The LQFP pinouts are shown in the following figures.



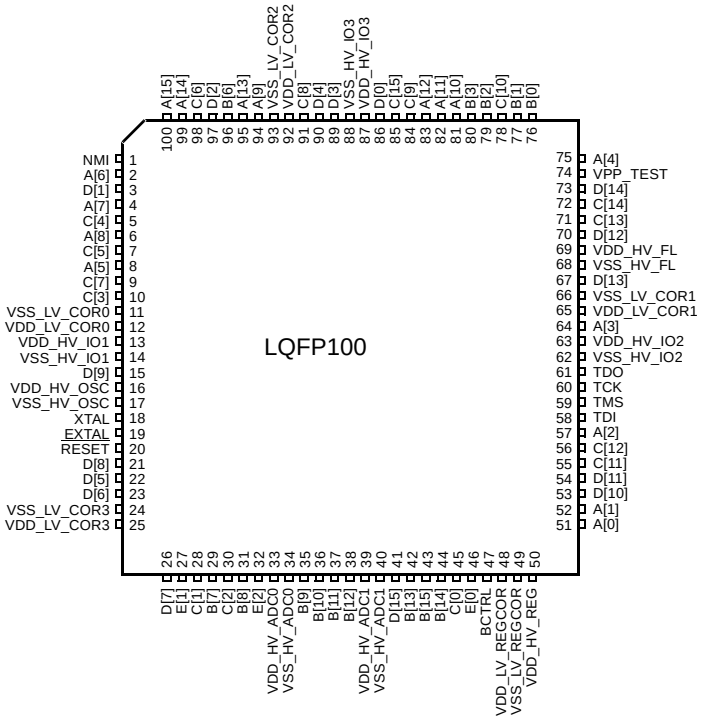
Note: Availability of port pin alternate functions depends on product selection.

Figure 2. 144-pin LQFP pinout – Full featured configuration (top view)



Note: Availability of port pin alternate functions depends on product selection.

Figure 3. 100-pin LQFP pinout – Airbag configuration (top view)



Note: Availability of port pin alternate functions depends on product selection.

Figure 4. 100-pin LQFP pinout – Full featured configuration (top view)

2.2 Pin description

The following sections provide signal descriptions and related information about the functionality and configuration of the SPC560P44Lx, SPC560P50Lx devices.

2.2.1 Power supply and reference voltage pins

Table 5 lists the power supply and reference voltage for the SPC560P44Lx, SPC560P50Lx devices.

Table 5. Supply pins

Supply		Pin	
Symbol	**Description**	**100-pin**	**144-pin**
VREG control and power supply pins. Pins available on 100-pin and 144-pin package.			
BCTRL	Voltage regulator external NPN ballast base control pin	47	69
$V_{DD\_HV\_REG}$ (3.3 V or 5.0 V)	Voltage regulator supply voltage	50	72
$V_{DD\_LV\_REGCOR}$	1.2 V decoupling pins for core logic and regulator feedback. Decoupling capacitor must be connected between this pins and $V_{SS\_LV\_REGCOR}$.	48	70
$V_{SS\_LV\_REGCOR}$	1.2 V decoupling pins for core logic and regulator feedback. Decoupling capacitor must be connected between this pins and $V_{DD\_LV\_REGCOR}$.	49	71
ADC_0/ADC_1 reference and supply voltage. Pins available on 100-pin and 144-pin package.			
$V_{DD\_HV\_ADC0}$ (1)	ADC_0 supply and high reference voltage	33	50
$V_{SS\_HV\_ADC0}$	ADC_0 ground and low reference voltage	34	51
$V_{DD\_HV\_ADC1}$	ADC_1 supply and high reference voltage	39	56
$V_{SS\_HV\_ADC1}$	ADC_1 ground and low reference voltage	40	57
Power supply pins (3.3 V or 5.0 V). All pins available on 144-pin package. Five pairs (V_{DD}; V_{SS}) available on 100-pin package.			
$V_{DD\_HV\_IO0}$ (2)	Input/Output supply voltage	—	6
$V_{SS\_HV\_IO0}$ (2)	Input/Output ground	—	7
$V_{DD\_HV\_IO1}$	Input/Output supply voltage	13	21
$V_{SS\_HV\_IO1}$	Input/Output ground	14	22
$V_{DD\_HV\_IO2}$	Input/Output supply voltage	63	91
$V_{SS\_HV\_IO2}$	Input/Output ground	62	90
$V_{DD\_HV\_IO3}$	Input/Output supply voltage	87	126
$V_{SS\_HV\_IO3}$	Input/Output ground	88	127
$V_{DD\_HV\_FL}$	Code and data flash supply voltage	69	97
$V_{SS\_HV\_FL}$	Code and data flash supply ground	68	96
$V_{DD\_HV\_OSC}$	Crystal oscillator amplifier supply voltage	16	27
$V_{SS\_HV\_OSC}$	Crystal oscillator amplifier ground	17	28
Power supply pins (1.2 V). All pins available on 100-pin and 144-pin package.			
$V_{DD\_LV\_COR0}$	1.2 V Decoupling pins for core logic. Decoupling capacitor must be connected between these pins and the nearest $V_{SS\_LV\_COR}$ pin.	12	18
$V_{SS\_LV\_COR0}$	1.2 V Decoupling pins for core logic. Decoupling capacitor must be connected between these pins and the nearest $V_{DD\_LV\_COR}$ pin.	11	17

Table 7. Pin muxing (continued)

Port pin	Pad configuration register (PCR)	Alternate function[1], [2]	Functions	Peripheral[3]	I/O direction [4]	Pad speed[5]		Pin No.	
						SRC = 0	SRC = 1	100-pin	144-pin
D[14]	PCR[62]	ALT0 ALT1 ALT2 ALT3 —	GPIO[62] B[1] CS3 — SIN	SIUL FlexPWM_0 DSPI_3 — DSPI_3	I/O O O — I	Slow	Medium	73	105
D[15]	PCR[63]	ALT0 ALT1 ALT2 ALT3 —	GPIO[63] — — — AN[4]	SIUL — — — ADC_1	Input only	—	—	41	58
Port E(16-bit)									
E[0]	PCR[64]	ALT0 ALT1 ALT2 ALT3 —	GPIO[64] — — — AN[5]	SIUL — — — ADC_1	Input only	—	—	46	68
E[1]	PCR[65]	ALT0 ALT1 ALT2 ALT3 —	GPIO[65] — — — AN[4]	SIUL — — — ADC_0	Input only	—	—	27	39
E[2]	PCR[66]	ALT0 ALT1 ALT2 ALT3 —	GPIO[66] — — — AN[5]	SIUL — — — ADC_0	Input only	—	—	32	49
E[3]	PCR[67]	ALT0 ALT1 ALT2 ALT3 —	GPIO[67] — — — AN[6]	SIUL — — — ADC_0	Input only	—	—	—	40
E[4]	PCR[68]	ALT0 ALT1 ALT2 ALT3 —	GPIO[68] — — — AN[7]	SIUL — — — ADC_0	Input only	—	—	—	42

3. The difference between ADC voltage supplies must be less than 100 mV, $|V_{DD\_HV\_ADC1} - V_{DD\_HV\_ADC0}| < 100$ mV.
4. To be connected to emitter of external NPN. Low voltage supplies are not under user control—they are produced by an on-chip voltage regulator—but for the device to function properly the low voltage grounds ($V_{SS\_LV\_xxx}$) must be shorted to high voltage grounds ($V_{SS\_HV\_xxx}$) and the low voltage supply pins ($V_{DD\_LV\_xxx}$) must be connected to the external ballast emitter.
5. The low voltage supplies ($V_{DD\_LV\_xxx}$) are not all independent.

$V_{DD\_LV\_COR1}$ and $V_{DD\_LV\_COR2}$ are shorted internally via double bonding connections with lines that provide the low voltage supply to the data flash module. Similarly, $V_{SS\_LV\_COR1}$ and $V_{SS\_LV\_COR2}$ are internally shorted.

$V_{DD\_LV\_REGCOR}$ and $V_{DD\_LV\_REGCORx}$ are physically shorted internally, as are $V_{SS\_LV\_REGCOR}$ and $V_{SS\_LV\_CORx}$.

Table 11. Recommended operating conditions (3.3 V)

Symbol		Parameter	Conditions	Value		Unit
				Min	Max(1)	
V_{SS}	SR	Device ground	—	0	0	V
$V_{DD\_HV\_IOx}$(2)	SR	3.3 V input/output supply voltage	—	3.0	3.6	V
$V_{SS\_HV\_IOx}$	SR	Input/output ground voltage	—	0	0	V
$V_{DD\_HV\_FL}$	SR	3.3 V code and data flash supply voltage	—	3.0	3.6	V
			Relative to $V_{DD\_HV\_IOx}$	$V_{DD\_HV\_IOx} - 0.1$	$V_{DD\_HV\_IOx} + 0.1$	
$V_{SS\_HV\_FL}$	SR	Code and data flash ground	—	0	0	V
$V_{DD\_HV\_OSC}$	SR	3.3 V crystal oscillator amplifier supply voltage	—	3.0	3.6	V
			Relative to $V_{DD\_HV\_IOx}$	$V_{DD\_HV\_IOx} - 0.1$	$V_{DD\_HV\_IOx} + 0.1$	
$V_{SS\_HV\_OSC}$	SR	3.3 V crystal oscillator amplifier reference voltage	—	0	0	V
$V_{DD\_HV\_REG}$	SR	3.3 V voltage regulator supply voltage	—	3.0	3.6	V
			Relative to $V_{DD\_HV\_IOx}$	$V_{DD\_HV\_IOx} - 0.1$	$V_{DD\_HV\_IOx} + 0.1$	
$V_{DD\_HV\_ADC0}$(3)	SR	3.3 V ADC_0 supply and high reference voltage	—	3.0	5.5	V
			Relative to $V_{DD\_HV\_REG}$	$V_{DD\_HV\_REG} - 0.1$	5.5	
$V_{SS\_HV\_ADC0}$	SR	ADC_0 ground and low reference voltage	—	0	0	V
$V_{DD\_HV\_ADC1}$(3)	SR	3.3 V ADC_1 supply and high reference voltage	—	3.0	5.5	V
			Relative to $V_{DD\_HV\_REG}$	$V_{DD\_HV\_REG} - 0.1$	5.5	
$V_{SS\_HV\_ADC1}$	SR	ADC_1 ground and low reference voltage	—	0	0	V
$V_{DD\_LV\_REGCOR}$(4),(5)	CC	Internal supply voltage	—	—	—	V
$V_{SS\_LV\_REGCOR}$(4)	SR	Internal reference voltage	—	0	0	V
$V_{DD\_LV\_CORx}$(4),(5)	CC	Internal supply voltage	—	—	—	V

3.8.2 Voltage monitor electrical characteristics

The device implements a Power-on Reset module to ensure correct power-up initialization, as well as three low voltage detectors to monitor the V_{DD} and the V_{DD_LV} voltage while device is supplied:

- POR monitors V_{DD} during the power-up phase to ensure device is maintained in a safe reset state
- LVDHV3 monitors V_{DD} to ensure device reset below minimum functional supply
- LVDHV5 monitors V_{DD} when application uses device in the 5.0 V ± 10 % range
- LVDLVCOR monitors low voltage digital power domain

Table 19. Low voltage monitor electrical characteristics

Symbol	C	Parameter	Conditions (1)	Value		Unit
				Min	Max	
V_{PORH}	T	Power-on reset threshold	—	1.5	2.7	V
V_{PORUP}	P	Supply for functional POR module	T_A = 25 °C	1.0	—	V
$V_{REGLVDMOK\_H}$	P	Regulator low voltage detector high threshold	—	—	2.95	V
$V_{REGLVDMOK\_L}$	P	Regulator low voltage detector low threshold	—	2.6	—	V
$V_{FLLVDMOK\_H}$	P	Flash low voltage detector high threshold	—	—	2.95	V
$V_{FLLVDMOK\_L}$	P	Flash low voltage detector low threshold	—	2.6	—	V
$V_{IOLVDMOK\_H}$	P	I/O low voltage detector high threshold	—	—	2.95	V
$V_{IOLVDMOK\_L}$	P	I/O low voltage detector low threshold	—	2.6	—	V
$V_{IOLVDM5OK\_H}$	P	I/O 5V low voltage detector high threshold	—	—	4.4	V
$V_{IOLVDM5OK\_L}$	P	I/O 5V low voltage detector low threshold	—	3.8	—	V
$V_{MLVDDOK\_H}$	P	Digital supply low voltage detector high	—	—	1.145	V
$V_{MLVDDOK\_L}$	P	Digital supply low voltage detector low	—	1.08	—	V

1. V_{DD} = 3.3V ± 10% / 5.0V ± 10%, T_A = –40 °C to $T_{A\ MAX}$, unless otherwise specified

3.9 Power up/down sequencing

To prevent an overstress event or a malfunction within and outside the device, the SPC560P44Lx, SPC560P50Lx implements the following sequence to ensure each module is started only when all conditions for switching it ON are available:

- A POWER_ON module working on voltage regulator supply controls the correct start-up of the regulator. This is a key module ensuring safe configuration for all voltage regulator functionality when supply is below 1.5V. Associated POWER_ON (or POR) signal is active low.
- Several low voltage detectors, working on voltage regulator supply monitor the voltage of the critical modules (voltage regulator, I/Os, flash memory and low voltage domain). LVDs are gated low when POWER_ON is active.
- A POWER_OK signal is generated when all critical supplies monitored by the LVD are available. This signal is active high and released to all modules including I/Os, flash

Table 26. I/O weight (continued)

Pad	LQFP144		LQFP100	
	Weight 5V	Weight 3.3V	Weight 5V	Weight 3.3V
PAD[27]	1%	1%	1%	1%
PAD[28]	1%	1%	1%	1%
PAD[63]	1%	1%	1%	1%
PAD[72]	1%	1%	—	—
PAD[29]	1%	1%	1%	1%
PAD[73]	1%	1%	—	—
PAD[31]	1%	1%	1%	1%
PAD[74]	1%	1%	—	—
PAD[30]	1%	1%	1%	1%
PAD[75]	1%	1%	—	—
PAD[32]	1%	1%	1%	1%
PAD[76]	1%	1%	—	—
PAD[64]	1%	1%	1%	1%
PAD[0]	23%	20%	23%	20%
PAD[1]	21%	18%	21%	18%
PAD[107]	20%	17%	—	—
PAD[58]	19%	16%	19%	16%
PAD[106]	18%	16%	—	—
PAD[59]	17%	15%	17%	15%
PAD[105]	16%	14%	—	—
PAD[43]	15%	13%	15%	13%
PAD[104]	14%	13%	—	—
PAD[44]	13%	12%	13%	12%
PAD[103]	12%	11%	—	—
PAD[2]	11%	10%	11%	10%
PAD[101]	11%	9%	—	—
PAD[21]	10%	8%	10%	8%
TMS	1%	1%	1%	1%
TCK	1%	1%	1%	1%
PAD[20]	16%	11%	16%	11%
PAD[3]	4%	3%	4%	3%
PAD[61]	9%	8%	9%	8%
PAD[102]	11%	10%	—	—

Table 29. Main oscillator output electrical characteristics (3.3 V, NVUSRO[PAD3V5V] = 1)

Symbol		C	Parameter	Value		Unit
				Min	Max	
f_{OSC}	SR	—	Oscillator frequency	4	40	MHz
g_m	—	P	Transconductance	4	20	mA/V
V_{OSC}	—	T	Oscillation amplitude on XTAL pin	1	—	V
t_{OSCSU}	—	T	Start-up time(1),(2)	8	—	ms

1. The start-up time is dependent upon crystal characteristics, board leakage, etc., high ESR and excessive capacitive loads can cause long start-up time.
2. Value captured when amplitude reaches 90% of XTAL

Table 30. Input clock characteristics

Symbol		Parameter	Value			Unit
			Min	Typ	Max	
f_{OSC}	SR	Oscillator frequency	4	—	40	MHz
f_{CLK}	SR	Frequency in bypass	—	—	64	MHz
t_{rCLK}	SR	Rise/fall time in bypass	—	—	1	ns
t_{DC}	SR	Duty cycle	47.5	50	52.5	%

3.12 FMPLL electrical characteristics

Table 31. FMPLL electrical characteristics

Symbol	C	Parameter	Conditions(1)	Value		Unit
				Min	Max	
$f_{ref\_crystal}$ f_{ref_ext}	D	PLL reference frequency range(2)	Crystal reference	4	40	MHz
f_{PLLIN}	D	Phase detector input frequency range (after pre-divider)	—	4	16	MHz
$f_{FMPLLOUT}$	D	Clock frequency range in normal mode	—	16	120	MHz
f_{FREE}	P	Free-running frequency	Measured using clock division — typically /16	20	150	MHz
t_{CYC}	D	System clock period	—	—	1 / f_{SYS}	ns
f_{LORL} f_{LORH}	D	Loss of reference frequency window(3)	Lower limit	1.6	3.7	MHz
			Upper limit	24	56	
f_{SCM}	D	Self-clocked mode frequency(4),(5)	—	20	150	MHz

3.15 Flash memory electrical characteristics

Table 34. Program and erase specifications

Symbol	C	Parameter	Value				Unit
			Min	Typical(1)	Initial max(2)	Max(3)	
$T_{dwprogram}$	P	Double Word (64 bits) Program Time(4)	—	22	50	500	µs
T_{BKPRG}	P	Bank Program (512 KB)(4)(5)	—	1.45	1.65	33	s
	P	Bank Program (64 KB)(4)(5)	—	0.18	0.21	4.10	s
$T_{16kpperase}$	P	16 KB Block Pre-program and Erase Time	—	300	500	5000	ms
$T_{32kpperase}$	P	32 KB Block Pre-program and Erase Time	—	400	600	5000	ms
$T_{128kpperase}$	P	128 KB Block Pre-program and Erase Time	—	800	1300	7500	ms

1. Typical program and erase times assume nominal supply values and operation at 25 °C. All times are subject to change pending device characterization.
2. Initial factory condition: < 100 program/erase cycles, 25 °C, typical supply voltage.
3. The maximum program and erase times occur after the specified number of program/erase cycles. These maximum values are characterized but not guaranteed.
4. Actual hardware programming times. This does not include software overhead.
5. Typical Bank programming time assumes that all cells are programmed in a single pulse. In reality some cells will require more than one pulse, adding a small overhead to total bank programming time (see Initial Max column).

Table 35. Flash memory module life

Symbol	C	Parameter	Conditions	Value		Unit
				Min	Typ	
P/E	C	Number of program/erase cycles per block for 16 KB blocks over the operating temperature range (T_J)	—	100000	—	cycles
P/E	C	Number of program/erase cycles per block for 32 KB blocks over the operating temperature range (T_J)	—	10000	100000	cycles
P/E	C	Number of program/erase cycles per block for 128 KB blocks over the operating temperature range (T_J)	—	1000	100000	cycles
Retention	C	Minimum data retention at 85 °C average ambient temperature(1)	Blocks with 0–1000 P/E cycles	20	—	years
			Blocks with 10000 P/E cycles	10	—	years
			Blocks with 100000 P/E cycles	5	—	years

1. Ambient temperature averaged over duration of application, not to exceed recommended product operating temperature range.

Table 36. Flash memory read access timing

Symbol	C	Parameter	Conditions(1)	Max value	Unit
f_{max}	C	Maximum working frequency at given number of wait states in worst conditions	2 wait states	66	MHz
			0 wait states	18	

1. V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified

3.16 AC specifications

3.16.1 Pad AC specifications

Table 37. Output pin transition times

Symbol		C	Parameter	Conditions(1)		Value			Unit
						Min	Typ	Max	
t_{tr}	CC	D	Output transition time output pin(2) SLOW configuration	C_L = 25 pF	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	50	ns
		T		C_L = 50 pF		—	—	100	
		D		C_L = 100 pF		—	—	125	
		D		C_L = 25 pF	V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	40	
		T		C_L = 50 pF		—	—	50	
		D		C_L = 100 pF		—	—	75	
t_{tr}	CC	D	Output transition time output pin(2) MEDIUM configuration	C_L = 25 pF	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0 SIUL.PCRx.SRC = 1	—	—	10	ns
		T		C_L = 50 pF		—	—	20	
		D		C_L = 100 pF		—	—	40	
		D		C_L = 25 pF	V_{DD} = 3.3 V ± 10%, PAD3V5V = 1 SIUL.PCRx.SRC = 1	—	—	12	
		T		C_L = 50 pF		—	—	25	
		D		C_L = 100 pF		—	—	40	
t_{tr}	CC	D	Output transition time output pin(2) FAST configuration	C_L = 25 pF	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0 SIUL.PCRx.SRC = 1	—	—	4	ns
				C_L = 50 pF		—	—	6	
				C_L = 100 pF		—	—	12	
				C_L = 25 pF	V_{DD} = 3.3 V ± 10%, PAD3V5V = 1 SIUL.PCRx.SRC = 1	—	—	4	
				C_L = 50 pF		—	—	7	
				C_L = 100 pF		—	—	12	
t_{SYM}(3)	CC	T	Symmetric transition time, same drive strength between N and P transistor	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0		—	—	4	ns
				V_{DD} = 3.3 V ± 10%, PAD3V5V = 1		—	—	5	

1. V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 °C to $T_{A\ MAX}$, unless otherwise specified
2. C_L includes device and package capacitances (C_{PKG} < 5 pF).
3. Transition timing of both positive and negative slopes will differ maximum 50%

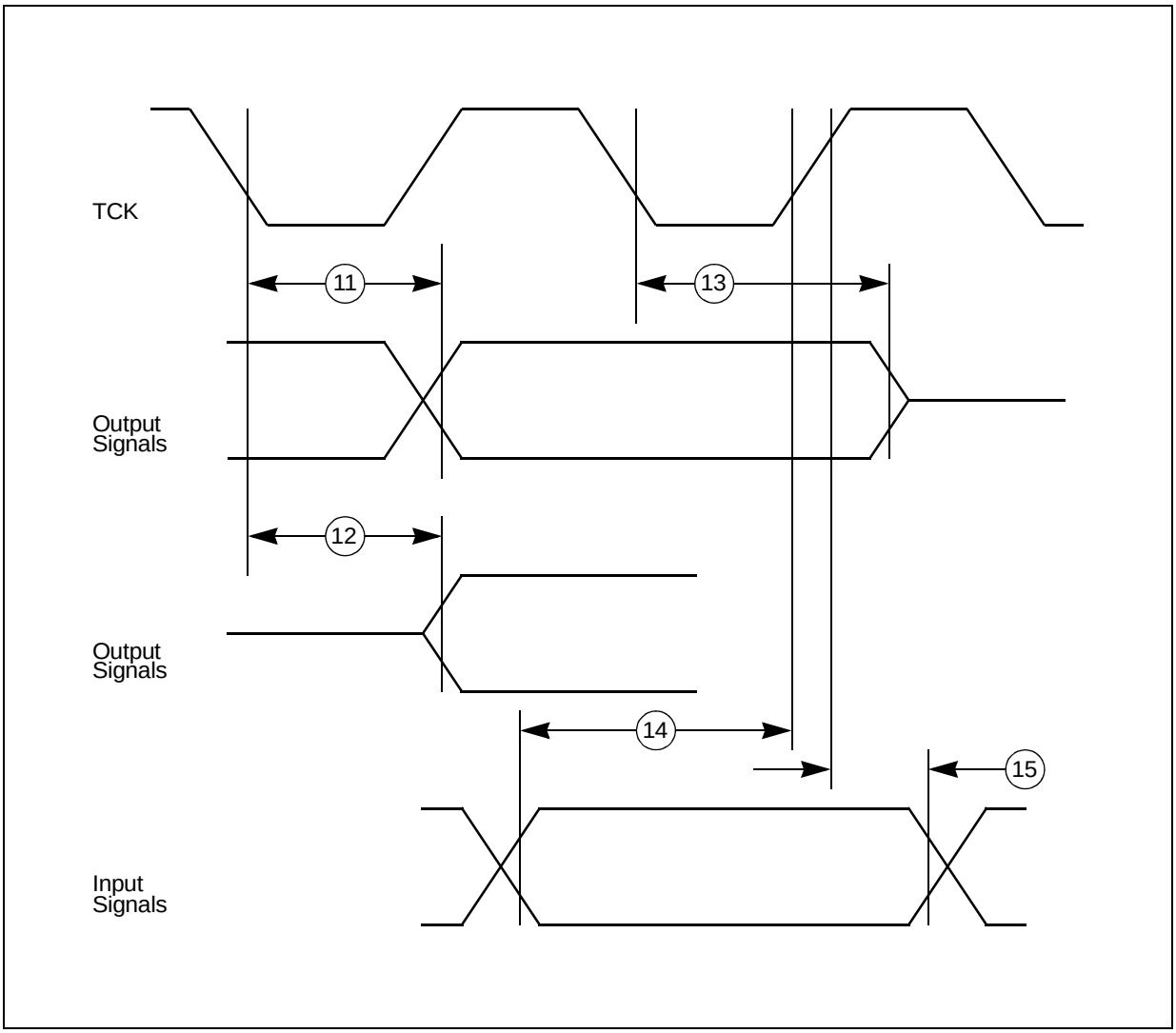


Figure 24. JTAG boundary scan timing

3.17.3 Nexus timing

Table 40. Nexus debug port timing(1)

No.	Symbol		C	Parameter	Value			Unit
					Min	Typ	Max	
1	t_{MCYC}	CC	D	MCKO cycle time	32	—	—	ns
2	t_{MDOV}	CC	D	MCKO low to MDO data valid(2)	—	—	6	ns
3	t_{MSEOV}	CC	D	MCKO low to $\overline{\text{MSEO}}$ data valid(2)	—	—	6	ns
4	t_{EVTOV}	CC	D	MCKO low to $\overline{\text{EVTO}}$ data valid(2)	—	—	6	ns
5	t_{TCYC}	CC	D	TCK cycle time	64(3)	—	—	ns

Table 40. Nexus debug port timing(1) (continued)

No.	Symbol		C	Parameter	Value			Unit
					Min	Typ	Max	
6	t_{NTDIS}	CC	D	TDI data setup time	6	—	—	ns
	t_{NTMSS}	CC	D	TMS data setup time	6	—	—	ns
7	t_{NTDIH}	CC	D	TDI data hold time	10	—	—	ns
	t_{NTMSH}	CC	D	TMS data hold time	10	—	—	ns
8	t_{TDOV}	CC	D	TCK low to TDO data valid	—	—	35	ns
9	t_{TDOI}	CC	D	TCK low to TDO data invalid	6	—	—	ns

1. All Nexus timing relative to MCKO is measured from 50% of MCKO and 50% of the respective signal.
2. MDO, $\overline{\text{MSEO}}$, and $\overline{\text{EVTO}}$ data is held valid until next MCKO low cycle.
3. Lower frequency is required to be fully compliant to standard.

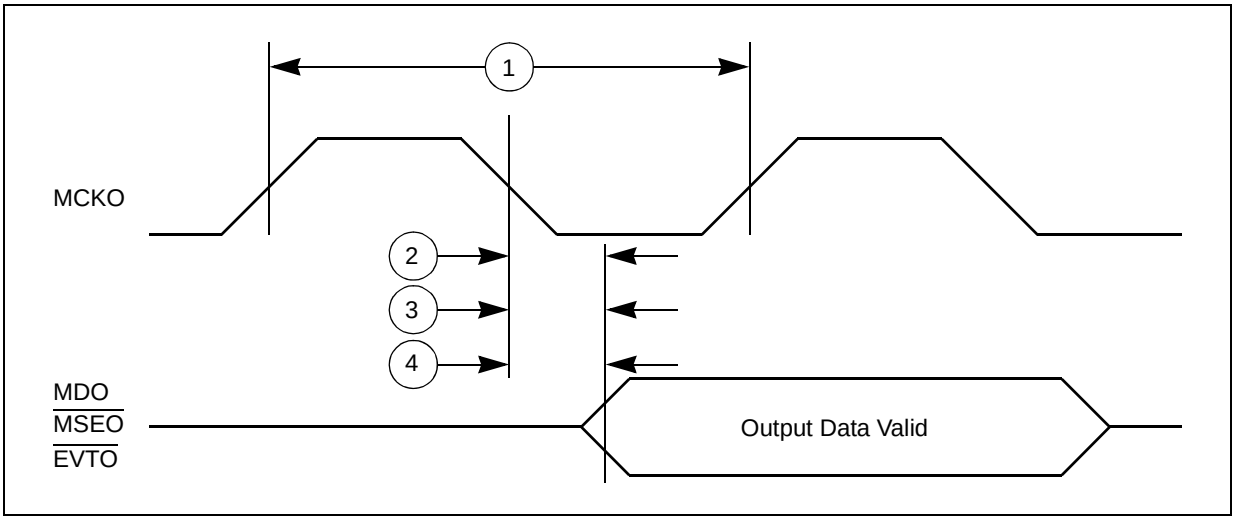


Figure 25. Nexus output timing

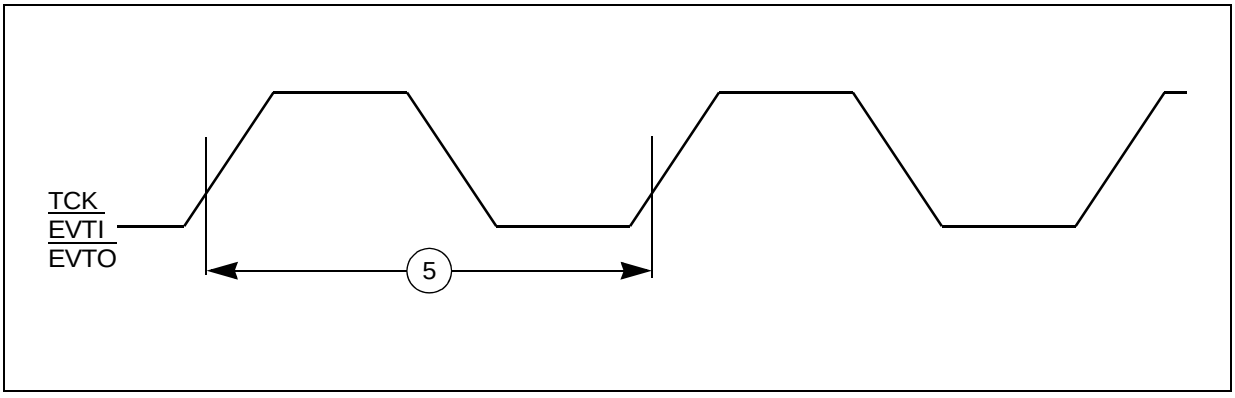
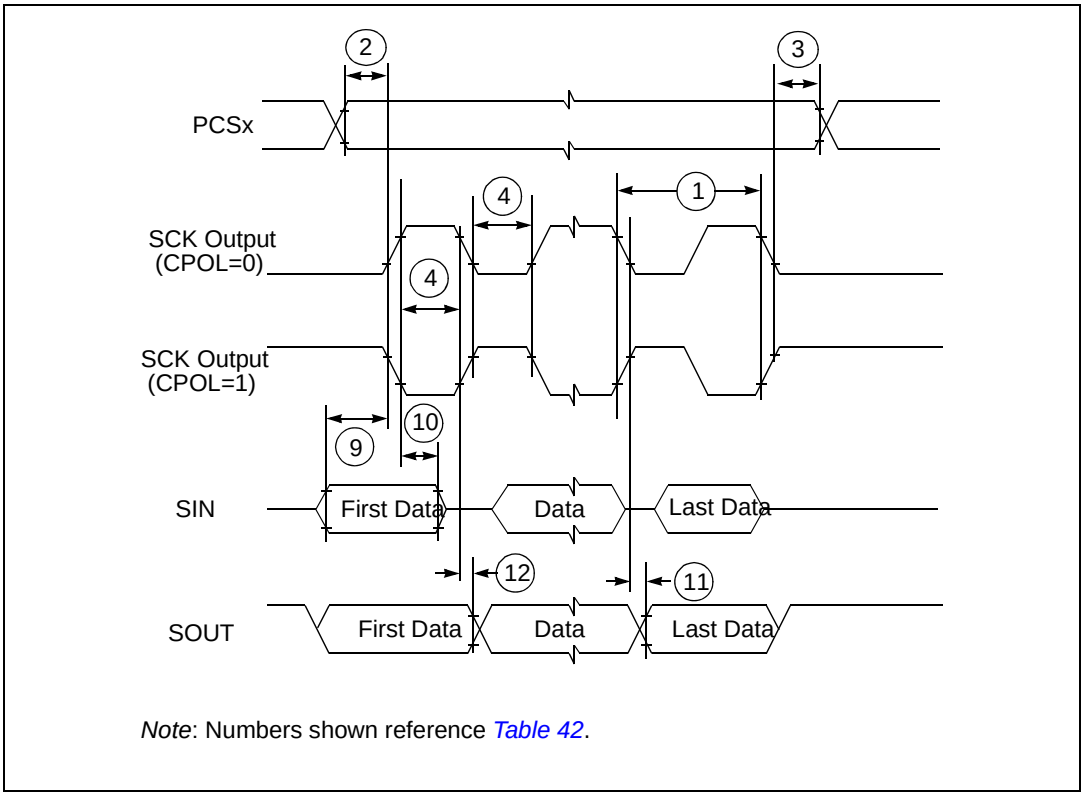


Figure 26. Nexus event trigger and test clock timings

Table 42. DSPI timing(1) (continued)

No.	Symbol		C	Parameter	Conditions	Value		Unit
						Min	Max	
11	t_{SUO}	CC	D	Data valid (after SCK edge)	Master (MTFE = 0)	—	12	ns
					Slave	—	36	
					Master (MTFE = 1, CPHA = 0)	—	12	
					Master (MTFE = 1, CPHA = 1)	—	12	
12	t_{HO}	CC	D	Data hold time for outputs	Master (MTFE = 0)	–2	—	ns
					Slave	6	—	
					Master (MTFE = 1, CPHA = 0)	6	—	
					Master (MTFE = 1, CPHA = 1)	–2	—	

1. All timing is provided with 50 pF capacitance on output, 1 ns transition time on input signal.



Note: Numbers shown reference *Table 42*.

Figure 29. DSPI classic SPI timing – Master, CPHA = 0

5 Ordering information

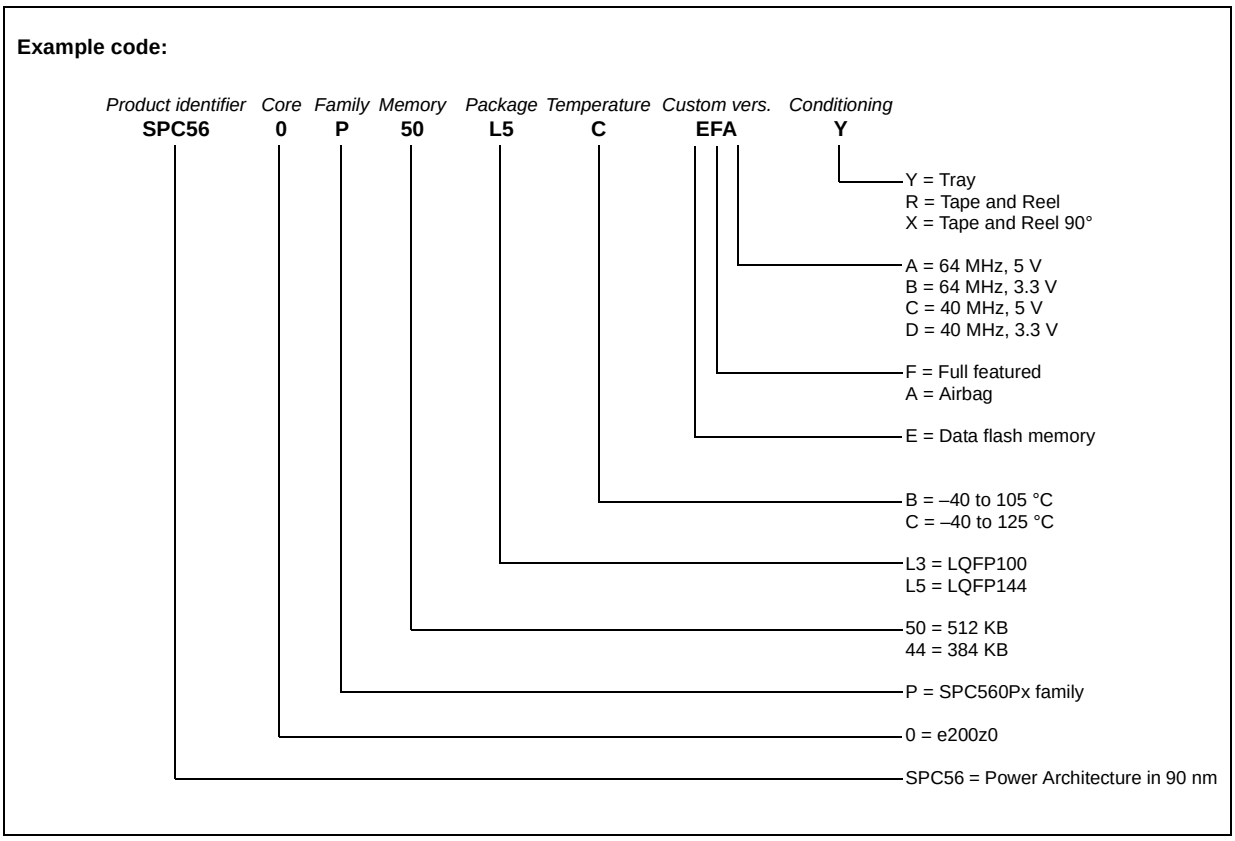


Figure 40. Commercial product code structure[(a)]

a. Not all configurations are available on the market. Please contact your ST sales representative to get the list of orderable commercial part number.

6 Revision history

Table 46 summarizes revisions to this document.

Table 46. Revision history

Date	Revision	Changes
28-Aug-2008	1	Initial release
25-Nov-2008	2	*Table 7*: TDO and TDI pins (Port pins B[4:5] are single function pins. *Table 12*, *Table 13*: Thermal characteristics added. *Table 11*, *Table 12*: EMI testing specifications split into separate tables for Normal mode and Airbag mode; data to be added in a later revision. *Table 16*, *Table 17*, *Table 19*, *Table 20*: Supply current specifications split into separate tables for Normal mode and Airbag mode; data to be added in a later revision. *Table 23*: ● Values for I_{OL} and I_{OH} (in Conditions column) changed. ● Max values for V_{OH_S}, V_{OH_M}, V_{OH_F} and V_{OH_SYM} deleted. ● V_{ILR} max value changed. ● I_{PUR} min and max values changed. *Table 27*: Sensitivity value changed. *Table 30*: Most values in table changed.
05-Mar-2009	3	● Description of system requirements, controller characteristics and how controller characteristics are guaranteed updated. ● Electrical parameters updated. ● EMI characteristics are now in one table; values have been updated. ● ESD characteristics are now in one table. ● Electrical parameters are identified as either system requirements or controller characteristics. Method used to guarantee each controller characteristic is noted in table. ● AC Timings: 1149.1 (JTAG) Timing, Nexus Timing, External Interrupt Timing, and DSPI Timing sections deleted