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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

#### Details

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Product Status	Active
Core Processor	e200z0h
Core Size	32-Bit Single-Core
Speed	64MHz
Connectivity	CANbus, LINbus, SPI, UART/USART
Peripherals	DMA, POR, PWM, WDT
Number of I/O	107
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	40K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 26x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/spc560p50l5befar

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

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The flash memory module provides the following features:

- As much as 576 KB flash memory
  - 8 blocks (32 KB + 2×16 KB + 32 KB + 32 KB + 3×128 KB) code flash
  - 4 blocks (16 KB + 16 KB + 16 KB + 16 KB) data flash
  - Full Read While Write (RWW) capability between code and data flash
- Four 128-bit wide prefetch buffers to provide single cycle in-line accesses (prefetch buffers can be configured to prefetch code or data or both)
- Typical flash memory access time: 0 wait states for buffer hits, 2 wait states for page buffer miss at 64 MHz
- Hardware managed flash memory writes handled by 32-bit RISC Krypton engine
- Hardware and software configurable read and write access protections on a per-master basis
- Configurable access timing allowing use in a wide range of system frequencies
- Multiple-mapping support and mapping-based block access timing (up to 31 additional cycles) allowing use for emulation of other memory types.
- Software programmable block program/erase restriction control
- Erase of selected block(s)
- Read page sizes
  - Code flash memory: 128 bits (4 words)
  - Data flash memory: 32 bits (1 word)
- ECC with single-bit correction, double-bit detection for data integrity
  - Code flash memory: 64-bit ECC
  - Data flash memory: 64-bit ECC
- Embedded hardware program and erase algorithm
- Erase suspend, program suspend and erase-suspended program
- Censorship protection scheme to prevent flash memory content visibility
- Hardware support for EEPROM emulation

#### 1.5.5 Static random access memory (SRAM)

The SPC560P44Lx, SPC560P50Lx SRAM module provides up to 40 KB of general-purpose memory.

The SRAM module provides the following features:

- Supports read/write accesses mapped to the SRAM from any master
- Up to 40 KB general purpose SRAM
- Supports byte (8-bit), half word (16-bit), and word (32-bit) writes for optimal use of memory
- Typical SRAM access time: 0 wait-state for reads and 32-bit writes; 1 wait state for 8and 16-bit writes if back to back with a read to same memory block

#### 1.5.6 Interrupt controller (INTC)

The interrupt controller (INTC) provides priority-based preemptive scheduling of interrupt requests, suitable for statically scheduled hard real-time systems. The INTC handles 147 selectable-priority interrupt sources.



### 1.5.13 System timer module (STM)

The STM module implements these features:

- One 32-bit up counter with 8-bit prescaler
- Four 32-bit compare channels
- Independent interrupt source for each channel
- Counter can be stopped in debug mode

### 1.5.14 Software watchdog timer (SWT)

The SWT has the following features:

- 32-bit time-out register to set the time-out period
- Programmable selection of system or oscillator clock for timer operation
- Programmable selection of window mode or regular servicing
- Programmable selection of reset or interrupt on an initial time-out
- Master access protection
- Hard and soft configuration lock bits
- Reset configuration inputs allow timer to be enabled out of reset

### 1.5.15 Fault collection unit (FCU)

The FCU provides an independent fault reporting mechanism even if the CPU is malfunctioning.

The FCU module has the following features:

- FCU status register reporting the device status
- Continuous monitoring of critical fault signals
- User selection of critical signals from different fault sources inside the device
- Critical fault events trigger 2 external pins (user selected signal protocol) that can be used externally to reset the device and/or other circuitry (for example, safety relay or FlexRay transceiver)
- Faults are latched into a register

### 1.5.16 System integration unit – Lite (SIUL)

The SPC560P44Lx, SPC560P50Lx SIUL controls MCU pad configuration, external interrupt, general purpose I/O (GPIO), and internal peripheral multiplexing.

The pad configuration block controls the static electrical characteristics of I/O pins. The GPIO block provides uniform and discrete input/output control of the I/O pins of the MCU.

Symbol	Description	Direction	Pad sp	beed <sup>(1)</sup>	Pin		
Symbol	Description	Direction	SRC = 0	SRC = 1	100-pin	144-pin	
TMS	JTAG state machine control	Bidirectional	Slow	Fast	59	87	
тск	JTAG clock	Input only	Slow	—	60	88	
TDI	Test Data In	Input only	Slow	Medium	58	86	
TDO	Test Data Out	Output only	Slow	Fast	61	89	
	Reset pin, available on	100-pin and 144-	pin packag	e.			
RESET	Bidirectional reset with Schmitt trigger characteristics and noise filter	Bidirectional	Medium	—	20	31	
	Test pin, available on 1	00-pin and 144-p	oin package	).			
VPP_TEST	Pin for testing purpose only. To be tied to ground in normal operating mode.	_	_	_	74	107	

#### Table 6. System pins (continued)

1. SCR values refer to the value assigned to the Slew Rate Control bits of the pad configuration register.

### 2.2.3 Pin muxing

Table 7 defines the pin list and muxing for the SPC560P44Lx, SPC560P50Lx devices.

Each row of *Table 7* shows all the possible ways of configuring each pin, via alternate functions. The default function assigned to each pin after reset is the ALTO function.

SPC560P44Lx, SPC560P50Lx devices provide four main I/O pad types, depending on the associated functions:

- *Slow pads* are the most common, providing a compromise between transition time and low electromagnetic emission.
- Medium pads provide fast enough transition for serial communication channels with controlled current to reduce electromagnetic emission.
- *Fast pads* provide maximum speed. They are used for improved NEXUS debugging capability.
- Symmetric pads are designed to meet FlexRay requirements.

Medium and Fast pads can use slow configuration to reduce electromagnetic emission, at the cost of reducing AC performance. For more information, see the datasheet's "Pad AC Specifications" section.



Table 7.	Pin r	nuxing
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Port	Pad	Alternate			I/O	Pad s	peed <sup>(5)</sup>	Pin	No.
pin	configuration register (PCR)	function <sup>(1),</sup> (2)	Functions	Peripheral <sup>(3)</sup>	direction (4)	SRC = 0	SRC = 1	100-pin	144-pin
				Port A (16-bit)					
A[0]	PCR[0]	ALTO ALT1 ALT2 ALT3 —	GPIO[0] ETC[0] SCK F[0] EIRQ[0]	SIUL eTimer_0 DSPI_2 FCU_0 SIUL	I/O I/O O I	Slow	Medium	51	73
A[1]	PCR[1]	ALTO ALT1 ALT2 ALT3 —	GPIO[1] ETC[1] SOUT F[1] EIRQ[1]	SIUL eTimer_0 DSPI_2 FCU_0 SIUL	I/O I/O O I	Slow	Medium	52	74
A[2] <sup>(6)</sup>	PCR[2]	ALT0 ALT1 ALT2 ALT3 — — —	GPIO[2] ETC[2] — A[3] SIN ABS[0] EIRQ[2]	SIUL eTimer_0 — FlexPWM_0 DSPI_2 MC_RGM SIUL	I/O I/O - O I I I	Slow	Medium	57	84
A[3] <sup>(6)</sup>	PCR[3]	ALT0 ALT1 ALT2 ALT3 — —	GPIO[3] ETC[3] CS0 B[3] ABS[2] EIRQ[3]	SIUL eTimer_0 DSPI_2 FlexPWM_0 MC_RGM SIUL	I/O I/O I/O O I I	Slow	Medium	64	92
A[4] <sup>(6)</sup>	PCR[4]	ALT0 ALT1 ALT2 ALT3 — —	GPIO[4] ETC[0] CS1 ETC[4] FAB EIRQ[4]	SIUL eTimer_1 DSPI_2 eTimer_0 MC_RGM SIUL	I/O I/O O I/O I I	Slow	Medium	75	108
A[5]	PCR[5]	ALTO ALT1 ALT2 ALT3 —	GPIO[5] CS0 ETC[5] CS7 EIRQ[5]	SIUL DSPI_1 eTimer_1 DSPI_0 SIUL	I/O I/O I/O O I	Slow	Medium	8	14
A[6]	PCR[6]	ALTO ALT1 ALT2 ALT3 —	GPIO[6] SCK — — EIRQ[6]	SIUL DSPI_1 — SIUL	I/O I/O — I	Slow	Medium	2	2



Port	Pad configuration f				Alternate			I/O	Pad sp	beed <sup>(5)</sup>		No.
nin	configuration register (PCR)	function <sup>(1),</sup> (2)	Functions Peripheral <sup>(3)</sup> c		direction (4)	SRC = 0	SRC = 1	100-pin	144-pin			
		ALT0	GPIO[23]	SIUL								
		ALT1		—								
B[7]	PCR[23]	ALT2		—	Input only	_	_	29	43			
		ALT3		ADC_0								
		_	AN[0] RXD	LIN_0								
		ALT0										
		ALT0 ALT1	GPIO[24]	SIUL								
		ALT2	_	_		_	_	31				
B[8]	PCR[24]	ALT3		_	Input only				47			
		_	AN[1]	ADC_0								
		—	ETC[5]	eTimer_0								
		ALT0	GPIO[25]	SIUL								
		ALT1	_	—								
B[9]	PCR[25]	ALT2		—	Input only	—	—	35	52			
		ALT3	—	—								
		—	AN[11]	ADC_0 / ADC_1								
	DODION	ALT0	GPIO[26]	SIUL								
DI ( O)		ALT1		—		_		36				
B[10]	PCR[26]	ALT2 ALT3		—	Input only		_		53			
		ALI3	 AN[12]	 ADC_0 / ADC_1								
		ALT0	GPIO[27]	SIUL								
		ALT1	—									
B[11]	PCR[27]	ALT2	_	_	Input only	_	_	37	54			
		ALT3		_								
		—	AN[13]	ADC_0 / ADC_1								
		ALT0	GPIO[28]	SIUL								
		ALT1	_	—								
B[12]	PCR[28]	ALT2		—	Input only	—	—	38	55			
		ALT3	—	—								
		_	AN[14]	ADC_0 / ADC_1								
		ALT0	GPIO[29]	SIUL								
		ALT1	_	—								
B[13]	PCR[29]	ALT2 ALT3	_		Input only	—	—	42	60			
		ALIS	 AN[0]	ADC_1								
		_	RXD	LIN_1								

## Table 7. Pin muxing (continued)



Port	Pad	Alternate			I/O	Pad s	peed <sup>(5)</sup>	Pin	No.
pin	configuration register (PCR)	(0)	Functions Peripheral <sup>(3)</sup>		direction (4)	SRC = 0	SRC = 1	100-pin	144-pin
F[14]	PCR[94]	ALTO ALT1 ALT2 ALT3	GPIO[94] TXD — —	SIUL LIN_1 —	V0 0	Slow	Medium	_	115
F[15]	PCR[95]	ALT0 ALT1 ALT2 ALT3 —	GPIO[95] — — RXD	SIUL — — LIN_1	I/O       	Slow	Medium		113
				Port G (12-bit)					
G[0]	PCR[96]	ALTO ALT1 ALT2 ALT3 —	GPIO[96] F[0] — EIRQ[30]	SIUL FCU_0 — SIUL	I/O O — I	Slow	Medium	_	38
G[1]	PCR[97]	ALTO ALT1 ALT2 ALT3 —	GPIO[97] F[1] — — EIRQ[31]	SIUL FCU_0 — SIUL	I/O O — I	Slow	Medium		141
G[2]	PCR[98]	ALTO ALT1 ALT2 ALT3	GPIO[98] X[2] —	SIUL FlexPWM_0 — —	I/O I/O —	Slow	Medium		102
G[3]	PCR[99]	ALT0 ALT1 ALT2 ALT3	GPIO[99] A[2] — —	SIUL FlexPWM_0 —	I/O O —	Slow	Medium	_	104
G[4]	PCR[100]	ALTO ALT1 ALT2 ALT3	GPIO[100] B[2] — —	SIUL FlexPWM_0 —	I/O O —	Slow	Medium	_	100
G[5]	PCR[101]	ALTO ALT1 ALT2 ALT3	GPIO[101] X[3] — —	SIUL FlexPWM_0 —	I/O I/O —	Slow	Medium	_	85
G[6]	PCR[102]	ALTO ALT1 ALT2 ALT3	GPIO[102] A[3] — —	SIUL FlexPWM_0 — —	I/O O — —	Slow	Medium	_	98

### Table 7. Pin muxing (continued)



- 3. The difference between ADC voltage supplies must be less than 100 mV,  $|V_{DD_HV_ADC1} V_{DD_HV_ADC0}| < 100 mV$ .
- To be connected to emitter of external NPN. Low voltage supplies are not under user control—they are produced by an on-chip voltage regulator—but for the device to function properly the low voltage grounds (V<sub>SS\_LV\_xxx</sub>) must be shorted to high voltage grounds (V<sub>SS\_HV\_xxx</sub>) and the low voltage supply pins (V<sub>DD\_LV\_xxx</sub>) must be connected to the external ballast emitter.
- 5. The low voltage supplies (V\_DD\_LV\_xxx) are not all independent.
- V<sub>DD\_LV\_COR1</sub> and V<sub>DD\_LV\_COR2</sub> are shorted internally via double bonding connections with lines that provide the low voltage supply to the data flash module. Similarly, V<sub>SS\_LV\_COR1</sub> and V<sub>SS\_LV\_COR2</sub> are internally shorted.

V<sub>DD\_LV\_REGCOR</sub> and V<sub>DD\_LV\_REGCORx</sub> are physically shorted internally, as are V<sub>SS\_LV\_REGCOR</sub> and V<sub>SS\_LV\_CORx</sub>.

<b>.</b>			•	Val	ue			
Symbol		Parameter Conditions		Min	Max <sup>(1)</sup>	Unit		
V <sub>SS</sub>	SR	Device ground	—	0	0	V		
V <sub>DD_HV_IOx</sub> <sup>(2)</sup>	SR	3.3 V input/output supply voltage	—	3.0	3.6	V		
$V_{SS_HV_IOx}$	SR	Input/output ground voltage	—	0	0	V		
		2.2.V. and and data flach	—	3.0	3.6			
V <sub>DD_HV_FL</sub> S		Supply vollage	Relative to V <sub>DD_HV_IOx</sub>	$V_{DD_HV_IOx} - 0.1$	V <sub>DD_HV_IOx</sub> + 0.1	V		
V <sub>SS_HV_FL</sub>	SR	Code and data flash ground	—	0	0	V		
		3.3 V crystal oscillator amplifier	—	3.0	3.6			
V <sub>DD_HV_OSC</sub>	SR	SR	SR	supply voltage	Relative to V <sub>DD_HV_IOx</sub>	$V_{DD_HV_IOx} - 0.1$	$V_{DD_HV_IOx} + 0.1$	V
V <sub>SS_HV_OSC</sub>	SR	3.3 V crystal oscillator amplifier reference voltage	—	0	0	V		
		voltage	—	3.0	3.6			
$V_{DD_HV_REG}$			Relative to V <sub>DD_HV_IOx</sub>	$V_{DD_HV_IOx} - 0.1$	$V_{DD_HV_IOx} + 0.1$	V		
		3.3 V ADC_0 supply and high	—	3.0	5.5			
$V_{DD_HV_ADC0}^{(3)}$	SR	reference voltage	Relative to V <sub>DD_HV_REG</sub>	$V_{DD_HV_REG} - 0.1$	5.5	V		
V <sub>SS_HV_ADC0</sub>	SR	ADC_0 ground and low reference voltage	_	0	0	V		
		3.3 V ADC_1 supply and high	—	3.0	5.5			
V <sub>DD_HV_ADC1</sub> <sup>(3)</sup>	SR	reference voltage	Relative to V <sub>DD_HV_REG</sub>	$V_{DD_HV_REG} - 0.1$	5.5	V		
V <sub>SS_HV_ADC1</sub>	SR	ADC_1 ground and low reference voltage	_	0	0	V		
V <sub>DD_LV_REGCOR</sub> <sup>(4),</sup>	сс	Internal supply voltage	_	_	_	V		
V <sub>SS_LV_REGCOR</sub> <sup>(4)</sup>	SR	Internal reference voltage	—	0	0	V		
V <sub>DD_LV_CORx</sub> <sup>(4),(5)</sup>		Internal supply voltage	_	_		V		

Recommended operating conditions (3.3 V) Table 11.



- 2. Junction-to-board thermal resistance determined per JEDEC JESD51-8. Thermal test board meets JEDEC specification for the specified package.
- 3. Junction-to-case at the top of the package determined using MIL-STD 883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer.
- 4. Thermal characterization parameter indicating the temperature difference between the board and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JB.
- 5. Thermal characterization parameter indicating the temperature difference between the case and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JC.

Symbol	Parameter	Conditions	Typical value	Unit
R <sub>θJA</sub>	Thermal resistance junction-to-ambient, natural convection <sup>(1)</sup>	Single layer board—1s	47.3	°C/ W
	natural convection <sup>(1)</sup>	Four layer board—2s2p	35.3	°C/ W
$R_{ extsf{ heta}JB}$	Thermal resistance junction-to-board <sup>(2)</sup>	Four layer board—2s2p	19.1	°C/ W
R <sub>θJCtop</sub>	Thermal resistance junction-to-case (top) <sup>(3)</sup>	Single layer board—1s	9.7	°C/ W
$\Psi_{JB}$	Junction-to-board, natural convection <sup>(4)</sup>	Operating conditions	19.1	°C/ W
$\Psi_{JC}$	Junction-to-case, natural convection <sup>(5)</sup>	Operating conditions	0.8	°C/ W

Table 13. Thermal characteristics for 100-pin LQFP

1. Junction-to-ambient thermal resistance determined per JEDEC JESD51-7. Thermal test board meets JEDEC specification for this package.

2. Junction-to-board thermal resistance determined per JEDEC JESD51-8. Thermal test board meets JEDEC specification for the specified package.

3. Junction-to-case at the top of the package determined using MIL-STD 883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer.

- 4. Thermal characterization parameter indicating the temperature difference between the board and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JB.
- 5. Thermal characterization parameter indicating the temperature difference between the case and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JC.

#### 3.5.2 General notes for specifications at maximum junction temperature

An estimation of the chip junction temperature, T<sub>J</sub>, can be obtained from *Equation 1*:

#### Equation 1 $T_J = T_A + (R_{\theta JA} * P_D)$

where:

 $T_A$ = ambient temperature for the package (°C) $R_{\theta JA}$ = junction to ambient thermal resistance (°C/W) $P_D$ = power dissipation in the package (W)

The junction to ambient thermal resistance is an industry standard value that provides a quick and easy estimation of thermal performance. Unfortunately, there are two values in



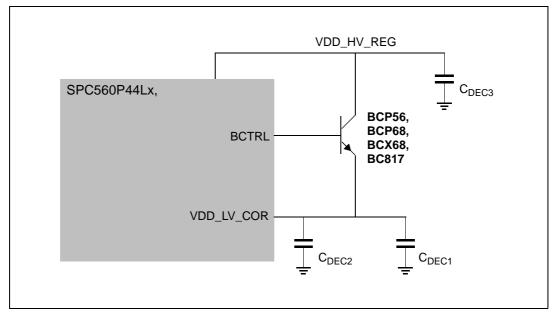


Figure 10. Configuration without resistor on base

Table 18.	Voltage	e reg	gulator electrical characteri	stics (configuration withou	ut resistor on bas	se)

Symbol		с	Parameter	Conditions		Value		Unit
Symbol		C	Falameter	Conditions	Min	Тур	Max	Unit
V <sub>DD_LV_REGCOR</sub>	сс	Ρ	Output voltage under maximum load run supply current configuration	Post-trimming	1.15	_	1.32	V
C <sub>DEC1</sub>	SR	_	External decoupling/stability ceramic capacitor	4 capacitances	40	56	_	μF
R <sub>REG</sub>	SR		Resulting ESR of all four C <sub>DEC1</sub>	Absolute maximum value between 100 kHz and 10 MHz	Ι		45	mΩ
C <sub>DEC2</sub>	SR	_	External decoupling/stability ceramic capacitor	4 capacitances of 100 nF each	400	_	_	nF
C <sub>DEC3</sub>	SR		External decoupling/stability ceramic capacitor on VDD_HV_REG	_	40		_	μF
L <sub>Reg</sub>	SR		Resulting ESL of V_DD_HV_REG BCTRL and V_DD_LV_CORx pins	—			15	nH



Symbol	с		Parameter	Conditions		Va	lue	Unit
Symbol	C		Parameter	Conditions		Тур	Max	Unit
			RUN—Maximum mode <sup>(1)</sup>		40 MHz	62	77	
	-			V <sub>DD_LV_CORx</sub>	64 MHz	MHz 71 8	88	
	Т		DUN. Tracing lange de (2)	externally forced at 1.3 V	40 MHz	45	56	
			RUN—Typical mode <sup>(2)</sup>		64 MHz	52	65	
I <sub>DD_LV_CORx</sub>	Р		RUN—Maximum mode <sup>(3)</sup>	V <sub>DD_LV_CORx</sub> externally forced at 1.3 V	64 MHz	60	75	
		Р	ent	HALT mode <sup>(4)</sup>	V <sub>DD_LV_CORx</sub> externally forced at 1.3 V	_	1.5	10
		Supply current	STOP mode <sup>(5)</sup>	V <sub>DD_LV_CORx</sub> externally forced at 1.3 V	_	1	10	mA
		Sup	Flash during read	V <sub>DD_HV_FL</sub> at 5.0 V	—	10	12	
I <sub>DD_FLASH</sub>	Т		Flash during erase operation on 1 flash module	V <sub>DD_HV_FL</sub> at 5.0 V	_	15	19	
			ADC—Maximum mode <sup>(1)</sup>		ADC_1	3.5	5	
	т			V <sub>DD_HV_ADC0</sub> at 5.0 V	ADC_0	3	4	
DD_ADC	1			V <sub>DD_HV_ADC1</sub> at 5.0 V f <sub>ADC</sub> = 16 MHz	ADC_1	0.8	1	
			ADC—Typical mode <sup>(2)</sup> $t_{ADC} = 16 \text{ MHz}$		ADC_0	0.005	0.006	
I <sub>DD_OSC</sub>	Т		Oscillator	V <sub>DD_OSC</sub> at 5.0 V	8 MHz	2.6	3.2	

Table 22.Supply current (5.0 V, NVUSRO[PAD3V5V] = 0)

1. Maximum mode: FlexPWM, ADCs, CTU, DSPI, LINFlex, FlexCAN, 15 output pins, 1st and 2nd PLL enabled. I/O supply current excluded.

2. Typical mode configurations: DSPI, LINFlex, FlexCAN, 15 output pins, 1st PLL only. I/O supply current excluded.

 Code fetched from RAM, PLL\_0: 64 MHz system clock (x4 multiplier with 16 MHz XTAL), PLL\_1 is ON at PHI\_div2 = 120 MHz and PHI\_div3 = 80 MHz, auxiliary clock sources set that all peripherals receive maximum frequency, all peripherals enabled.

4. Halt mode configurations: code fetched from RAM, code and data flash memories in low power mode, OSC/PLL\_0/PLL\_1 are OFF, core clock frozen, all peripherals are disabled.

5. STOP "P" mode Device Under Test (DUT) configuration: code fetched from RAM, code and data flash memories OFF, OSC/PLL\_0/PLL\_1 are OFF, core clock frozen, all peripherals are disabled.

### 3.10.3 DC electrical characteristics (3.3 V)

*Table 23* gives the DC electrical characteristics at 3.3 V ( $3.0 \text{ V} < \text{V}_{\text{DD}_{\text{HV}_{\text{IOx}}}} < 3.6 \text{ V}$ , NVUSRO[PAD3V5V] = 1); see *Figure 14*.

#### Table 23. DC electrical characteristics (3.3 V, NVUSRO[PAD3V5V] = 1)<sup>(1)</sup>

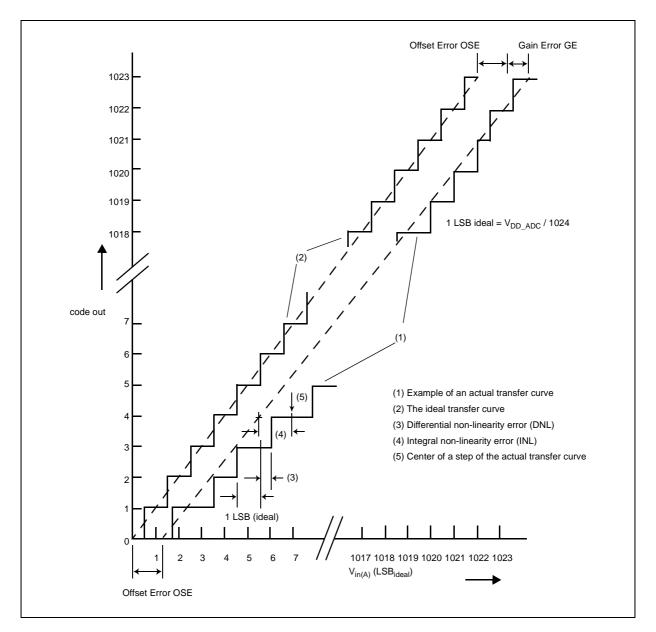
Symbol	<u>د</u>	Parameter	Conditions	Value		
	C		Conditions	Min	Мах	Unit
VII	D	Low level input voltage	—	-0.1 <sup>(2)</sup>	—	V
	Ρ	Low level input voltage	—	_	0.35 V <sub>DD_HV_IOx</sub>	V



Table 26.	I/O weight	(continued)
-----------	------------	-------------

Ded	LQ	FP144	LQFP100		
Pad	Weight 5V	Weight 3.3V	Weight 5V	Weight 3.3V	
PAD[86]	9%	6%	—	_	
MODO[0]	12%	8%	_		
PAD[7]	4%	4%	11%	10%	
PAD[36]	5%	4%	11%	9%	
PAD[8]	5%	4%	10%	9%	
PAD[37]	5%	4%	10%	9%	
PAD[5]	5%	4%	9%	8%	
PAD[39]	5%	4%	9%	8%	
PAD[35]	5%	4%	8%	7%	
PAD[87]	12%	9%	—	_	
PAD[88]	9%	6%	—		
PAD[89]	10%	7%	—	_	
PAD[90]	15%	11%	—	_	
PAD[91]	6%	5%	—	_	
PAD[57]	8%	7%	8%	7%	
PAD[56]	13%	11%	13%	11%	
PAD[53]	14%	12%	14%	12%	
PAD[54]	15%	13%	15%	13%	
PAD[55]	25%	22%	25%	22%	
PAD[96]	27%	24%	—	_	
PAD[65]	1%	1%	1%	1%	
PAD[67]	1%	1%	—	_	
PAD[33]	1%	1%	1%	1%	
PAD[68]	1%	1%	—	_	
PAD[23]	1%	1%	1%	1%	
PAD[69]	1%	1%	—	_	
PAD[34]	1%	1%	1%	1%	
PAD[70]	1%	1%	—	_	
PAD[24]	1%	1%	1%	1%	
PAD[71]	1%	1%	—	_	
PAD[66]	1%	1%	1%	1%	
PAD[25]	1%	1%	1%	1%	
PAD[26]	1%	1%	1%	1%	





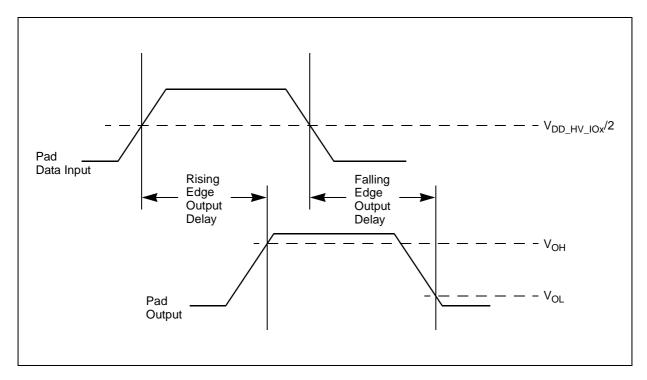


### 3.14.1 Input impedance and ADC accuracy

To preserve the accuracy of the A/D converter, it is necessary that analog input pins have low AC impedance. Placing a capacitor with good high frequency characteristics at the input pin of the device can be effective: the capacitor should be as large as possible, ideally infinite. This capacitor contributes to attenuating the noise present on the input pin; further, it sources charge during the sampling phase, when the analog signal source is a highimpedance source.

A real filter can typically be obtained by using a series resistance with a capacitor on the input pin (simple RC filter). The RC filtering may be limited according to the source impedance value of the transducer or circuit supplying the analog signal to be measured.



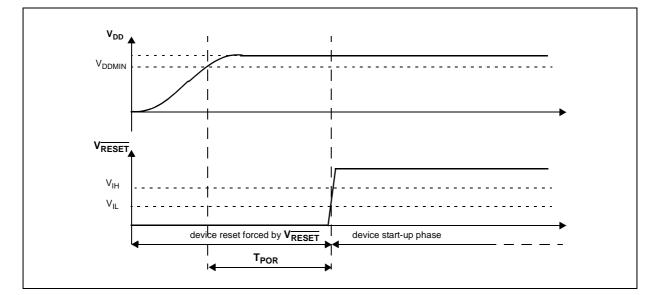




## 3.17 AC timing characteristics

## 3.17.1 RESET pin characteristics

The SPC560P44Lx, SPC560P50Lx implements a dedicated bidirectional RESET pin.



#### Figure 20. Start-up reset requirements



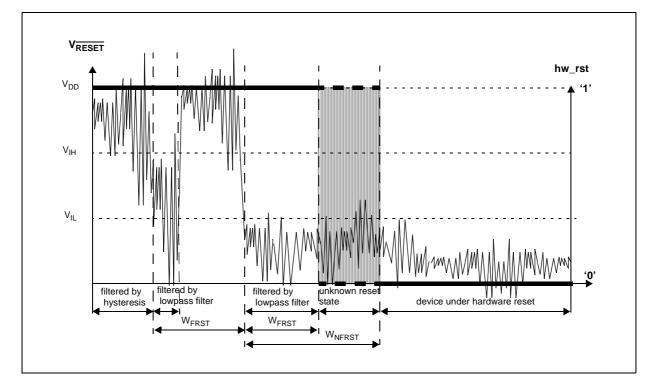


Figure 21. Noise filtering on reset signal

Table 38.	RESET electrical cl	naracteristics
Table 50.		anacteristics

Symbol		с	Parameter	Conditions <sup>(1)</sup>		Unit		
		C	Farameter	Conditions	Min	Тур	Max	Unit
V <sub>IH</sub>	SR		Input High Level CMOS 0 (Schmitt Trigger)		0.65V <sub>DD</sub>	_	V <sub>DD</sub> +0.4	V
V <sub>IL</sub>	OIX	Р	Input low Level CMOS (Schmitt Trigger)	_	-0.4		$0.35V_{DD}$	V
V <sub>HYS</sub>	сс	С	Input hysteresis CMOS (Schmitt Trigger)	_	0.1V <sub>DD</sub>		—	V
				Push Pull, I <sub>OL</sub> = 2mA, V <sub>DD</sub> = 5.0 V ± 10%, PAD3V5V = 0 (recommended)	_	_	0.1V <sub>DD</sub>	
V <sub>OL</sub>	сс	Ρ	Output low level	Push Pull, I <sub>OL</sub> = 1mA, V <sub>DD</sub> = 5.0 V ± 10%, PAD3V5V = 1 <sup>(2)</sup>	_	_	0.1V <sub>DD</sub>	V
				Push Pull, I <sub>OL</sub> = 1mA, V <sub>DD</sub> = 3.3 V ± 10%, PAD3V5V = 1 (recommended)		_	0.5	



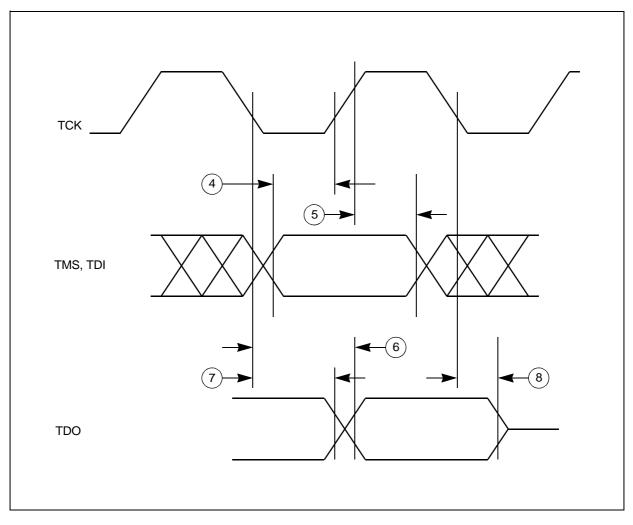


Figure 23. JTAG test access port timing



No.	Symbol		с	Desemptor	Va	Unit		
NO.			C	Parameter	Min	Тур	Max	Unit
6	t <sub>NTDIS</sub>	CC	D	TDI data setup time	6	—	—	ns
Ö	t <sub>NTMSS</sub>	CC	D	TMS data setup time	6	—	—	ns
7	t <sub>NTDIH</sub>	CC	D	TDI data hold time	10	—	—	ns
	t <sub>NTMSH</sub>	CC	D	TMS data hold time	10	—	—	ns
8	t <sub>TDOV</sub>	CC	D	TCK low to TDO data valid	—	—	35	ns
9	t <sub>TDOI</sub>	CC	D	TCK low to TDO data invalid	6	—	_	ns

 Table 40.
 Nexus debug port timing<sup>(1)</sup> (continued)

1. All Nexus timing relative to MCKO is measured from 50% of MCKO and 50% of the respective signal.

2. MDO, MSEO, and EVTO data is held valid until next MCKO low cycle.

3. Lower frequency is required to be fully compliant to standard.

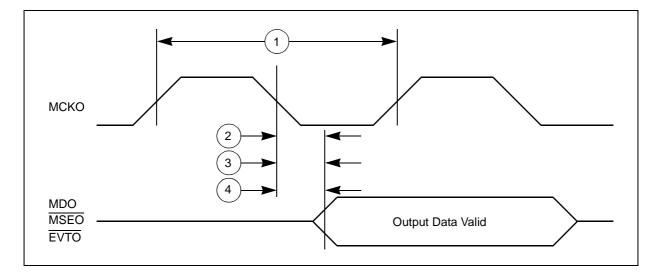


Figure 25. Nexus output timing

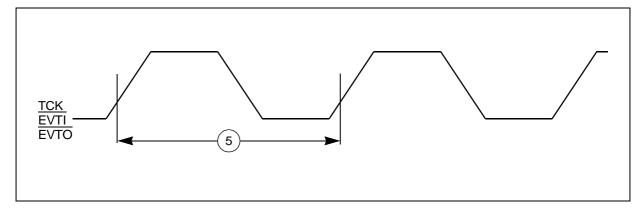


Figure 26. Nexus event trigger and test clock timings



	Dimensions								
Symbol		mm		inches <sup>(1)</sup>					
	Min	Тур	Max	Min	Тур	Мах			
А	_	—	1.600	—	—	0.0630			
A1	0.050	—	0.150	0.0020	—	0.0059			
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571			
b	0.170	0.220	0.270	0.0067	0.0087	0.0106			
С	0.090	—	0.200	0.0035	—	0.0079			
D	21.800	22.000	22.200	0.8583	0.8661	0.8740			
D1	19.800	20.000	20.200	0.7795	0.7874	0.7953			
D3	_	17.500	_	_	0.6890				
Е	21.800	22.000	22.200	0.8583	0.8661	0.8740			
E1	19.800	20.000	20.200	0.7795	0.7874	0.7953			
E3	_	17.500	_	_	0.6890				
е	_	0.500	—	—	0.0197	—			
L	0.450	0.600	0.750	0.0177	0.0236	0.0295			
L1	_	1.000	—	—	0.0394	—			
k	0.0°	3.5°	7.0°	3.5°	0.0°	7.0°			
ccc <sup>(2)</sup>		0.080	1	0.0031					

#### Table 43. LQFP144 mechanical data

1. Values in inches are converted from millimeters (mm) and rounded to four decimal digits.

2. Tolerance



# 5 Ordering information

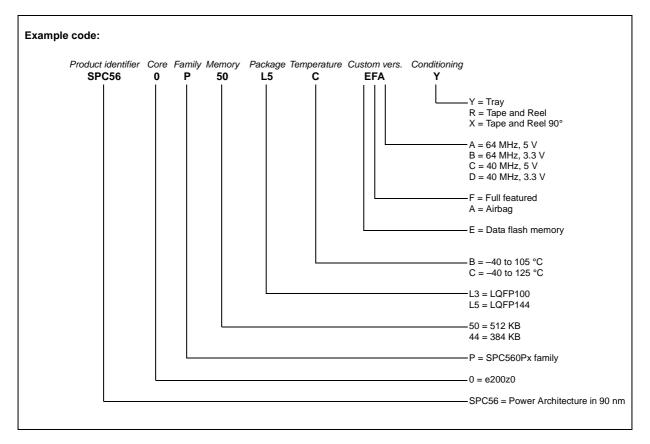


Figure 40. Commercial product code structure<sup>(a)</sup>

a. Not all configurations are available on the market. Please contact your ST sales representative to get the list of orderable commercial part number.



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