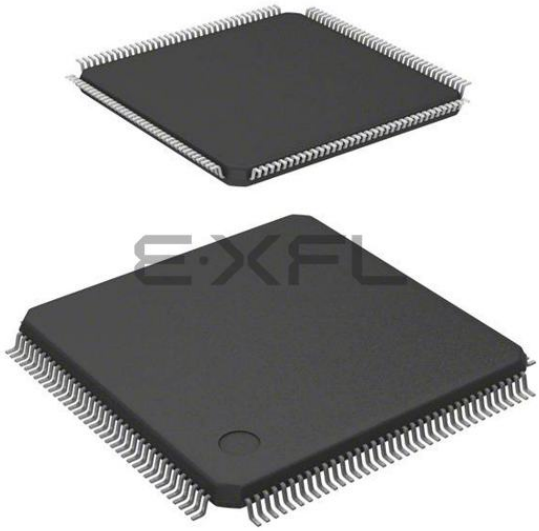

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	e200z0h
Core Size	32-Bit Single-Core
Speed	64MHz
Connectivity	CANbus, LINbus, SPI, UART/USART
Peripherals	DMA, POR, PWM, WDT
Number of I/O	107
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	40K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 26x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/spc560p50l5cefay

The FlexCAN module provides the following features:

- Full implementation of the CAN protocol specification, version 2.0B
  - Standard data and remote frames
  - Extended data and remote frames
  - Up to 8-bytes data length
  - Programmable bit rate up to 1 Mbit/s
- 32 message buffers of up to 8-bytes data length
- Each message buffer configurable as Rx or Tx, all supporting standard and extended messages
- Programmable loop-back mode supporting self-test operation
- 3 programmable mask registers
- Programmable transmit-first scheme: lowest ID or lowest buffer number
- Time stamp based on 16-bit free-running timer
- Global network time, synchronized by a specific message
- Maskable interrupts
- Independent of the transmission medium (an external transceiver is assumed)
- High immunity to EMI
- Short latency time due to an arbitration scheme for high-priority messages
- Transmit features
  - Supports configuration of multiple mailboxes to form message queues of scalable depth
  - Arbitration scheme according to message ID or message buffer number
  - Internal arbitration to guarantee no inner or outer priority inversion
  - Transmit abort procedure and notification
- Receive features
  - Individual programmable filters for each mailbox
  - 8 mailboxes configurable as a six-entry receive FIFO
  - 8 programmable acceptance filters for receive FIFO
- Programmable clock source
  - System clock
  - Direct oscillator clock to avoid PLL jitter

1.5.21 Safety port (FlexCAN)

The SPC560P44Lx, SPC560P50Lx MCU has a second CAN controller synthesized to run at high bit rates to be used as a safety port. The CAN module of the safety port provides the following features:

- Identical to the FlexCAN module
- Bit rate as fast as 7.5 Mbit/s at 60 MHz CPU clock using direct connection between CAN modules (no physical transceiver required)
- 32 message buffers of up to 8 bytes data length
- Can be used as a second independent CAN module

1.5.22 FlexRay

The FlexRay module provides the following features:

- Full implementation of FlexRay Protocol Specification 2.1
- 32 configurable message buffers can be handled
- Dual channel or single channel mode of operation, each as fast as 10 Mbit/s data rate
- Message buffers configurable as Tx, Rx or RxFIFO
- Message buffer size configurable
- Message filtering for all message buffers based on FrameID, cycle count and message ID
- Programmable acceptance filters for RxFIFO message buffers

1.5.23 Serial communication interface module (LINFlex)

The LINFlex (local interconnect network flexible) on the SPC560P44Lx, SPC560P50Lx features the following:

- Supports LIN Master mode, LIN Slave mode and UART mode
- LIN state machine compliant to LIN1.3, 2.0, and 2.1 specifications
- Handles LIN frame transmission and reception without CPU intervention
- LIN features
  - Autonomous LIN frame handling
  - Message buffer to store Identifier and as much as 8 data bytes
  - Supports message length as long as 64 bytes
  - Detection and flagging of LIN errors (sync field, delimiter, ID parity, bit framing, checksum, and time-out)
  - Classic or extended checksum calculation
  - Configurable Break duration as long as 36-bit times
  - Programmable baud rate prescalers (13-bit mantissa, 4-bit fractional)
  - Diagnostic features: Loop back; Self Test; LIN bus stuck dominant detection
  - Interrupt-driven operation with 16 interrupt sources
- LIN slave mode features
  - Autonomous LIN header handling
  - Autonomous LIN response handling
- UART mode
  - Full-duplex operation
  - Standard non return-to-zero (NRZ) mark/space format
  - Data buffers with 4-byte receive, 4-byte transmit
  - Configurable word length (8-bit or 9-bit words)
  - Error detection and flagging
  - Parity, Noise and Framing errors
  - Interrupt-driven operation with four interrupt sources
  - Separate transmitter and receiver CPU interrupt sources
  - 16-bit programmable baud-rate modulus counter and 16-bit fractional
  - 2 receiver wake-up methods

The JTAG controller provides the following features:

- IEEE Test Access Port (TAP) interface with 4 pins (TDI, TMS, TCK, TDO)
- Selectable modes of operation include JTAGC/debug or normal system operation.
- A 5-bit instruction register that supports the following IEEE 1149.1-2001 defined instructions:
  - BYPASS, IDCODE, EXTEST, SAMPLE, SAMPLE/PRELOAD
- A 5-bit instruction register that supports the additional following public instructions:
  - ACCESS_AUX_TAP_NPC, ACCESS_AUX_TAP_ONCE
- 3 test data registers: a bypass register, a boundary scan register, and a device identification register.
- A TAP controller state machine that controls the operation of the data registers, instruction register and associated circuitry.

1.5.32 On-chip voltage regulator (VREG)

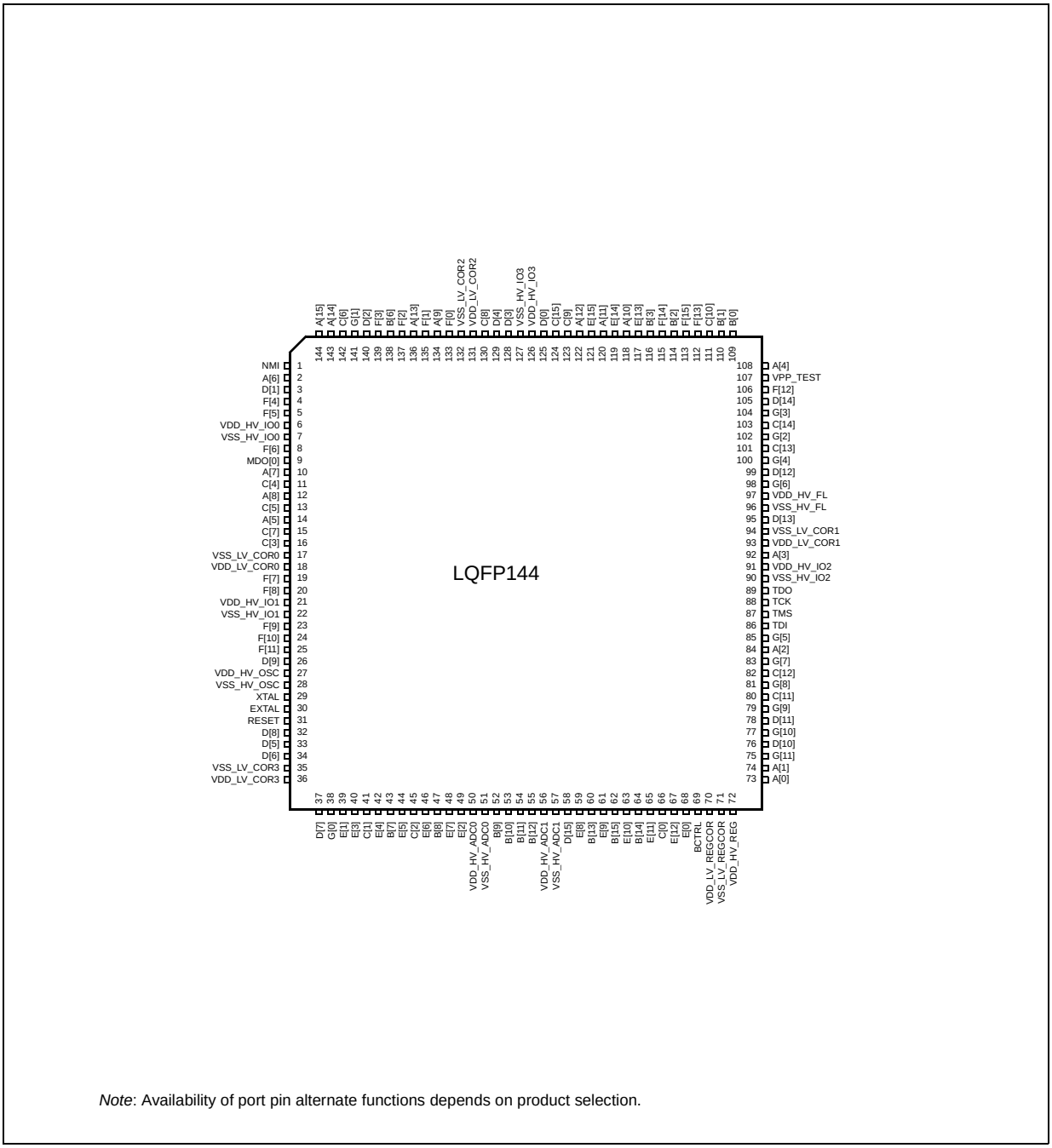
The on-chip voltage regulator module provides the following features:

- Uses external NPN (negative-positive-negative) transistor
- Regulates external 3.3 V /5.0 V down to 1.2 V for the core logic
- Low voltage detection on the internal 1.2 V and I/O voltage 3.3 V

2 Package pinouts and signal descriptions

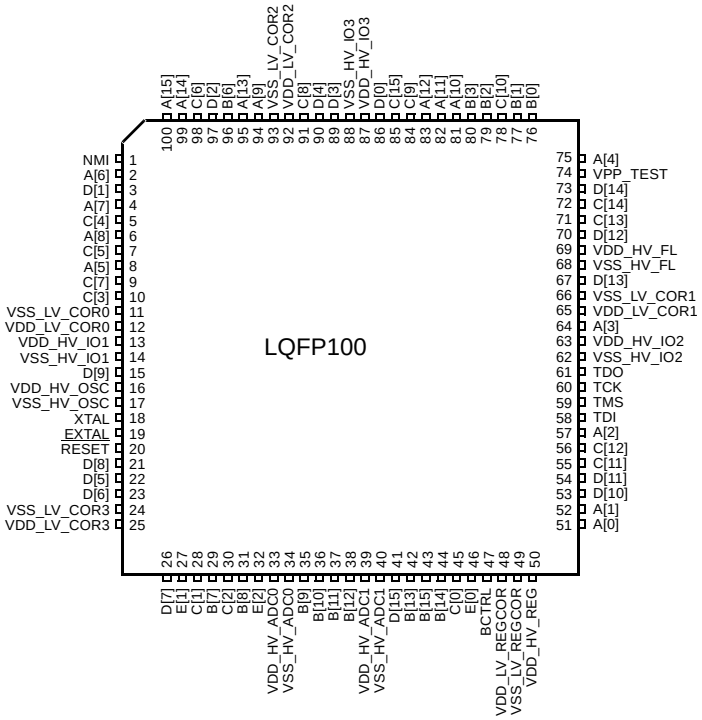
2.1 Package pinouts

The LQFP pinouts are shown in the following figures.



Note: Availability of port pin alternate functions depends on product selection.

Figure 2. 144-pin LQFP pinout – Full featured configuration (top view)



Note: Availability of port pin alternate functions depends on product selection.

Figure 4. 100-pin LQFP pinout – Full featured configuration (top view)

2.2 Pin description

The following sections provide signal descriptions and related information about the functionality and configuration of the SPC560P44Lx, SPC560P50Lx devices.

2.2.1 Power supply and reference voltage pins

Table 5 lists the power supply and reference voltage for the SPC560P44Lx, SPC560P50Lx devices.

3 Electrical characteristics

3.1 Introduction

This section contains device electrical characteristics as well as temperature and power considerations.

This microcontroller contains input protection against damage due to high static voltages. However, it is advisable to take precautions to avoid application of any voltage higher than the specified maximum rated voltages.

To enhance reliability, unused inputs can be driven to an appropriate logic voltage level (V_{DD} or V_{SS}). This can be done by the internal pull-up or pull-down resistors, which are provided by the device for most general purpose pins.

The following tables provide the device characteristics and its demands on the system.

In the tables where the device logic provides signals with their respective timing characteristics, the symbol “CC” for Controller Characteristics is included in the Symbol column.

In the tables where the external system must provide signals with their respective timing characteristics to the device, the symbol “SR” for System Requirement is included in the Symbol column.

Caution: All of the following parameter values can vary depending on the application and must be confirmed during silicon characterization or silicon reliability trial.

3.2 Parameter classification

The electrical parameters are guaranteed by various methods. To give the customer a better understanding, the classifications listed in *Table 8* are used and the parameters are tagged accordingly in the tables where appropriate.

Table 8. Parameter classifications

Classification tag	Tag description
P	Those parameters are guaranteed during production testing on each individual device.
C	Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.
T	Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.
D	Those parameters are derived mainly from simulations.

Note: The classification is shown in the column labeled “C” in the parameter tables where appropriate.

1. C.E. Triplett and B. Joiner, *An Experimental Characterization of a 272 PBGA Within an Automotive Engine Controller Module*, Proceedings of SemiTherm, San Diego, 1998, pp. 47–54.
2. G. Kromann, S. Shidore, and S. Addison, *Thermal Modeling of a PBGA for Air-Cooled Applications*, Electronic Packaging and Production, pp. 53–58, March 1998.
3. B. Joiner and V. Adams, *Measurement and Simulation of Junction to Board Thermal Resistance and Its Application in Thermal Modeling*, Proceedings of SemiTherm, San Diego, 1999, pp. 212–220.

3.6 Electromagnetic interference (EMI) characteristics

Table 14. EMI testing specifications

Symbol	Parameter	Conditions	Clocks	Frequency	Level (Max)	Unit
V_{EME}	Radiated emissions	Device configuration, test conditions and EM testing per standard IEC61967-2 Supply voltage = 5 V DC Ambient temperature = 25 °C Worst-case orientation	f_{OSC} 8 MHz f_{CPU} 64 MHz No PLL frequency modulation	150 kHz–150 MHz	16	dBµV
				150–1000 MHz	15	
				IEC Level	M	—
			f_{OSC} 8 MHz f_{CPU} 64 MHz 1% PLL frequency modulation	150 kHz–150 MHz	15	dBµV
				150–1000 MHz	14	
				IEC Level	M	—

3.7 Electrostatic discharge (ESD) characteristics

Table 15. ESD ratings(1),(2)

Symbol		Parameter	Conditions	Value	Unit
$V_{ESD(HBM)}$	S R	Electrostatic discharge (Human Body Model)	—	2000	V
$V_{ESD(CDM)}$	S R	Electrostatic discharge (Charged Device Model)	—	750 (corners)	V
				500 (other)	

1. All ESD testing is in conformity with CDF-AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.
2. A device will be defined as a failure if after exposure to ESD pulses the device no longer meets the device specification requirements. Complete DC parametric and functional testing shall be performed per applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

3.8 Power management electrical characteristics

3.8.1 Voltage regulator electrical characteristics

The internal voltage regulator requires an external NPN ballast to be connected as shown in *Figure 9*. *Table 16* contains all approved NPN ballast components. Capacitances should be placed on the board as near as possible to the associated pins. Care should also be taken to limit the serial inductance of the $V_{DD\_HV\_REG}$, BCTRL and $V_{DD\_LV\_CORx}$ pins to less than

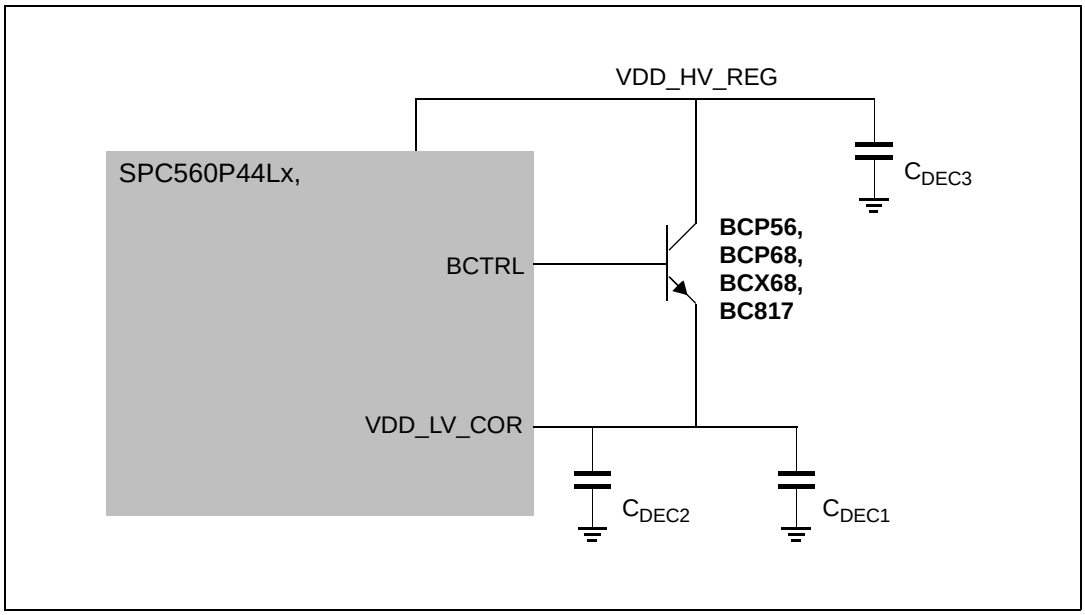


Figure 10. Configuration without resistor on base

Table 18. Voltage regulator electrical characteristics (configuration without resistor on base)

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
$V_{DD\_LV\_REGCOR}$	CC	P	Output voltage under maximum load run supply current configuration	Post-trimming	1.15	—	1.32	V
C_{DEC1}	SR	—	External decoupling/stability ceramic capacitor	4 capacitances	40	56	—	µF
R_{REG}	SR	—	Resulting ESR of all four C_{DEC1}	Absolute maximum value between 100 kHz and 10 MHz	—	—	45	mΩ
C_{DEC2}	SR	—	External decoupling/stability ceramic capacitor	4 capacitances of 100 nF each	400	—	—	nF
C_{DEC3}	SR	—	External decoupling/stability ceramic capacitor on VDD_HV_REG	—	40	—	—	µF
L_{Reg}	SR	—	Resulting ESL of $V_{DD\_HV\_REG}$, BCTRL and $V_{DD\_LV\_CORx}$ pins	—	—	—	15	nH

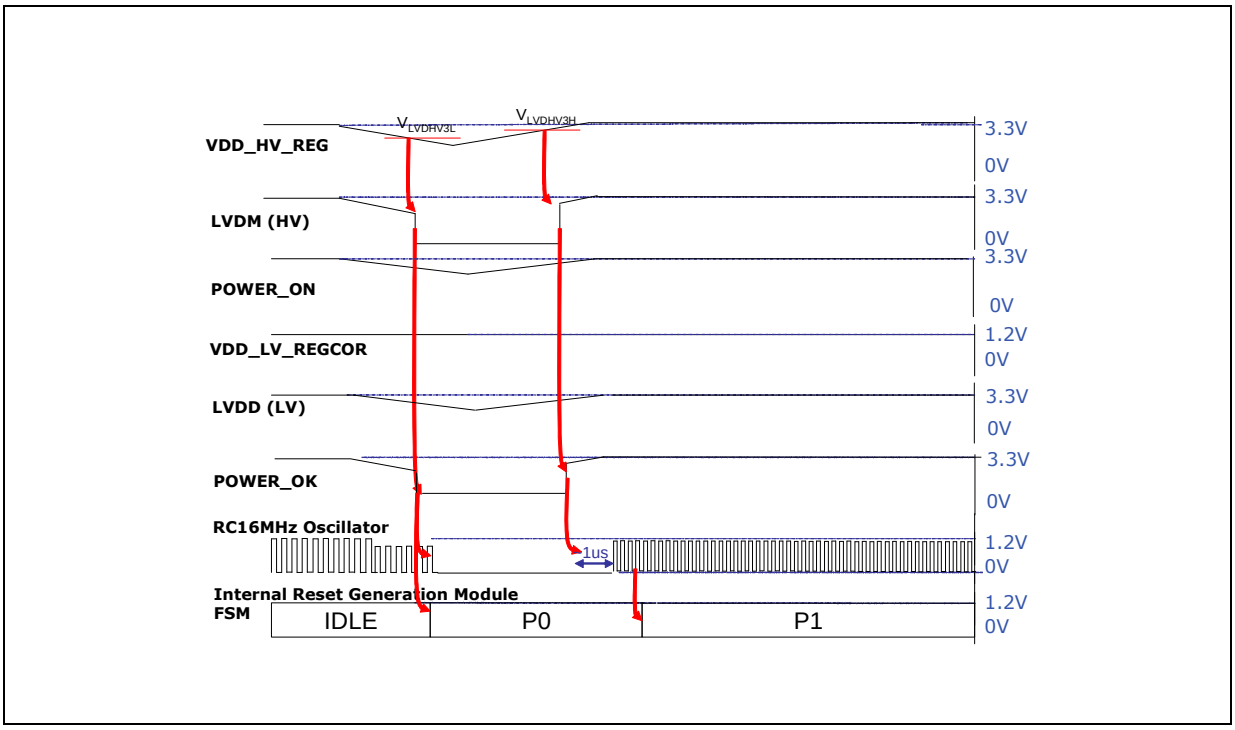


Figure 13. Brown-out typical sequence

3.10 DC electrical characteristics

3.10.1 NVUSRO register

Portions of the device configuration, such as high voltage supply, and watchdog enable/disable after reset are controlled via bit values in the non-volatile user options (NVUSRO) register.

For a detailed description of the NVUSRO register, please refer to the device reference manual.

NVUSRO[PAD3V5V] field description

The DC electrical characteristics are dependent on the PAD3V5V bit value. *Table 20* shows how NVUSRO[PAD3V5V] controls the device configuration.

Table 20. PAD3V5V field description

Value(1)	Description
0	High voltage supply is 5.0 V
1	High voltage supply is 3.3 V

1. Default manufacturing value before flash initialization is ‘1’ (3.3 V).

Table 24. Supply current (3.3 V, NVUSRO[PAD3V5V] = 1)

Symbol	C	Parameter		Conditions		Value		Unit
						Typ	Max	
$I_{DD\_LV\_CORx}$	T	Supply current	RUN—Maximum mode(1)	$V_{DD\_LV\_CORx}$ externally forced at 1.3 V	40 MHz	62	77	mA
					64 MHz	71	89	
			RUN—Typical mode(2)		40 MHz	45	56	
					64 MHz	53	66	
	P		RUN—Maximum mode(3)	$V_{DD\_LV\_CORx}$ externally forced at 1.3 V	64 MHz	60	75	
			HALT mode(4)	$V_{DD\_LV\_CORx}$ externally forced at 1.3 V	—	1.5	10	
			STOP mode(5)	$V_{DD\_LV\_CORx}$ externally forced at 1.3 V	—	1	10	
I_{DD_FLASH}	T		Flash during read on single mode	$V_{DD\_HV\_FL}$ at 3.3 V	—	8	10	
			Flash during erase operation on single mode	$V_{DD\_HV\_FL}$ at 3.3 V	—	10	12	
I_{DD_ADC}	T		ADC—Maximum mode(1)	$V_{DD\_HV\_ADC0}$ at 3.3 V $V_{DD\_HV\_ADC1}$ at 3.3 V f_{ADC} = 16 MHz	ADC_1	2.5	4	
					ADC_0	2	4	
			ADC—Typical mode(2)		ADC_1	0.8	1	
					ADC_0	0.005	0.006	
I_{DD_OSC}	T		Oscillator	V_{DD_OSC} at 3.3 V	8 MHz	2.4	3	

1. Maximum mode: FlexPWM, ADCs, CTU, DSPI, LINFlex, FlexCAN, 15 output pins, 1st and 2nd PLL enabled. I/O supply current excluded.
2. Typical mode: DSPI, LINFlex, FlexCAN, 15 output pins, 1st PLL only. I/O supply current excluded.
3. Code fetched from RAM, PLL_0: 64 MHz system clock (x4 multiplier with 16 MHz XTAL), PLL_1 is ON at PHI_div2 = 120 MHz and PHI_div3 = 80 MHz, auxiliary clock sources set that all peripherals receive maximum frequency, all peripherals enabled.
4. Halt mode configurations: code fetched from RAM, code and data flash memories in low power mode, OSC/PLL_0/PLL_1 are OFF, core clock frozen, all peripherals are disabled.
5. STOP “P” mode Device Under Test (DUT) configuration: code fetched from RAM, code and data flash memories OFF, OSC/PLL_0/PLL_1 are OFF, core clock frozen, all peripherals are disabled.

3.10.4 Input DC electrical characteristics definition

Figure 14 shows the DC electrical characteristics behavior as function of time.

Table 26. I/O weight (continued)

Pad	LQFP144		LQFP100	
	Weight 5V	Weight 3.3V	Weight 5V	Weight 3.3V
PAD[86]	9%	6%	—	—
MODO[0]	12%	8%	—	—
PAD[7]	4%	4%	11%	10%
PAD[36]	5%	4%	11%	9%
PAD[8]	5%	4%	10%	9%
PAD[37]	5%	4%	10%	9%
PAD[5]	5%	4%	9%	8%
PAD[39]	5%	4%	9%	8%
PAD[35]	5%	4%	8%	7%
PAD[87]	12%	9%	—	—
PAD[88]	9%	6%	—	—
PAD[89]	10%	7%	—	—
PAD[90]	15%	11%	—	—
PAD[91]	6%	5%	—	—
PAD[57]	8%	7%	8%	7%
PAD[56]	13%	11%	13%	11%
PAD[53]	14%	12%	14%	12%
PAD[54]	15%	13%	15%	13%
PAD[55]	25%	22%	25%	22%
PAD[96]	27%	24%	—	—
PAD[65]	1%	1%	1%	1%
PAD[67]	1%	1%	—	—
PAD[33]	1%	1%	1%	1%
PAD[68]	1%	1%	—	—
PAD[23]	1%	1%	1%	1%
PAD[69]	1%	1%	—	—
PAD[34]	1%	1%	1%	1%
PAD[70]	1%	1%	—	—
PAD[24]	1%	1%	1%	1%
PAD[71]	1%	1%	—	—
PAD[66]	1%	1%	1%	1%
PAD[25]	1%	1%	1%	1%
PAD[26]	1%	1%	1%	1%

Table 36. Flash memory read access timing

Symbol	C	Parameter	Conditions(1)	Max value	Unit
f_{max}	C	Maximum working frequency at given number of wait states in worst conditions	2 wait states	66	MHz
			0 wait states	18	

1. V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified

3.16 AC specifications

3.16.1 Pad AC specifications

Table 37. Output pin transition times

Symbol		C	Parameter	Conditions(1)		Value			Unit
						Min	Typ	Max	
t_{tr}	CC	D	Output transition time output pin(2) SLOW configuration	C_L = 25 pF	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	50	ns
		T		C_L = 50 pF		—	—	100	
		D		C_L = 100 pF		—	—	125	
		D		C_L = 25 pF	V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	40	
		T		C_L = 50 pF		—	—	50	
		D		C_L = 100 pF		—	—	75	
t_{tr}	CC	D	Output transition time output pin(2) MEDIUM configuration	C_L = 25 pF	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0 SIUL.PCRx.SRC = 1	—	—	10	ns
		T		C_L = 50 pF		—	—	20	
		D		C_L = 100 pF		—	—	40	
		D		C_L = 25 pF	V_{DD} = 3.3 V ± 10%, PAD3V5V = 1 SIUL.PCRx.SRC = 1	—	—	12	
		T		C_L = 50 pF		—	—	25	
		D		C_L = 100 pF		—	—	40	
t_{tr}	CC	D	Output transition time output pin(2) FAST configuration	C_L = 25 pF	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0 SIUL.PCRx.SRC = 1	—	—	4	ns
				C_L = 50 pF		—	—	6	
				C_L = 100 pF		—	—	12	
				C_L = 25 pF	V_{DD} = 3.3 V ± 10%, PAD3V5V = 1 SIUL.PCRx.SRC = 1	—	—	4	
				C_L = 50 pF		—	—	7	
				C_L = 100 pF		—	—	12	
t_{SYM}(3)	CC	T	Symmetric transition time, same drive strength between N and P transistor	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0		—	—	4	ns
				V_{DD} = 3.3 V ± 10%, PAD3V5V = 1		—	—	5	

1. V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 °C to $T_{A\ MAX}$, unless otherwise specified
2. C_L includes device and package capacitances (C_{PKG} < 5 pF).
3. Transition timing of both positive and negative slopes will differ maximum 50%

Table 38. $\overline{\text{RESET}}$ electrical characteristics (continued)

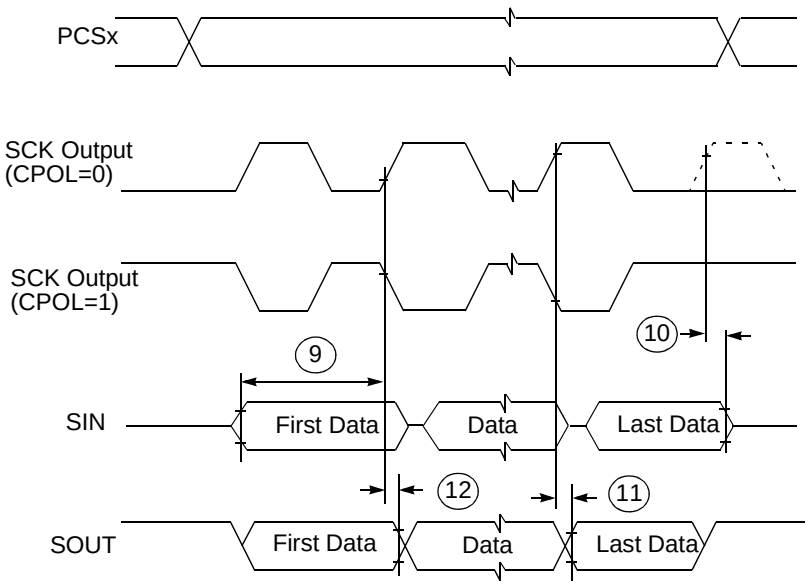
Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
t_{tr}	CC	D	Output transition time output pin[3] MEDIUM configuration	C_L = 25pF, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	10	ns
				C_L = 50pF, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	20	
				C_L = 100pF, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	40	
				C_L = 25pF, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	12	
				C_L = 50pF, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	25	
				C_L = 100pF, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	40	
W_{FRST}	SR	P	$\overline{\text{RESET}}$ input filtered pulse	—	—	—	40	ns
W_{NFRST}	SR	P	$\overline{\text{RESET}}$ input not filtered pulse	—	500	—	—	ns
t_{POR}	CC	D	Maximum delay before internal reset is released after all V_{DD_HV} reach nominal supply	Monotonic V_{DD_HV} supply ramp	—	—	1	ms
$\lvert I_{WPU} \rvert$	CC	P	Weak pull-up current absolute value	V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	10	—	150	µA
				V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	10	—	150	
				V_{DD} = 5.0 V ± 10%, PAD3V5V = 1[4]	10	—	250	

1. V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 °C to $T_{A\ MAX}$, unless otherwise specified
2. This is a transient configuration during power-up, up to the end of reset PHASE2 (refer to RGM module section of device reference manual).
3. C_L includes device and package capacitance (C_{PKG} < 5 pF).
4. The configuration PAD3V5 = 1 when V_{DD} = 5 V is only transient configuration during power-up. All pads but RESET and Nexus output (MDOx, EVTO, MCKO) are configured in input or in high impedance state.

3.17.2 IEEE 1149.1 interface timing

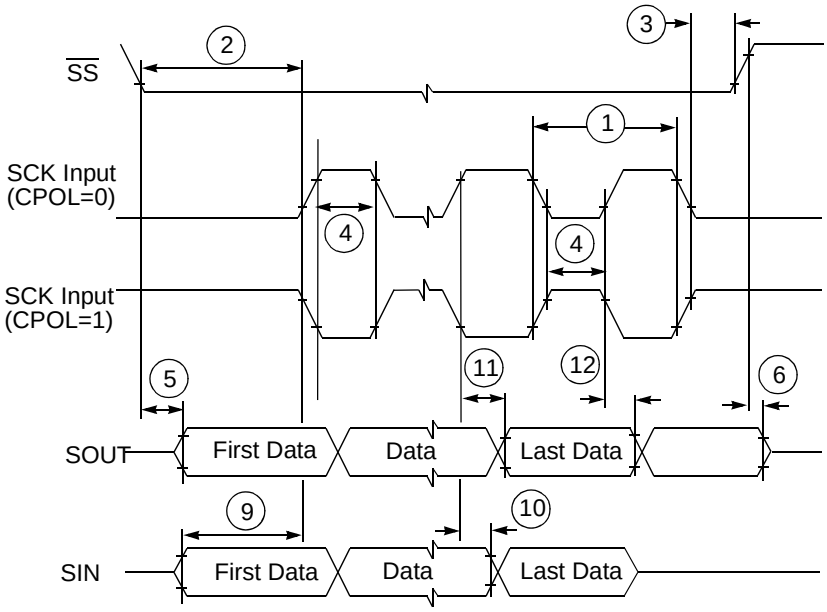
Table 39. JTAG pin AC electrical characteristics

No.	Symbol		C	Parameter	Conditions	Value		Unit
						Min	Max	
1	t_{JCYC}	CC	D	TCK cycle time	—	100	—	ns
2	t_{JDC}	CC	D	TCK clock pulse width (measured at $V_{DD\_HV\_IOx}$/2)	—	40	60	ns
3	$t_{TCKRISE}$	CC	D	TCK rise and fall times (40% – 70%)	—	—	3	ns
4	t_{TMSS}, t_{TDIS}	CC	D	TMS, TDI data setup time	—	5	—	ns



Note: Numbers shown reference *Table 42*.

Figure 34. DSPI modified transfer format timing – Master, CPHA = 1



Note: Numbers shown reference *Table 42*.

Figure 35. DSPI modified transfer format timing – Slave, CPHA = 0

4.2.2 LQFP100 mechanical outline drawing

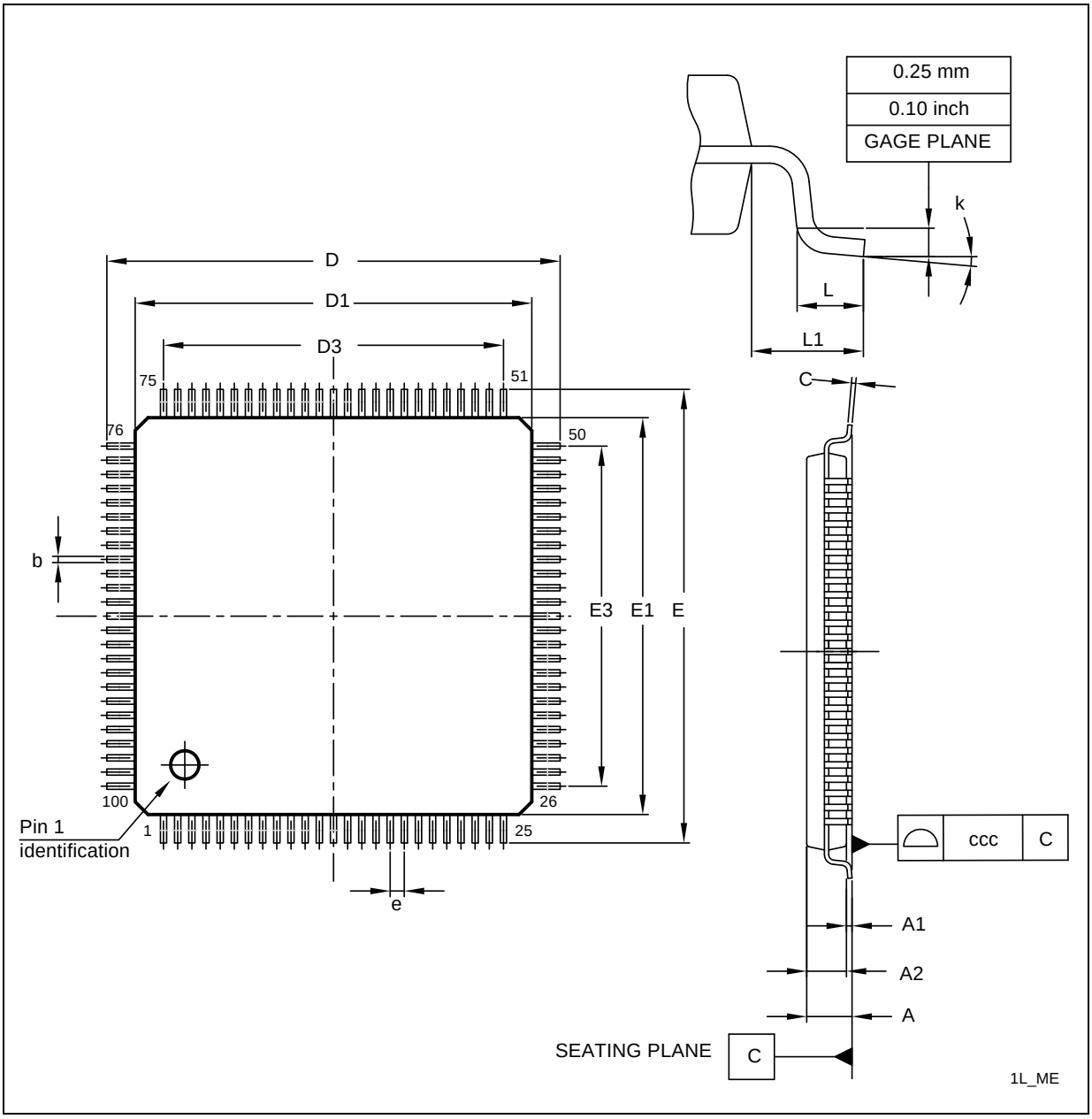


Figure 39. LQFP100 package mechanical drawing

Table 44. LQFP100 package mechanical data

Symbol	Dimensions					
	mm			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	—	—	1.600	—	—	0.0630
A1	0.050	—	0.150	0.0020	—	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	—	0.200	0.0035	—	0.0079
D	15.800	16.000	16.200	0.6220	0.6299	0.6378
D1	13.800	14.000	14.200	0.5433	0.5512	0.5591
D3	—	12.000	—	—	0.4724	—
E	15.800	16.000	16.200	0.6220	0.6299	0.6378
E1	13.800	14.000	14.200	0.5433	0.5512	0.5591
E3	—	12.000	—	—	0.4724	—
e	—	0.500	—	—	0.0197	—
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	—	1.000	—	—	0.0394	—
k	0.0°	3.5°	7.0°	0.0°	3.5°	7.0°
ccc[2]	0.08			0.0031		

1. Values in inches are converted from millimeters (mm) and rounded to four decimal digits.
2. Tolerance

5 Ordering information

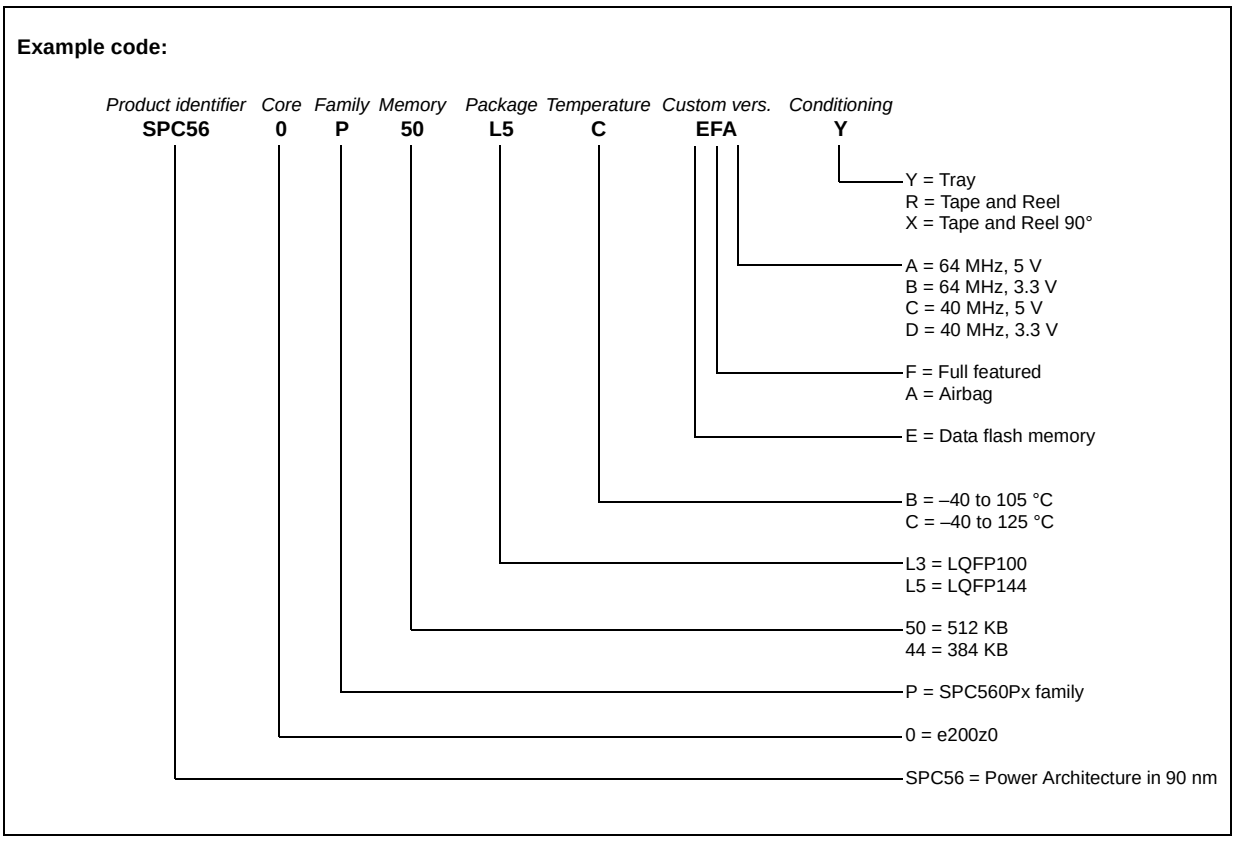


Figure 40. Commercial product code structure[(a)]

a. Not all configurations are available on the market. Please contact your ST sales representative to get the list of orderable commercial part number.

Table 46. Revision history (continued)

Date	Revision	Changes
07-Apr-2011	7 (cont'd)	SPC560P44Lx, SPC560P50Lx device configuration differences: Removed "temperature" row (temperature information is provided in Order codes) Updated SPC560P44Lx, SPC560P50Lx block diagram Added SPC560P44Lx, SPC560P50Lx series block summary Added *Section 1.5 Feature details* *Section 2.1, Package pinouts*: removed alternate functions from pinout diagrams Supply pins: updated descriptions of power supply pins (1.2 V) System pins: updated table Pin muxing: added rows "B[4]" and "B[5] *Section 3.3, Absolute maximum ratings*: added voltage specifications to titles of *Figure 5* and *Figure 6*; in *Table 9*, changed row "V_{SS_HV} / Digital Ground" to "V_{SS} / Device Ground"; updated symbols *Section 3.4, Recommended operating conditions*: added voltage specifications to titles of *Figure 7* and *Figure 8* Recommended operating conditions (5.0 V), and Recommended operating conditions (3.3 V): changed row "V_{SS_HV} / Digital Ground" to "V_{SS} / Device Ground"; updated symbols Updated *Section 3.5.1, Package thermal characteristics* Updated *Section 3.6, Electromagnetic interference (EMI) characteristics* *Section 3.8.1, Voltage regulator electrical characteristics*: amended titles of *Table 16* and *Table 19* Voltage regulator electrical characteristics (configuration without resistor on base) and Voltage regulator electrical characteristics (configuration with resistor on base): updated symbol and values for $V_{DD\_LV\_REGCOR}$ Low voltage monitor electrical characteristics: Updated $V_{MLVDDOK\_H}$ max value—was 1.15 V; is 1.145 V *Section 3.10, DC electrical characteristics*: reorganized contents Updated *Section 3.10.1, NVUSRO register* (includes adding *Section NVUSRO[OSCILLATOR_MARGIN] field description*) Supply current (5.0 V, NVUSRO[PAD3V5V] = 0): updated symbols Corrected parameter descriptions in DC electrical characteristics (3.3 V, NVUSRO[PAD3V5V] = 1): – V_{OL_F}—was "Fast, high level output voltage"; is "Fast, low level output voltage" – V_{OL_SYM}—was "Symmetric, high level output voltage"; is "Symmetric, low level output voltage" Supply current (3.3 V, NVUSRO[PAD3V5V] = 1): updated symbols Main oscillator output electrical characteristics (5.0 V, NVUSRO[PAD3V5V] = 0): replaced instances of EXTAL with XTAL Main oscillator output electrical characteristics (3.3 V, NVUSRO[PAD3V5V] = 1): replaced instances of EXTAL with XTAL FMPLL electrical characteristics: replaced "PLLMRFM" with "FMPLL" in table title; updated conditions; removed f_{sys} row; updated $f_{FMPLLOUT}$ min value ADC conversion characteristics: updated symbols; added row t_{ADC_PU} Flash memory read access timing: added footnote to "Conditions" column *Section 3.16.1, Pad AC specifications*: added Pad output delay diagram In the range of figures "DSPI Classic SPI Timing — Master, CPHA = 0" to "DSPI PCS Strobe (PCSS) Timing": added note Updated Order codes Updated "Commercial product code structure" figure *Table 45*: Added abbreviations "DUT", "NPN", and "RBW"

Table 46. Revision history (continued)

Date	Revision	Changes
18-Jul-2012	8	Updated *Table 1 (Device summary)* *Section 1.5.4, Flash memory*: Changed “Data flash memory: 32-bit ECC” to “Data flash memory: 64-bit ECC” *Figure 40 (Commercial product code structure)*, replaced "C = 60 MHz, 5 V" and "D = 60 MHz, 3.3 V" with respectively "C = 40 MHz, 5 V" and "D = 40 MHz, 3.3 V" *Table 9 (Absolute maximum ratings)*, updated TV_{DD} parameter, the minimum value to 3.0 V/s and the maximum value to 0.5 V/µs *Table 7 (Pin muxing)*, changed the description in the column "I/O direction" from "I/O" to "O" for the following port pins: A[10] with function B[0] A[11] with function A[0] A[11] with function A[2] A[12] with function A[2] A[12] with function B[2] A[13] with function B[2] C[7] with function A[1] C[10] with function A[3] C[15] with function A[1] D[0] with function B[1] D[10] with function A[0] D[11] with function B[0] D[13] with function A[1] D[14] with function B[1] Updated *Section 3.8.1, Voltage regulator electrical characteristics* Added *Table 27 (I/O consumption)* *Section 3.10, DC electrical characteristics*: deleted references to “oscillator margin” deleted subsection “NVUSRO[OSCILLATOR_MARGIN] field description” *Table 21 (DC electrical characteristics (5.0 V, NVUSRO[PAD3V5V] = 0))*, added IPU row for $\overline{\text{RESET}}$ pin *Table 23 (DC electrical characteristics (3.3 V, NVUSRO[PAD3V5V] = 1))*, added IPU row for $\overline{\text{RESET}}$ pin *Table 33 (ADC conversion characteristics)*, added V_{INAN} entry Removed “Order codes” table *Figure 40 (Commercial product code structure)*: added a footnote updated “E = Data flash memory”
18-Sep-2013	9	Updated Disclaimer