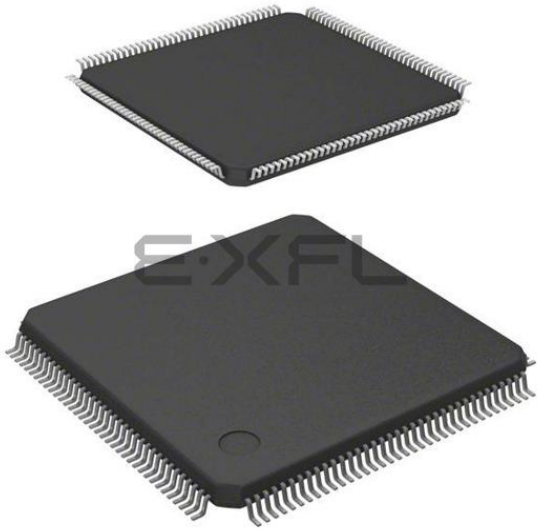

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z0h
Core Size	32-Bit Single-Core
Speed	64MHz
Connectivity	CANbus, LINbus, SPI, UART/USART
Peripherals	DMA, POR, PWM, WDT
Number of I/O	107
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	40K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 26x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/spc560p50l5cefby

The flash memory module provides the following features:

- As much as 576 KB flash memory
  - 8 blocks (32 KB + 2×16 KB + 32 KB + 32 KB + 3×128 KB) code flash
  - 4 blocks (16 KB + 16 KB + 16 KB + 16 KB) data flash
  - Full Read While Write (RWW) capability between code and data flash
- Four 128-bit wide prefetch buffers to provide single cycle in-line accesses (prefetch buffers can be configured to prefetch code or data or both)
- Typical flash memory access time: 0 wait states for buffer hits, 2 wait states for page buffer miss at 64 MHz
- Hardware managed flash memory writes handled by 32-bit RISC Krypton engine
- Hardware and software configurable read and write access protections on a per-master basis
- Configurable access timing allowing use in a wide range of system frequencies
- Multiple-mapping support and mapping-based block access timing (up to 31 additional cycles) allowing use for emulation of other memory types.
- Software programmable block program/erase restriction control
- Erase of selected block(s)
- Read page sizes
  - Code flash memory: 128 bits (4 words)
  - Data flash memory: 32 bits (1 word)
- ECC with single-bit correction, double-bit detection for data integrity
  - Code flash memory: 64-bit ECC
  - Data flash memory: 64-bit ECC
- Embedded hardware program and erase algorithm
- Erase suspend, program suspend and erase-suspended program
- Censorship protection scheme to prevent flash memory content visibility
- Hardware support for EEPROM emulation

1.5.5 Static random access memory (SRAM)

The SPC560P44Lx, SPC560P50Lx SRAM module provides up to 40 KB of general-purpose memory.

The SRAM module provides the following features:

- Supports read/write accesses mapped to the SRAM from any master
- Up to 40 KB general purpose SRAM
- Supports byte (8-bit), half word (16-bit), and word (32-bit) writes for optimal use of memory
- Typical SRAM access time: 0 wait-state for reads and 32-bit writes; 1 wait state for 8- and 16-bit writes if back to back with a read to same memory block

1.5.6 Interrupt controller (INTC)

The interrupt controller (INTC) provides priority-based preemptive scheduling of interrupt requests, suitable for statically scheduled hard real-time systems. The INTC handles 147 selectable-priority interrupt sources.

Digital part:

- 2 × 13 input channels including 4 channels shared between the 2 converters
- 4 analog watchdogs comparing ADC results against predefined levels (low, high, range) before results are stored in the appropriate ADC result location,
- 2 modes of operation: Normal mode or CTU control mode
- Normal mode features
  - Register-based interface with the CPU: control register, status register, 1 result register per channel
  - ADC state machine managing 3 request flows: regular command, hardware injected command, software injected command
  - Selectable priority between software and hardware injected commands
  - 4 analog watchdogs comparing ADC results against predefined levels (low, high, range)
  - DMA compatible interface
- CTU control mode features
  - Triggered mode only
  - 4 independent result queues (2 × 16 entries, 2 × 4 entries)
  - Result alignment circuitry (left justified; right justified)
  - 32-bit read mode allows to have channel ID on one of the 16-bit part
  - DMA compatible interfaces

1.5.28 Cross triggering unit (CTU)

The cross triggering unit allows automatic generation of ADC conversion requests on user selected conditions without CPU load during the PWM period and with minimized CPU load for dynamic configuration.

It implements the following features:

- Double buffered trigger generation unit with as many as eight independent triggers generated from external triggers
- Trigger generation unit configurable in sequential mode or in triggered mode
- Each Trigger can be appropriately delayed to compensate the delay of external low pass filter
- Double buffered global trigger unit allowing eTimer synchronization and/or ADC command generation
- Double buffered ADC command list pointers to minimize ADC-trigger unit update
- Double buffered ADC conversion command list with as many as 24 ADC commands
- Each trigger has the capability to generate consecutive commands
- ADC conversion command allows to control ADC channel from each ADC, single or synchronous sampling, independent result queue selection

1.5.29 Nexus development interface (NDI)

The NDI (Nexus Development Interface) block provides real-time development support capabilities for the SPC560P44Lx, SPC560P50Lx Power Architecture based MCU in compliance with the IEEE-ISTO 5001-2003 standard. This development support is supplied for MCUs without requiring external address and data pins for internal visibility. The NDI

block is an integration of several individual Nexus blocks that are selected to provide the development support interface for this device. The NDI block interfaces to the host processor and internal busses to provide development support as per the IEEE-ISTO 5001-2003 Class 2+ standard. The development support provided includes access to the MCU's internal memory map and access to the processor's internal registers during run time.

The Nexus Interface provides the following features:

- Configured via the IEEE 1149.1
- All Nexus port pins operate at V_{DDIO} (no dedicated power supply)
- Nexus 2+ features supported
  - Static debug
  - Watchpoint messaging
  - Ownership trace messaging
  - Program trace messaging
  - Real time read/write of any internally memory mapped resources through JTAG pins
  - Overrun control, which selects whether to stall before Nexus overruns or keep executing and allow overwrite of information
  - Watchpoint triggering, watchpoint triggers program tracing
- Auxiliary Output Port
  - 4 MDO (Message Data Out) pins
  - MCKO (Message Clock Out) pin
  - 2 $\overline{\text{MSEO}}$ (Message Start/End Out) pins
  - $\overline{\text{EVTO}}$ (Event Out) pin
- Auxiliary Input Port
  - $\overline{\text{EVTI}}$ (Event In) pin

1.5.30 Cyclic redundancy check (CRC)

The CRC computing unit is dedicated to the computation of CRC off-loading the CPU. The CRC module features:

- Support for CRC-16-CCITT (*x*25 protocol):
  - $x^{16} + x^{12} + x^5 + 1$
- Support for CRC-32 (Ethernet protocol):
  - $x^{32} + x^{26} + x^{23} + x^{22} + x^{16} + x^{12} + x^{11} + x^{10} + x^8 + x^7 + x^5 + x^4 + x^2 + x + 1$
- Zero wait states for each write/read operations to the CRC_CFG and CRC_INP registers at the maximum frequency

1.5.31 IEEE 1149.1 JTAG controller

The JTAG controller (JTAGC) block provides the means to test chip functionality and connectivity while remaining transparent to system logic when not in test mode. All data input to and output from the JTAGC block is communicated in serial format. The JTAGC block is compliant with the IEEE standard.

Table 7. Pin muxing (continued)

Port pin	Pad configuration register (PCR)	Alternate function[1], [2]	Functions	Peripheral[3]	I/O direction [4]	Pad speed[5]		Pin No.	
						SRC = 0	SRC = 1	100-pin	144-pin
D[14]	PCR[62]	ALT0 ALT1 ALT2 ALT3 —	GPIO[62] B[1] CS3 — SIN	SIUL FlexPWM_0 DSPI_3 — DSPI_3	I/O O O — I	Slow	Medium	73	105
D[15]	PCR[63]	ALT0 ALT1 ALT2 ALT3 —	GPIO[63] — — — AN[4]	SIUL — — — ADC_1	Input only	—	—	41	58
Port E(16-bit)									
E[0]	PCR[64]	ALT0 ALT1 ALT2 ALT3 —	GPIO[64] — — — AN[5]	SIUL — — — ADC_1	Input only	—	—	46	68
E[1]	PCR[65]	ALT0 ALT1 ALT2 ALT3 —	GPIO[65] — — — AN[4]	SIUL — — — ADC_0	Input only	—	—	27	39
E[2]	PCR[66]	ALT0 ALT1 ALT2 ALT3 —	GPIO[66] — — — AN[5]	SIUL — — — ADC_0	Input only	—	—	32	49
E[3]	PCR[67]	ALT0 ALT1 ALT2 ALT3 —	GPIO[67] — — — AN[6]	SIUL — — — ADC_0	Input only	—	—	—	40
E[4]	PCR[68]	ALT0 ALT1 ALT2 ALT3 —	GPIO[68] — — — AN[7]	SIUL — — — ADC_0	Input only	—	—	—	42

3 Electrical characteristics

3.1 Introduction

This section contains device electrical characteristics as well as temperature and power considerations.

This microcontroller contains input protection against damage due to high static voltages. However, it is advisable to take precautions to avoid application of any voltage higher than the specified maximum rated voltages.

To enhance reliability, unused inputs can be driven to an appropriate logic voltage level (V_{DD} or V_{SS}). This can be done by the internal pull-up or pull-down resistors, which are provided by the device for most general purpose pins.

The following tables provide the device characteristics and its demands on the system.

In the tables where the device logic provides signals with their respective timing characteristics, the symbol “CC” for Controller Characteristics is included in the Symbol column.

In the tables where the external system must provide signals with their respective timing characteristics to the device, the symbol “SR” for System Requirement is included in the Symbol column.

Caution: All of the following parameter values can vary depending on the application and must be confirmed during silicon characterization or silicon reliability trial.

3.2 Parameter classification

The electrical parameters are guaranteed by various methods. To give the customer a better understanding, the classifications listed in *Table 8* are used and the parameters are tagged accordingly in the tables where appropriate.

Table 8. Parameter classifications

Classification tag	Tag description
P	Those parameters are guaranteed during production testing on each individual device.
C	Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.
T	Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.
D	Those parameters are derived mainly from simulations.

Note: The classification is shown in the column labeled “C” in the parameter tables where appropriate.

2. Junction-to-board thermal resistance determined per JEDEC JESD51-8. Thermal test board meets JEDEC specification for the specified package.
3. Junction-to-case at the top of the package determined using MIL-STD 883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer.
4. Thermal characterization parameter indicating the temperature difference between the board and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JB.
5. Thermal characterization parameter indicating the temperature difference between the case and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JC.

Table 13. Thermal characteristics for 100-pin LQFP

Symbol	Parameter	Conditions	Typical value	Unit
$R_{\theta JA}$	Thermal resistance junction-to-ambient, natural convection(1)	Single layer board—1s	47.3	°C/W
		Four layer board—2s2p	35.3	°C/W
$R_{\theta JB}$	Thermal resistance junction-to-board(2)	Four layer board—2s2p	19.1	°C/W
$R_{\theta JCtop}$	Thermal resistance junction-to-case (top)(3)	Single layer board—1s	9.7	°C/W
Ψ_{JB}	Junction-to-board, natural convection(4)	Operating conditions	19.1	°C/W
Ψ_{JC}	Junction-to-case, natural convection(5)	Operating conditions	0.8	°C/W

1. Junction-to-ambient thermal resistance determined per JEDEC JESD51-7. Thermal test board meets JEDEC specification for this package.
2. Junction-to-board thermal resistance determined per JEDEC JESD51-8. Thermal test board meets JEDEC specification for the specified package.
3. Junction-to-case at the top of the package determined using MIL-STD 883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer.
4. Thermal characterization parameter indicating the temperature difference between the board and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JB.
5. Thermal characterization parameter indicating the temperature difference between the case and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JC.

3.5.2 General notes for specifications at maximum junction temperature

An estimation of the chip junction temperature, T_J, can be obtained from *Equation 1*:

Equation 1 $T_J = T_A + (R_{\theta JA} * P_D)$

where:

T_A = ambient temperature for the package (°C)

$R_{\theta JA}$ = junction to ambient thermal resistance (°C/W)

P_D = power dissipation in the package (W)

The junction to ambient thermal resistance is an industry standard value that provides a quick and easy estimation of thermal performance. Unfortunately, there are two values in

3.10.2 DC electrical characteristics (5 V)

Table 21 gives the DC electrical characteristics at 5 V (4.5 V < $V_{DD\_HV\_IOx}$ < 5.5 V, NVUSRO[PAD3V5V] = 0); see *Figure 14*.

Table 21. DC electrical characteristics (5.0 V, NVUSRO[PAD3V5V] = 0)

Symbol	C	Parameter	Conditions	Value		Unit
				Min	Max	
V_{IL}	D	Low level input voltage	—	–0.1(1)	—	V
	P		—	—	0.35 $V_{DD\_HV\_IOx}$	V
V_{IH}	P	High level input voltage	—	0.65 $V_{DD\_HV\_IOx}$	—	V
	D		—	—	$V_{DD\_HV\_IOx}$ + 0.1(1)	V
V_{HYS}	T	Schmitt trigger hysteresis	—	0.1 $V_{DD\_HV\_IOx}$	—	V
V_{OL_S}	P	Slow, low level output voltage	I_{OL} = 3 mA	—	0.1 $V_{DD\_HV\_IOx}$	V
V_{OH_S}	P	Slow, high level output voltage	I_{OH} = –3 mA	0.8 $V_{DD\_HV\_IOx}$	—	V
V_{OL_M}	P	Medium, low level output voltage	I_{OL} = 3 mA	—	0.1 $V_{DD\_HV\_IOx}$	V
V_{OH_M}	P	Medium, high level output voltage	I_{OH} = –3 mA	0.8 $V_{DD\_HV\_IOx}$	—	V
V_{OL_F}	P	Fast, low level output voltage	I_{OL} = 3 mA	—	0.1 $V_{DD\_HV\_IOx}$	V
V_{OH_F}	P	Fast, high level output voltage	I_{OH} = –3 mA	0.8 $V_{DD\_HV\_IOx}$	—	V
V_{OL_SYM}	P	Symmetric, low level output voltage	I_{OL} = 3 mA	—	0.1 $V_{DD\_HV\_IOx}$	V
V_{OH_SYM}	P	Symmetric, high level output voltage	I_{OH} = –3 mA	0.8 $V_{DD\_HV\_IOx}$	—	V
I_{PU}	P	Equivalent pull-up current	V_{IN} = V_{IL}	–130	—	µA
			V_{IN} = V_{IH}	—	–10	
I_{PD}	P	Equivalent pull-down current	V_{IN} = V_{IL}	10	—	µA
			V_{IN} = V_{IH}	—	130	
I_{IL}	P	Input leakage current (all bidirectional ports)	T_A = –40 to 125 °C	–1	1	µA
I_{IL}	P	Input leakage current (all ADC input-only ports)	T_A = –40 to 125 °C	–0.5	0.5	µA
C_{IN}	D	Input capacitance	—	—	10	pF
I_{PU}	D	$\overline{\text{RESET}}$, equivalent pull-up current	V_{IN} = V_{IL}	–130	—	µA
			V_{IN} = V_{IH}	—	–10	

1. “SR” parameter values must not exceed the absolute maximum ratings shown in *Table 9*.

Table 23. DC electrical characteristics (3.3 V, NVUSRO[PAD3V5V] = 1)(1) (continued)

Symbol	C	Parameter	Conditions	Value		Unit
				Min	Max	
V_{IH}	P	High level input voltage	—	0.65 $V_{DD\_HV\_IOx}$	—	V
	D		—	—	$V_{DD\_HV\_IOx}$ + 0.1(2)	V
V_{HYS}	T	Schmitt trigger hysteresis	—	0.1 $V_{DD\_HV\_IOx}$	—	V
V_{OL_S}	P	Slow, low level output voltage	I_{OL} = 1.5 mA	—	0.5	V
V_{OH_S}	P	Slow, high level output voltage	I_{OH} = –1.5 mA	$V_{DD\_HV\_IOx}$ – 0.8	—	V
V_{OL_M}	P	Medium, low level output voltage	I_{OL} = 2 mA	—	0.5	V
V_{OH_M}	P	Medium, high level output voltage	I_{OH} = –2 mA	$V_{DD\_HV\_IOx}$ – 0.8	—	V
V_{OL_F}	P	Fast, low level output voltage	I_{OL} = 1.5 mA	—	0.5	V
V_{OH_F}	P	Fast, high level output voltage	I_{OH} = –1.5 mA	$V_{DD\_HV\_IOx}$ – 0.8	—	V
V_{OL_SYM}	P	Symmetric, low level output voltage	I_{OL} = 1.5 mA	—	0.5	V
V_{OH_SYM}	P	Symmetric, high level output voltage	I_{OH} = –1.5 mA	$V_{DD\_HV\_IOx}$ – 0.8	—	V
I_{PU}	P	Equivalent pull-up current	V_{IN} = V_{IL}	–130	—	µA
			V_{IN} = V_{IH}	—	–10	
I_{PD}	P	Equivalent pull-down current	V_{IN} = V_{IL}	10	—	µA
			V_{IN} = V_{IH}	—	130	
I_{IL}	P	Input leakage current (all bidirectional ports)	T_A = –40 to 125 °C	—	1	µA
I_{IL}	P	Input leakage current (all ADC input-only ports)	T_A = –40 to 125 °C	—	0.5	µA
C_{IN}	D	Input capacitance	—	—	10	pF
I_{PU}	D	$\overline{\text{RESET}}$, equivalent pull-up current	V_{IN} = V_{IL}	–130	—	µA
			V_{IN} = V_{IH}	—	–10	

1. These specifications are design targets and subject to change per device characterization.
2. “SR” parameter values must not exceed the absolute maximum ratings shown in *Table 9*.

Table 26. I/O weight (continued)

Pad	LQFP144		LQFP100	
	Weight 5V	Weight 3.3V	Weight 5V	Weight 3.3V
PAD[86]	9%	6%	—	—
MODO[0]	12%	8%	—	—
PAD[7]	4%	4%	11%	10%
PAD[36]	5%	4%	11%	9%
PAD[8]	5%	4%	10%	9%
PAD[37]	5%	4%	10%	9%
PAD[5]	5%	4%	9%	8%
PAD[39]	5%	4%	9%	8%
PAD[35]	5%	4%	8%	7%
PAD[87]	12%	9%	—	—
PAD[88]	9%	6%	—	—
PAD[89]	10%	7%	—	—
PAD[90]	15%	11%	—	—
PAD[91]	6%	5%	—	—
PAD[57]	8%	7%	8%	7%
PAD[56]	13%	11%	13%	11%
PAD[53]	14%	12%	14%	12%
PAD[54]	15%	13%	15%	13%
PAD[55]	25%	22%	25%	22%
PAD[96]	27%	24%	—	—
PAD[65]	1%	1%	1%	1%
PAD[67]	1%	1%	—	—
PAD[33]	1%	1%	1%	1%
PAD[68]	1%	1%	—	—
PAD[23]	1%	1%	1%	1%
PAD[69]	1%	1%	—	—
PAD[34]	1%	1%	1%	1%
PAD[70]	1%	1%	—	—
PAD[24]	1%	1%	1%	1%
PAD[71]	1%	1%	—	—
PAD[66]	1%	1%	1%	1%
PAD[25]	1%	1%	1%	1%
PAD[26]	1%	1%	1%	1%

Table 27. I/O consumption (continued)

Symbol		C	Parameter	Conditions[1]		Value			Unit
						Min	Typ	Max	
I_{RMSMED}	CC	D	Root medium square I/O current for MEDIUM configuration	C_L = 25 pF, 13 MHz	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	6.6	mA
				C_L = 25 pF, 40 MHz		—	—	13.4	
				C_L = 100 pF, 13 MHz		—	—	18.3	
				C_L = 25 pF, 13 MHz	V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	5	
				C_L = 25 pF, 40 MHz		—	—	8.5	
				C_L = 100 pF, 13 MHz		—	—	11	
I_{RMSFST}	CC	D	Root medium square I/O current for FAST configuration	C_L = 25 pF, 40 MHz	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	22	mA
				C_L = 25 pF, 64 MHz		—	—	33	
				C_L = 100 pF, 40 MHz		—	—	56	
				C_L = 25 pF, 40 MHz	V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	14	
				C_L = 25 pF, 64 MHz		—	—	20	
				C_L = 100 pF, 40 MHz		—	—	35	
I_{AVGSEG}	SR	D	Sum of all the static I/O current within a supply segment	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0		—	—	70	mA
				V_{DD} = 3.3 V ± 10%, PAD3V5V = 1		—	—	65	

1. V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified
2. Stated maximum values represent peak consumption that lasts only a few ns during I/O transition.

3.11 Main oscillator electrical characteristics

The SPC560P44Lx, SPC560P50Lx provides an oscillator/resonator driver.

Table 28. Main oscillator output electrical characteristics (5.0 V, NVUSRO[PAD3V5V] = 0)

Symbol		C	Parameter	Value		Unit
				Min	Max	
f_{OSC}	SR	—	Oscillator frequency	4	40	MHz
g_m	—	P	Transconductance	6.5	25	mA/V
V_{OSC}	—	T	Oscillation amplitude on XTAL pin	1	—	V
t_{OSCSU}	—	T	Start-up time[1],[2]	8	—	ms

1. The start-up time is dependent upon crystal characteristics, board leakage, etc., high ESR and excessive capacitive loads can cause long start-up time.
2. Value captured when amplitude reaches 90% of XTAL

3.15 Flash memory electrical characteristics

Table 34. Program and erase specifications

Symbol	C	Parameter	Value				Unit
			Min	Typical(1)	Initial max(2)	Max(3)	
$T_{dwprogram}$	P	Double Word (64 bits) Program Time(4)	—	22	50	500	µs
T_{BKPRG}	P	Bank Program (512 KB)(4)(5)	—	1.45	1.65	33	s
	P	Bank Program (64 KB)(4)(5)	—	0.18	0.21	4.10	s
$T_{16kpperase}$	P	16 KB Block Pre-program and Erase Time	—	300	500	5000	ms
$T_{32kpperase}$	P	32 KB Block Pre-program and Erase Time	—	400	600	5000	ms
$T_{128kpperase}$	P	128 KB Block Pre-program and Erase Time	—	800	1300	7500	ms

1. Typical program and erase times assume nominal supply values and operation at 25 °C. All times are subject to change pending device characterization.
2. Initial factory condition: < 100 program/erase cycles, 25 °C, typical supply voltage.
3. The maximum program and erase times occur after the specified number of program/erase cycles. These maximum values are characterized but not guaranteed.
4. Actual hardware programming times. This does not include software overhead.
5. Typical Bank programming time assumes that all cells are programmed in a single pulse. In reality some cells will require more than one pulse, adding a small overhead to total bank programming time (see Initial Max column).

Table 35. Flash memory module life

Symbol	C	Parameter	Conditions	Value		Unit
				Min	Typ	
P/E	C	Number of program/erase cycles per block for 16 KB blocks over the operating temperature range (T_J)	—	100000	—	cycles
P/E	C	Number of program/erase cycles per block for 32 KB blocks over the operating temperature range (T_J)	—	10000	100000	cycles
P/E	C	Number of program/erase cycles per block for 128 KB blocks over the operating temperature range (T_J)	—	1000	100000	cycles
Retention	C	Minimum data retention at 85 °C average ambient temperature(1)	Blocks with 0–1000 P/E cycles	20	—	years
			Blocks with 10000 P/E cycles	10	—	years
			Blocks with 100000 P/E cycles	5	—	years

1. Ambient temperature averaged over duration of application, not to exceed recommended product operating temperature range.

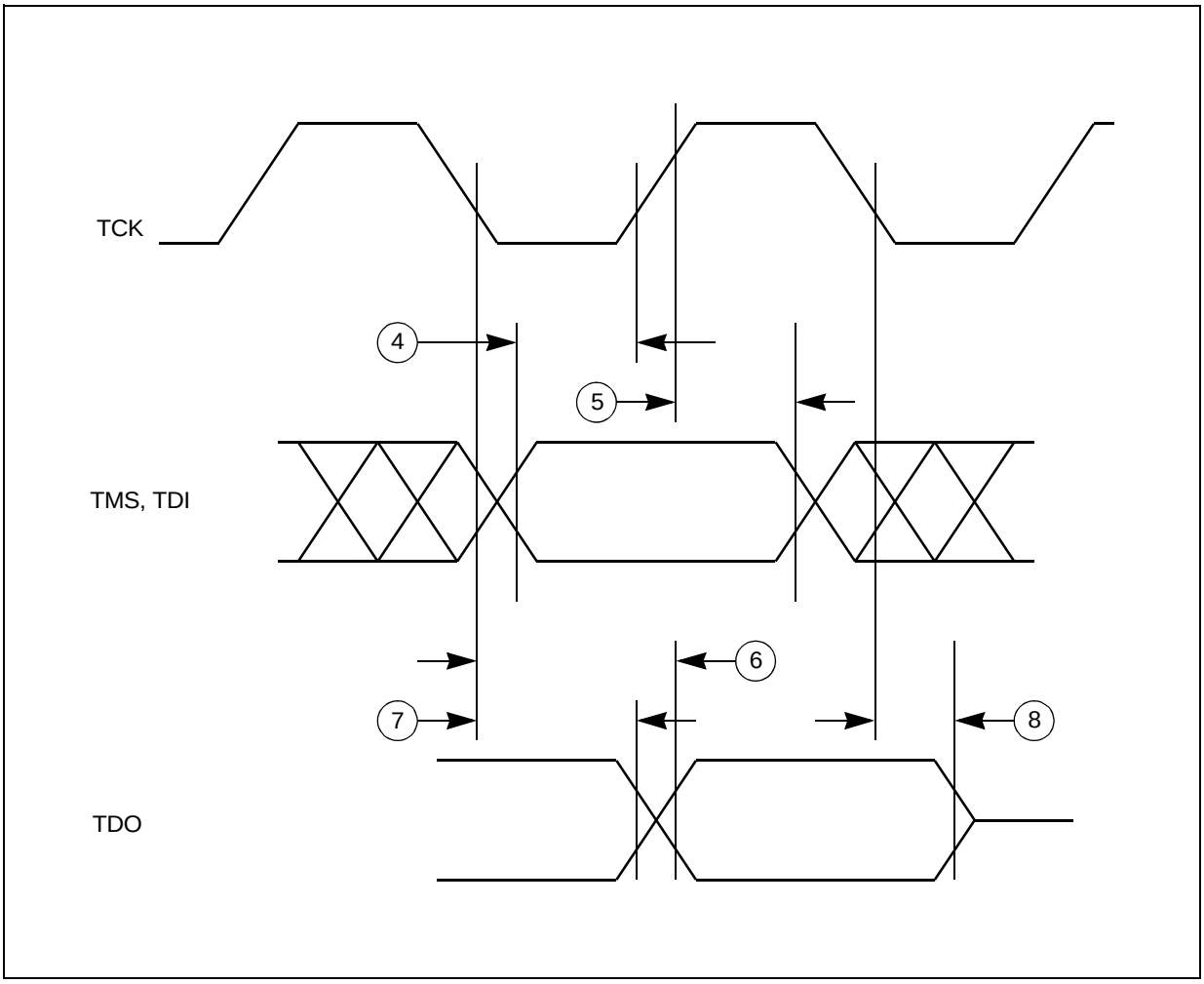


Figure 23. JTAG test access port timing

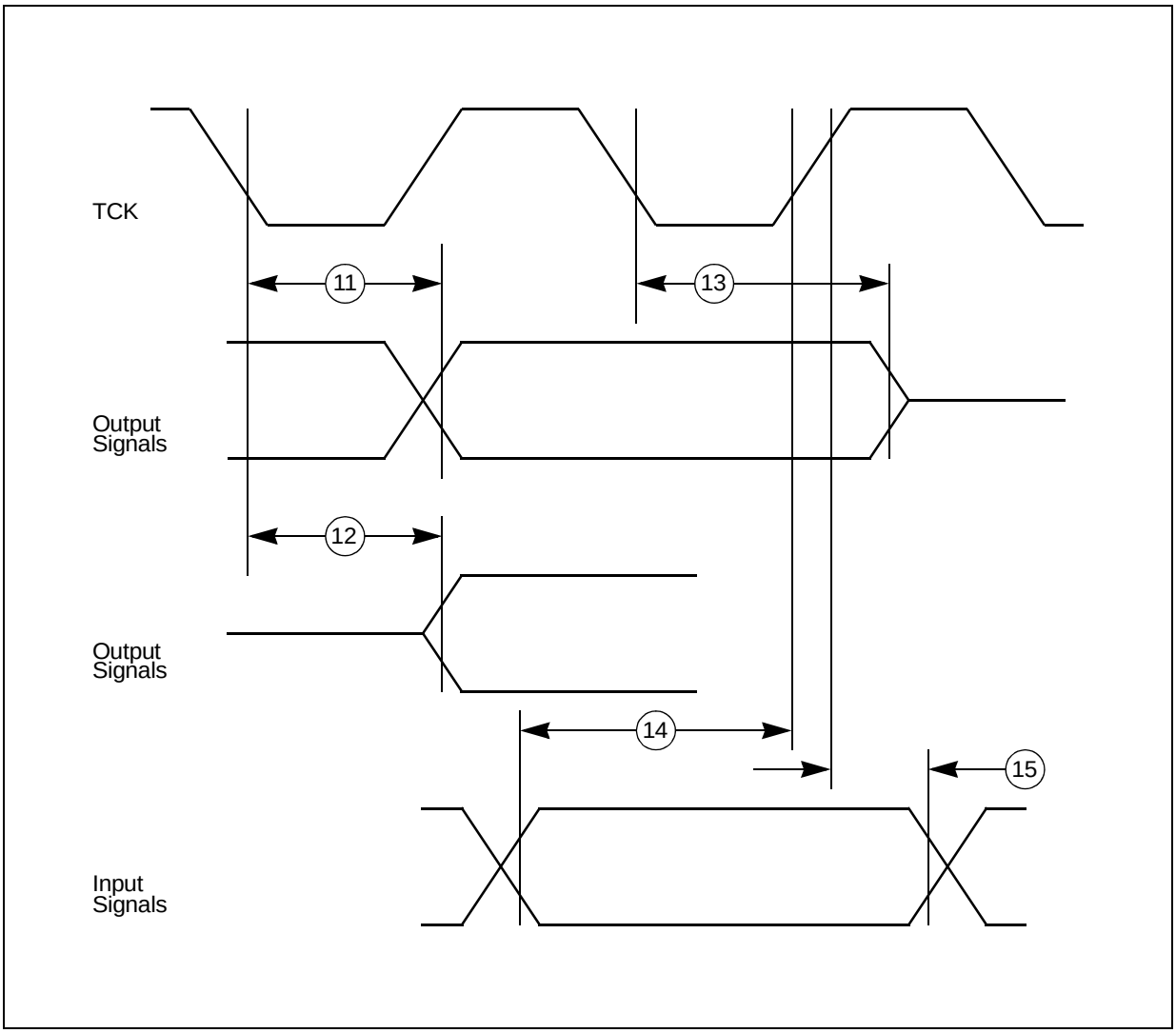


Figure 24. JTAG boundary scan timing

3.17.3 Nexus timing

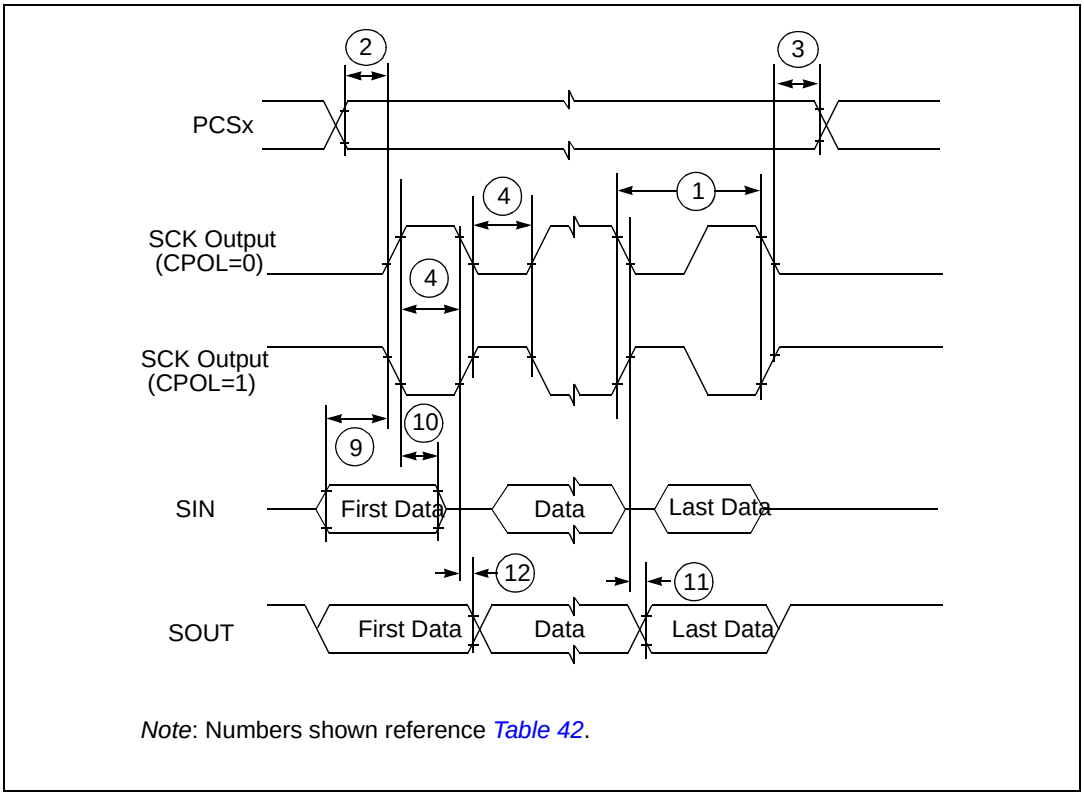
Table 40. Nexus debug port timing(1)

No.	Symbol		C	Parameter	Value			Unit
					Min	Typ	Max	
1	t_{MCYC}	CC	D	MCKO cycle time	32	—	—	ns
2	t_{MDOV}	CC	D	MCKO low to MDO data valid(2)	—	—	6	ns
3	t_{MSEOV}	CC	D	MCKO low to $\overline{\text{MSEO}}$ data valid(2)	—	—	6	ns
4	t_{EVTOV}	CC	D	MCKO low to $\overline{\text{EVTO}}$ data valid(2)	—	—	6	ns
5	t_{TCYC}	CC	D	TCK cycle time	64(3)	—	—	ns

Table 42. DSPI timing(1) (continued)

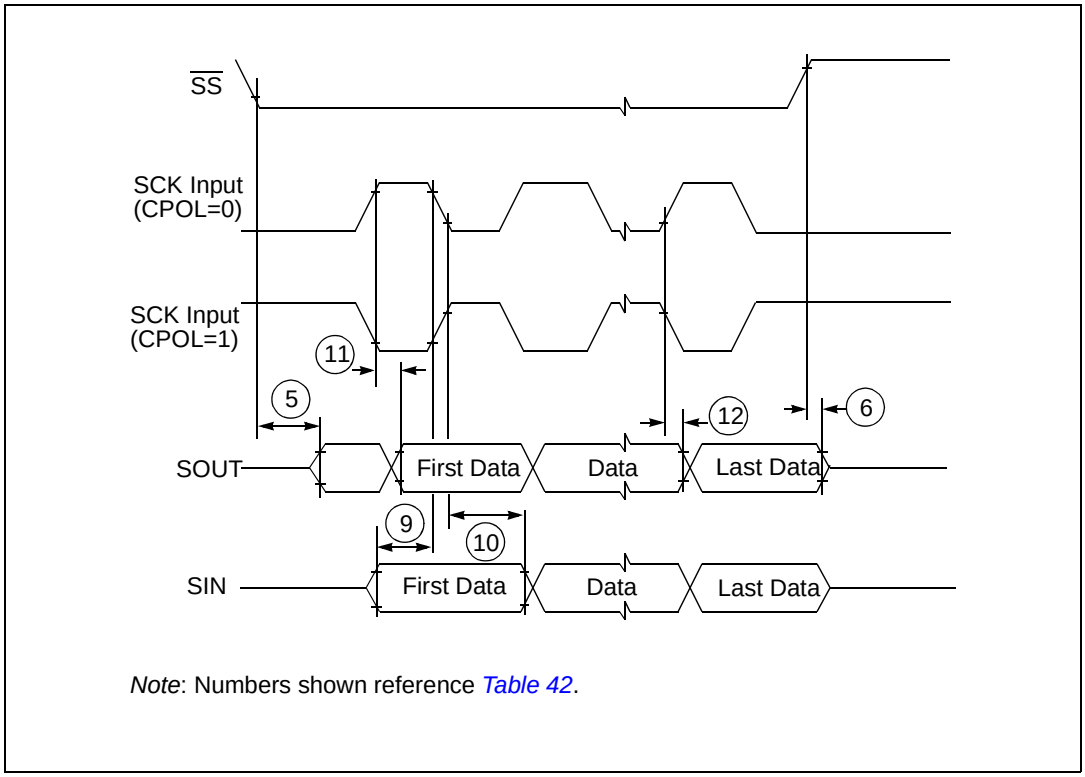
No.	Symbol		C	Parameter	Conditions	Value		Unit
						Min	Max	
11	t_{SUO}	CC	D	Data valid (after SCK edge)	Master (MTFE = 0)	—	12	ns
					Slave	—	36	
					Master (MTFE = 1, CPHA = 0)	—	12	
					Master (MTFE = 1, CPHA = 1)	—	12	
12	t_{HO}	CC	D	Data hold time for outputs	Master (MTFE = 0)	–2	—	ns
					Slave	6	—	
					Master (MTFE = 1, CPHA = 0)	6	—	
					Master (MTFE = 1, CPHA = 1)	–2	—	

1. All timing is provided with 50 pF capacitance on output, 1 ns transition time on input signal.



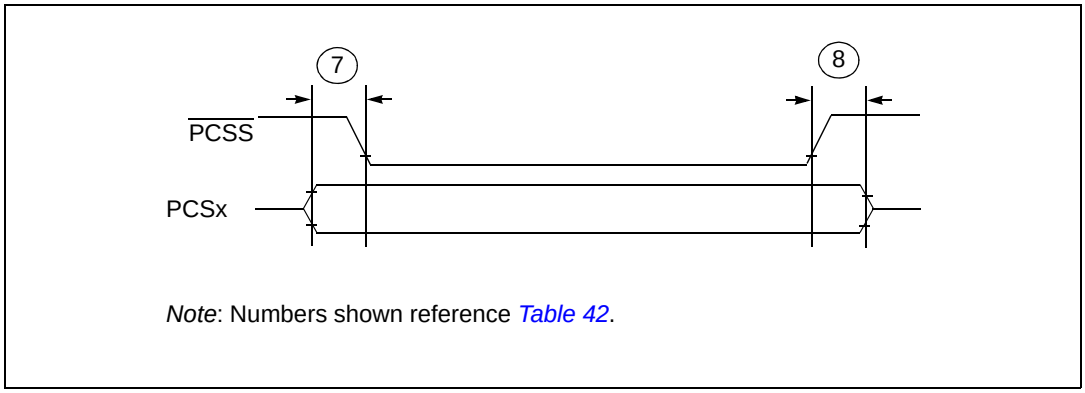
Note: Numbers shown reference *Table 42*.

Figure 29. DSPI classic SPI timing – Master, CPHA = 0



Note: Numbers shown reference *Table 42*.

Figure 36. DSPI modified transfer format timing – Slave, CPHA = 1



Note: Numbers shown reference *Table 42*.

Figure 37. DSPI PCS strobe ($\overline{\text{PCSS}}$) timing

4 Package characteristics

4.1 ECOPACK®

IIn order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

4.2 Package mechanical data

4.2.1 LQFP144 mechanical outline drawing

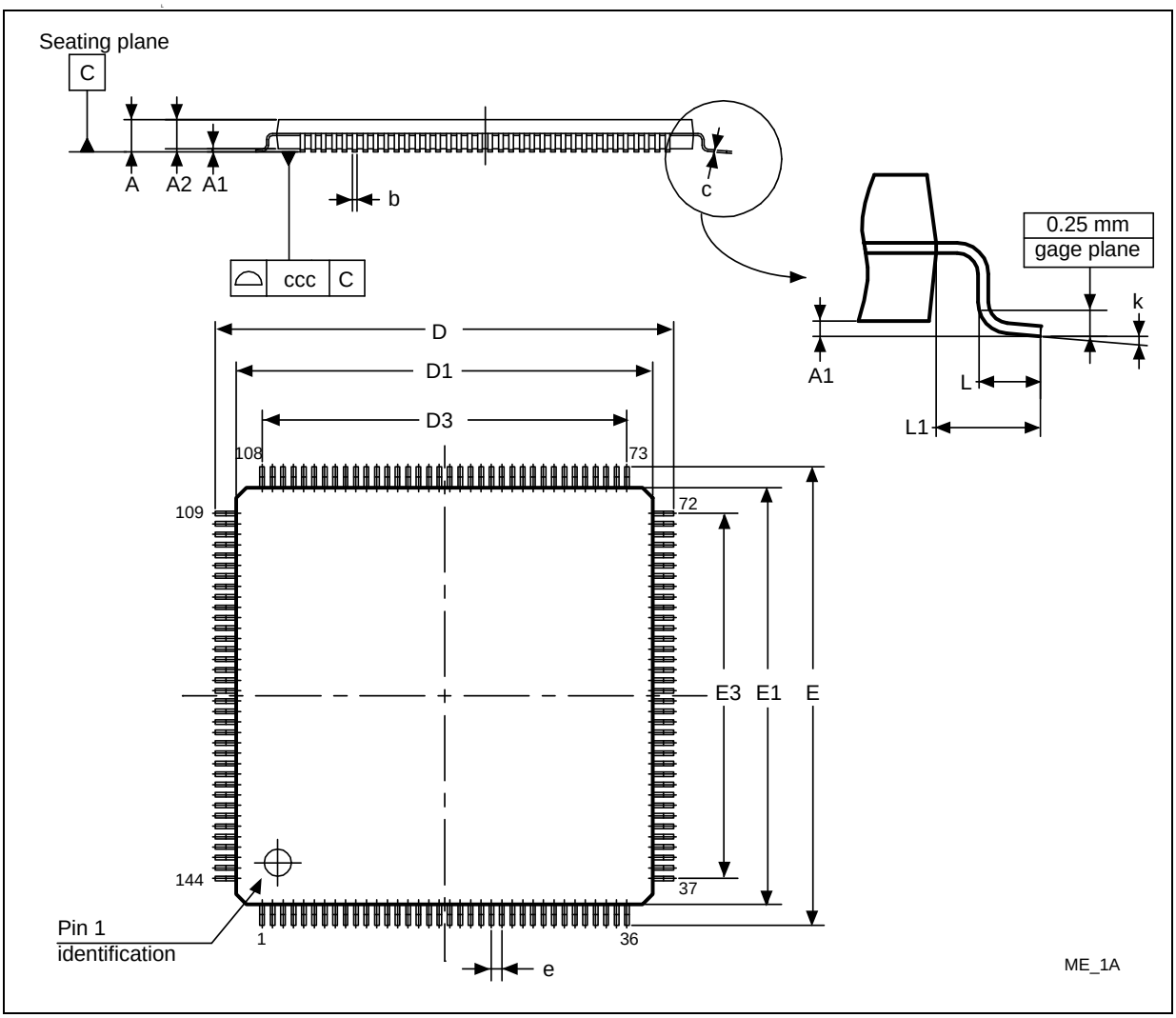


Figure 38. LQFP144 package mechanical drawing

4.2.2 LQFP100 mechanical outline drawing

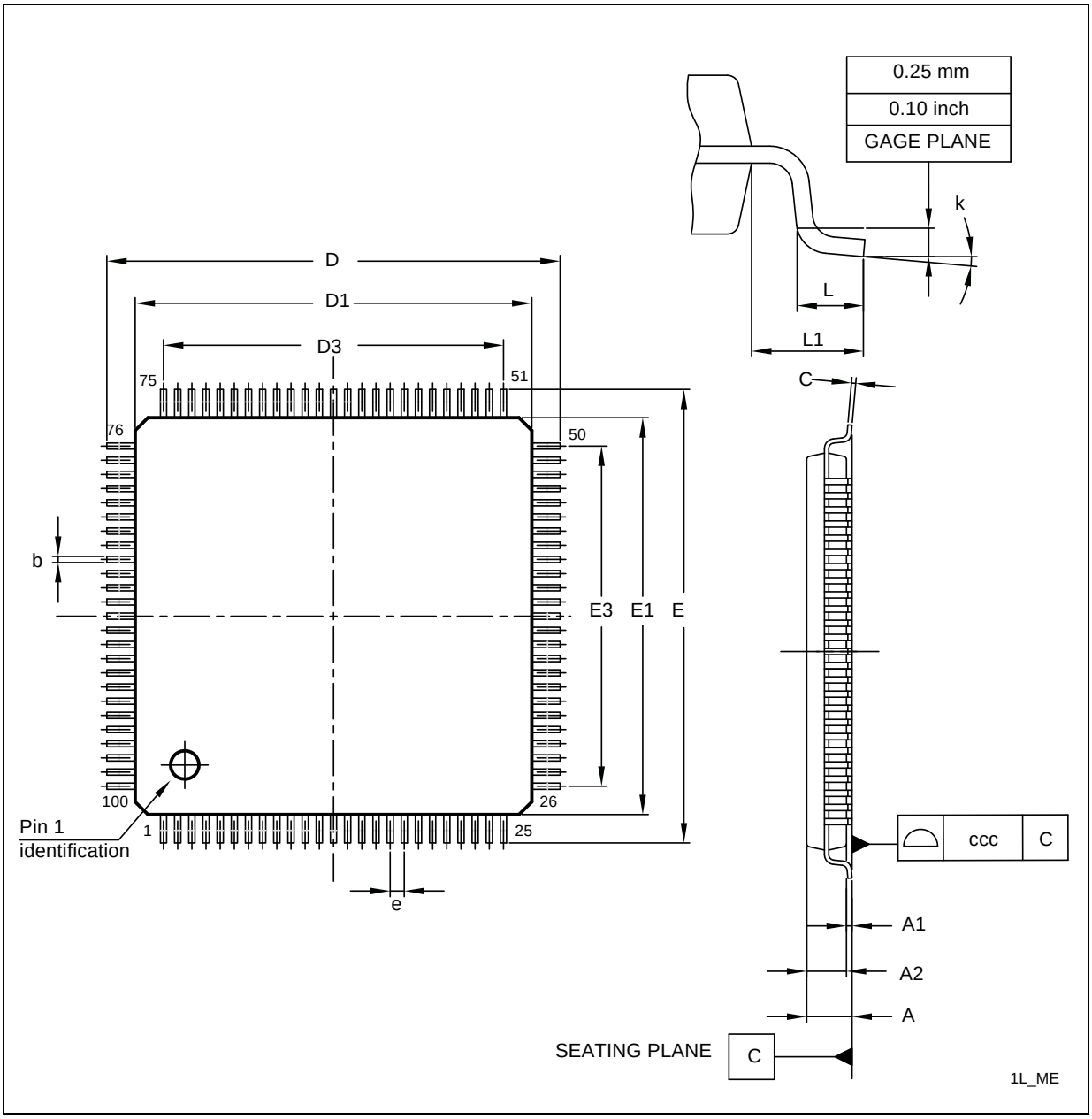


Figure 39. LQFP100 package mechanical drawing

5 Ordering information

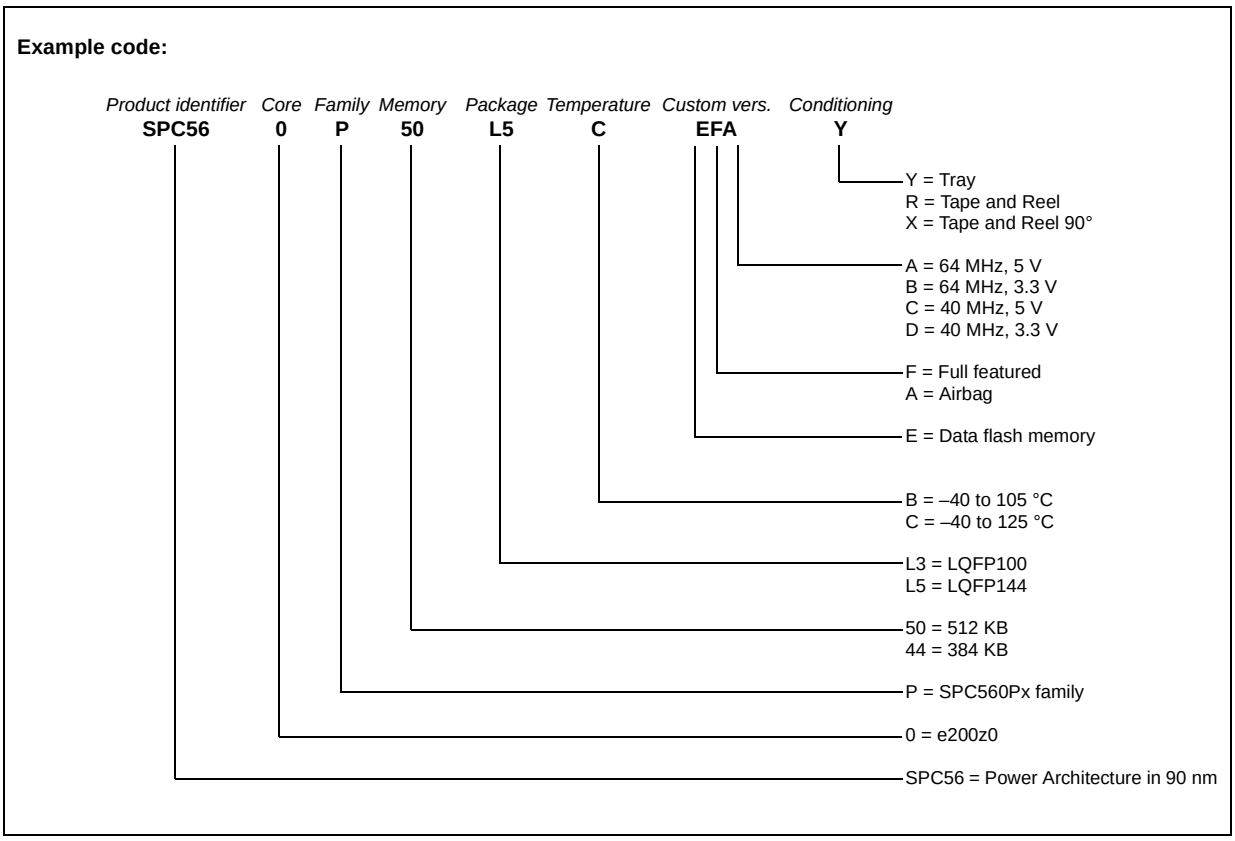


Figure 40. Commercial product code structure[(a)]

a. Not all configurations are available on the market. Please contact your ST sales representative to get the list of orderable commercial part number.

Table 46. Revision history (continued)

Date	Revision	Changes
07-Jul-2009	4	Through all document: – Replaced all “RESET_B” occurrences with “$\overline{\text{RESET}}$” through all document. – AC Timings: 1149.1 (JTAG) Timing, Nexus Timing, External Interrupt Timing, and DSPI Timing sections inserted again. – Electrical parameters updated. *Section , Features*: – Specified LIN 2.1 in communications interfaces feature. *Table 2* – Added row for Data Flash. *Table 4* – Added a footnote regarding the decoupling capacitors. *Table 6* – Removed the “other function“ column. – Rearranged the contents. *Table 14* – Updated definition of Condition column. *Table 19* – merged in an unique Table the power consumption data related to "Maximum mode" and "Airbag mode". *Table 21* – merged in an unique Table the power consumption data related to "Maximum mode" and "Airbag mode". *Table 29* – Updated the parameter definition of ΔRCMVAR. – Removed the condition definition of ΔRCMVAR. *Table 29* – Added t_{ADC_C} and TUE rows. *Table 30* – Added t_{ADC_C} and TUE rows. – Removed $R_{sw2.}$ *Table 33* – Added. *Table 29* – Updated and added footnotes. *Section 3.16.1 RESET Pin Characteristics* – Replaces whole section. *Table 38* – Renamed the “Flash (KB)“ heading column in “Code Flash / Data Flash (EE) (KB)“ – Replaced the value of RAM from 32 to 36KB in the last four rows.

Table 46. Revision history (continued)

Date	Revision	Changes
18-Jul-2012	8	Updated *Table 1 (Device summary)* *Section 1.5.4, Flash memory*: Changed “Data flash memory: 32-bit ECC” to “Data flash memory: 64-bit ECC” *Figure 40 (Commercial product code structure)*, replaced "C = 60 MHz, 5 V" and "D = 60 MHz, 3.3 V" with respectively "C = 40 MHz, 5 V" and "D = 40 MHz, 3.3 V" *Table 9 (Absolute maximum ratings)*, updated TV_{DD} parameter, the minimum value to 3.0 V/s and the maximum value to 0.5 V/µs *Table 7 (Pin muxing)*, changed the description in the column "I/O direction" from "I/O" to "O" for the following port pins: A[10] with function B[0] A[11] with function A[0] A[11] with function A[2] A[12] with function A[2] A[12] with function B[2] A[13] with function B[2] C[7] with function A[1] C[10] with function A[3] C[15] with function A[1] D[0] with function B[1] D[10] with function A[0] D[11] with function B[0] D[13] with function A[1] D[14] with function B[1] Updated *Section 3.8.1, Voltage regulator electrical characteristics* Added *Table 27 (I/O consumption)* *Section 3.10, DC electrical characteristics*: deleted references to “oscillator margin” deleted subsection “NVUSRO[OSCILLATOR_MARGIN] field description” *Table 21 (DC electrical characteristics (5.0 V, NVUSRO[PAD3V5V] = 0))*, added IPU row for $\overline{\text{RESET}}$ pin *Table 23 (DC electrical characteristics (3.3 V, NVUSRO[PAD3V5V] = 1))*, added IPU row for $\overline{\text{RESET}}$ pin *Table 33 (ADC conversion characteristics)*, added V_{INAN} entry Removed “Order codes” table *Figure 40 (Commercial product code structure)*: added a footnote updated “E = Data flash memory”
18-Sep-2013	9	Updated Disclaimer