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Understanding Embedded - Microprocessors

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Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM® Cortex®-A8
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	600MHz
Co-Processors/DSP	Multimedia; NEON™ SIMD
RAM Controllers	LPDDR, DDR2
Graphics Acceleration	Yes
Display & Interface Controllers	Keypad, LCD
Ethernet	10/100Mbps (1)
SATA	-
USB	USB 2.0 (3), USB 2.0 + PHY (1)
Voltage - I/O	1.2V, 1.875V, 2.775V, 3.0V
Operating Temperature	-40°C ~ 125°C (TJ)
Security Features	ARM TZ, Boot Security, Cryptography, RTIC, Secure Fusebox, Secure JTAG, Secure Memory, Secure RTC
Package / Case	529-LFBGA
Supplier Device Package	529-BGA (19x19)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mcimx514ajm6cr2

Table 2. i.MX51A Digital and Analog Modules (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
EMI	External Memory Interface	Connectivity Peripherals	The EMI is an external and internal memory interface. It performs arbitration between multi-AXI masters to multi-memory controllers, divided into four major channels: fast memories (Mobile DDR, DDR2) channel, slow memories (NOR-FLASH/PSRAM/NAND-FLASH and so on) channel, internal memory (RAM, ROM) channel and graphical memory (GMEM) Channel. In order to increase the bandwidth performance, the EMI separates the buffering and the arbitration between different channels so parallel accesses can occur. By separating the channels, slow accesses do not interfere with fast accesses. EMI features: • 64-bit and 32-bit AXI ports • Enhanced arbitration scheme for fast channel, including dynamic master priority, and taking into account which pages are open or closed and what type (Read or Write) was the last access • Flexible bank interleaving • Supports 16/32-bit Mobile DDR up to 200 MHz SDCLK (mDDR400) • Supports 16/32-bit (Non-Mobile) DDR2 up to 200 MHz SDCLK (DDR2-400) • Supports up to 2 Gbit Mobile DDR memories • Supports 16-bit (in muxed mode only) PSRAM memories (sync and async operating modes), at slow frequency, for debugging purposes • Supports 32-bit NOR-Flash memories (only in muxed mode), at slow frequencies for debugging purposes • Supports 4/8-ECC, page sizes of 512 Bytes, 2 Kbytes and 4 Kbytes • NAND-Flash (including MLC) • Multiple chip selects • Enhanced Mobile DDR memory controller, supporting access latency hiding • Supports watermarking for security (Internal and external memories) • Supports Samsung OneNAND™ (only in muxed I/O mode)
EPIT-1 EPIT-2	Enhanced Periodic Interrupt Timer	Timer Peripherals	Each EPIT is a 32-bit “set and forget” timer that starts counting after the EPIT is enabled by software. It is capable of providing precise interrupts at regular intervals with minimal processor intervention. It has a 12-bit prescaler for division of input clock frequency to get the required time setting for the interrupts to occur, and counter values can be programmed on the fly.
eSDHC-1 eSDHC-2 eSDHC-3	Enhanced Multi-Media Card/ Secure Digital Host Controller	Connectivity Peripherals	The features of the eSDHC module, when serving as host, include the following: • Conforms to SD Host Controller Standard Specification version 2.0 • Compatible with the MMC System Specification version 4.2 • Compatible with the SD Memory Card Specification version 2.0 • Compatible with the SDIO Card Specification version 1.2 • Designed to work with SD Memory, miniSD Memory, SDIO, miniSDIO, SD Combo, MMC and MMC RS cards • Configurable to work in one of the following modes: —SD/SDIO 1-bit, 4-bit —MMC 1-bit, 4-bit, 8-bit • Full-/high-speed mode • Host clock frequency variable between 32 kHz to 52 MHz • Up to 200 Mbps data transfer for SD/SDIO cards using four parallel data lines • Up to 416 Mbps data transfer for MMC cards using eight parallel data lines

Table 2. i.MX51A Digital and Analog Modules (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
TZIC	TrustZone Aware Interrupt Controller	ARM/Control	The TrustZone Interrupt Controller (TZIC) collects interrupt requests from all i.MX51 sources and routes them to the ARM core. Each interrupt can be configured as a normal or a secure interrupt. Software Force Registers and software Priority Masking are also supported.
UART-1 UART-2 UART-3	UART Interface	Connectivity Peripherals	Each of the UART modules supports the following serial data transmit/receive protocols and configurations: • 7 or 8 bit data words, 1 or 2 stop bits, programmable parity (even, odd, or none) • Programmable baud rates up to 4 MHz. This is a higher max baud rate relative to the 1.875 MHz, which is stated by the TIA/EIA-232-F standard and previous Freescale UART modules. • 32-byte FIFO on Tx and 32 half-word FIFO on Rx supporting auto-baud • IrDA 1.0 support (up to SIR speed of 115200 bps) • Option to operate as 8-pins full UART, DCE, or DTE
USB	USB 2.0 High-Speed OTG and 3x Hosts	Connectivity Peripherals	USB-OTG contains one high-speed OTG module, which is internally connected to the on-chip HS USB PHY. There are an additional three high-speed host modules that require external USB PHYs.
VPU	Video Processing Unit	Multimedia Peripherals	A high-performing video processing unit (VPU), which covers many SD-level video decoders and SD-level encoders as a multi-standard video codec engine as well as several important video processing such as rotation and mirroring. VPU Features: • MPEG-4 decode: 720p, 30 fps, simple profile and advanced simple profile • MPEG-4 encode: D1, 25/30 fps, simple profile • H.263 decode: 720p, 30 fps, profile 3 • H.263 encode: D1, 25/30 fps, profile 3 • H.264 decode: 720p, 30 fps, baseline, main, and high profile • H.264 encode: D1, 25/30 fps, baseline profile • MPEG-2 decode: 720p, 30 fps, MP-ML • MPEG-2 encode: D1, 25/30 fps, MP-ML (in software with partial acceleration in hardware) • VC-1 decode: 720p, 30 fps, simple, main, and advanced profile • DivX decode: 720p, 30 fps versions 3, 4, and 5 • RV10 decode: 720p, 30 fps • MJPEG decode: 32 Mpix/s • MJPEG encode: 64 Mpix/s
WDOG-1	Watch Dog	Timer Peripherals	The Watch Dog Timer supports two comparison points during each counting period. Each of the comparison points is configurable to evoke an interrupt to the ARM core, and a second point evokes an external event on the WDOG line.

Table 13 shows the i.MX51 operating ranges.

Table 13. i.MX51A Operating Ranges

Symbol	Parameter	Minimum[1]	Nominal[2]	Maximum[1]	Unit
VDDGP MCIMX51xA products	ARM core supply voltage $0 < f_{ARM} \leq 600$ MHz	0.95	1.0	1.1	V
	ARM core supply voltage Stop mode	0.9	0.95	1.05	V
VCC MCIMX51xA products	Peripheral supply voltage High Performance Mode (HPM) The clock frequencies are derived from AXI and AHB buses using 133 or 166 MHz (as needed). The DDR clock rate is 200 MHz. **Note:** For detailed information about the use of 133 or 166 MHz clocks, see i.MX51 Multimedia Applications Processor Reference Manual (MCIMX51RM).	1.175	1.225	1.275	V
	Peripheral supply voltage—Stop mode	0.9	0.95	1.275	V
VDDA	Memory arrays voltage—Run Mode	1.15	1.20	1.275	V
	Memory arrays voltage—Stop Mode	0.9	0.95	1.275	V
VDD_DIG_PLL_A VDD_DIG_PLL_B	PLL Digital supplies	1.15	1.2	1.35	V
VDD_ANA_PLL_A VDD_ANA_PLL_B	PLL Analog supplies	1.75	1.8	1.95	V
NVCC_EMI NVCC_PER5 NVCC_PER10 NVCC_PER11 NVCC_PER12 NVCC_PER13 NVCC_PER14	GPIO EMI Supply and additional digital power supplies.	1.65	1.875 or 2.775	3.1	V
NVCC_IPUx[3] NVCC_PER3 NVCC_PER8 NVCC_PER9	GPIO IPU Supply and additional digital power supplies.	1.65	1.875 or 2.775	3.1	V
NVCC_EMI_DRAM	DDR and Fuse Read Supply	1.65	1.8	1.95	V
VDD_FUSE[4]	Fusebox Program Supply (Write Only)	3.0	—	3.3	V
NVCC_NANDF_x[5] NVCC_PER15 NVCC_PER17	Ultra High voltage I/O (UHVIO) supplies		—		V
	UHVIO_L	1.65	1.875	1.95	
	UHVIO_H	2.5	2.775	3.1	
	UHVIO_UH	3.0	3.3	3.6	
NVCC_USBPHY NVCC_OSC	USB_PHY analog supply, oscillator analog supply[6]	2.25	2.5	2.75	V
TVDAC_DHVDD, NVCC_TV_BACK, AHVDDRGB	TVE-to-DAC level shifter supply, cable detector supply, analog power supply to RGB channel	2.69	2.75	2.91	V

4.3.7 USB Port Electrical DC Characteristics

Table 23 and Table 24 list the electrical DC characteristics.

Table 23. USBOTG Interface Electrical Specification

Parameter	Symbol	Signals	Min	Max	Unit	Test Conditions
Input High Voltage	VIH	USB_VPOUT USB_VMOUT USB_XRXD, USB_VPIN, USB_VMIN	VDD x 0.7	VDD	V	—
Input low Voltage	VIL	USB_VPOUT USB_VMOUT USB_XRXD, USB_VPIN, USB_VMIN	0	VDD × 0.3	V	—
Output High Voltage	VOH	USB_VPOUT USB_VMOUT USB_TXENB	VDD – 0.43	—	V	7 mA Drv at IOH = 5 mA
Output Low Voltage	VOL	USB_VPOUT USB_VMOUT USB_TXENB	—	0.43	V	7 mA Drv at IOH = 5 mA

Table 24. USB Interface Electrical Specification

Parameter	Symbol	Signals	Min	Max	Unit	Test Conditions
Input High Voltage	VIH	USB_DAT_VP USB_SE0_VM USB_RCV, USB_VP1, USB_VM1	VDD x 0.7	VDD	V	—
Input Low Voltage	VIL	USB_DAT_VP USB_SE0_VM USB_RCV, USB_VP1, USB_VM1	0	VDD x 0.3	V	—
Output High Voltage	VOH	USB_DAT_VP USB_SE0_VM USB_TXOE_B	VDD –0.43	—	V	7 mA Drv at Iout = 5 mA
Output Low Voltage	VOL	USB_DAT_VP USB_SE0_VM USB_TXOE_B	—	0.43	V	7 mA Drv at Iout = 5 mA

Figure 6 depicts the load circuit for output pads for standard- and fast-mode. Figure 7 depicts the output pad transition time definition. Figure 8 depicts load circuit with external pull-up current source for HS-mode. Figure 9 depicts HS-mode timing definition.

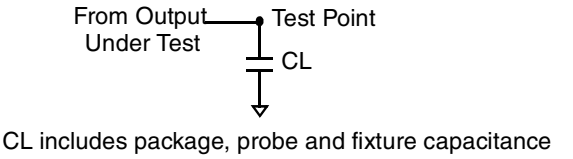


Figure 6. Load Circuit for Standard and Fast-Mode

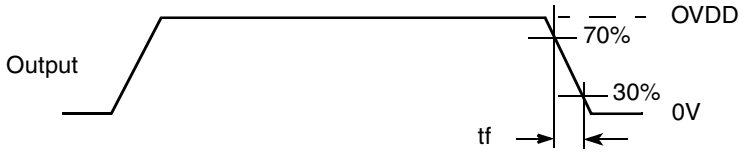
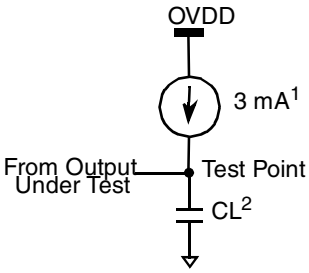
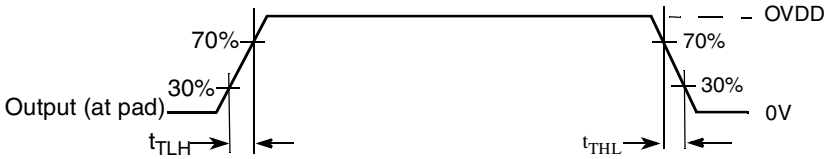


Figure 7. Definition of Timing for Standard and Fast-Mode



Notes:
[1]Load current when output is between 0.3×OVDD and 0.7×OVDD
[2]CL includes package, probe, and fixture capacitance.

Figure 8. Load Circuit for HS-Mode with External Pull-Up Current Source



PA3Max = max of t_{TLH} and t_{THL}
PA4Max = max t_{THL}

Figure 9. Definition of Timing for HS-Mode

1 Max condition for tpr, tpo, tps and didt: wcs model, 1.1 V, IO 1.65 V, 105 °C and s0-s5=111111. Typ condition for tpr, tpo, tps and didt: typ model, 1.2 V, IO 1.8 V, 25 °C and s0-s5=101010. Min condition for tpr, tpo, tps and didt: bcs model, 1.3 V, IO 1.95 V, –40 °C and s0-s5=000000.

2 Max condition for trfi and tpi: wcs model, 1.1 V, IO 1.65 V and 105 °C. Typ condition for trfi and tpi: typ model, 1.2 V, IO 1.8 V and 25 °C. Min condition for trfi and tpi: bcs model, 1.3 V, IO 1.95 V and –40 °C.

3 Hysteresis mode is recommended for input with transition time greater than 25 ns.

AC electrical characteristics in DDR2 mode for Fast mode and for ovdd=1.65–1.95V, ipp_hve=0 are placed in Table 41.

Table 41. AC Electrical Characteristics of DDR2_clk IO Pads for Fast mode and for ovdd=1.65–1.95 V

Parameter	Symbol	Test Condition	Min rise/fall	Typ	Max rise/fall	Units
Output Pad Transition Times[1]	tpr	15pF 35pF	0.58/0.57 1.29/1.28	0.45/0.44 0.97/0.93	0.45/0.45 0.82/0.85	ns
Output Pad Propagation Delay, 50%-50%[1]	tpo	15pF 35pF	1.05/1.03 1.54/1.56	1.40/1.31 1.75/1.69	2.12/1.96 2.43/2.31	ns
Output Pad Slew Rate[1]	tps	15pF 35pF	2.02/2.05 0.91/0.91	2.40/2.45 1.11/1.16	2.20/2.20 1.21/1.16	V/ns
Output Pad di/dt[1]	di/dt	—	390	201	99	mA/ns
Input Pad Transition Times[2]	trfi	1.2 pF	0.09/0.09	0.132/0.128	0.212/0.213	ns
Input Pad Propagation Delay (DDR input), 50%-50%[2]	tpi	1.2 pF	0.3/0.36	0.5/0.52	0.82/0.94	ns
Maximum Input Transition Times[3]	trm	—	—	—	5	ns

1 Max condition for tpr, tpo, tps and didt: wcs model, 1.1 V, IO 1.65 V, 105 °C and s0-s5=111111. Typ condition for tpr, tpo, tps and didt: typ model, 1.2 V, IO 1.8 V, 25 °C and s0-s5=101010. Min condition for tpr, tpo, tps and didt: bcs model, 1.3 V, IO 1.95 V, -40 °C and s0-s5=000000.

2 Max condition for trfi and tpi: wcs model, 1.1 V, IO 1.65 V and 105 °C. Typ condition for trfi and tpi: typ model, 1.2 V, IO 1.8 V and 25 °C. Min condition for trfi and tpi: bcs model, 1.3 V, IO 1.95 V and -40 °C.

3 Hysteresis mode is recommended for input with transition time greater than 25 ns.

AC electrical characteristics in DDR2 mode for Slow mode and for ovdd=1.65-1.95V, ipp_hve=0 are placed in Table 42.

Table 42. AC Electrical Characteristics of DDR2_clk IO Pads for Slow mode and for ovdd=1.65 – 1.95 V (ipp_hve=0)

Parameter	Symbol	Test Condition	Min rise/fall	Typ	Max rise/fall	Units
Output Pad Transition Times[1]	tpr	15pF 35pF	0.74/0.76 1.40/1.39	0.69/0.72 1.18/1.20	1.04/1.01 1.48/1.47	ns
Output Pad Propagation Delay, 50%-50%[1]	tpo	15pF 35pF	1.56/1.61 2.12/2.22	2.02/2.08 2.49/2.61	3.45/3.33 4.05/3.98	ns
Output Pad Slew Rate[1]	tps	15pF 35pF	1.58/1.54 0.84/0.84	1.57/1.50 0.92/0.90	0.95/0.98 0.67/0.67	V/ns

Table 42. AC Electrical Characteristics of DDR2_clk IO Pads for Slow mode and for ovdd=1.65 – 1.95 V (ipp_hve=0) (continued)

Parameter	Symbol	Test Condition	Min rise/fall	Typ	Max rise/fall	Units
Output Pad di/dt[1]	di/dt	—	82	40	19	mA/ns
Input Pad Transition Times[2]	trfi	1.2 pF	0.09/0.09	0.132/0.128	0.212/0.213	ns
Input Pad Propagation Delay (DDR input), 50%-50%[2]	tpi	1.2 pF	0.3/0.36	0.5/0.52	0.82/0.94	ns
Maximum Input Transition Times[3]	trm	—	—	—	5	ns

1 Max condition for tpr, tpo, tps and didt: wcs model, 1.1 V, IO 1.65 V, 105 °C and s0-s5=111111. Typ condition for tpr, tpo, tps and didt: typ model, 1.2 V, IO 1.8 V, 25 °C and s0-s5=101010. Min condition for tpr, tpo, tps and didt: bcs model, 1.3 V, IO 1.95 V, -40 °C and s0-s5=000000.

2 Max condition for trfi and tpi: wcs model, 1.1 V, IO 1.65 V and 105 °C. Typ condition for trfi and tpi: typ model, 1.2 V, IO 1.8 V and 25 °C. Min condition for trfi and tpi: bcs model, 1.3 V, IO 1.95 V and -40 °C.

3 Hysteresis mode is recommended for input with transition time greater than 25 ns.

AC electrical characteristics in DDR mobile for Fast mode and ovdd=1.65-1.95V, ipp_hve=0 are placed in Table 43.

Table 43. AC Electrical Characteristics of DDR_clk mobile IO Pads for Fast mode and ovdd=1.65 – 1.95 V (ipp_hve=0)

Parameter	Symbol	Test Condition	Min rise/fall	Typ	Max rise/fall	Units
Output Pad Transition Times (High Drive)[1]	tpr	15pF 35pF	1.35/1.32 3.01/2.96	1.03/1.03 2.29/2.30	0.89/0.89 1.84/1.92	ns
Output Pad Transition Times (Medium Drive)[1]	tpr	15pF 35pF	1.98/1.98 4.52/4.38	1.55/1.54 3.46/3.45	1.29/1.30 2.80/2.88	ns
Output Pad Transition Times (Low Drive)[1]	tpr	15pF 35pF	3.99/3.94 8.93/8.86	3.10/3.04 6.77/6.85	2.50/2.57 5.40/5.68	ns
Output Pad Propagation Delay (High Drive)[1]	tpo	15pF 35pF	1.60/1.58 2.74/2.81	1.85/1.74 2.71/2.67	2.58/2.31 3.26/3.08	ns
Output Pad Propagation Delay (Medium Drive)[1]	tpo	15pF 35pF	2.07/2.08 3.79/3.92	2.19/2.12 3.46/3.51	2.86/2.62 3.87/3.77	ns
Output Pad Propagation Delay (Low Drive)[1]	tpo	15pF 35pF	3.47/3.57 6.94/7.26	3.23/3.25 5.84/6.06	3.69/3.55 5.73/5.87	ns
Output Pad Slew Rate (High Drive)[1]	tps	15pF 35pF	0.87/0.89 0.39/0.40	1.05/1.05 0.47/0.47	1.11/1.11 0.54/0.52	V/ns
Output Pad Slew Rate (Medium Drive)[1]	tps	15pF 35pF	0.59/0.59 0.26/0.27	0.70/0.70 0.31/0.31	0.77/0.76 0.35/0.34	V/ns
Output Pad Slew Rate (Low Drive)[1]	tps	15pF 35pF	0.29/0.30 0.13/0.13	0.35/0.36 0.16/0.16	0.40/0.39 0.18/0.17	V/ns
Output Pad di/dt (High Drive)[1]	di/dt	—	185	91	46	mA/ns
Output Pad di/dt (Medium drive)[1]	di/dt	—	124	61	31	mA/ns

1 t is the maximal WEIM logic (axi_clk) cycle time. The maximum allowed axi_clk frequency is 133 MHz, whereas the maximum allowed BCLK frequency is 104 MHz. As a result, if BCD = 0, axi_clk must be ≤ 104 MHz. If BCD = 1, then 133 MHz is allowed for axi_clk, resulting in a BCLK of 66.5 MHz. When the clock branch to WEIM is decreased to 104 MHz, other busses are impacted which are clocked from this source. See the CCM chapter of the i.MX51 Reference Manual for a detailed clock tree description.

2 BCLK parameters are being measured from the 50% point, that is, high is defined as 50% of signal value and low is defined as 50% as signal value.

3 For signal measurements “High” is defined as 80% of signal value and “Low” is defined as 20% of signal value.

4.6.7.4 Examples of WEIM Synchronous Accesses

Figure 22 to Figure 25 provide few examples of basic WEIM accesses to external memory devices with the timing parameters mentioned previously for specific control parameters settings.

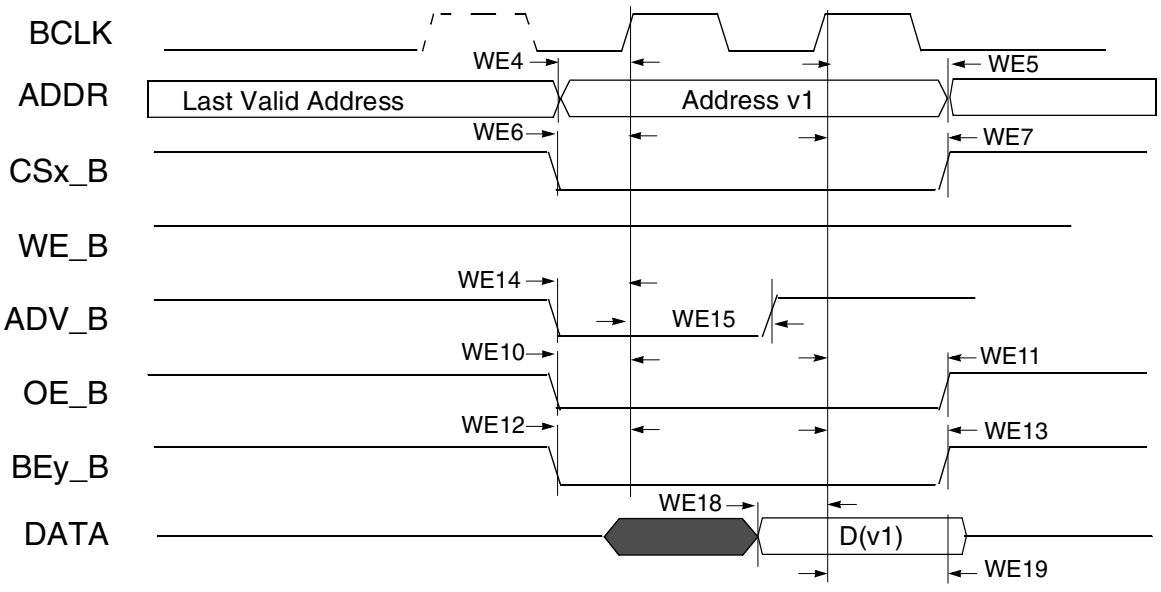


Figure 22. Synchronous Memory Read Access, WSC=1

Table 69. eSDHCv2 Interface Timing Specification (continued)

ID	Parameter	Symbols	Min	Max	Unit
SD7	eSDHC Input Setup Time	t_{ISU}	2.5	—	ns
SD8	eSDHC Input Hold Time	t_{IH}[5]	2.5	—	ns

1 In low speed mode, card clock must be lower than 400 kHz, voltage ranges from 2.7 to 3.6 V.

2 In normal speed mode for SD/SDIO card, clock frequency can be any value between 0–25 MHz. In high-speed mode, clock frequency can be any value between 0–50 MHz.

3 In normal speed mode for MMC card, clock frequency can be any value between 0–20 MHz. In high-speed mode, clock frequency can be any value between 0–52 MHz.

4 Measurement taken with CLoad = 20 pF

5 To satisfy hold timing, the delay difference between clock input and cmd/data input must not exceed 2 ns.

4.7.4 FEC AC Timing Parameters

This section describes the electrical information of the Fast Ethernet Controller (FEC) module. The FEC is designed to support both 10 and 100 Mbps Ethernet/IEEE 802.3 networks. An external transceiver interface and transceiver function are required to complete the interface to the media. The FEC supports the 10/100 Mbps MII (18 pins in total) and the 10 Mbps-only 7-wire interface, which uses 7 of the MII pins, for connection to an external Ethernet transceiver. For the pin list of MII and 7-wire, see i.MX51 Multimedia Applications Processor Reference Manual (MCIMX51RM).

This section describes the AC timing specifications of the FEC.

4.7.4.1 MII Receive Signal Timing

The MII receive signal timing involves the FEC_RXD[3:0], FEC_RX_DV, FEC_RX_ER, and FEC_RX_CLK signals. The receiver functions correctly up to a FEC_RX_CLK maximum frequency of 25 MHz + 1%. There is no minimum frequency requirement but the processor clock frequency must exceed twice the FEC_RX_CLK frequency. Table 70 lists the MII receive channel signal timing parameters and Figure 43 shows MII receive signal timings.

Table 70. MII Receive Signal Timing

Num	Characteristic[1]	Min	Max	Unit
M1	FEC_RXD[3:0], FEC_RX_DV, FEC_RX_ER to FEC_RX_CLK setup	5	—	ns
M2	FEC_RX_CLK to FEC_RXD[3:0], FEC_RX_DV, FEC_RX_ER hold	5	—	ns
M3	FEC_RX_CLK pulse width high	35%	65%	FEC_RX_CLK period
M4	FEC_RX_CLK pulse width low	35%	65%	FEC_RX_CLK period

1 FEC_RX_DV, FEC_RX_CLK, and FEC_RXD0 have same timing in 10 Mbps 7-wire interface mode.

- VSYNC—Vertical synchronization
- DRDY—Active data

All synchronous display controls are generated on base of an internal generated “local start point”. The synchronous display controls can be placed on time axis with DI’s offset, up and down parameters. The display access can be whole number of DI clock (Tdiclk) only. The IPP_DATA can not be moved relative to the local start point.

4.7.8.5.2 LCD Interface Functional Description

Figure 53 depicts the LCD interface timing for a generic active matrix color TFT panel. In this figure signals are shown with negative polarity. The sequence of events for active matrix interface timing is:

- DI_CLK internal DI clock, used for calculation of other controls.
- IPP_DISP_CLK latches data into the panel on its negative edge (when positive polarity is selected). In active mode, IPP_DISP_CLK runs continuously.
- HSYNC causes the panel to start a new line. (Usually IPP_PIN_2 is used as HSYNC)
- VSYNC causes the panel to start a new frame. It always encompasses at least one HSYNC pulse. (Usually IPP_PIN_3 is used as VSYNC)
- DRDY acts like an output enable signal to the CRT display. This output enables the data to be shifted onto the display. When disabled, the data is invalid and the trace is off.
  (For DRDY can be used either synchronous or asynchronous generic purpose pin as well.)

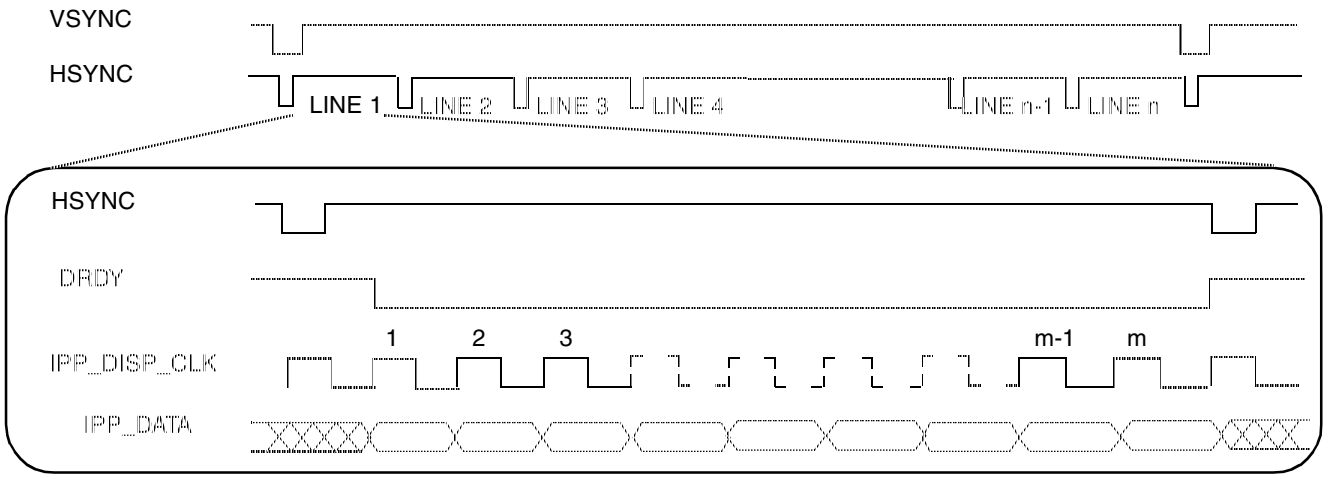


Figure 53. Interface Timing Diagram for TFT (Active Matrix) Panels

4.7.8.5.3 TFT Panel Sync Pulse Timing Diagrams

Figure 54 depicts the horizontal timing (timing of one line), including both the horizontal sync pulse and the data. All shown on the figure parameters are programmable. All controls are started by corresponding

internal events—local start points. The timing diagrams correspond to inverse polarity of the IPP_DISP_CLK signal and active-low polarity of the HSYNC, VSYNC and DRDY signals.

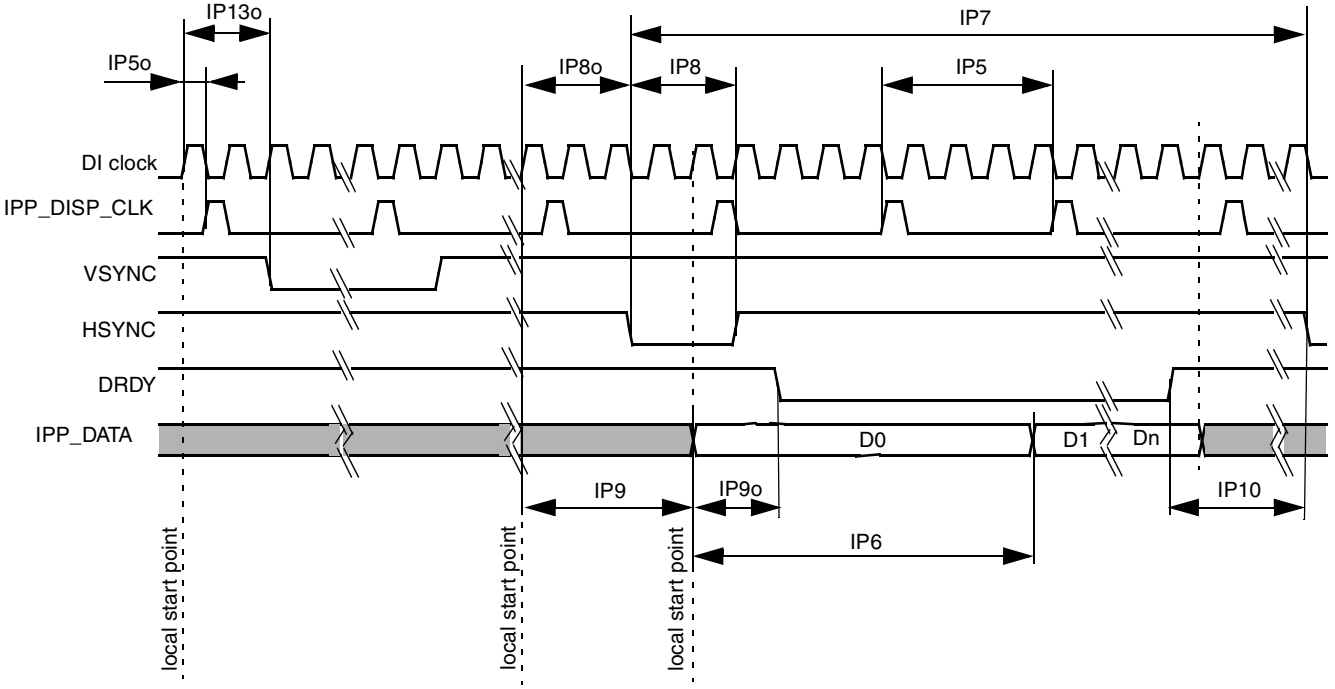


Figure 54. TFT Panels Timing Diagram—Horizontal Sync Pulse

Figure 55 depicts the vertical timing (timing of one frame). All parameters shown in the figure are programmable.

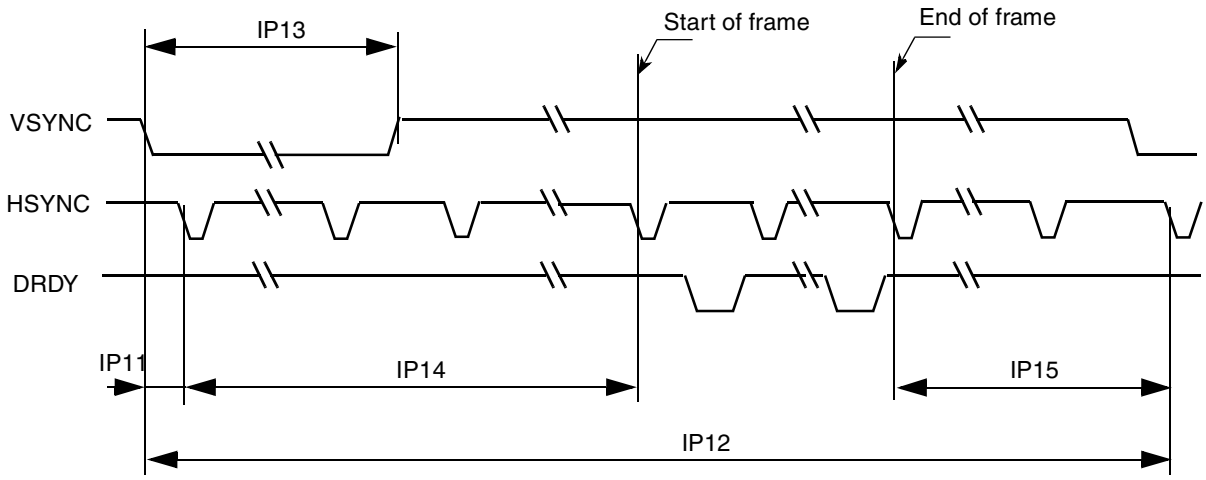


Figure 55. TFT Panels Timing Diagram—Vertical Sync Pulse

The maximal accuracy of UP/DOWN edge of IPP_DATA is

$$Accuracy = T_{diclk} \pm 0.75ns$$

The DISP_CLK_PERIOD, DI_CLK_PERIOD parameters are programmed via registers.

Figure 56 shows the synchronous display interface timing diagram for access level. The DISP_CLK_DOWN and DISP_CLK_UP parameters are set by using the register. Table 81 shows the timing characteristics for the diagram shown in Figure 56.

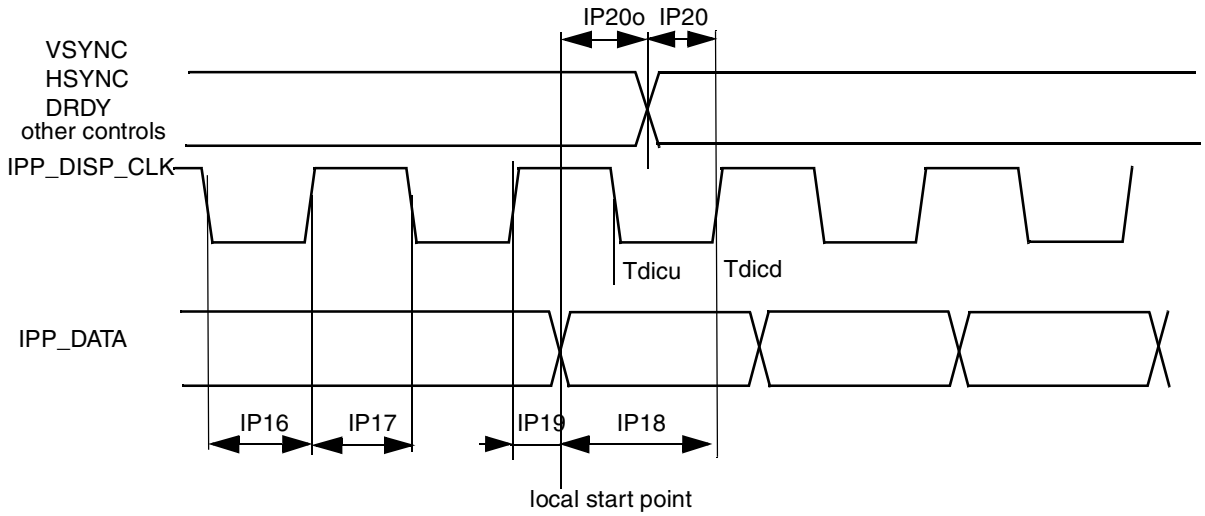


Figure 56. Synchronous Display Interface Timing Diagram—Access Level

Table 81. Synchronous Display Interface Timing Characteristics (Access Level)

ID	Parameter	Symbol	Min	Typ[1]	Max	Unit
IP16	Display interface clock low time	Tckl	Tdicd-Tdicu–1.5	Tdicd[2]–Tdicu[3]	Tdicd–Tdicu+1.5	ns
IP17	Display interface clock high time	Tckh	Tdicp–Tdicd+Tdicu–1.5	Tdicp–Tdicd+Tdicu	Tdicp–Tdicd+Tdicu+1.5	ns
IP18	Data setup time	Tdsu	Tdicd–1.5	Tdicu	—	ns
IP19	Data holdup time	Tdhd	Tdicp–Tdicd–1.5	Tdicp–Tdicu	—	ns
IP20o	Control signals offset times (defines for each pin)	Tocsu	Tocsu–1.5	Tocsu	Tocsu+1.5	—
IP20	Control signals setup time to display interface clock (defines for each pin)	Tcsu	Tdicd–1.5–Tocsu%Tdicp	Tdicu	—	ns

[1]The exact conditions have not been finalized, but will likely match the current customer requirement for their specific display. These conditions may be chip specific.

joining the internal data lines to the bidirectional external line according to the IPP_OBE_DISPB_SD_D signal provided by the IPU.

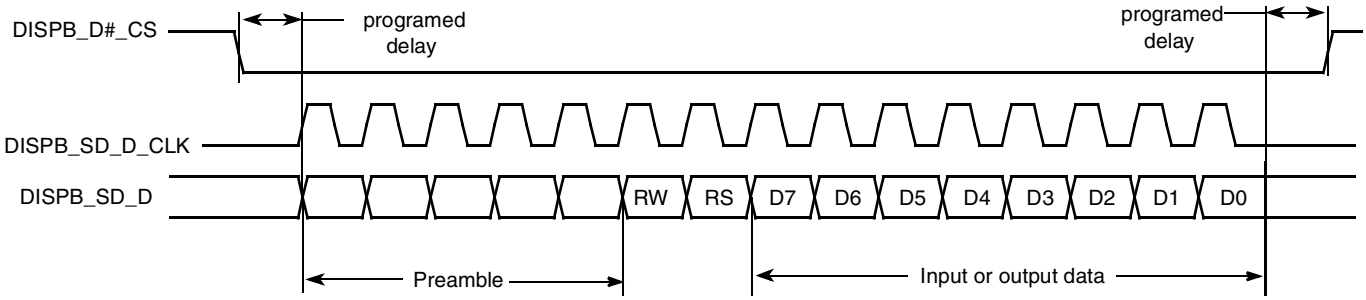


Figure 64. 3-Wire Serial Interface Timing Diagram

Figure 65 depicts timing diagram of the 4-wire serial interface. For this interface, there are separate input and output data lines both inside and outside the chip.

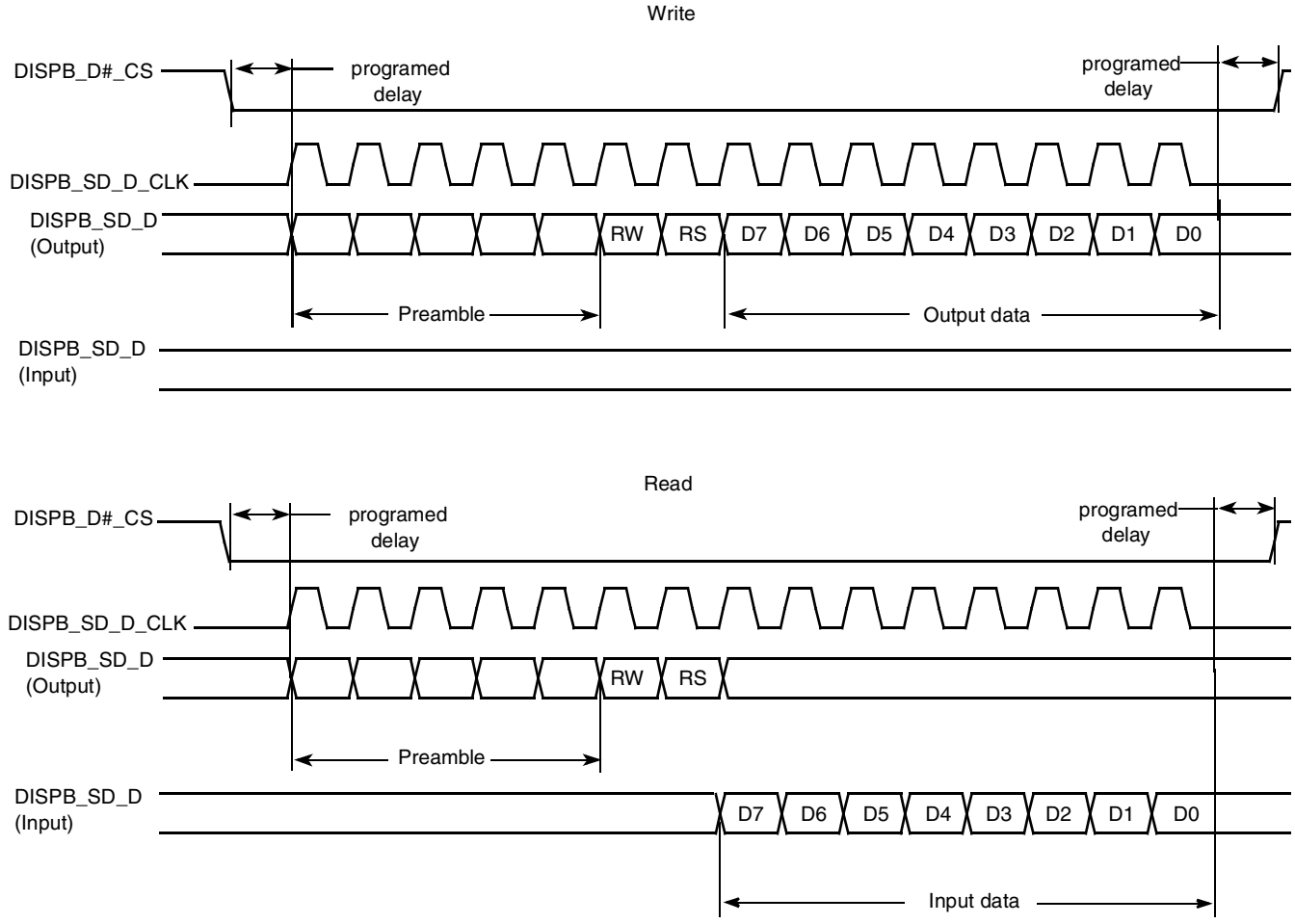


Figure 65. 4-Wire Serial Interface Timing Diagram

Table 102. SSI Transmitter Timing with Internal Clock

ID	Parameter	Min	Max	Unit
Internal Clock Operation				
SS1	(Tx/Rx) CK clock period	81.4	—	ns
SS2	(Tx/Rx) CK clock high period	36.0	—	ns
SS3	(Tx/Rx) CK clock rise time	—	6.0	ns
SS4	(Tx/Rx) CK clock low period	36.0	—	ns
SS5	(Tx/Rx) CK clock fall time	—	6.0	ns
SS6	(Tx) CK high to FS (bl) high	—	15.0	ns
SS8	(Tx) CK high to FS (bl) low	—	15.0	ns
SS10	(Tx) CK high to FS (wl) high	—	15.0	ns
SS12	(Tx) CK high to FS (wl) low	—	15.0	ns
SS14	(Tx/Rx) Internal FS rise time	—	6.0	ns
SS15	(Tx/Rx) Internal FS fall time	—	6.0	ns
SS16	(Tx) CK high to STXD valid from high impedance	—	15.0	ns
SS17	(Tx) CK high to STXD high/low	—	15.0	ns
SS18	(Tx) CK high to STXD high impedance	—	15.0	ns
SS19	STXD rise/fall time	—	6.0	ns
Synchronous Internal Clock Operation				
SS42	SRXD setup before (Tx) CK falling	30	—	ns
SS43	SRXD hold after (Tx) CK falling	0.0	—	ns
SS52	Loading	—	25.0	pF

NOTE

- All the timings for the SSI are given for a non-inverted serial clock polarity (TSCKP/RSCKP = 0) and a non-inverted frame sync (TFSI/RFSI = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal STCK/SRCK and/or the frame sync STFS/SRFS shown in the tables and in the figures.
- All timings are on Audiomux Pads when SSI is being used for data transfer.
- The terms WL and BL refer to Word Length (WL) and Bit Length (BL).
- ”Tx” and “Rx” refer to the Transmit and Receive sections of the SSI.
- For internal Frame Sync operation using external clock, the FS timing is same as that of Tx Data (for example, during AC97 mode of operation).

Table 103. SSI Receiver Timing with Internal Clock (continued)

ID	Parameter	Min	Max	Unit
Oversampling Clock Operation				
SS47	Oversampling clock period	15.04	—	ns
SS48	Oversampling clock high period	6.0	—	ns
SS49	Oversampling clock rise time	—	3.0	ns
SS50	Oversampling clock low period	6.0	—	ns
SS51	Oversampling clock fall time	—	3.0	ns

NOTE

- All the timings for the SSI are given for a non-inverted serial clock polarity (TSCKP/RSCKP = 0) and a non-inverted frame sync (TFSI/RFSI = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal STCK/SRCK and/or the frame sync STFS/SRFS shown in the tables and in the figures.
- All timings are on Audiomux Pads when SSI is being used for data transfer.
- “Tx” and “Rx” refer to the Transmit and Receive sections of the SSI.
- The terms WL and BL refer to Word Length (WL) and Bit Length (BL).
- For internal Frame Sync operation using external clock, the FS timing is same as that of Tx Data (for example, during AC97 mode of operation).

Table 114. Definitions of USB Receive Waveform in DAT_SE0 Bi-Directional Mode

ID	Parameter	Signal Name	Direction	Min	Max	Unit	Conditions/ Reference Signal
US1	TX Rise/Fall Time	USB_DAT_VP	Out	—	5.0	ns	50 pF
US2	TX Rise/Fall Time	USB_SE0_VM	Out	—	5.0	ns	50 pF
US3	TX Rise/Fall Time	USB_TXOE_B	Out	—	5.0	ns	50 pF
US4	TX Duty Cycle	USB_DAT_VP	Out	49.0	51.0	%	—
US7	RX Rise/Fall Time	USB_DAT_VP	In	—	3.0	ns	35 pF
US8	RX Rise/Fall Time	USB_SE0_VM	In	—	3.0	ns	35 pF

4.7.17.1.2 USB DAT_SE0 Unidirectional Mode

Table 115 shows the signal definitions in DAT_SE0 unidirectional mode

Table 115. Signal Definitions—DAT_SE0 Unidirectional Mode

Name	Direction	Signal Description
USB_TXOE_B	Out	Transmit enable, active low
USB_DAT_VP	Out	TX data when USB_TXOE_B is low
USB_SE0_VM	Out	SE0 drive when USB_TXOE_B is low
USB_VP1	In	Buffered data on DP when USB_TXOE_B is high
USB_VM1	In	Buffered data on DM when USB_TXOE_B is high
USB_RCV	In	Differential RX data when USB_TXOE_B is high

Figure 102 and Figure 103 shows the USB transmit/receive waveform in DAT_SE0 uni-directional mode respectively.

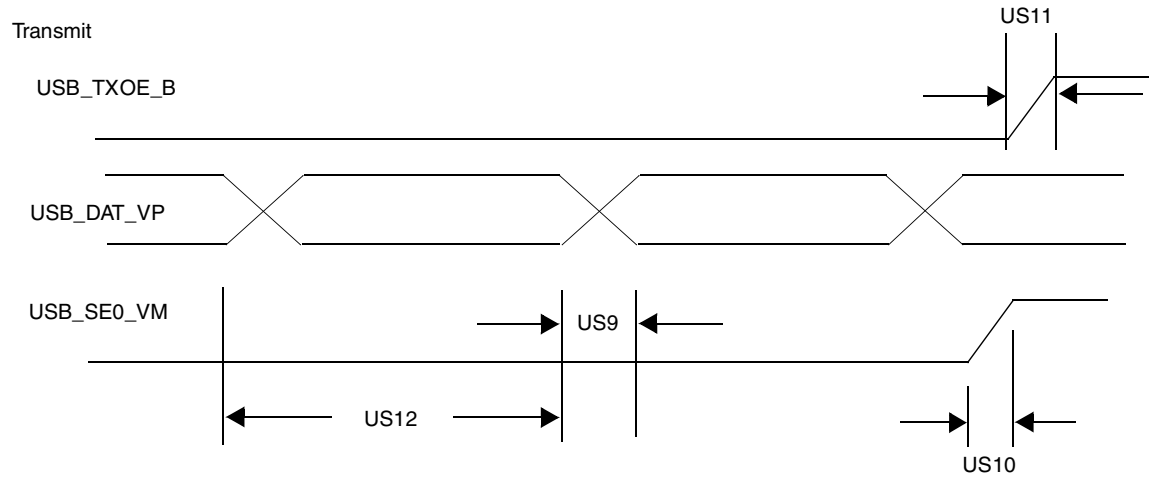


Figure 102. USB Transmit Waveform in DAT_SE0 Uni-directional Mode

Table 125. USB PHY System Clocking Parameters (continued)

Parameter	Conditions	Min	Typ	Max	Unit
Jitter (peak-peak)	<1.2 MHz	0	—	50	ps
Jitter (peak-peak)	>1.2 MHz	0	—	100	ps
Duty-cycle	—	40	—	60	%

4.7.19.4 USB PHY Voltage Thresholds

Table 126 lists the USB PHY voltage thresholds.

Table 126. VBUS Comparators Thresholds

Parameter	Conditions	Min	Typ	Max	Unit
A-Device Session Valid	—	0.8	1.4	2.0	V
B-Device Session Valid	—	0.8	1.4	4.0	V
B-Device Session End	—	0.2	0.45	0.8	V
VBUS Valid Comparator Threshold[1]	—	4.4	4.6	4.75	V

[1] For VBUS maximum rating, see Table 11 on page 17

5 Package Information and Contact Assignments

This section includes the contact assignment information and mechanical package drawing.

5.1 19 x 19 mm Package Information

This section contains the outline drawing, signal assignment map, ground/power/reference ID (by ball grid location) for the 19 × 19 mm, 0.8 mm pitch package.

Table 128. 19 x 19 mm Signal Assignments, Power Rails, and I/O (continued)

Contact Name	Contact Assignment	Power Rail	I/O Buffer Type	Direction after Reset[1]	Configuraton after Reset[1]
DI1_D0_CS	U21	NVCC_IPU2	GPIO	Output	High
DI1_D1_CS	AB23	NVCC_IPU2	GPIO	Output	High
DI1_DISP_CLK	J18	NVCC_IPU6	GPIO	Output	Low
DI1_PIN11	Y22	NVCC_IPU2	GPIO	Output	High
DI1_PIN12	AA22	NVCC_IPU2	GPIO	Output	High
DI1_PIN13	T20	NVCC_IPU2	GPIO	Output	High
DI1_PIN15	H20	NVCC_IPU6	GPIO	Output	High
DI1_PIN2	G23	NVCC_IPU6	GPIO	Output	High
DI1_PIN3	G22	NVCC_IPU6	GPIO	Output	High
DI2_DISP_CLK	J21	NVCC_IPU7	GPIO	Output	High
DI2_PIN2	J20	NVCC_IPU7	GPIO	Output	High
DI2_PIN3	K18	NVCC_IPU7	GPIO	Output	High
DI2_PIN4	H23	NVCC_IPU7	GPIO	Input	Keeper
DISP1_DAT0	N20	NVCC_HS6	HSGPIO	Input	Keeper
DISP1_DAT1	N21	NVCC_HS6	HSGPIO	Input	Keeper
DISP1_DAT10[3]	D22	NVCC_IPU4	GPIO	Input	Keeper
DISP1_DAT11[3]	D23	NVCC_IPU4	GPIO	Input	Keeper
DISP1_DAT12[3]	E21	NVCC_IPU4	GPIO	Input	Keeper
DISP1_DAT13[3]	F20	NVCC_IPU4	GPIO	Input	Keeper
DISP1_DAT14[3]	E22	NVCC_IPU4	GPIO	Input	Keeper
DISP1_DAT15[3]	G19	NVCC_IPU4	GPIO	Input	Keeper
DISP1_DAT16[3]	E23	NVCC_IPU5	GPIO	Input	Keeper
DISP1_DAT17[3]	F21	NVCC_IPU5	GPIO	Input	Keeper
DISP1_DAT18[3]	G20	NVCC_IPU5	GPIO	Input	Keeper
DISP1_DAT19[3]	H18	NVCC_IPU5	GPIO	Input	Keeper
DISP1_DAT2	U22	NVCC_HS6	HSGPIO	Input	Keeper
DISP1_DAT20[3]	F23	NVCC_IPU5	GPIO	Input	Keeper
DISP1_DAT21[3]	H19	NVCC_IPU5	GPIO	Input	Keeper
DISP1_DAT22[3]	F22	NVCC_IPU5	GPIO	Input	Keeper
DISP1_DAT23[3]	G21	NVCC_IPU5	GPIO	Input	Keeper
DISP1_DAT3	U23	NVCC_HS6	HSGPIO	Input	Keeper
DISP1_DAT4	T22	NVCC_HS6	HSGPIO	Input	Keeper

Table 128. 19 x 19 mm Signal Assignments, Power Rails, and I/O (continued)

Contact Name	Contact Assignment	Power Rail	I/O Buffer Type	Direction after Reset[1]	Configuraton after Reset[1]
DISP1_DAT5	T23	NVCC_HS6	HSGPIO	Input	Keeper
DISP1_DAT6[3]	C22	NVCC_IPU4	GPIO	Input	Keeper
DISP1_DAT7[3]	C23	NVCC_IPU4	GPIO	Input	Keeper
DISP1_DAT8[3]	D21	NVCC_IPU4	GPIO	Input	Keeper
DISP1_DAT9[3]	E20	NVCC_IPU4	GPIO	Input	Keeper
DISP2_DAT0	R21	NVCC_IPU8	GPIO	Input	Keeper
DISP2_DAT1	M19	NVCC_IPU8	GPIO	Input	Keeper
DISP2_DAT10	W22	NVCC_IPU9	GPIO	Input	Keeper
DISP2_DAT11	R19	NVCC_IPU9	GPIO	Input	Keeper
DISP2_DAT12	Y23	NVCC_IPU9	GPIO	Input	Keeper
DISP2_DAT13	T19	NVCC_IPU9	GPIO	Input	Keeper
DISP2_DAT14	AA23	NVCC_IPU9	GPIO	Input	Keeper
DISP2_DAT15	T21	NVCC_IPU9	GPIO	Input	Keeper
DISP2_DAT2	P20	NVCC_HS4_2	HSGPIO	Input	Keeper
DISP2_DAT3	P21	NVCC_HS4_2	HSGPIO	Input	Keeper
DISP2_DAT4	V22	NVCC_HS4_2	HSGPIO	Input	Keeper
DISP2_DAT5	V23	NVCC_HS4_2	HSGPIO	Input	Keeper
DISP2_DAT6	N19	NVCC_IPU8	GPIO	Input	Keeper
DISP2_DAT7	W23	NVCC_IPU8	GPIO	Input	Keeper
DISP2_DAT8	P19	NVCC_IPU9	GPIO	Input	Keeper
DISP2_DAT9	R20	NVCC_IPU9	GPIO	Input	Keeper
DISPB2_SER_CLK	AC22	NVCC_IPU2	GPIO	Output	High
DISPB2_SER_DIN	U19	NVCC_IPU2	GPIO	Input	100 kΩ pull-up
DISPB2_SER_DIO	V21	NVCC_IPU2	GPIO	Input	100 kΩ pull-up
DISPB2_SER_RS	W21	NVCC_IPU2	GPIO	Output	High
DN	K22	VDDA33	Analog	Output	–
DP	K23	VDDA33	Analog	Output	–
DRAM_A0	AB1	NVCC_EMI_DRAM	DDR2	Output	High
DRAM_A1	AA2	NVCC_EMI_DRAM	DDR2	Output	High
DRAM_A10	V2	NVCC_EMI_DRAM	DDR2	Output	High
DRAM_A11	U4	NVCC_EMI_DRAM	DDR2	Output	High
DRAM_A12	U2	NVCC_EMI_DRAM	DDR2	Output	High

6 Revision History

Table 131 provides a revision history for this data sheet.

Table 131. i.MX51 Data Sheet Document Revision History

Rev. Number	Date	Substantive Change(s)
Rev. 6	10/2012	• In Table 25, "I/O Leakage Current," on page 29, updated supply rail names for SD1 and SD2 to NVCC_PER15 and NVCC_PER17, respectively. • Updated Section 4.6.7.3, “General WEIM Timing-Synchronous Mode.” • Updated Section 4.6.7.4, “Examples of WEIM Synchronous Accesses.” • Updated Section 4.6.7.5, “General WEIM Timing-Asynchronous Mode.”
Rev. 5	03/2012	• In Table 4, "JTAG Controller Interface Summary," on page 13, changed On-Chip Termination column value for JTAG_MOD from “100 kΩ pull-down” to “100 kΩ pull-up.” • In Section 3.7, “USB-OTG IOMUX Pin Configuration,” removed the third sentence from the first paragraph and added a note after Table 9. • In Section 4.3.4, “Ultra-High Voltage I/O (UHVIO) DC Parameters,” added clarification about UHVIO I/O cell HVE bit functionality after Table 21. • In Section 4.6.9, “DDR2 SDRAM Specific Parameters:” —Updated Table 58, "DDR2 SDRAM Timing Parameter Table," on page 67 —Added a note after Table 58 —Updated Figure 36, "DDR2 SDRAM Write Cycle Timing Diagram," on page 69 —Updated Table 60, "DDR2 SDRAM Write Cycle Parameter Table," on page 69 —Added a note after Table 60 —Updated Figure 37, "DDR2 SDRAM DQ versus DQS and SDCLK Read Cycle Timing Diagram," on page 71 —Updated Table 63, "DDR2 SDRAM Read Cycle Parameter Table," on page 71 —Added a note after Table 63 • In Section 4.7.8.2, “Electrical Characteristics,” changed signal name in the second sentence of the first paragraph from “SENSB_MCLK” to “SENSB_PIX_CLK.” • In Table 128, "19 x 19 mm Signal Assignments, Power Rails, and I/O," on page 155, changed Configuraton after Reset column value for contacts, DI1_D0_CS, DI1_D1_CS, DI1_PIN11, and DI1_PIN12, from “Low” to “High.” • In Table 128, "19 x 19 mm Signal Assignments, Power Rails, and I/O," on page 155, changed Configuraton after Reset column value for contact, JTAG_MOD, from “100 kΩ pull-down” to “100 kΩ pull-up.” • In Table 128, "19 x 19 mm Signal Assignments, Power Rails, and I/O," on page 155, changed Power Rail column value for contacts, UART1_CTS, UART1_RTS, UART1_RXD, UART1_TXD, UART2_RXD, UART2_TXD, UART3_RXD, and UART3_TXD, from “NVVCC_PER12” to “NVCC_PER12.” • In Table 129, "Fuse Override Contacts," on page 167: —Added a footnote for contact, DISP1_DAT6 —Removed information about contact, EIM_A23, because the signal configuration it corresponds to, BT_HPN_EN, is not in use. • Corrected cross-references throughout the document.
Rev. 4	08/2010	• Removed table footnote in Table 47, "CAMP Electrical Parameters (CKIH1, CKIH2)," on page 46. • Updated Table 52, "WEIM Interface Pinout in Various Configurations," on page 53.