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Understanding Embedded - Microprocessors

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Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM® Cortex®-A8
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	600MHz
Co-Processors/DSP	Multimedia; NEON™ SIMD
RAM Controllers	LPDDR, DDR2
Graphics Acceleration	Yes
Display & Interface Controllers	Keypad, LCD
Ethernet	10/100Mbps (1)
SATA	-
USB	USB 2.0 (3), USB 2.0 + PHY (1)
Voltage - I/O	1.2V, 1.875V, 2.775V, 3.0V
Operating Temperature	-40°C ~ 125°C (TJ)
Security Features	ARM TZ, Boot Security, Cryptography, RTIC, Secure Fusebox, Secure JTAG, Secure Memory, Secure RTC
Package / Case	529-LFBGA
Supplier Device Package	529-BGA (19x19)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcimx516ajm6cr2

Table 3. Special Signal Considerations (continued)

Signal Name	Remarks
VREF	When using VREF with DDR-2 I/O, the nominal 0.9 V reference voltage must be half of the NVCC_EMI_DRAM supply. The user must tie VREF to a precision external resistor divider. Use a 1 kΩ 0.5% resistor to GND and a 1 kΩ 0.5% resistor to NVCC_EMI_DRAM. Shunt each resistor with a closely-mounted 0.1 µF capacitor. To reduce supply current, a pair of 1.5 kΩ 0.1% resistors can be used. Using resistors with recommended tolerances ensures the ± 2% VREF tolerance (per the DDR-2 specification) is maintained when four DDR-2 ICs plus the i.MX51 are drawing current on the resistor divider. **Note:** When VREF is used with mDDR this signal must be tied to GND.
VREFOUT	This signal determines the Triple Video DAC (TVDAC) reference voltage. The user must tie VREFOUT to an external 1.05 kΩ 1% resistor to GND.
VREG	This regulator is no longer used and should be floated by the user.
XTAL/EXTAL	The user should tie a fundamental-mode crystal across XTAL and EXTAL. The crystal must be rated for a maximum drive level of 100 µW or higher. An ESR (equivalent series resistance) of 80 Ω or less is recommended. Freescale BSP (Board Support Package) software requires 24 MHz on EXTAL. The crystal can be eliminated if an external 24 MHz oscillator is available. In this case, EXTAL must be directly driven by the external oscillator and XTAL is floated. The EXTAL signal level must swing from NVCC_OSC to GND. If the clock is used for USB, then there are strict jitter requirements: < 50 ps peak-to-peak below 1.2 MHz and < 100 ps peak-to-peak above 1.2 MHz for the USB PHY. The COSC_EN bit in the CCM (Clock Control Module) must be cleared to put the on-chip oscillator circuit in bypass mode which allows EXTAL to be externally driven. COSC_EN is bit 12 in the CCR register of the CCM.

Table 4. JTAG Controller Interface Summary

JTAG	I/O Type	On-Chip Termination
JTAG_TCK	Input	100 kΩ pull-down
JTAG_TMS	Input	47 kΩ pull-up
JTAG_TDI	Input	47 kΩ pull-up
JTAG_TDO	3-state output	Keeper
JTAG_TRSTB	Input	47 kΩ pull-up
JTAG_DE_B	Input/open-drain output	47 kΩ pull-up
JTAG_MOD	Input	100 kΩ pull-up

3 IOMUX Configuration for Boot Media

The information provided in this section describes the contacts assigned for each type of bootable media. It also includes data about the clocks used during boot flow and their frequencies. Signals that can be multiplexed appear in tables throughout this section. See the IOMUXC chapter in the *i.MX51 Multimedia Applications Processor Reference Manual* (MCIMX51RM) for details about how to program the IOMUX controller.

Table 13. i.MX51A Operating Ranges (continued)

Symbol	Parameter	Minimum[1]	Nominal[2]	Maximum[1]	Unit
NVCC_HS4_1 NVCC_HS4_2 NVCC_HS6 NVCC_HS10	HS-GPIO additional digital power supplies	1.65	—	3.1	V
NVCC_I2C	I^2C and HS-I^2C I/O Supply[7]	1.65	1.875	1.95	V
		2.7	3.0	3.3	
NVCC_SRTC_ POW	SRTC Core and I/O Supply (LVIO)	1.1	1.2	1.3	V
VDDA33	USB PHY I/O analog supply	3.0	3.3	3.6	V
VBUS	See Table 11 and Table 126 for details. This is not a power supply.	—	—	—	—

1 Voltage at the package power supply contact must be maintained between the minimum and maximum voltages. The design must allow for supply tolerances and system voltage drops.

2 The nominal values for the supplies indicate the target setpoint for a tolerance no tighter than ± 50 mV. Use of supplies with a tighter tolerance allows reduction of the setpoint with commensurate power savings.

3 The NVCC_IPUx rails are isolated from one another. This allows the connection of different supply voltages for each one. For example, NVCC_IPU2 can operate at 1.8 V while NVCC_IPU4 operates at 3.0 V.

4 In Read mode, Freescale recommends VDD_FUSE be floated or grounded. Tying VDD_FUSE to a positive supply (3.0 V–3.3 V) increases the possibility of inadvertently blowing fuses and is not recommended.

5 The NAND Flash supplies are composed of three groups: A, B, and C. Each group can be powered with a different supply voltage. For example, NVCC_NANDF_A = 1.8 V, NVCC_NANDF_B = 3.0 V, NVCC_NANDF_C = 2.7 V.

6 The analog supplies should be isolated in the application design. Use of series inductors is recommended.

7 Operation of the HS-I^2C and I^2C is not guaranteed when operated between the supply voltages of 1.95 to 2.7 V.

Table 14. Interface Frequency

Parameter Description	Symbol	Min	Max	Unit
JTAG: TCK Operating Frequency	f_{tck}	See Table 99, "JTAG Timing," on page 130		MHz
CKIL: Operating Frequency	f_{ckil}	See Table 74, "FPM Specifications," on page 80		kHz
CKIH: Operating Frequency	f_{ckih}	See Table 47, "CAMP Electrical Parameters (CKIH1, CKIH2)," on page 46		MHz
XTAL Oscillator	f_{xtal}	22	27	MHz

4.1.1 Supply Current

Table 15 shows the fuse supply current.

Table 15. Fuse Supply Current[1]

Description	Symbol	Min	Typ	Max	Unit
eFuse Program Current.[2] Current required to program one eFuse bit: The associated VDD_FUSE supply per Table 13.	$I_{program}$	—	60	120	mA

1 Max condition for tpr, tpo, tps and didt: wcs model, 1.1 V, IO 1.65 V, 105 °C and s0-s5=111111. Typ condition for tpr, tpo, tps and didt: typ model, 1.2 V, IO 1.8 V, 25 °C and s0-s5 = 101010. Min condition for tpr, tpo, tps and didt: bcs model, 1.3 V, IO 1.95 V, –40 °C and s0-s5 = 000000.

2 Max condition for trfi and tpi: wcs model, 1.1 V, IO 1.65 V and 105 °C. Typ condition for trfi and tpi: typ model, 1.2 V, IO 1.8 V and 25 °C. Min condition for trfi and tpi: bcs model, 1.3 V, IO 1.95 V and –40 °C.

3 Hysteresis mode is recommended for input with transition time greater than 25 ns.

AC electrical characteristics in DDR mobile for Fast mode and ovdd=1.65 – 1.95 V, ipp_hve=0 are placed in Table 39.

Table 39. AC Electrical Characteristics of DDR mobile IO Pads for Fast Mode and ovdd=1.65–1.95 V (ipp_hve=0)

Parameter	Symbol	Test Condition	Min rise/fall	Typ	Max rise/fall	Units
Output Pad Transition Times (High Drive)[1]	tpr	15pF 35pF	1.35/1.31 2.99/2.94	1.02/1.03 2.28/2.29	0.89/0.89 1.85/1.94	ns
Output Pad Transition Times (Medium Drive)[1]	tpr	15pF 35pF	2.00/1.99 4.55/4.44	1.56/1.53 3.38/3.45	1.28/1.32 2.79/2.85	ns
Output Pad Transition Times (Low Drive)[1]	tpr	15pF 35pF	4.08/3.92 8.93/8.95	3.11/3.06 6.84/6.81	2.50/2.61 5.56/5.76	ns
Output Pad Propagation Delay (High Drive)[1]	tpo	15pF 35pF	1.54/1.52 2.69/2.75	1.73/1.62 2.59/2.55	2.36/2.09 3.04/2.86	ns
Output Pad Propagation Delay (Medium Drive)[1]	tpo	15pF 35pF	2.00/2.02 3.75/3.86	2.08/2.00 3.38/3.39	2.64/2.40 3.65/3.56	ns
Output Pad Propagation Delay (Low Drive)[1]	tpo	15pF 35pF	3.43/3.52 6.92/7.20	3.13/3.13 5.72/5.94	3.47/3.34 5.49/5.65	ns
Output Pad Slew Rate (High Drive)[1]	tps	15pF 35pF	0.87/0.89 0.39/0.40	1.06/1.05 0.47/0.47	1.11/1.11 0.54/0.51	V/ns
Output Pad Slew Rate (Medium Drive)[1]	tps	15pF 35pF	0.58/0.59 0.26/0.26	0.69/0.71 0.32/0.31	0.77/0.75 0.35/0.35	V/ns
Output Pad Slew Rate (Low Drive)[1]	tps	15pF 35pF	0.29/0.30 0.13/0.13	0.35/0.35 0.16/0.16	0.40/0.38 0.18/0.17	V/ns
Output Pad di/dt (High Drive)[1]	di/dt	—	185	91	46	mA/ns
Output Pad di/dt (Medium drive)[1]	di/dt	—	124	61	31	mA/ns
Output Pad di/dt (Low drive)[1]	di/dt	—	62	30	16	mA/ns
Input Pad Transition Times[2]	trfi	1.2 pF	0.09/0.09	0.132/0.128	0.212/0.213	ns
Input Pad Propagation Delay without Hysteresis (CMOS input), 50%-50%[2]	tpi	1.2 pF	0.45/0.93	0.6/0.58	0.9/0.88	ns
Input Pad Propagation Delay with Hysteresis (CMOS input), 50%-50%[2]	tpi	1.2 pF	0.55/0.55	0.71/0.7	1.03/0.98	ns
Input Pad Propagation Delay (DDR input), 50%-50%[2]	tpi	1.2 pF	0.38/0.38	0.58/0.61	1.014/1.07	—
Maximum Input Transition Times[3]	trm	—	—	—	5	ns

1 Max condition for tpr, tpo, tps and didt: wcs model, 1.1 V, IO 1.65 V, 105 °C and s0-s5=111111. Typ condition for tpr, tpo, tps and didt: typ model, 1.2 V, IO 1.8 V, 25 °C and s0-s5 = 101010. Min condition for tpr, tpo, tps and didt: bcs model, 1.3 V, IO 1.95 V, –40 °C and s0-s5 = 000000.

2 Max condition for trfi and tpi: wcs model, 1.1 V, IO 1.65 V and 105 °C. Typ condition for trfi and tpi: typ model, 1.2 V, IO 1.8 V and 25 °C. Min condition for trfi and tpi: bcs model, 1.3 V, IO 1.95 V and –40 °C.

3 Hysteresis mode is recommended for input with transition time greater than 25 ns.

AC electrical characteristics in DDR mobile for Slow mode and ovdd=1.65-1.95V, ipp_hve=0 are placed in Table 40.

Table 40. AC Electrical Characteristics of DDR mobile IO Pads for Slow Mode ovdd=1.65–1.95 V (ipp_hve=0)

Parameter	Symbol	Test Condition	Min rise/fall	Typ	Max rise/fall	Units
Output Pad Transition Times (High Drive)[1]	tpr	15pF 35pF	1.42/1.43 3.03/2.92	1.20/1.27 2.39/2.38	1.43/1.49 2.35/2.46	ns
Output Pad Transition Times (Medium Drive)[1]	tpr	15pF 35pF	2.04/2.04 4.51/4.49	1.68/1.74 3.47/3.50	1.82/1.91 3.16/3.30	ns
Output Pad Transition Times (Low Drive)[1]	tpr	15pF 35pF	4.08/3.93 9.06/8.93	3.16/3.19 6.92/6.93	2.90/3.01 5.74/5.96	ns
Output Pad Propagation Delay (High Drive)[1]	tpo	15pF 35pF	2.00/2.17 3.15/3.42	2.33/2.50 3.24/3.52	3.70/3.70 4.63/4.75	ns
Output Pad Propagation Delay (Medium Drive)[1]	tpo	15pF 35pF	2.47/2.68 4.2/4.53	2.72/2.92 4.01/4.37	4.10/4.16 5.33/5.55	ns
Output Pad Propagation Delay (Low Drive)[1]	tpo	15pF 35pF	3.87/4.18 7.32/7.86	3.78/4.10 6.35/6.90	5.13/5.30 7.25/7.73	ns
Output Pad Slew Rate (High Drive)[1]	tps	15pF 35pF	0.82/0.82 0.39/0.40	0.90/0.85 0.45/0.49	0.69/0.66 0.42/0.40	V/ns
Output Pad Slew Rate (Medium Drive)[1]	tps	15pF 35pF	0.57/0.57 0.26/0.26	0.70/0.62 0.31/0.31	0.54/0.52 0.31/0.30	V/ns
Output Pad Slew Rate (Low Drive)[1]	tps	15pF 35pF	0.29/0.30 0.13/0.13	0.34/0.34 0.16/0.16	0.34/0.33 0.17/0.17	V/ns
Output Pad di/dt (High Drive)[1]	di/dt		47	14	9	mA/ns
Output Pad di/dt (Medium drive)[1]	di/dt	—	27	9	6	mA/ns
Output Pad di/dt (Low drive)[1]	di/dt	—	12	5	3	mA/ns
Input Pad Transition Times[2]	trfi	1.2 pF	0.09/0.09	0.132/0.128	0.212/0.213	ns
Input Pad Propagation Delay without Hysteresis (CMOS input), 50%-50%[2]	tpi	1.2 pF	0.45/0.93	0.6/0.58	0.9/0.88	ns
Input Pad Propagation Delay with Hysteresis (CMOS input), 50%-50%[2]	tpi	1.2 pF	0.55/0.55	0.71/0.7	1.03/0.98	ns
Input Pad Propagation Delay (DDR input), 50%-50%[2]	tpi	1.2 pF	0.38/0.38	0.58/0.61	1.014/1.07	—
Maximum Input Transition Times[3]	trm	—	—	—	5	ns

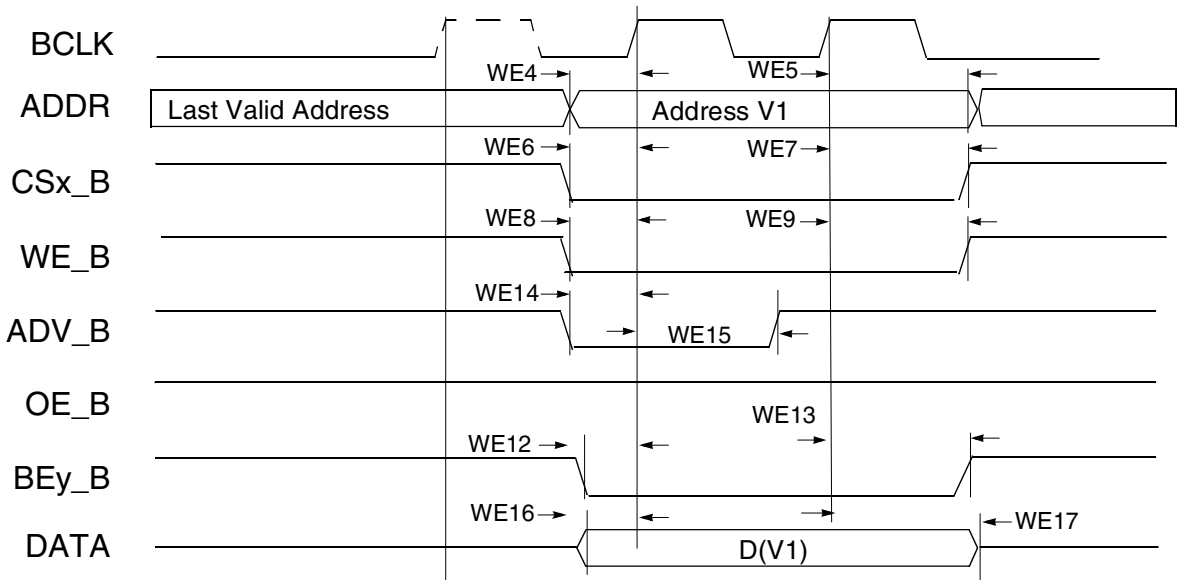

Figure 23. Synchronous Memory, Write Access, WSC=1, WBEA=0, and WADVN=0

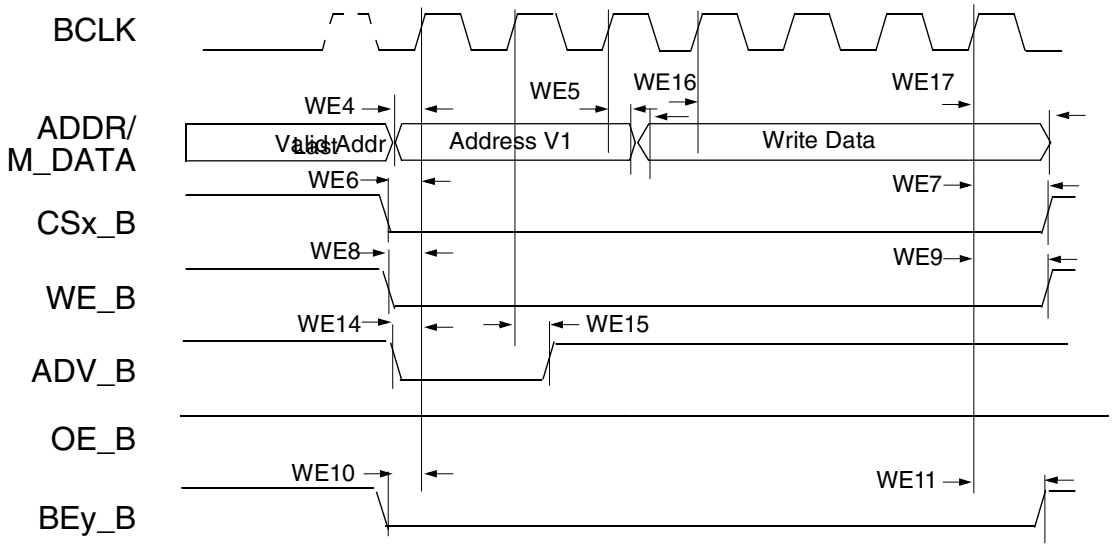

Figure 24. Muxed Address/Data (A/D) Mode, Synchronous Write Access, WSC=6, ADVA=0, ADVN=1, and ADH=1

NOTE

In 32-bit muxed address/data (A/D) mode the 16 MSBs are driven on the data bus.

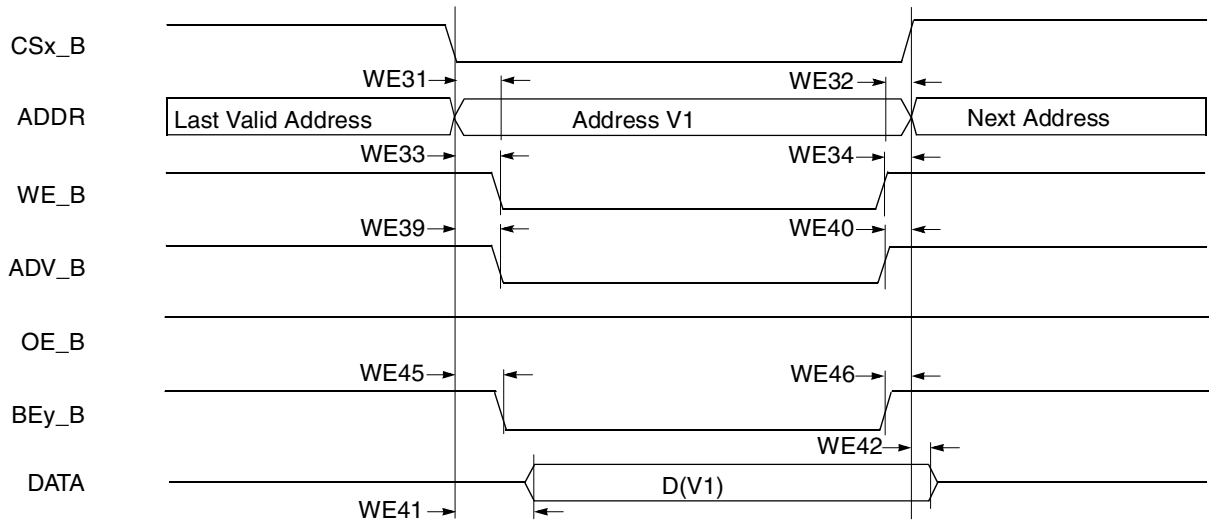

Figure 28. Asynchronous Memory Write Access

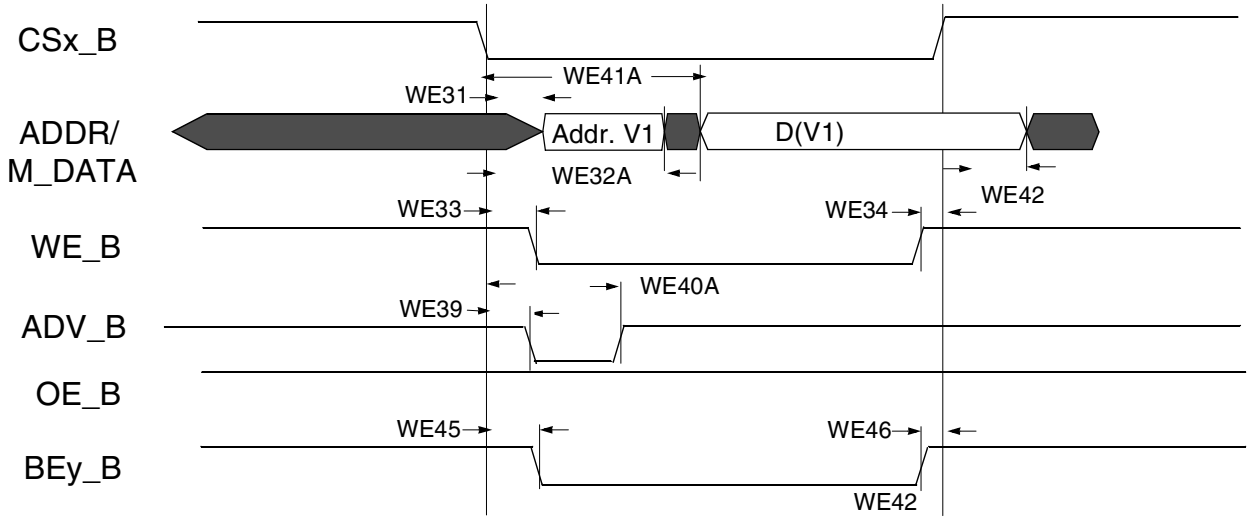

Figure 29. Asynchronous A/D Muxed Write Access

4.6.9 DDR2 SDRAM Specific Parameters

Figure 35 shows the timing parameters for DDR2. The timing parameters for this diagram appear in Table 58.

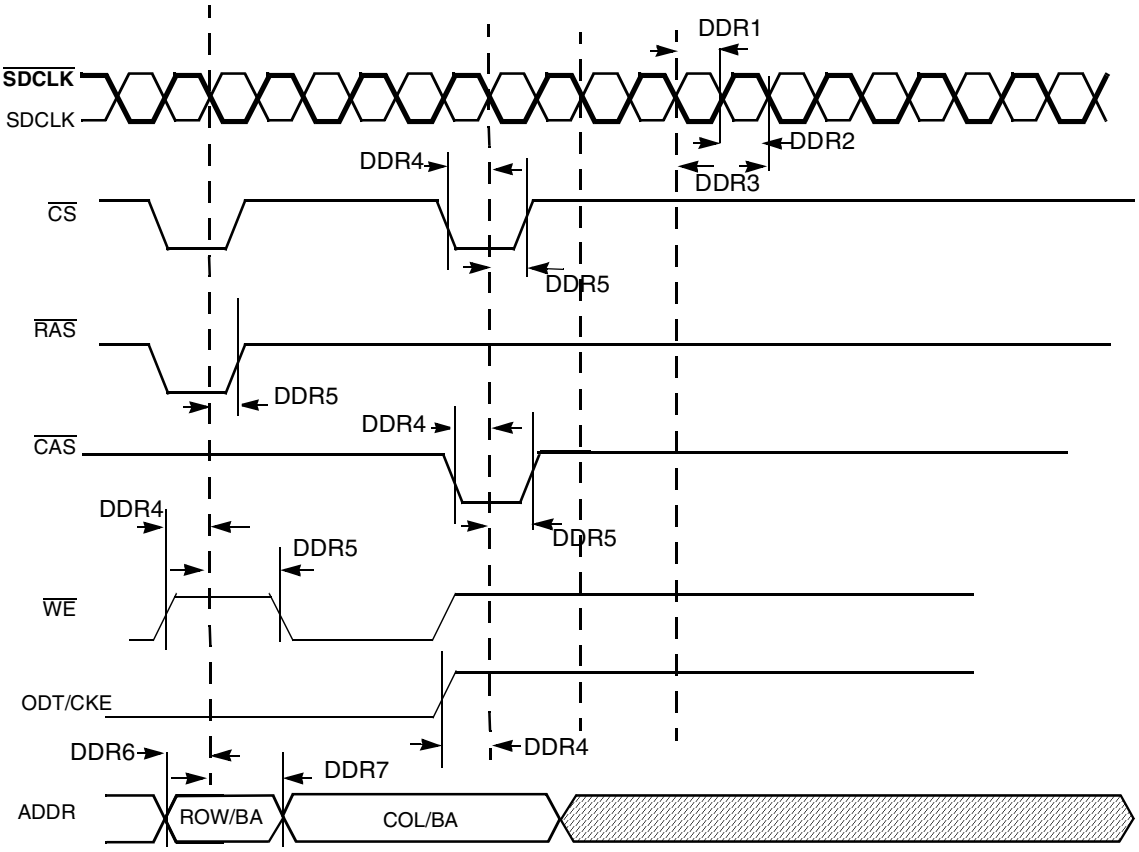

Figure 35. DDR2 SDRAM Basic Timing Parameters

Table 58. DDR2 SDRAM Timing Parameter Table

ID	Parameter	Symbol	SDCLK = 200 MHz		Unit
			Min	Max	
DDR1	SDRAM clock high-level width	t_{CH}	0.45	0.55	t_{CK}
DDR2	SDRAM clock low-level width	t_{CL}	0.45	0.55	t_{CK}
DDR3	SDRAM clock cycle time	t_{CK}	5	—	ns
DDR4	CS, RAS, CAS, CKE, WE, ODT setup time	t_{IS}[1]	1.5	—	ns
DDR5	CS, RAS, CAS, CKE, WE, ODT hold time	t_{IH}[1]	1.7	—	ns

Table 58. DDR2 SDRAM Timing Parameter Table (continued)

ID	Parameter	Symbol	SDCLK = 200 MHz		Unit
			Min	Max	
DDR6	Address output setup time	t_{IS}[1]	1.7	—	ns
DDR7	Address output hold time	t_{IH}[1]	1.5	—	ns

[1] These values are for command/address slew rates of 1 V/ns and SDCLK / SDCLK_B differential slew rate of 2 V/ns. For different values use the settings shown in Table 59.

NOTE

Measurements are taken from Vref to Vref (cross-point to cross-point), but JEDEC timings for single-ended signals are defined from Vref to Vil(ac) max or to Vih(ac) min.

Table 59. Derating Values for DDR2-400 (SDCLK = 200 MHz)

Command / Address Slew Rate (V/ns)	SDCLK Differential Slew Rates[1,2]						Unit
	2.0 V/ns		1.5 V/ns		1.0 V/ns		
	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	
4.0	+187	+94	+217	+124	+247	+154	ps
3.5	+179	+89	+209	+119	+239	+149	ps
3.0	+167	+83	+197	+113	+227	+143	ps
2.5	+150	+75	+180	+105	+210	+135	ps
2.0	+125	+45	+155	+75	+185	+105	ps
1.5	+83	+21	+113	+51	+143	+81	ps
1.0	+0	+0	+30	+30	+60	+60	ps
0.9	–11	–14	+19	+16	+49	+46	ps
0.8	–25	–31	+5	–1	+35	+29	ps
0.7	–43	–54	–13	–24	+17	+6	ps
0.6	–67	–83	–37	–53	–7	–23	ps
0.5	–110	–125	–80	–95	–50	–65	ps
0.4	–175	–188	–145	–158	–115	–128	ps
0.3	–285	–292	–255	–262	–225	–232	ps
0.25	–350	–375	–320	–345	–290	–315	ps
0.2	–525	–500	–495	–470	–465	–440	ps
0.15	–800	–708	–770	–678	–740	–648	ps
0.1	–1450	–1125	–1420	–1095	–1390	–1065	ps

4.7.4.3 MII Async Inputs Signal Timing (FEC_CRS and FEC_COL)

Table 72 lists MII asynchronous inputs signal timing information. Figure 45 shows MII asynchronous input timings listed in Table 72.

Table 72. MII Async Inputs Signal Timing

Num	Characteristic	Min	Max	Unit
M9[1]	FEC_CRS to FEC_COL minimum pulse width	1.5	—	FEC_TX_CLK period

[1] FEC_COL has the same timing in 10 Mbit 7-wire interface mode.

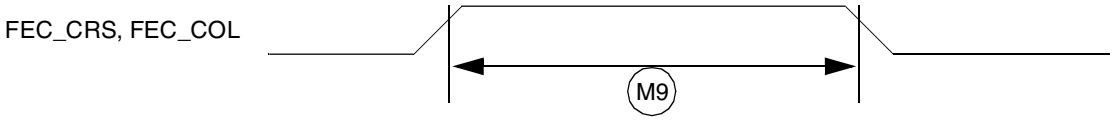

Figure 45. MII Async Inputs Timing Diagram

4.7.4.4 MII Serial Management Channel Timing (FEC_MDIO and FEC_MDC)

Table 73 lists MII serial management channel timings. Figure 46 shows MII serial management channel timings listed in Table 73. The MDC frequency should be equal to or less than 2.5 MHz to be compliant with the IEEE 802.3 MII specification. However the FEC can function correctly with a maximum MDC frequency of 15 MHz.

Table 73. MII Transmit Signal Timing

ID	Characteristic	Min	Max	Unit
M10	FEC_MDC falling edge to FEC_MDIO output invalid (minimum propagation delay)	0	—	ns
M11	FEC_MDC falling edge to FEC_MDIO output valid (max propagation delay)	—	5	ns
M12	FEC_MDIO (input) to FEC_MDC rising edge setup	18	—	ns
M13	FEC_MDIO (input) to FEC_MDC rising edge hold	0	—	ns
M14	FEC_MDC pulse width high	40%	60%	FEC_MDC period
M15	FEC_MDC pulse width low	40%	60%	FEC_MDC period

- VSYNC—Vertical synchronization
- DRDY—Active data

All synchronous display controls are generated on base of an internal generated “local start point”. The synchronous display controls can be placed on time axis with DI’s offset, up and down parameters. The display access can be whole number of DI clock (Tdiclk) only. The IPP_DATA can not be moved relative to the local start point.

4.7.8.5.2 LCD Interface Functional Description

Figure 53 depicts the LCD interface timing for a generic active matrix color TFT panel. In this figure signals are shown with negative polarity. The sequence of events for active matrix interface timing is:

- DI_CLK internal DI clock, used for calculation of other controls.
- IPP_DISP_CLK latches data into the panel on its negative edge (when positive polarity is selected). In active mode, IPP_DISP_CLK runs continuously.
- HSYNC causes the panel to start a new line. (Usually IPP_PIN_2 is used as HSYNC)
- VSYNC causes the panel to start a new frame. It always encompasses at least one HSYNC pulse. (Usually IPP_PIN_3 is used as VSYNC)
- DRDY acts like an output enable signal to the CRT display. This output enables the data to be shifted onto the display. When disabled, the data is invalid and the trace is off.
  (For DRDY can be used either synchronous or asynchronous generic purpose pin as well.)

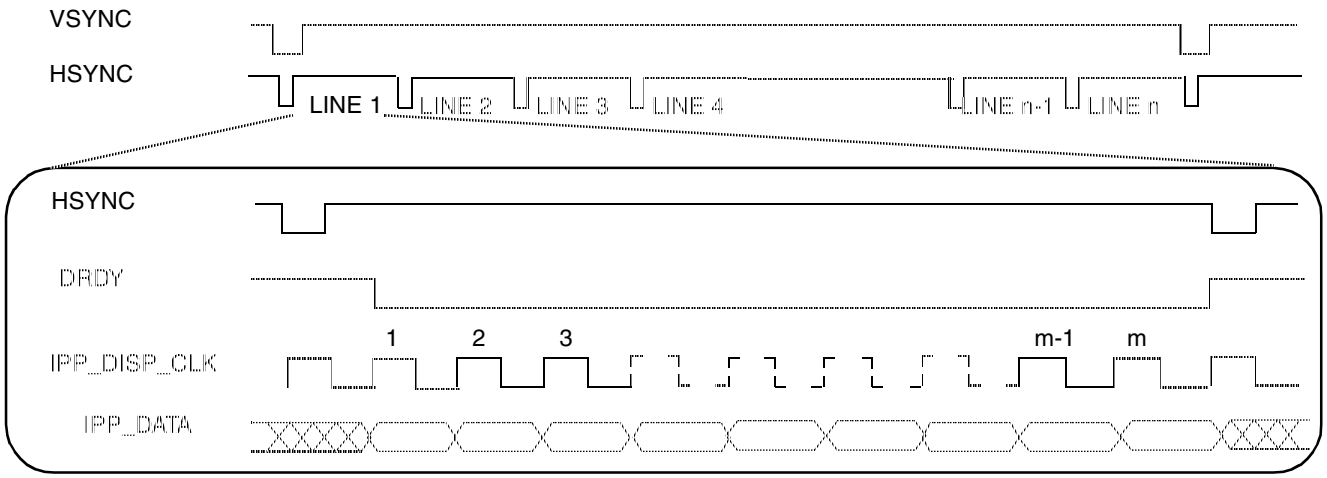

Figure 53. Interface Timing Diagram for TFT (Active Matrix) Panels

4.7.8.5.3 TFT Panel Sync Pulse Timing Diagrams

Figure 54 depicts the horizontal timing (timing of one line), including both the horizontal sync pulse and the data. All shown on the figure parameters are programmable. All controls are started by corresponding

internal events—local start points. The timing diagrams correspond to inverse polarity of the IPP_DISP_CLK signal and active-low polarity of the HSYNC, VSYNC and DRDY signals.

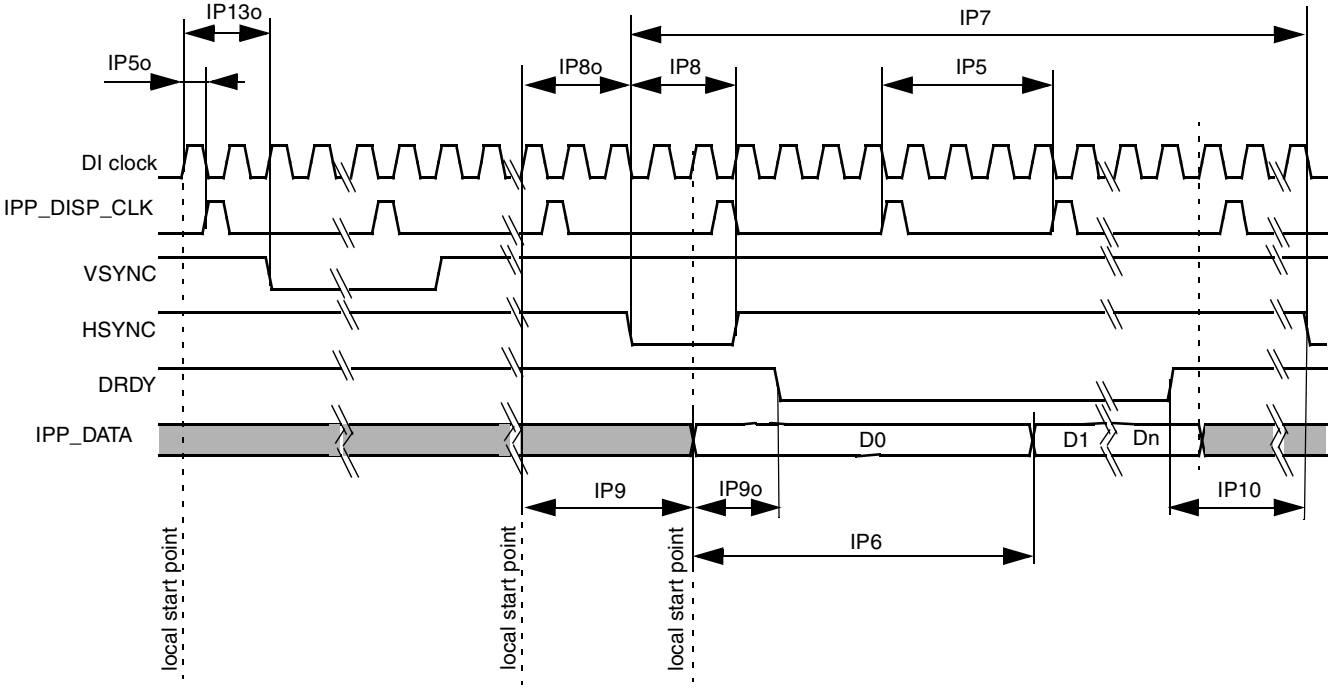

Figure 54. TFT Panels Timing Diagram—Horizontal Sync Pulse

Figure 55 depicts the vertical timing (timing of one frame). All parameters shown in the figure are programmable.

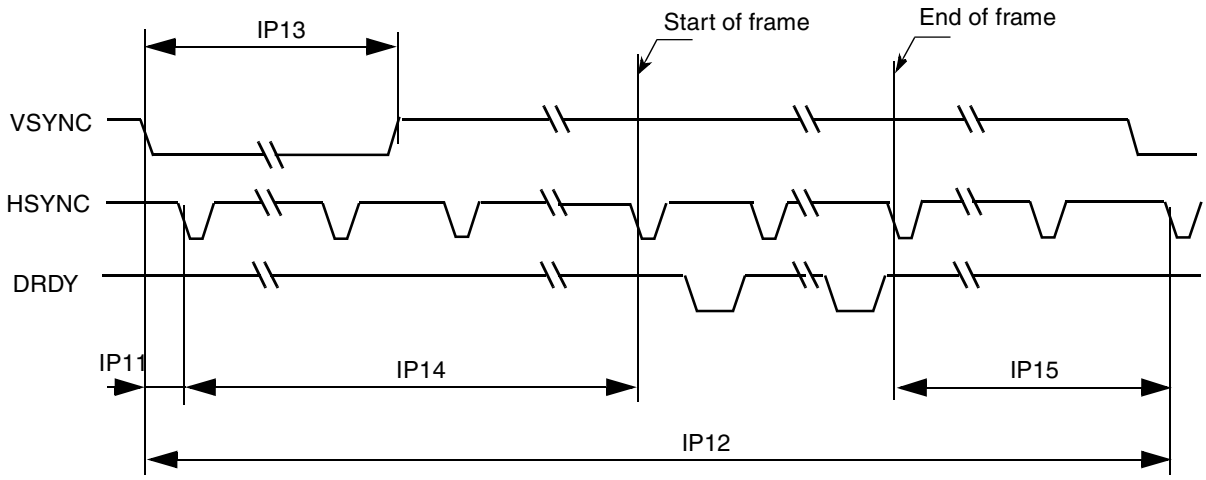

Figure 55. TFT Panels Timing Diagram—Vertical Sync Pulse

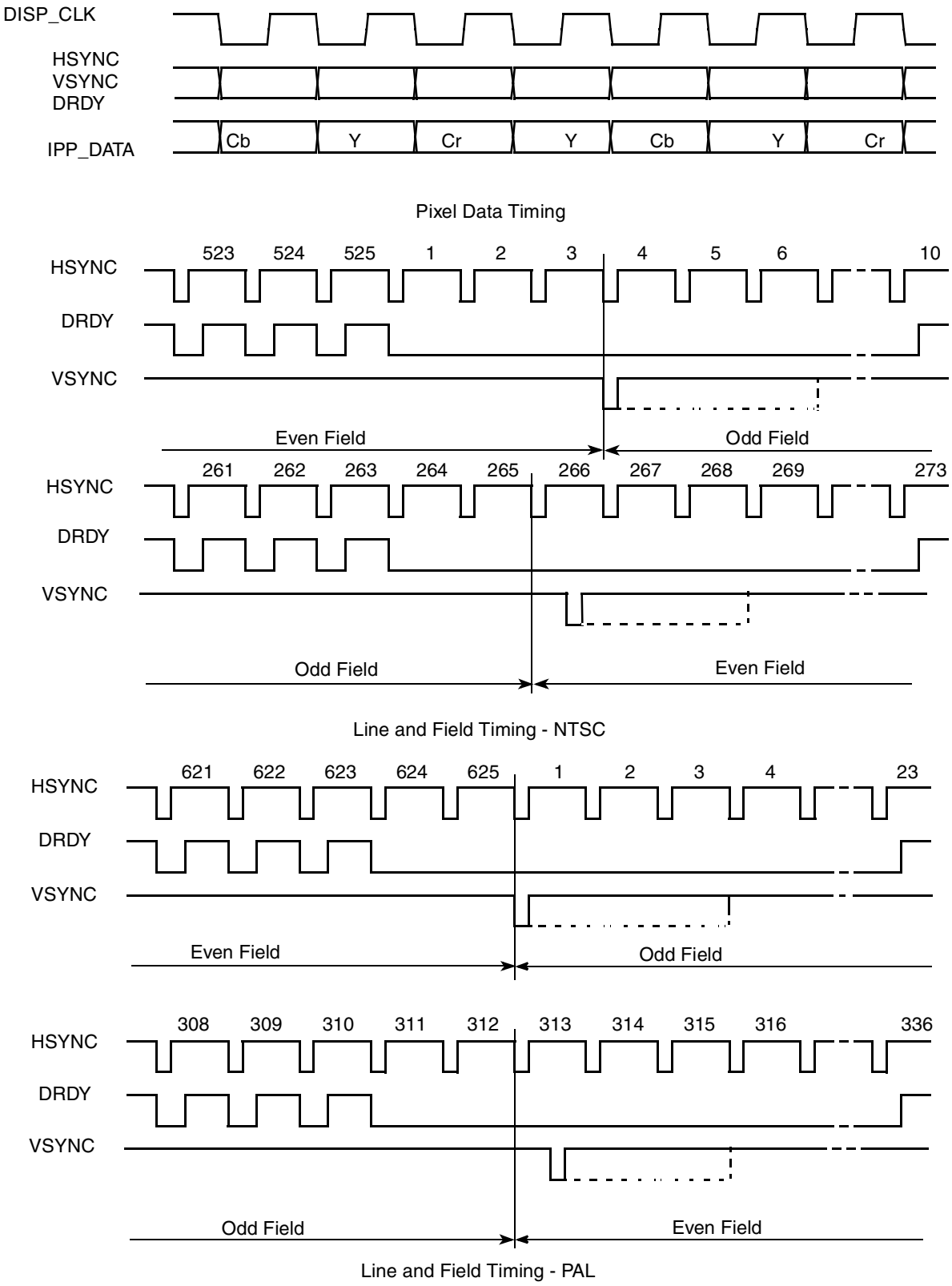

Figure 57. TV Encoder Interface Timing Diagram

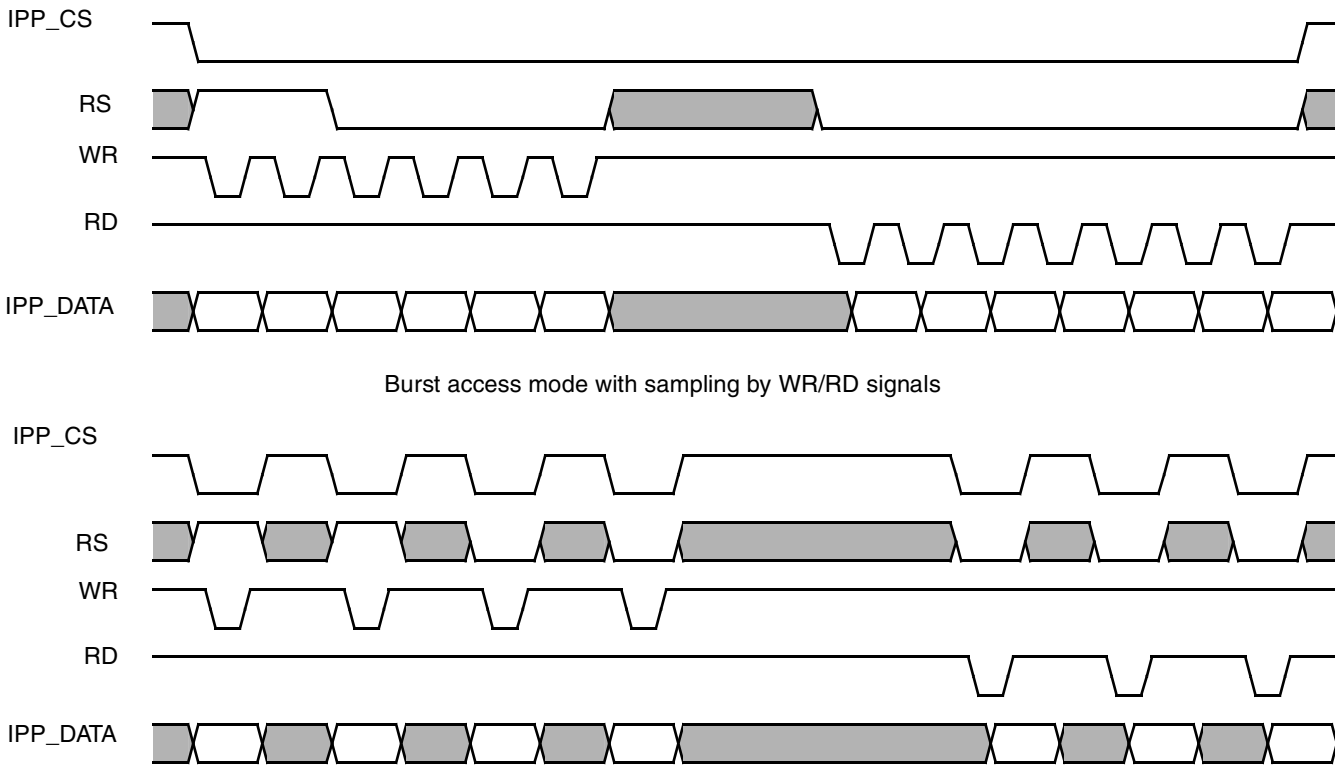

Figure 59. Asynchronous Parallel System 80 Interface (Type 2) Timing Diagram

Figure 72 depicts the timing of the PWM, and Table 89 lists the PWM timing parameters.

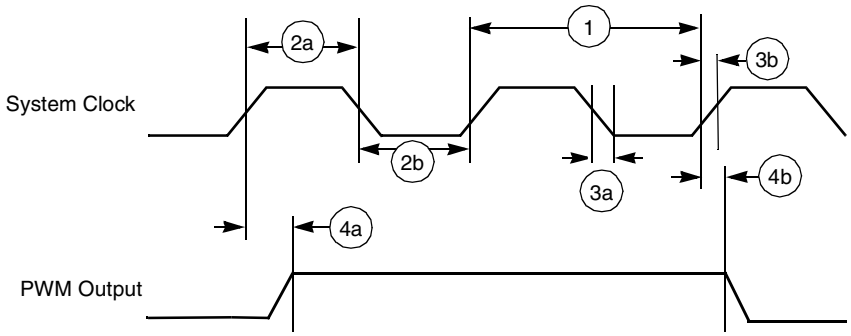

Figure 72. PWM Timing

Table 89. PWM Output Timing Parameter

Ref. No.	Parameter	Min	Max	Unit
1	System CLK frequency[1]	0	ipg_clk	MHz
2a	Clock high time	12.29	—	ns
2b	Clock low time	9.91	—	ns
3a	Clock fall time	—	0.5	ns
3b	Clock rise time	—	0.5	ns
4a	Output delay time	—	9.37	ns
4b	Output setup time	8.71	—	ns

[1] CL of PWMO = 30 pF

4.7.11 P-ATA Timing Parameters

This section describes the timing parameters of the Parallel ATA module which are compliant with ATA/ATAPI-5 specification.

Parallel ATA module can work on PIO/Multi-Word DMA/Ultra DMA transfer modes. Each transfer mode has different data transfer rate, Ultra DMA mode 4 data transfer rate is up to 66 Mbyte/s. Parallel ATA module interface consist of a total of 29 pins, Some pins act on different function in different transfer mode. There are different requirements of timing relationships among the function pins conform with ATA/ATAPI-5 specification and these requirements are configurable by the ATA module registers.

Table 99. JTAG Timing (continued)

ID	Parameter[1,2]	All Frequencies		Unit
		Min	Max	
SJ9	TMS, TDI data hold time	25	—	ns
SJ10	TCK low to TDO data valid	—	44	ns
SJ11	TCK low to TDO high impedance	—	44	ns
SJ12	$\overline{\text{TRST}}$ assert time	100	—	ns
SJ13	$\overline{\text{TRST}}$ set-up time to TCK low	40	—	ns

1 T_{DC} = target frequency of SJC
2 V_M = mid-point voltage

4.7.14 SPDIF Timing Parameters

Table 100 shows the timing parameters for the Sony/Philips Digital Interconnect Format (SPDIF).

Table 100. SPDIF Timing

Characteristics	Symbol	All Frequencies		Unit
		Min	Max	
SPDIFOUT output (load = 50 pF) • Skew • Transition rising • Transition falling	—	 — — —	 1.5 24.2 31.3	ns
SPDIFOUT output (load = 30 pF) • Skew • Transition rising • Transition falling	—	 — — —	 1.5 13.6 18.0	ns

4.7.15 SSI Timing Parameters

This section describes the timing parameters of the SSI module. The connectivity of the serial synchronous interfaces is summarized in Table 101.

Table 101. AUDMUX Port Allocation

Port	Signal Nomenclature	Type and Access
AUDMUX port 1	SSI 1	Internal
AUDMUX port 2	SSI 2	Internal
AUDMUX port 3	AUD3	External—AUD3 I/O
AUDMUX port 4	AUD4	External—EIM or CSPI1 I/O via IOMUX
AUDMUX port 5	AUD5	External—EIM or SD1 I/O via IOMUX

4.7.17.1.1 USB DAT_SE0 Bi-Directional Mode

Table 113 shows the signal definitions in DAT_SE0 bi-directional mode and Figure 100 shows the USB transmit waveform in DAT_SE0 bi-directional mode.

Table 113. Signal Definitions—DAT_SE0 Bi-Directional Mode

Name	Direction	Signal Description
USB_TXOE_B	Out	Transmit enable, active low
USB_DAT_VP	Out In	TX data when USB_TXOE_B is low Differential RX data when USB_TXOE_B is high
USB_SE0_VM	Out In	SE0 drive when USB_TXOE_B is low SE0 RX indicator when USB_TXOE_B is high

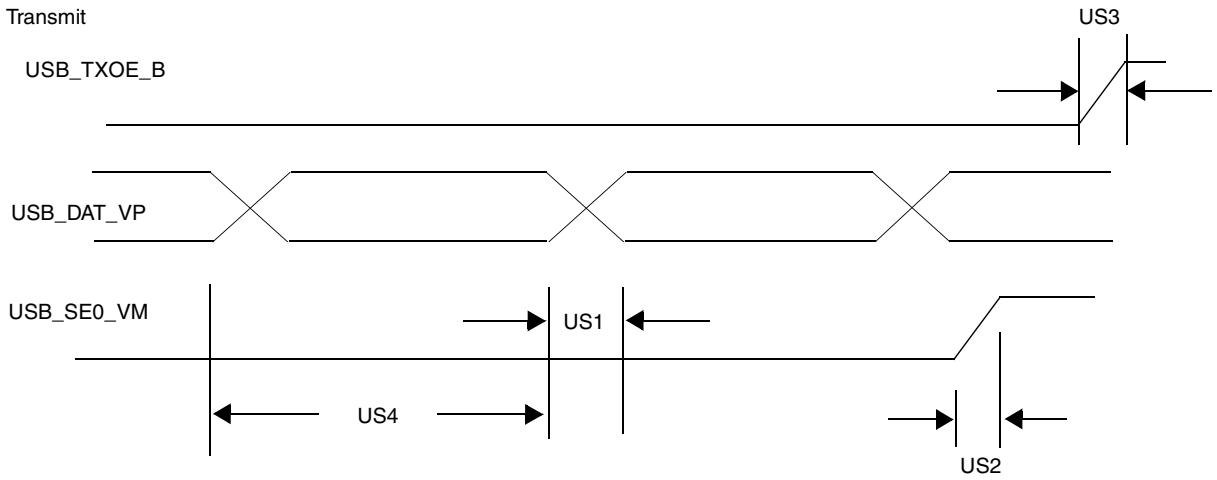

Figure 100. USB Transmit Waveform in DAT_SE0 Bi-Directional Mode

Figure 101 shows the USB receive waveform in DAT_SE0 bi-directional mode and Table 114 shows the definitions of USB receive waveform in DAT_SE0 bi-directional mode.

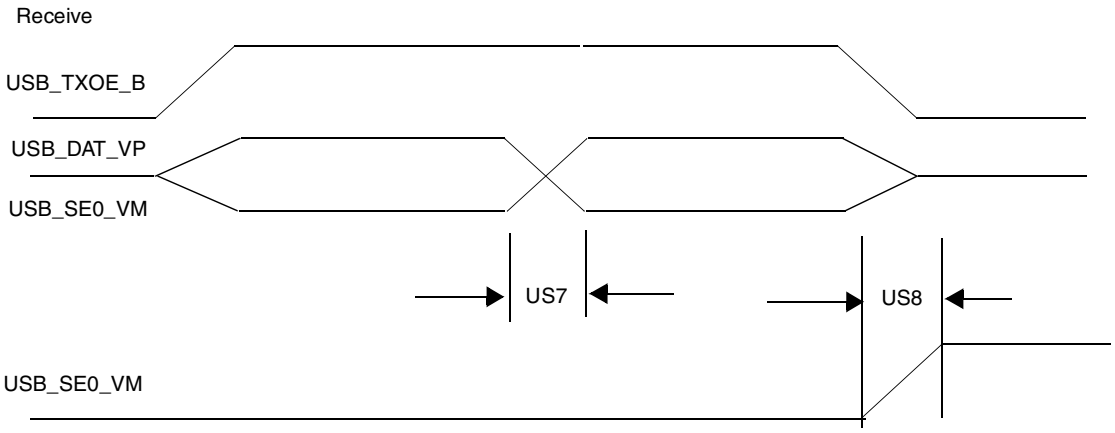

Figure 101. USB Receive Waveform in DAT_SE0 Bi-Directional Mode

Table 114. Definitions of USB Receive Waveform in DAT_SE0 Bi-Directional Mode

ID	Parameter	Signal Name	Direction	Min	Max	Unit	Conditions/ Reference Signal
US1	TX Rise/Fall Time	USB_DAT_VP	Out	—	5.0	ns	50 pF
US2	TX Rise/Fall Time	USB_SE0_VM	Out	—	5.0	ns	50 pF
US3	TX Rise/Fall Time	USB_TXOE_B	Out	—	5.0	ns	50 pF
US4	TX Duty Cycle	USB_DAT_VP	Out	49.0	51.0	%	—
US7	RX Rise/Fall Time	USB_DAT_VP	In	—	3.0	ns	35 pF
US8	RX Rise/Fall Time	USB_SE0_VM	In	—	3.0	ns	35 pF

4.7.17.1.2 USB DAT_SE0 Unidirectional Mode

Table 115 shows the signal definitions in DAT_SE0 unidirectional mode

Table 115. Signal Definitions—DAT_SE0 Unidirectional Mode

Name	Direction	Signal Description
USB_TXOE_B	Out	Transmit enable, active low
USB_DAT_VP	Out	TX data when USB_TXOE_B is low
USB_SE0_VM	Out	SE0 drive when USB_TXOE_B is low
USB_VP1	In	Buffered data on DP when USB_TXOE_B is high
USB_VM1	In	Buffered data on DM when USB_TXOE_B is high
USB_RCV	In	Differential RX data when USB_TXOE_B is high

Figure 102 and Figure 103 shows the USB transmit/receive waveform in DAT_SE0 uni-directional mode respectively.

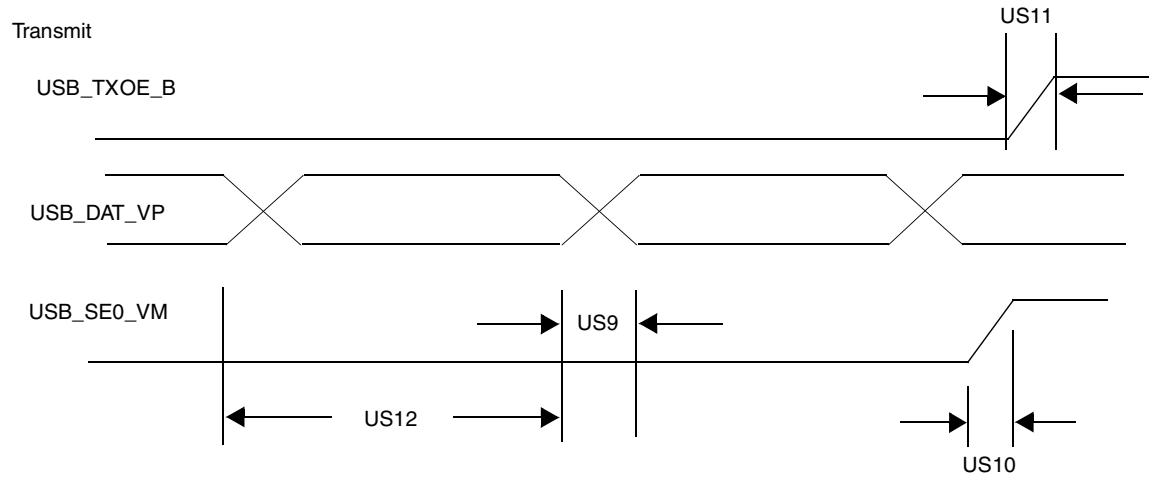

Figure 102. USB Transmit Waveform in DAT_SE0 Uni-directional Mode

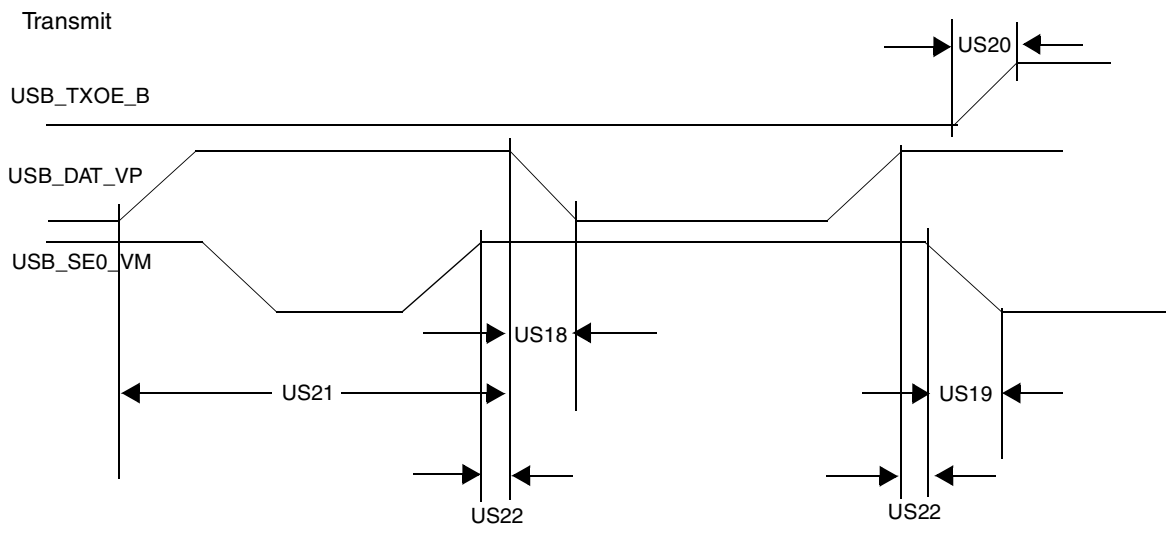

Figure 104. USB Transmit Waveform in VP_VM Bi-Directional Mode

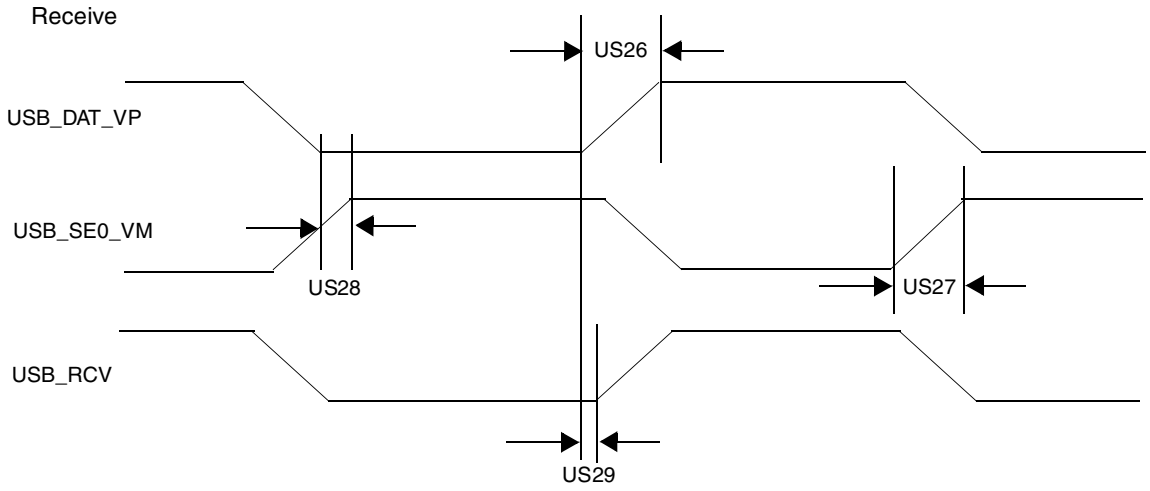

Figure 105. USB Receive Waveform in VP_VM Bi-Directional Mode

Table 118 shows the USB port timing specification in VP_VM bi-directional mode.

Table 118. USB Port Timing Specification in VP_VM Bi-directional Mode

ID	Parameter	Signal Name	Direction	Min	Max	Unit	Condition/Reference Signal
US18	TX Rise/Fall Time	USB_DAT_VP	Out	—	5.0	ns	50 pF
US19	TX Rise/Fall Time	USB_SE0_VM	Out	—	5.0	ns	50 pF
US20	TX Rise/Fall Time	USB_TXOE_B	Out	—	5.0	ns	50 pF
US21	TX Duty Cycle	USB_DAT_VP	Out	49.0	51.0	%	—
US22	TX Overlap	USB_SE0_VM	Out	–3.0	3.0	ns	USB_DAT_VP

Table 127. 19 x 19 mm Ground, Power, Sense, and Reference Contact Assignments (continued)

Contact Name	Contact Assignment
NVCC_IPU2	T18
NVCC_IPU4	G16
NVCC_IPU5	H17
NVCC_IPU6	J17
NVCC_IPU7	K17
NVCC_IPU8	P18
NVCC_IPU9	R18
NVCC_NANDF_A	E6, F5
NVCC_NANDF_B	G9
NVCC_NANDF_C	G10
NVCC_OSC	W17
NVCC_PER3	U18
NVCC_PER5	G15
NVCC_PER8	H16
NVCC_PER9	H10
NVCC_PER10	H11
NVCC_PER11	G11
NVCC_PER12	G12
NVCC_PER13	G13
NVCC_PER14	U13
NVCC_PER15	H15
NVCC_PER17	G14
NVCC_SRTC_POW	U14
NVCC_TV_BACK	U16
NVCC_USBPHY	L17
RREFEXT	K19
SGND	J11
SVCC	H14
SVDDGP	F13
TVDAC_DHVDD	V16
VBUS	K20
VCC	H13, J15, J16, K15, K16, L7, L15, M7, N7, N17, P7, P17, R17, T8, T9, T10, T11, T12, T17
VDD_ANA_PLL_A	V6

Table 128. 19 x 19 mm Signal Assignments, Power Rails, and I/O (continued)

Contact Name	Contact Assignment	Power Rail	I/O Buffer Type	Direction after Reset[1]	Configuraton after Reset[1]
NANDF_D5	A5	NVCC_NANDF_C	UHVIO	Input	Keeper
NANDF_D6	B6	NVCC_NANDF_C	UHVIO	Input	Keeper
NANDF_D7	C6	NVCC_NANDF_B	UHVIO	Input	Keeper
NANDF_D8	A4	NVCC_NANDF_B	UHVIO	Input	Keeper
NANDF_D9	E7	NVCC_NANDF_B	UHVIO	Input	Keeper
NANDF_RB0	D2	NVCC_NANDF_A	UHVIO	Input	100 kΩ pull-up
NANDF_RB1	D4	NVCC_NANDF_A	UHVIO	Input	100 kΩ pull-up
NANDF_RB2	D3	NVCC_NANDF_A	UHVIO	Input	100 kΩ pull-up
NANDF_RB3	C1	NVCC_NANDF_A	UHVIO	Input	100 kΩ pull-up
NANDF_RDY_INT	B3	NVCC_NANDF_B	UHVIO	Input	100 kΩ pull-up
NANDF_RE_B	E2	NVCC_NANDF_A	UHVIO	Output	—
NANDF_WE_B	E1	NVCC_NANDF_A	UHVIO	Output	—
NANDF_WP_B	D1	NVCC_NANDF_A	UHVIO	Output	—
OWIRE_LINE	E14	NVCC_PER12	GPIO	Input	100 kΩ pull-up
PMIC_INT_REQ	AA16	NVCC_SRTC_POW	GPIO	Input	100 kΩ pull-up
PMIC_ON_REQ	W16	NVCC_SRTC_POW	GPIO	Input	100 kΩ pull-up
PMIC_RDY	AA17	NVCC_SRTC_POW	GPIO	Input	100 kΩ pull-up
PMIC_STBY_REQ	Y15	NVCC_SRTC_POW	GPIO	Input	100 kΩ pull-up
POR_B	U20	NVCC_PER3	LVIO	Input	100 kΩ pull-up
RESET_IN_B	Y21	NVCC_PER3	LVIO	Input	100 kΩ pull-up
SD1_CLK	A17	NVCC_PER15	UHVIO	Output	—
SD1_CMD	E16	NVCC_PER15	UHVIO	Input	47 kΩ pull-up
SD1_DATA0	D16	NVCC_PER15	UHVIO	Input	47 kΩ pull-up
SD1_DATA1	A18	NVCC_PER15	UHVIO	Input	47 kΩ pull-up
SD1_DATA2	F17	NVCC_PER15	UHVIO	Input	47 kΩ pull-up
SD1_DATA3	A19	NVCC_PER15	UHVIO	Input	360 kΩ pull-down
SD2_CLK	B18	NVCC_PER17	UHVIO	Output	—
SD2_CMD	G17	NVCC_PER17	UHVIO	Input	47 kΩ pull-up
SD2_DATA0	E17	NVCC_PER17	UHVIO	Input	47 kΩ pull-up
SD2_DATA1	B19	NVCC_PER17	UHVIO	Input	47 kΩ pull-up
SD2_DATA2	D17	NVCC_PER17	UHVIO	Input	47 kΩ pull-up
SD2_DATA3	C17	NVCC_PER17	UHVIO	Input	360 kΩ pull-down