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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	ARM® Cortex®-A7
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	528MHz
Co-Processors/DSP	Multimedia; NEON™ SIMD
RAM Controllers	LPDDR2, DDR3, DDR3L
Graphics Acceleration	No
Display & Interface Controllers	LVDS
Ethernet	10/100Mbps (1)
SATA	-
USB	USB 2.0 + PHY (2)
Voltage - I/O	1.2V, 1.35V, 1.5V, 1.8V, 2.5V, 2.8V, 3.3V
Operating Temperature	-40°C ~ 125°C (TJ)
Security Features	ARM TZ, A-HAB, CAAM, CSU, SJC, SNVS
Package / Case	289-LFBGA
Supplier Device Package	289-MAPBGA (14x14)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mcimx6g1avm05aa

The features of the i.MX 6UltraLite processor include[1]:

- Single-core ARM Cortex-A7—The single core A7 provides a cost-effective and power-efficient solution.
- Multilevel memory system—The multilevel memory system of each device is based on the L1 instruction and data caches, L2 cache, and internal and external memory. The device supports many types of external memory devices, including DDR3, low voltage DDR3, LPDDR2, NOR Flash, NAND Flash (MLC and SLC), OneNAND™, Quad SPI, and managed NAND, including eMMC up to rev 4.4/4.41/4.5.
- Smart speed technology—Power management implemented throughout the IC that enables multimedia features and peripherals to consume minimum power in both active and various low power modes.
- Dynamic voltage and frequency scaling—The processor improves the power efficiency by scaling the voltage and frequency to optimize performance.
- Multimedia powerhouse—Multimedia performance is enhanced by a multilevel cache system, NEON™ MPE (Media Processor Engine) co-processor, a programmable smart DMA (SDMA) controller, an asynchronous audio sample rate converter, and a Pixel processing pipeline (PXP) to support 2D image processing, including color-space conversion, scaling, alpha-blending, and rotation.
- Ethernet interfaces—10/100 Mbps Ethernet controllers.
- Human-machine interface—Support digital parallel display interface.
- Interface flexibility—Each processor supports connections to a variety of interfaces: High-speed USB on-the-go with PHY, multiple expansion card port (high-speed MMC/SDIO host and other), 12-bit ADC module, CAN port, smart card interface compatible with EMV Standard v4.3, and a variety of other popular interfaces (such as UART, I^2C, and I^2S serial audio).
- Automotive environment support—Each processor includes interfaces, such as CAN, three SAI audio interfaces, and an asynchronous sample rate converter for multichannel/multisource audio.
- Advanced security—The processor delivers hardware-enabled security features that enable secure e-commerce, digital rights management (DRM), information encryption, secure boot, and secure software downloads. The security features are discussed in detail in the *i.MX 6UltraLite Security Reference Manual* (IMX6ULSRM).
- Integrated power management—The processor integrates linear regulators and internally generate voltage levels for different domains. This significantly simplifies system power management structure.

For a comprehensive list of the i.MX 6UltraLite features, see Section 1.2, "Features"".

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1. The actual feature set depends on the part numbers as described in the Table 1 and Table 2.

Table 2. Detailed Peripherals Information (continued)[1,2,3]

Peripheral Name	Instance	G0	G1	G2	G3
SDIO	uSDHC1	Y	Y	Y	Y
	uSDHC2	Y	Y	Y	Y
UART	UART1	Y	Y	Y	Y
	UART2	Y	Y	Y	Y
	UART3	Y	Y	Y	Y
	UART4	Y	Y	Y	Y
	UART5	NA	Y	Y	Y
	UART6	NA	Y	Y	Y
	UART7	NA	Y	Y	Y
	UART8	NA	Y	Y	Y
ISO7816-3	SIM1	NA	Y	Y	Y
	SIM2	NA	Y	Y	Y
I2C	I2C1	Y	Y	Y	Y
	I2C2	Y	Y	Y	Y
	I2C3	NA	Y	Y	Y
	I2C4	NA	Y	Y	Y
SPI	ECSPI1	Y	Y	Y	Y
	ECSPI2	Y	Y	Y	Y
	ECSPI3	NA	Y	Y	Y
	ECSPI4	NA	Y	Y	Y
I2S/SAI	SAI1	Y	Y	Y	Y
	SAI2	NA	Y	Y	Y
	SAI3	NA	Y	Y	Y

Table 3. i.MX 6UltraLite Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
CSU	Central Security Unit	Security	The Central Security Unit (CSU) is responsible for setting comprehensive security policy within the i.MX 6UltraLite platform.
DAP	Debug Access Port	System Control Peripherals	The DAP provides real-time access for the debugger without halting the core to: • System memory and peripheral registers • All debug configuration registers The DAP also provides debugger access to JTAG scan chains. The DAP module is internal to the Cortex-A7 Core Platform.
eCSPI1 eCSPI2 eCSPI3 eCSPI4	Configurable SPI	Connectivity Peripherals	Full-duplex enhanced Synchronous Serial Interface, with data rate up to 52 Mbit/s. It is configurable to support Master/Slave modes, four chip selects to support multiple peripherals.
EIM	NOR-Flash /PSRAM interface	Connectivity Peripherals	The EIM NOR-FLASH / PSRAM provides: • Support 16-bit PSRAM memories (sync and async operating modes), at slow frequency • Support 16-bit NOR-Flash memories, at slow frequency • Multiple chip selects
EMV SIM1 EMV SIM2	Europay, Master and Visa Subscriber Identification Module	Connectivity peripherals	EMV SIM is designed to facilitate communication to Smart Cards compatible to the EMV version 4.3 standard (Book 1) and Smart Cards compatible with ISO/IEC 7816-3 standard.
ENET1 ENET2	Ethernet Controller	Connectivity Peripherals	The Ethernet Media Access Controller (MAC) is designed to support 10/100 Mbit/s Ethernet/IEEE 802.3 networks. An external transceiver interface and transceiver function are required to complete the interface to the media. The module has dedicated hardware to support the IEEE 1588 standard. See the ENET chapter of the reference manual for details.
EPIT1 EPIT2	Enhanced Periodic Interrupt Timer	Timer Peripherals	Each EPIT is a 32-bit "set and forget" timer that starts counting after the EPIT is enabled by software. It is capable of providing precise interrupts at regular intervals with minimal processor intervention. It has a 12-bit prescaler for division of input clock frequency to get the required time setting for the interrupts to occur, and counter value can be programmed on the fly.
FLEXCAN1 FLEXCAN2	Flexible Controller Area Network	Connectivity Peripherals	The CAN protocol was primarily, but not only, designed to be used as a vehicle serial data bus, meeting the specific requirements of this field: real-time processing, reliable operation in the Electromagnetic interference (EMI) environment of a vehicle, cost-effectiveness and required bandwidth. The FlexCAN module is a full implementation of the CAN protocol specification, Version 2.0 B, which supports both standard and extended message frames.

Table 3. i.MX 6UltraLite Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
QSPI	Quad SPI	Connectivity peripherals	Quad SPI module act as an interface to external serial flash devices. This module contains the following features: • Flexible sequence engine to support various flash vendor devices • Single pad/Dual pad/Quad pad mode of operation • Single Data Rate/Double Data Rate mode of operation • Parallel Flash mode • DMA support • Memory mapped read access to connected flash devices • Multi-master access with priority and flexible and configurable buffer for each master
SAI1 SAI2 SAI3	—	—	The SAI module provides a synchronous audio interface (SAI) that supports full duplex serial interfaces with frame synchronization, such as I2S, AC97, TDM, and codec/DSP interfaces.
SDMA	Smart Direct Memory Access	System Control Peripherals	The SDMA is multi-channel flexible DMA engine. It helps in maximizing system performance by off-loading the various cores in dynamic data routing. It has the following features: • Powered by a 16-bit instruction-set micro-RISC engine • Multi-channel DMA supporting up to 32 time-division multiplexed DMA channels • 48 events with total flexibility to trigger any combination of channels • Memory accesses including linear, FIFO, and 2D addressing • Shared peripherals between ARM and SDMA • Very fast context-switching with 2-level priority based preemptive multi-tasking • DMA units with auto-flush and prefetch capability • Flexible address management for DMA transfers (increment, decrement, and no address changes on source and destination address) • DMA ports can handle unit-directional and bi-directional flows (copy mode) • Support of byte-swapping • Library of Scripts and API is available
2x SIMv2	Smart Card	Connectivity peripherals	Smart card interface compliant with ISO7816.

i.MX 6UltraLite Automotive Applications Processors, Rev. 2.2, 05/2017

Table 9. 14x14 MM (VM) Thermal Resistance Data[1]

Rating	Test Conditions	Symbol	Value	Unit	Notes
Junction to Board	—	$R_{\theta JB}$	21.8	°C/W	5
Junction to Case	—	$R_{\theta JC}$	19.3	°C/W	6
Junction to Package Top	Natural Convection	Ψ_{JT}	2.3	°C/W	7
Junction to Package Bottom	Natural Convection	Ψ_{JB}	12.0	°C/W	8

1 As per JEDEC JESD51-2 the intent of (thermal resistance) measurement is solely for a thermal performance comparison of one package to another in a standardized environment. This methodology is not meant to and will not predict the performance of a package in an application-specific environment.

2 Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.

3 Per SEMI G38-87 and JEDEC JESD51-2 with the single layer board horizontal.

4 Per JEDEC JESD51-6 with the board horizontal.

5 Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

6 Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).

7 Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

8 Thermal characterization parameter indicating the temperature difference between package bottom center and the junction temperature per JEDEC JESD51-12. When Greek letters are not available, the thermal characterization parameter is written as Psi-JB

4.1.3   Operating ranges

Table 10 provides the operating ranges of the i.MX 6UltraLite processors. For details on the chip's power structure, see the "Power Management Unit (PMU)" chapter of the *i.MX 6UltraLite Reference Manual* (IMX6ULRM).

The system clock input XTALI is used to generate the main system clock. It supplies the PLLs and other peripherals. The system clock input can be connected to either external oscillator or a crystal using internal oscillator amplifier.

Table 12 shows the interface frequency requirements.

Table 12. External Input Clock Frequency

Parameter Description	Symbol	Min	Typ	Max	Unit
RTC_XTALI Oscillator[1,2]	f_{ckil}	—	32.768[3]/32.0	—	kHz
XTALI Oscillator[2,4]	f_{xtal}	—	24	—	MHz

[1] External oscillator or a crystal with internal oscillator amplifier.

[2] The required frequency stability of this clock source is application dependent. For recommendations, see the Hardware Development Guide for *i.MX 6UltraLite Applications Processors* (IMX6ULHDG).

[3] Recommended nominal frequency 32.768 kHz.

[4] External oscillator or a fundamental frequency crystal with internal oscillator amplifier.

The typical values shown in Table 12 are required for use with NXP BSPs to ensure precise time keeping and USB operation. For RTC_XTALI operation, two clock sources are available.

- On-chip 40 kHz ring oscillator—this clock source has the following characteristics:
  — Approximately 25 μA more Idd than crystal oscillator
  — Approximately ±50% tolerance
  — No external component required
  — Starts up quicker than 32 kHz crystal oscillator
- External crystal oscillator with on-chip support circuit:
  — At power up, ring oscillator is utilized. After crystal oscillator is stable, the clock circuit switches over to the crystal oscillator automatically.
  — Higher accuracy than ring oscillator
  — If no external crystal is present, then the ring oscillator is utilized

The decision of choosing a clock source should be taken based on real-time clock use and precision time-out.

4.1.5   Maximum supply currents

The data shown in Table 13 represent a use case designed specifically to show the maximum current consumption possible. All cores are running at the defined maximum frequency and are limited to L1 cache accesses only to ensure no pipeline stalls. Although a valid condition, it would have a very limited practical use case, if at all, and be limited to an extremely low duty cycle unless the intention was to specifically show the worst case power consumption.

4.4.2 528 MHz PLL

Table 17. 528 MHz PLL's Electrical Parameters

Parameter	Value
Clock output range	528 MHz PLL output
Reference clock	24 MHz
Lock time	<11250 reference cycles

4.4.3 Ethernet PLL

Table 18. Ethernet PLL's Electrical Parameters

Parameter	Value
Clock output range	500 MHz
Reference clock	24 MHz
Lock time	<11250 reference cycles

4.4.4 480 MHz PLL

Table 19. 480 MHz PLL's Electrical Parameters

Parameter	Value
Clock output range	480 MHz PLL output
Reference clock	24 MHz
Lock time	<383 reference cycles

4.4.5 ARM PLL

Table 20. ARM PLL's Electrical Parameters

Parameter	Value
Clock output range	648 MHz ~ 1296 MHz
Reference clock	24 MHz
Lock time	<2250 reference cycles

4.10.2   MMDC supported DDR3/DDR3L/LPDDR2 configurations

Table 40 shows the MMDC supported DDR3/DDR3L/LPDDR2 configurations.

Table 40. i.MX 6UltraLite Supported DDR3/DDR3L/LPDDR2 Configurations

Parameter	DDR3	DDR3L	LDDDR2
Clock frequency	400 MHz	400 MHz	400 MHz
Bus width	16-bit	16-bit	16-bit
Channel	Single	Single	Single
Chip selects	2	2	2

4.11   General-Purpose Media Interface (GPMI) timing

The i.MX 6UltraLite GPMI controller is a flexible interface NAND Flash controller with 8-bit data width, up to 200 MB/s I/O speed and individual chip select.

It supports Asynchronous timing mode, Source Synchronous timing mode and Samsung Toggle timing mode separately described in the following subsections.

4.11.1   Asynchronous mode AC timing (ONFI 1.0 compatible)

Asynchronous mode AC timings are provided as multiplications of the clock cycle and fixed delay. The maximum I/O speed of GPMI in asynchronous mode is about 50 MB/s. Figure 21 through Figure 24 depicts the relative timing between GPMI signals at the module level for different operations under asynchronous mode. Table 41 describes the timing parameters (NF1–NF17) that are shown in the figures.
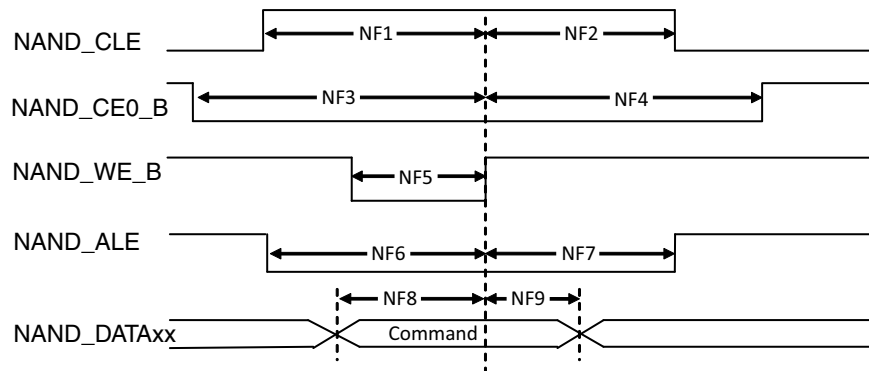

Figure 21. Command Latch Cycle Timing Diagram

Table 41. Asynchronous Mode Timing Parameters[1]

ID	Parameter	Symbol	Timing T = GPMI Clock Cycle		Unit
			Min.	**Max.**	
NF1	NAND_CLE setup time	tCLS	$(AS + DS) \times T - 0.12$ [see [2,3]]		ns
NF2	NAND_CLE hold time	tCLH	$DH \times T - 0.72$ [see [2]]		ns
NF3	NAND_CE0_B setup time	tCS	$(AS + DS + 1) \times T$ [see [3,2]]		ns
NF4	NAND_CE0_B hold time	tCH	$(DH+1) \times T - 1$ [see [2]]		ns
NF5	NAND_WE_B pulse width	tWP	$DS \times T$ [see [2]]		ns
NF6	NAND_ALE setup time	tALS	$(AS + DS) \times T - 0.49$ [see [3,2]]		ns
NF7	NAND_ALE hold time	tALH	$(DH \times T - 0.42$ [see [2]]		ns
NF8	Data setup time	tDS	$DS \times T - 0.26$ [see [2]]		ns
NF9	Data hold time	tDH	$DH \times T - 1.37$ [see [2]]		ns
NF10	Write cycle time	tWC	$(DS + DH) \times T$ [see [2]]		ns
NF11	NAND_WE_B hold time	tWH	$DH \times T$ [see [2]]		ns
NF12	Ready to NAND_RE_B low	tRR[4]	$(AS + 2) \times T$ [see [3,2]]	—	ns
NF13	NAND_RE_B pulse width	tRP	$DS \times T$ [see [2]]		ns
NF14	READ cycle time	tRC	$(DS + DH) \times T$ [see [2]]		ns
NF15	NAND_RE_B high hold time	tREH	$DH \times T$ [see [2]]		ns
NF16	Data setup on read	tDSR	—	$(DS \times T - 0.67)/18.38$ [see [5,6]]	ns
NF17	Data hold on read	tDHR	$0.82/11.83$ [see [5,6]]	—	ns

[1] GPMI's Async Mode output timing can be controlled by the module's internal registers
    HW_GPMI_TIMING0_ADDRESS_SETUP, HW_GPMI_TIMING0_DATA_SETUP, and HW_GPMI_TIMING0_DATA_HOLD.
    This AC timing depends on these registers settings. In the table, AS/DS/DH represents each of these settings.

[2]   AS minimum value can be 0, while DS/DH minimum value is 1.

[3] T = GPMI clock period -0.075ns (half of maximum p-p jitter).

[4] NF12 is guaranteed by the design.

[5] Non-EDO mode.

[6] EDO mode, GPMI clock ≈ 100 MHz
    (AS=DS=DH=1, GPMI_CTL1 [RDN_DELAY] = 8, GPMI_CTL1 [HALF_PERIOD] = 0).

In EDO mode (Figure 24), NF16/NF17 is different from the definition in non-EDO mode (Figure 23). They are called tREA/tRHOH (RE# access time/RE# HIGH to output hold). The typical values for them are 16 ns (max for tREA)/15 ns (min for tRHOH) at 50 MB/s EDO mode. In EDO mode, GPMI will sample NAND_DATAxx at rising edge of delayed NAND_RE_B provided by an internal DPLL. The delay value can be controlled by GPMI_CTRL1.RDN_DELAY (see the GPMI chapter of the *i.MX 6UltraLite Reference Manual*). The typical value of this control register is 0x8 at 50 MT/s EDO mode. But if the board delay is big enough and cannot be ignored, the delay value should be made larger to compensate the board delay.

Table 59. LCD Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
L1	LCD pixel clock frequency	tCLK(LCD)	—	150	MHz
L2	LCD pixel clock high (falling edge capture)	tCLKH(LCD)	3	—	ns
L3	LCD pixel clock low (rising edge capture)	tCLKL(LCD)	3	—	ns
L4	LCD pixel clock high to data valid (falling edge capture)	td(CLKH-DV)	-1	1	ns
L5	LCD pixel clock low to data valid (rising edge capture)	td(CLKL-DV)	-1	1	ns
L6	LCD pixel clock high to control signal valid (falling edge capture)	td(CLKH-CTRLV)	-1	1	ns
L7	LCD pixel clock low to control signal valid (rising edge capture)	td(CLKL-CTRLV)	-1	1	ns

4.12.8.1　LCDIF signal mapping

Table 60 lists the details about the mapping signals.

Table 60. LCD Signal Parameters

Pin name	8-bit DOTCLK LCD IF	16-bit DOTCLK LCD IF	18-bit DOTCLK LCD IF	24-bit DOTCLK LCD IF	8-bit DVI LCD IF
LCD_RS	—	—	—	—	CCIR_CLK
LCD_VSYNC* (Two options)	LCD_VSYNC	LCD_VSYNC	LCD_VSYNC	LCD_VSYNC	—
LCD_HSYNC	LCD_HSYNC	LCD_HSYNC	LCD_HSYNC	LCD_HSYNC	—
LCD_DOTCLK	LCD_DOTCLK	LCD_DOTCLK	LCD_DOTCLK	LCD_DOTCLK	—
LCD_ENABLE	LCD_ENABLE	LCD_ENABLE	LCD_ENABLE	LCD_ENABLE	—
LCD_D23	—	—	—	R[7]	—
LCD_D22	—	—	—	R[6]	—
LCD_D21	—	—	—	R[5]	—
LCD_D20	—	—	—	R[4]	—
LCD_D19	—	—	—	R[3]	—
LCD_D18	—	—	—	R[2]	—
LCD_D17	—	—	R[5]	R[1]	—
LCD_D16	—	—	R[4]	R[0]	—
LCD_D15 / VSYNC*	—	R[4]	R[3]	G[7]	—
LCD_D14 / HSYNC**	—	R[3]	R[2]	G[6]	—
LCD_D13 / LCD_DOTCLK **	—	R21]	R[1]	G[5]	—

Table 63. QuadSPI Output/Write Timing (SDR mode)

Symbol	Parameter	Value		Unit
		Min	**Max**	
T_{DVO}	Output data valid time	—	2	ns
T_{DHO}	Output data hold time	0	—	ns
T_{CK}	SCK clock period	10	—	ns
T_{CSS}	Chip select output setup time	3	—	SCK cycle(s)
T_{CSH}	Chip select output hold time	3	—	SCK cycle(s)

NOTE

T_{css} and T_{csh} are configured by the QuadSPIx_FLSHCR register, the default value of 3 are shown on the timing. Please refer to the *i.MX 6UltraLite Reference Manual (IMX6ULRM)* for more details.
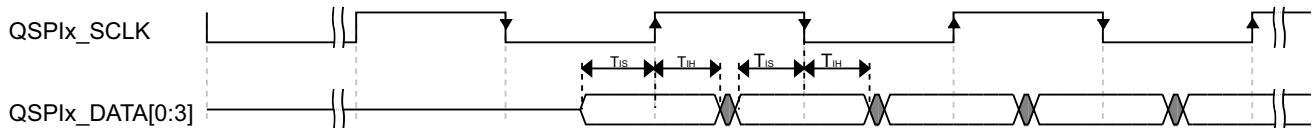
4.12.9.2 DDR mode

Figure 52. QuadSPI Input/Read Timing (DDR mode with internal sampling)

Table 64. QuadSPI Input/Read Timing (DDR mode with internal sampling)

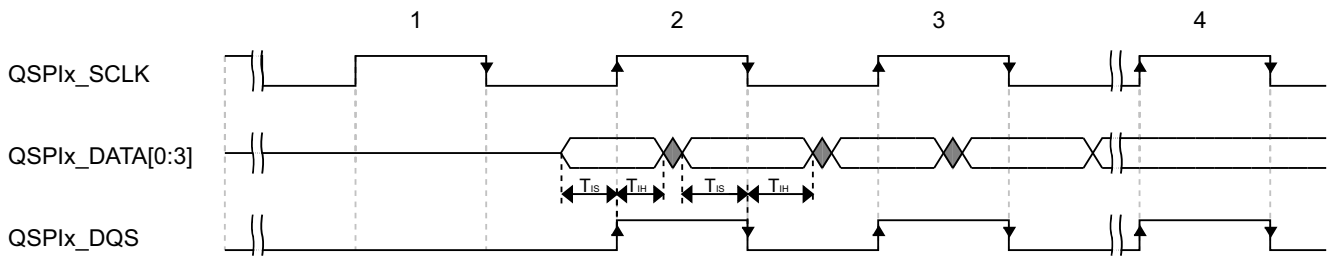| Symbol	Parameter	Value		Unit
		Min	**Max**	
T_{IS}	Setup time for incoming data	8.67	—	ns
T_{IH}	Hold time requirement for incoming data	0	—	ns

Figure 53. QuadSPI Input/Read Timing (DDR mode with loopback DQS sampling)

Table 65. QuadSPI Input/Read Timing (DDR mode with loopback DQS sampling)

Symbol	Parameter	Value		Unit
		Min	Max	
T_{IS}	Setup time for incoming data	2	—	ns
T_{IH}	Hold time requirement for incoming data	1	—	ns

NOTE

- For internal sampling, the timing values assumes using sample point 0, that is QuadSPIx_SMPR[SDRSMP] = 0.

- For loopback DQS sampling, the data strobe is output to the DQS pad together with the serial clock. The data strobe is looped back from DQS pad and used to sample input data.
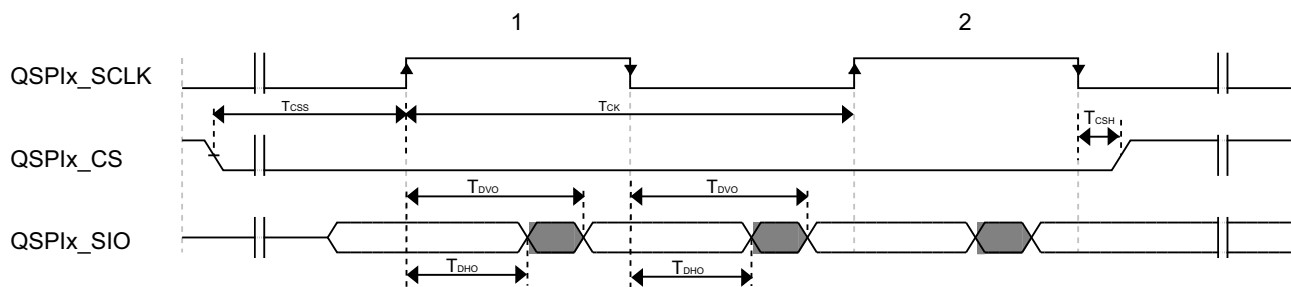

Figure 54. QuadSPI Output/Write Timing (DDR mode)

Table 66. QuadSPI Output/Write Timing (DDR mode)

Symbol	Parameter	Value		Unit
		Min	Max	
T_{DVO}	Output data valid time	—	$0.25 \times T_{SCLK} + 2$ ns	ns
T_{DHO}	Output data hold time	$0.25 \times T_{SCLK}$	—	ns
T_{CK}	SCK clock period	20	—	ns

Figure 55. SAI Timing — Master Modes

Table 68. Master Mode SAI Timing

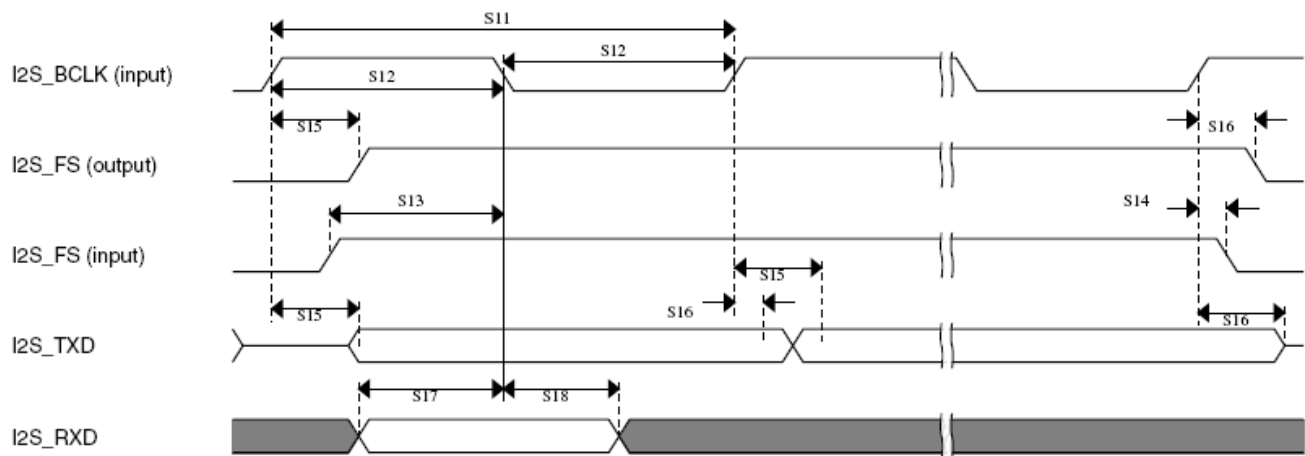| Num	Characteristic	Min	Max	Unit
S11	SAI_BCLK cycle time (input)	4 x t_{sys}	—	ns
S12	SAI_BCLK pulse width high/low (input)	40%	60%	BCLK period
S13	SAI_FS input setup before SAI_BCLK	10	—	ns
S14	SAI_FA input hold after SAI_BCLK	2	—	ns
S15	SAI_BCLK to SAI_TXD/SAI_FS output valid	—	20	ns
S16	SAI_BCLK to SAI_TXD/SAI_FS output invalid	0	—	ns
S17	SAI_RXD setup before SAI_BCLK	10	—	ns
S18	SAI_RXD hold after SAI_BCLK	2	—	ns

Figure 56. SAI Timing — Slave Modes

4.12.13.1.2 UART receiver

Figure 64 depicts the RS-232 serial mode receives timing with 8 data bit/1 stop bit format. Table 72 lists serial mode receive timing characteristics.
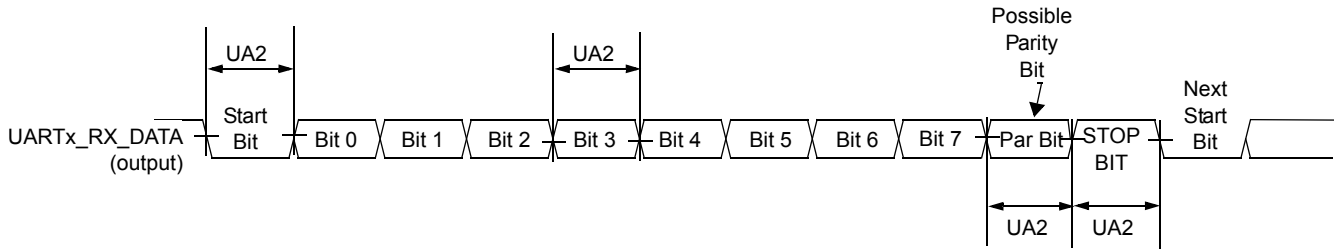

Figure 64. UART RS-232 Serial Mode Receive Timing Diagram

Table 72. RS-232 Serial Mode Receive Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
UA2	Receive Bit Time[1]	t_{Rbit}	$1/F_{baud\_rate}$[2] $- 1/(16 \times F_{baud\_rate})$	$1/F_{baud\_rate} + 1/(16 \times F_{baud\_rate})$	—

[1] The UART receiver can tolerate $1/(16 \times F_{baud\_rate})$ tolerance in each bit. But accumulation tolerance in one frame must not exceed $3/(16 \times F_{baud\_rate})$.

[2] F_{baud_rate}: Baud rate frequency. The maximum baud rate the UART can support is (*ipg_perclk* frequency)/16.

4.12.13.1.3 UART IrDA mode timing

The following subsections give the UART transmit and receive timings in IrDA mode.

UART IrDA mode transmitter

Figure 65 depicts the UART IrDA mode transmit timing, with 8 data bit/1 stop bit format. Table 73 lists the transmit timing characteristics.
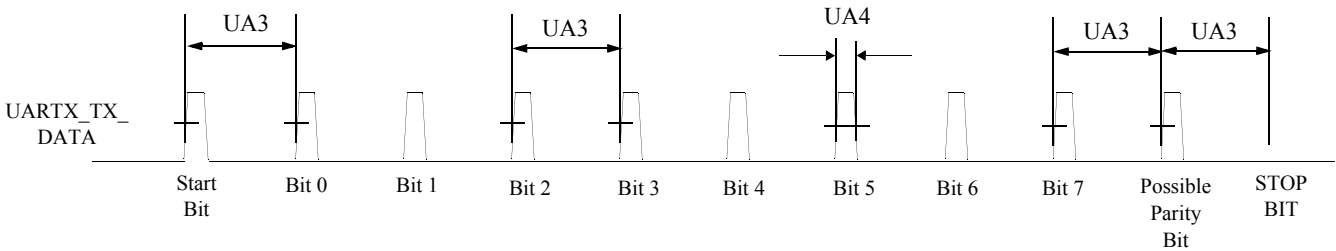

Figure 65. UART IrDA Mode Transmit Timing Diagram

Table 73. IrDA Mode Transmit Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
UA3	Transmit Bit Time in IrDA mode	t_{TIRbit}	$1/F_{baud\_rate}$[1] $- T_{ref\_clk}$[2]	$1/F_{baud\_rate} + T_{ref\_clk}$	—
UA4	Transmit IR Pulse Duration	$t_{TIRpulse}$	$(3/16) \times (1/F_{baud\_rate}) - T_{ref\_clk}$	$(3/16) \times (1/F_{baud\_rate}) + T_{ref\_clk}$	—

[1] F_{baud_rate}: Baud rate frequency. The maximum baud rate the UART can support is (*ipg_perclk* frequency)/16.

2 Typical values assume V_{DDAD} = 3.0 V, Temp = 25°C, F_{adck}=20 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

NOTE

The ADC electrical spec would be met with the calibration enabled configuration.

5   Boot mode configuration

This section provides information on boot mode configuration pins allocation and boot devices interfaces allocation.

5.1   Boot mode configuration pins

Table 77 provides boot options, functionality, fuse values, and associated pins. Several input pins are also sampled at reset and can be used to override fuse values, depending on the value of BT_FUSE_SEL fuse. The boot option pins are in effect when BT_FUSE_SEL fuse is '0' (cleared, which is the case for an unblown fuse). For detailed boot mode options configured by the boot mode pins, see the i.MX 6UltraLite Fuse Map document and the System Boot chapter in *i.MX 6UltraLite Reference Manual (IMX6ULRM)*.

Table 77. Fuses and Associated Pins Used for Boot

Pin	Direction at reset	eFuse name	Details
BOOT_MODE0	Input with 100 K pull-down	N/A	Boot mode selection
BOOT_MODE1	Input with 100 K pull-down	N/A	Boot mode selection

Table 78. QSPI Boot trough QSPI (continued)

NAND_READY_B	qspi.A_DATA[0]	Alt2	Yes	Yes					
NAND_CE0_B	qspi.A_DATA[1]	Alt2	Yes	Yes					
NAND_CE1_B	qspi.A_DATA[2]	Alt2	Yes	Yes					
NAND_CLE	qspi.A_DATA[3]	Alt2	Yes	Yes					
NAND_DATA05	qspi.B_DATA[3]	Alt2						Yes	
NAND_DATA04	qspi.B_DATA[2]	Alt2						Yes	
NAND_DATA03	qspi.B_DATA[1]	Alt2						Yes	
NAND_DATA02	qspi.B_DATA[0]	Alt2						Yes	
NAND_WE_B	qspi.B_SS0_B	Alt2						Yes	
NAND_RE_B	qspi.B_SCLK	Alt2						Yes	
NAND_DATA07	qspi.A_SS1_B	Alt2					Yes		
NAND_ALE	qspi.A_DQS	Alt2				Yes			
NAND_DATA00	qspi.B_SS1_B	Alt2							Yes
NAND_DATA01	qspi.B_DQS	Alt2						Yes	

Table 79. SPI Boot through ECSPI1

Ball Name	Signal Name	Mux Mode	Common	BOOT_CFG4 [5:4]=00b	BOOT_CFG4 [5:4]=01b	BOOT_CFG4 [5:4]=10b	BOOT_CFG4 [5:4]=11b
CSI_DATA07	ecspi1.MISO	Alt 3	Yes				
CSI_DATA06	ecspi1.MOSI	Alt 3	Yes				
CSI_DATA04	ecspi1.SCLK	Alt 3	Yes				
CSI_DATA05	ecspi1.SS0	Alt 3		Yes			
LCD_DATA05	ecspi1.SS1	Alt 8			Yes		
LCD_DATA06	ecspi1.SS2	Alt 8				Yes	
LCD_DATA07	ecspi1.SS3	Alt 8					Yes

Table 80. SPI Boot through ECSPI2

Ball Name	Signal Name	Mux Mode	Common	BOOT_CFG4[5:4]=00b	BOOT_CFG4 [5:4]=01b	BOOT_CFG4 [5:4]=10b	BOOT_CFG4 [5:4]=11b
CSI_DATA03	ecspi2.MISO	Alt 3	Yes				
CSI_DATA02	ecspi2.MOSI	Alt 3	Yes				
CSI_DATA00	ecspi2.SCLK	Alt 3	Yes				
CSI_DATA01	ecspi2.SS0	Alt 3		Yes			
LCD_HSYNC	ecspi2.SS1	Alt 8			Yes		

6.1.2 14x14 mm supplies contact assignments and functional contact assignments

Table 89 shows the device connection list for ground, sense, and reference contact signals.

Table 89. 14x14 mm Supplies Contact Assignment

Supply Rail Name	Ball(s) Position(s)	Remark
ADC_VREFH	M13	—
DRAM_VREF	p4	—
GPANAIO	R13	—
NGND_KEL0	M12	—
NVCC_CSI	F4	—
NVCC_DRAM	G6, H6, J6, K6, L6, M6	—
NVCC_DRAM_2P5	N6	—
NVCC_ENET	F13	—
NVCC_GPIO	J13	—
NVCC_LCD	E13	—
NVCC_NAND	E7	—
NVCC_PLL	P13	—
NVCC_SD1	C4	—
NVCC_UART	H13	—
VDD_ARM_CAP	G9, G10, G11, H11	—
VDD_HIGH_CAP	R14, R15	—
VDD_HIGH_IN	N13	—
VDD_SNVS_CAP	N12	—
VDD_SNVS_IN	P12	—
VDD_SOC_CAP	G8, H8, J8, J11, K8, K11, L8, L9, L10, L11	—
VDD_SOC_IN	H9, H10, J9, J10, K9, K10	—
VDD_USB_CAP	R12	—
VDDA_ADC_3P3	L13	—
VSS	A1, A17, C3, C7, C11, C15, E8, E11, F6, F7, F8, F9, F10,F11, F12, G3, G5, G7, G12, G15, H7, H12, J5, J7, J12, K7, K12, L3, L7, L12, M7, M8, M9, M10, M11, N3, N5, R3, R5, R7, R11, R16, R17, T14, U1, U14, U17	—

Table 91. 14x14 mm, 0.8 mm Pitch, Ball Map (continued)

N	M	L	K	J	H	G
DRAM_ODT0	DRAM_SDBA0	DRAM_ADDR05	DRAM_ADDR02	DRAM_SDWE_B	DRAM_SDBA1	DRAM_ADDR14
DRAM_CS0_B	DRAM_ADDR03	DRAM_ADDR09	DRAM_SDBA2	DRAM_CAS_B	DRAM_ADDR01	DRAM_ADDR06
VSS	DRAM_SDCKE0	VSS	DRAM_ADDR11	DRAM_SDCKE1	DRAM_ADDR13	VSS
DRAM_ZQPAD	DRAM_ADDR10	DRAM_ADDR12	DRAM_ADDR04	DRAM_ADDR08	DRAM_ADDR07	DRAM_RESET
VSS	DRAM_RAS_B	DRAM_ADDR00	DRAM_ADDR15	VSS	DRAM_CS1_B	VSS
NVCC_DRAM_2P5	NVCC_DRAM	NVCC_DRAM	NVCC_DRAM	NVCC_DRAM	NVCC_DRAM	NVCC_DRAM
TEST_MODE	VSS	VSS	VSS	VSS	VSS	VSS
SNVS_TAMPER5	VSS	VDD_SOC_CAP	VDD_SOC_CAP	VDD_SOC_CAP	VDD_SOC_CAP	VDD_SOC_CAP
SNVS_TAMPER8	VSS	VDD_SOC_CAP	VDD_SOC_IN	VDD_SOC_IN	VDD_SOC_IN	VDD_ARM_CAP
SNVS_TAMPER7	VSS	VDD_SOC_CAP	VDD_SOC_IN	VDD_SOC_IN	VDD_SOC_IN	VDD_ARM_CAP
SNVS_TAMPER6	VSS	VDD_SOC_CAP	VDD_SOC_CAP	VDD_SOC_CAP	VDD_ARM_CAP	VDD_ARM_CAP
VDD_SNVS_CAP	NGND_KEL0	VSS	VSS	VSS	VSS	VSS
VDD_HIGH_IN	ADC_VREFH	VDDA_ADC_3P3	GPIO1_IO00	NVCC_GPIO	NVCC_UART	UART5_RX_DATA
JTAG_TRST_B	JTAG_TCK	GPIO1_IO02	UART1_TX_DATA	UART1_RTS_B	UART2_RTS_B	UART3_RTS_B
JTAG_TDO	GPIO1_IO09	GPIO1_IO01	UART1_CTS_B	UART2_CTS_B	UART3_CTS_B	VSS
JTAG_TDI	GPIO1_IO04	GPIO1_IO07	UART1_RX_DATA	UART2_RX_DATA	UART3_RX_DATA	UART4_RX_DATA
GPIO1_IO08	GPIO1_IO05	GPIO1_IO03	GPIO1_IO06	UART2_TX_DATA	UART3_TX_DATA	UART4_TX_DATA
N	M	L	K	J	H	G

7   Revision history

Table 93 provides a revision history for this data sheet.

Table 93. i.MX 6UltraLite Data Sheet Document Revision History

Rev. Number	Date	Substantive Change(s)
0	01/2016	• Initial release
0.1	02/2016	• Updated Figure 1 Part Number Nomenclature—i.MX 6UltraLite • Updated Table 1 Ordering Information • Updated Table 3 i.MX 6UltraLite Modules List
1	04/2016	• Updated Table 3 i.MX 6UltraLite Module list for BCH descriptions • Updated Table 4 Special Signal Considerations • Added a note for Table 9 14x14 MM Package Thermal Resistance • Updated Table 14 Low Power Mode Current and Power Consumption • Added a note for Table 22 XTALI and RTC_XTALI DC Parameters • Updated Table 37 EIM Internal Module Multiplexing • Updated Table 50 SDR50/SDR104 Interface Timing Specification • Updated Table 90 14x14 mm Functional Contact Assignments and footnote • Updated Section 4.1.1, "Absolute maximum ratings" • Updated Section 4.6.3, "DDR I/O DC parameters" • Added Section 4.12.8, "LCD Controller (LCDIF) parameters" • Updated Section 4.12.9, "QUAD SPI (QSPI) timing parameters"
2	02/2017	• Updated Table 8, "Absolute Maximum Ratings" • Updated and added a footnote Table 10, "Operating Ranges" • Updated Section 4.2.1, "Power-Up sequence" and Section 4.2.2, "Power-Down sequence" • Removed Section 4.9.4 DDR SDRAM Specific Parameters (DDR3 and LPDDR2) • Updated Figure 18, "Asynchronous A/D Muxed Write Access" • Added a new Section 4.10, "Multi-Mode DDR Controller (MMDC)" • Added a new Section 4.12.8.1, "LCDIF signal mapping" • Updated Table 50, "SDR50/SDR104 Interface Timing Specification" • Updated Figure 40, "HS200 Mode Timing" • Updated Table 51, "HS200 Interface Timing Specification"
2.1	03/2017	• Updated the silicon revision definition in the Figure 1, "Part Number Nomenclature—i.MX 6UltraLite" • Added Rev.1.2 part numbers in the Table 1, "Ordering Information"
2.2	05/2017	• Changed terminology from "floating" to "not connected" • Added a footnote regarding maximum voltage allowance in the Table 8, "Absolute Maximum Ratings" • Replaced the MMDC compatible information with a cross reference in the Section 4.6.3, "DDR I/O DC parameters" and Section 4.7.2, "DDR I/O AC parameters" • Changed SD3 min to 1.7 ns in the Table 50, "SDR50/SDR104 Interface Timing Specification"