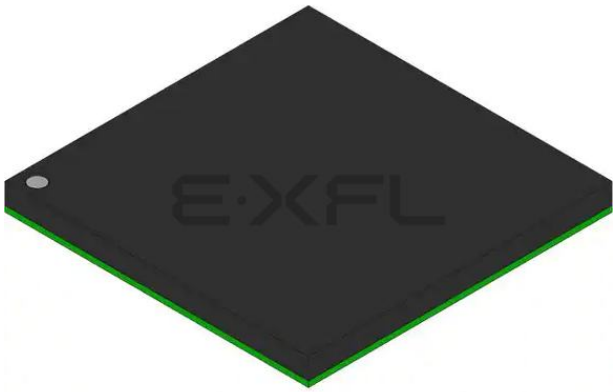

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-A7
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	528MHz
Co-Processors/DSP	Multimedia; NEON™ SIMD
RAM Controllers	LPDDR2, DDR3, DDR3L
Graphics Acceleration	No
Display & Interface Controllers	LCD, LVDS
Ethernet	10/100Mbps (2)
SATA	-
USB	USB 2.0 + PHY (2)
Voltage - I/O	1.2V, 1.35V, 1.5V, 1.8V, 2.5V, 2.8V, 3.3V
Operating Temperature	-40°C ~ 125°C (TJ)
Security Features	ARM TZ, A-HAB, CAAM, CSU, SJC, SNVS
Package / Case	289-LFBGA
Supplier Device Package	289-MAPBGA (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcimx6g2avm05aa

- A-HAB—Advanced High Assurance Boot—HABv4 with the new embedded enhancements: SHA-256, 2048-bit RSA key, version control mechanism, warm boot, CSU, and TZ initialization.

NOTE

The actual feature set depends on the part numbers as described in Table 1 and Table 2. Functions such as display and camera interfaces, connectivity interfaces, and security features are not offered on all derivatives.

2 Architectural overview

The following subsections provide an architectural overview of the i.MX 6UltraLite processor system.

2.1 Block diagram

Figure 2 shows the functional modules in the i.MX 6UltraLite processor system.

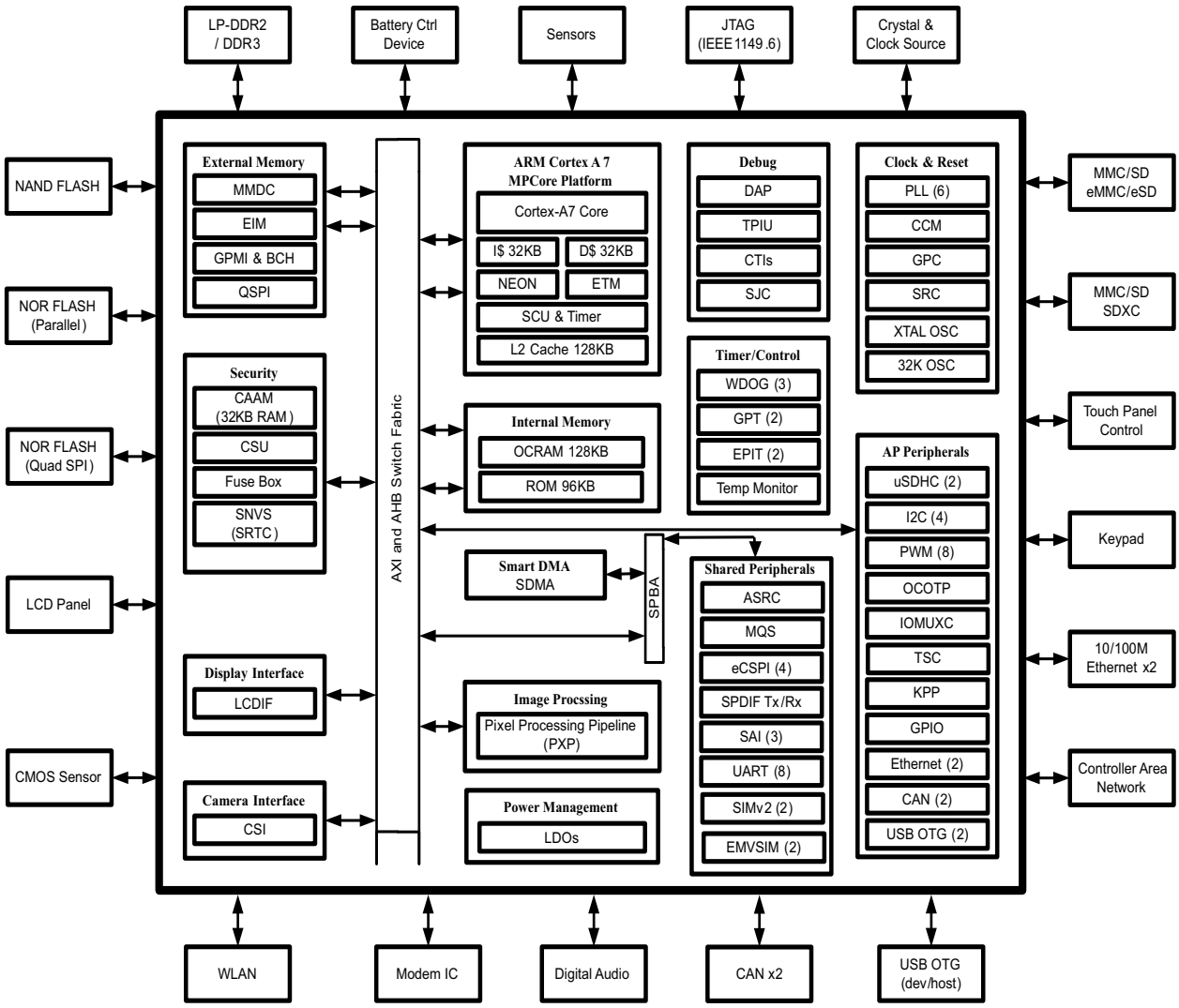

Figure 2. i.MX 6UltraLite System Block Diagram[1]

1. Some modules shown in this block diagram are not offered on all derivatives. See Table 2 for exceptions.

Table 4. Special Signal Considerations (continued)

Signal Name	Remarks
DRAM_VREF	When using DDR_VREF with DDR I/O, the nominal reference voltage must be half of the NVCC_DRAM supply. The user can tie DDR_VREF to a precision external resistor divider. Use a 1 kΩ 0.5% resistor to GND and a 1 kΩ 0.5% resistor to NVCC_DRAM. Shunt each resistor with a closely-mounted 0.1 µF capacitor. To reduce supply current, a pair of 1.5 kΩ 0.1% resistors can be used. Using resistors with recommended tolerances ensures the ± 2% DDR_VREF tolerance (per the DDR3 specification) is maintained when two DDR3 ICs plus the i.MX 6UltraLite are drawing current on the resistor divider.
ZQPAD	DRAM calibration resistor 240 Ω 1% used as reference during DRAM output buffer driver calibration should be connected between this pad and GND.
GPANAIO	This signal is reserved for NXP manufacturing use only. This output must remain unconnected.
JTAG_*nnnn*	The JTAG interface is summarized in Table 5. Use of external resistors is unnecessary. However, if external resistors are used, the user must ensure that the on-chip pull-up/down configuration is followed. For example, do not use an external pull down on an input that has on-chip pull-up.
	JTAG_TDO is configured with a keeper circuit such that the non-connected condition is eliminated if an external pull resistor is not present. An external pull resistor on JTAG_TDO is detrimental and should be avoided.
	JTAG_MOD is referenced as SJC_MOD in the i.MX 6UltraLite reference manual. Both names refer to the same signal. JTAG_MOD must be externally connected to GND for normal operation. Termination to GND through an external pull-down resistor (such as 1 kΩ) is allowed. JTAG_MOD set to hi configures the JTAG interface to mode compliant with IEEE1149.1 standard. JTAG_MOD set to low configures the JTAG interface for common SW debug adding all the system TAPs to the chain.
NC	These signals are No Connect (NC) and should be floated by the user.
POR_B	This cold reset negative logic input resets all modules and logic in the IC. May be used in addition to internally generated power on reset signal (logical AND, both internal and external signals are considered active low).
ONOFF	ONOFF can be configured in debounce, off to on time, and max time-out configurations. The debounce and off to on time configurations supports 0, 50, 100 and 500 ms. Debounce is used to generate the power off interrupt. While in the ON state, if ONOFF button is pressed longer than the debounce time, the power off interrupt is generated. Off to on time supports the time it takes to request power on after a configured button press time has been reached. While in the OFF state, if ONOFF button is pressed longer than the off to on time, the state will transition from OFF to ON. Max time-out configuration supports 5, 10, 15 seconds and disable. Max time-out configuration supports the time it takes to request power down after ONOFF button has been pressed for the defined time.
TEST_MODE	TEST_MODE is for NXP factory use. The user must tie this pin directly to GND.

Table 5. JTAG Controller Interface Summary

JTAG	I/O Type	On-chip Termination
JTAG_TCK	Input	47 kΩ pull-up
JTAG_TMS	Input	47 kΩ pull-up
JTAG_TDI	Input	47 kΩ pull-up

4.3.2.2 LDO_2P5

The LDO_2P5 module implements a programmable linear-regulator function from VDD_HIGH_IN (see Table 10 for minimum and maximum input requirements). Typical Programming Operating Range is 2.25 V to 2.75 V with the nominal default setting as 2.5 V. LDO_2P5 supplies the DDR IOs, USB Phy, E-fuse module, and PLLs. A programmable brown-out detector is included in the regulator that can be used by the system to determine when the load capability of the regulator is being exceeded, to take the necessary steps. Current-limiting can be enabled to allow for in-rush current requirements during start-up, if needed. Active-pull-down can also be enabled for systems requiring this feature. An alternate self-biased low-precision weak-regulator is included that can be enabled for applications needing to keep the output voltage alive during low-power modes where the main regulator driver and its associated global bandgap reference module are disabled. The output of the weak-regulator is not programmable and is a function of the input supply as well as the load current. Typically, with a 3 V input supply the weak-regulator output is 2.525 V and its output impedance is approximately 40 Ω

For information on external capacitor requirements for this regulator, see the *Hardware Development Guide for i.MX 6UltraLite Applications Processors* (IMX6ULHDG).

For additional information, see the *i.MX 6UltraLite Reference Manual* (IMX6ULRM).

4.3.2.3 LDO_USB

The LDO_USB module implements a programmable linear-regulator function from the USB VUSB voltages (4.4 V–5.5 V) to produce a nominal 3.0 V output voltage. A programmable brown-out detector is included in the regulator that can be used by the system to determine when the load capability of the regulator is being exceeded, to take the necessary steps. This regulator has a built in power-mux that allows the user to select to run the regulator from either USB VBUS supply, when both are present. If only one of the USB VBUS voltages is present, then, the regulator automatically selects this supply. Current limit is also included to help the system meet in-rush current targets.

For information on external capacitor requirements for this regulator, see the Hardware Development Guide for *i.MX 6UltraLite Applications Processors* (IMX6ULHDG).

For additional information, see the *i.MX 6UltraLite Reference Manual* (IMX6ULRM).

4.4 PLL’s electrical characteristics

4.4.1 Audio/Video PLL’s electrical parameters

Table 16. Audio/Video PLL’s Electrical Parameters

Parameter	Value
Clock output range	650 MHz ~1.3 GHz
Reference clock	24 MHz
Lock time	<11250 reference cycles

- Double Data Rate I/O (DDR) for LPDDR2, and DDR3/DDR3L modes

NOTE

GPIO and DDR I/O output driver impedance is measured with “long” transmission line of impedance Ztl attached to I/O pad and incident wave launched into transmission line. Rpu/Rpd and Ztl form a voltage divider that defines specific voltage of incident wave relative to OVDD. Output driver impedance is calculated from this voltage divider (see Figure 6).

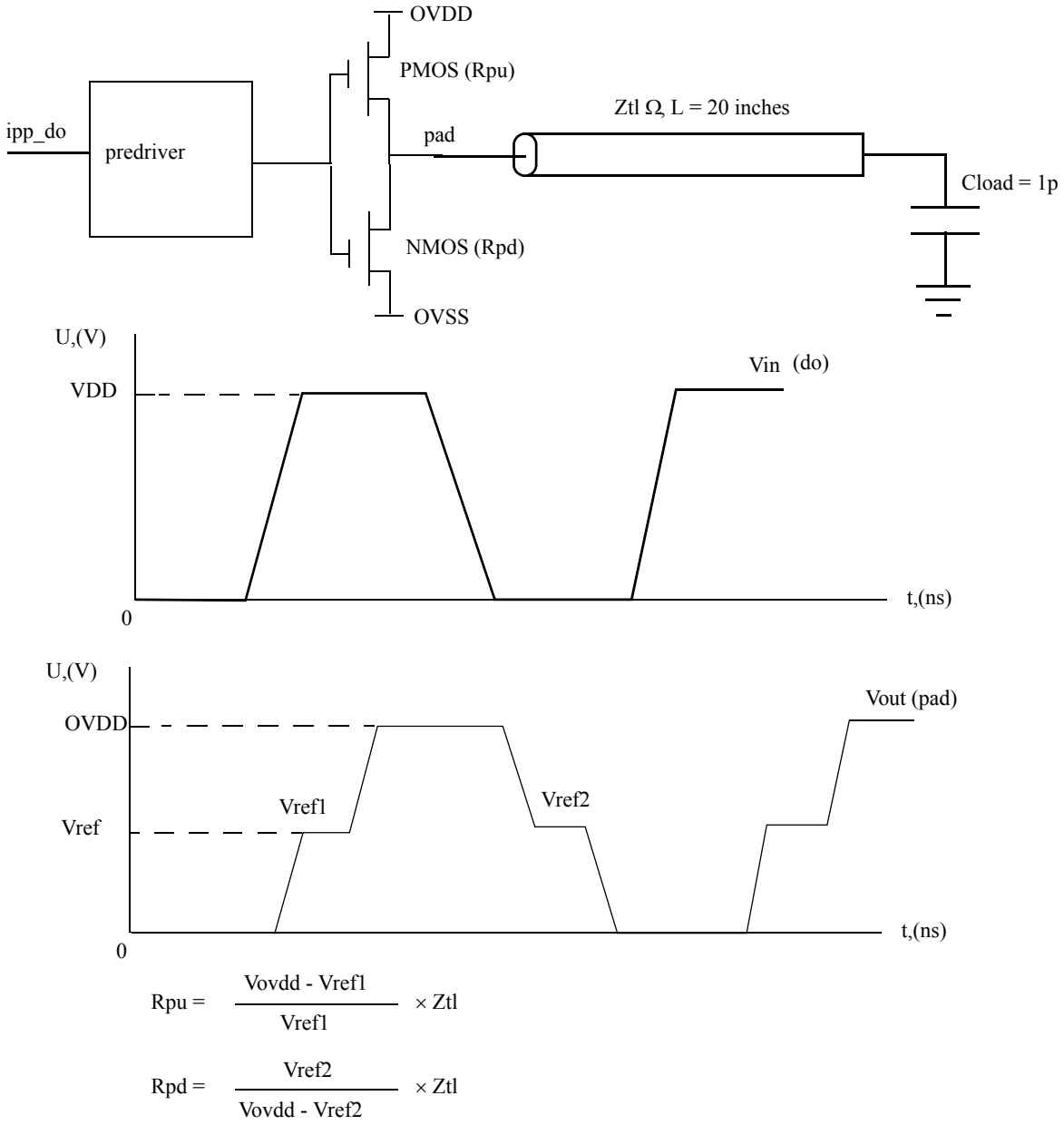

Figure 6. Impedance Matching Load for Measurement

4.9 System modules timing

This section contains the timing and electrical parameters for the modules in each i.MX 6UltraLite processor.

4.9.1 Reset timings parameters

Figure 7 shows the reset timing and Table 35 lists the timing parameters.

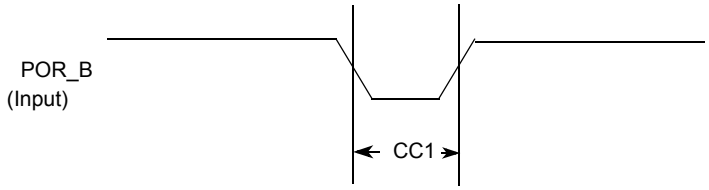

Figure 7. Reset Timing Diagram

Table 35. Reset Timing Parameters

ID	Parameter	Min	Max	Unit
CC1	Duration of POR_B to be qualified as valid.	1	—	RTC_XTALI cycle

4.9.2 WDOG reset timing parameters

Figure 8 shows the WDOG reset timing and Table 36 lists the timing parameters.

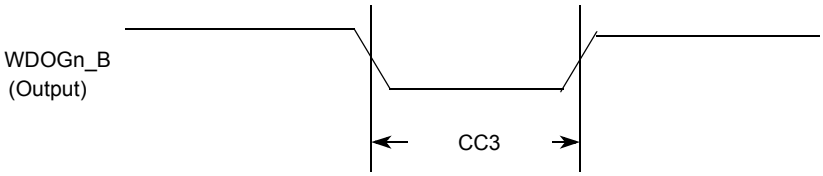

Figure 8. WDOGn_B Timing Diagram

Table 36. WDOGn_B Timing Parameters

ID	Parameter	Min	Max	Unit
CC3	Duration of WDOGn_B Assertion	1	—	RTC_XTALI cycle

NOTE

RTC_XTALI is approximately 32 kHz. RTC_XTALI cycle is one period or approximately 30 µs.

NOTE

WDOG1_B output signals (for each one of the Watchdog modules) do not have dedicated pins, but are muxed out through the IOMUX. See the IOMUX manual for detailed information.

General EIM Timing-Synchronous Mode

Figure 9, Figure 10, and Table 38 specify the timings related to the EIM module. All EIM output control signals may be asserted and deasserted by an internal clock synchronized to the EIM_BCLK rising edge according to corresponding assertion/negation control fields.

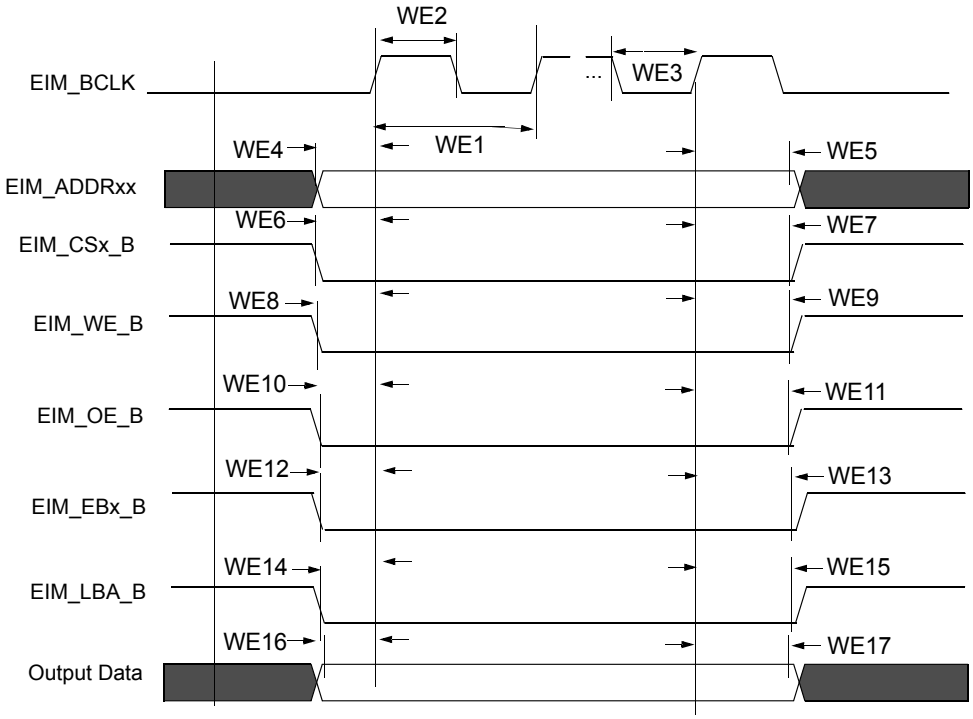

Figure 9. EIM Outputs Timing Diagram

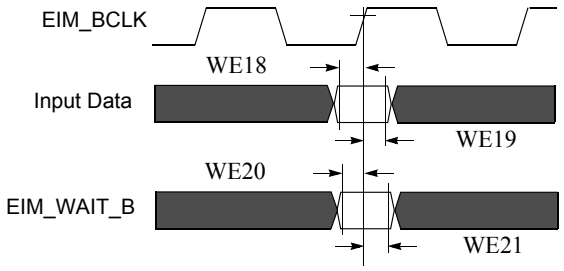

Figure 10. EIM Inputs Timing Diagram

4.9.3.2 Examples of EIM synchronous accesses

Table 38. EIM Bus Timing Parameters

ID	Parameter	Min[1]	Max[1]	Unit
WE1	EIM_BCLK Cycle time[2]	t x (k + 1)	—	ns
WE2	EIM_BCLK Low Level Width	0.4 x t x (k + 1)	—	ns
WE3	EIM_BCLK High Level Width	0.4 x t x (k + 1)	—	ns
WE4	Clock rise to address valid	-0.5 x t x (k + 1) - 1.25	-0.5 x t x (k + 1) + 2.25	ns

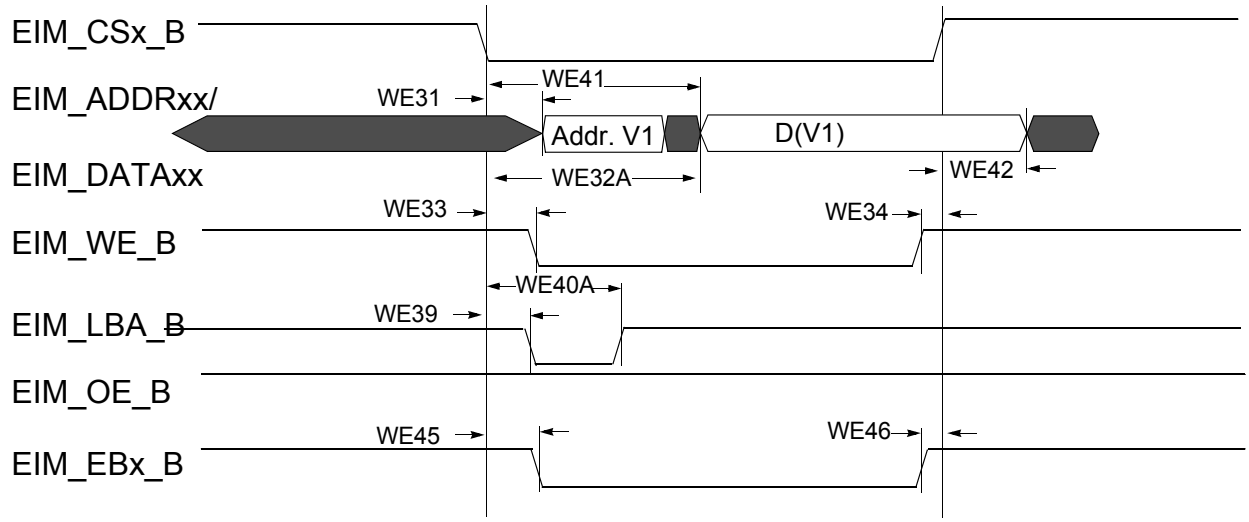

Figure 18. Asynchronous A/D Muxed Write Access

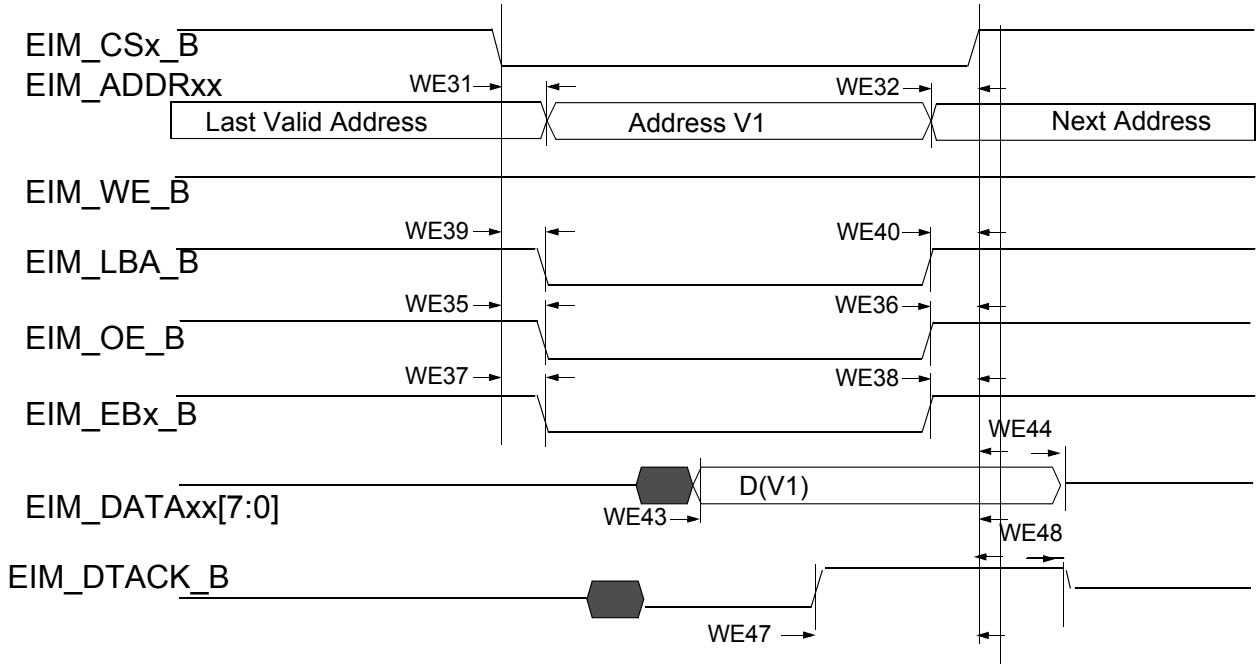

Figure 19. DTACK Mode Read Access (DAP=0)

Table 39. EIM Asynchronous Timing Parameters Table Relative Chip to Select[1,2]

Ref No.	Parameter	Determination by Synchronous measured parameters	Min	Max	Unit
WE37	EIM_CSx_B Valid to EIM_EBx_B Valid (Read access)	WE12 - WE6 + (RBEA - RCSA) x t	-3.5 + (RBEA - RCSA) x t	3.5 + (RBEA - RCSA) x t	ns
WE38	EIM_EBx_B Invalid to EIM_CSx_B Invalid (Read access)	WE7 - WE13 + (RBEN - RCSN) x t	-3.5 + (RBEN - RCSN) x t	3.5 + (RBEN- RCSN) x t	ns
WE39	EIM_CSx_B Valid to EIM_LBA_B Valid	WE14 - WE6 + (ADVA - CSA) x t	-3.5 + (ADVA - CSA) x t	3.5 + (ADVA - CSA) x t	ns
WE40	EIM_LBA_B Invalid to EIM_CSx_B Invalid (ADVL is asserted)	WE7 - WE15 - CSN x t	-3.5 - CSN x t	3.5 - CSN x t	ns
WE40A (muxed A/D)	EIM_CSx_B Valid to EIM_LBA_B Invalid	WE14 - WE6 + (ADVN + ADVA + 1 - CSA) x t	-3.5 + (ADVN + ADVA + 1 - CSA) x t	3.5 + (ADVN + ADVA + 1 - CSA) x t	ns
WE41	EIM_CSx_B Valid to Output Data Valid	WE16 - WE6 - WCSA x t	-3.5 - WCSA x t	3.5 - WCSA x t	ns
WE41A (muxed A/D)	EIM_CSx_B Valid to Output Data Valid	WE16 - WE6 + (WADVN + WADVA + ADH + 1 - WCSA) x t	-3.5 + (WADVN + WADVA + ADH + 1 - WCSA) x t	3.5 + (WADVN + WADVA + ADH + 1 - WCSA) x t	ns
WE42	Output Data Invalid to EIM_CSx_B Invalid	WE17 - WE7 - CSN x t	-3.5 - CSN x t	3.5 - CSN x t	ns
MAXCO	Output maximum delay from internal driving EIM_ADDRxx/control flip-flops to chip outputs	10	—	10	ns
MAXCSO	Output maximum delay from internal chip selects driving flip-flops to EIM_CSx_B out	10	—	10	ns
MAXDI	EIM_DATAxx maximum delay from chip input data to its internal flip-flop	5	—	5	ns
WE43	Input Data Valid to EIM_CSx_B Invalid	MAXCO - MAXCSO + MAXDI	MAXCO - MAXCSO + MAXDI	—	ns
WE44	EIM_CSx_B Invalid to Input Data Invalid	0	0	—	ns

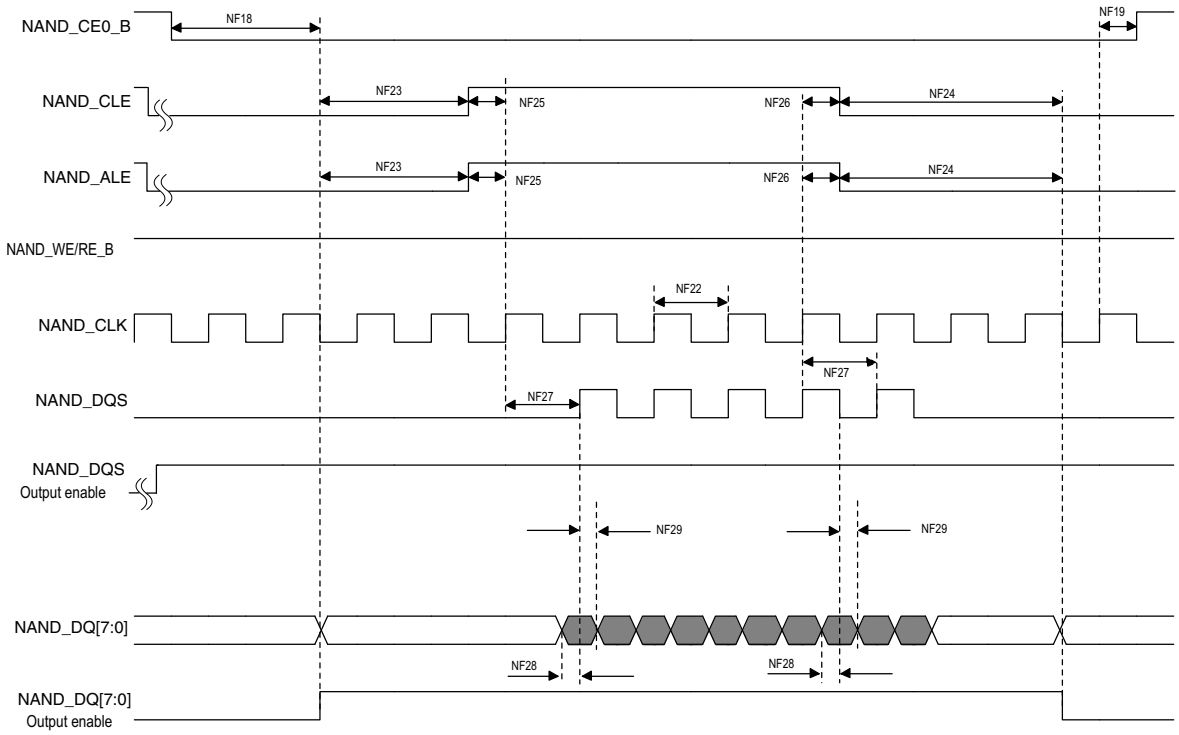

Figure 27. Source Synchronous Mode Data Write Timing Diagram

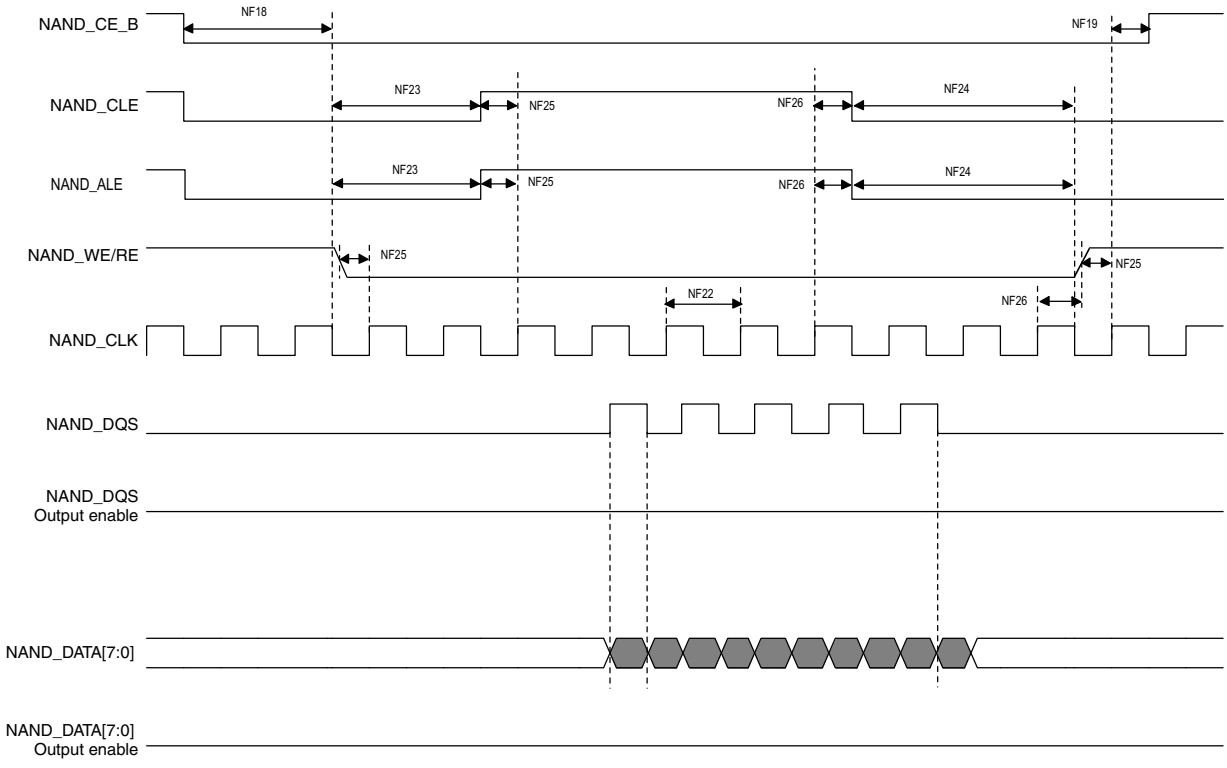

Figure 28. Source Synchronous Mode Data Read Timing Diagram

[2] SPI_RDY is sampled internally by ipg_clk and is asynchronous to all other CSPI signals.

4.12.2.2 ECSPI slave mode timing

Figure 36 depicts the timing of ECSPI in slave mode. Table 47 lists the ECSPI slave mode timing characteristics.

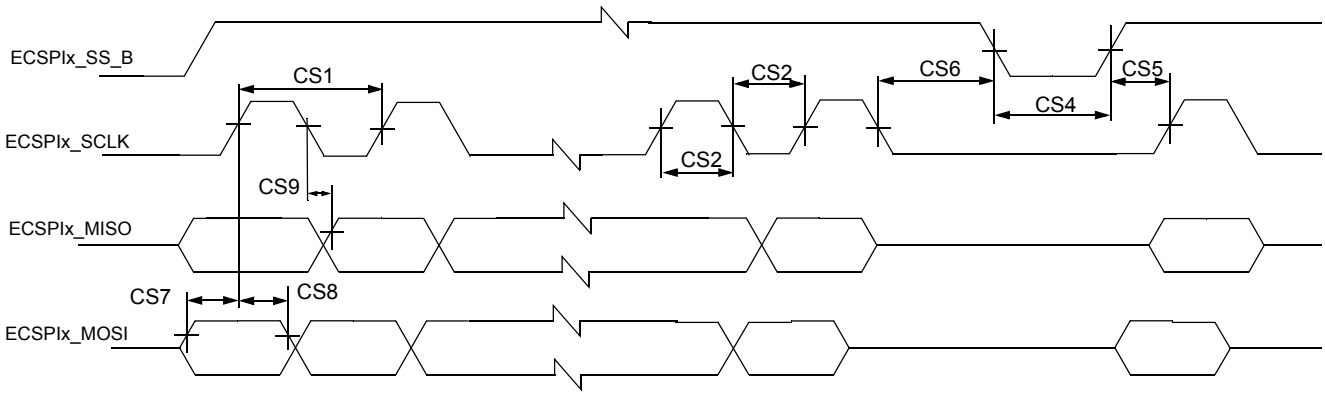

Figure 36. ECSPI Slave Mode Timing Diagram

Table 47. ECSPI Slave Mode Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
CS1	ECSPIx_SCLK Cycle Time–Read ECSPI_SCLK Cycle Time–Write	t_{clk}	15 43	—	ns
CS2	ECSPIx_SCLK High or Low Time–Read ECSPIx_SCLK High or Low Time–Write	t_{SW}	7 21.5	—	ns
CS4	ECSPIx_SS_B pulse width	t_{CSLH}	Half ECSPIx_SCLK period	—	ns
CS5	ECSPIx_SS_B Lead Time (CS setup time)	t_{SCS}	5	—	ns
CS6	ECSPIx_SS_B Lag Time (CS hold time)	t_{HCS}	5	—	ns
CS7	ECSPIx_MOSI Setup Time	t_{Smosi}	4	—	ns
CS8	ECSPIx_MOSI Hold Time	t_{Hmosi}	4	—	ns
CS9	ECSPIx_MISO Propagation Delay (C_{LOAD} = 20 pF)	t_{PDmiso}	4	19	ns

Table 48. SD/eMMC4.3 Interface Timing Specification (continued)

ID	Parameter	Symbols	Min	Max	Unit
uSDHC Input/Card Outputs SD_CMD, SDx_DATAx (Reference to CLK)					
SD7	uSDHC Input Setup Time	t_{ISU}	2.5	—	ns
SD8	uSDHC Input Hold Time[4]	t_{IH}	1.5	—	ns

1 In low speed mode, card clock must be lower than 400 kHz, voltage ranges from 2.7 to 3.6 V.

2 In normal (full) speed mode for SD/SDIO card, clock frequency can be any value between 0–25 MHz. In high-speed mode, clock frequency can be any value between 0–50 MHz.

3 In normal (full) speed mode for MMC card, clock frequency can be any value between 0–20 MHz. In high-speed mode, clock frequency can be any value between 0–52 MHz.

4 To satisfy hold timing, the delay difference between clock input and cmd/data input must not exceed 2 ns.

4.12.3.2 eMMC4.4/4.41 (dual data rate) AC timing

Figure 38 depicts the timing of eMMC4.4/4.41. Table 49 lists the eMMC4.4/4.41 timing characteristics. Be aware that only DATA is sampled on both edges of the clock (not applicable to CMD).

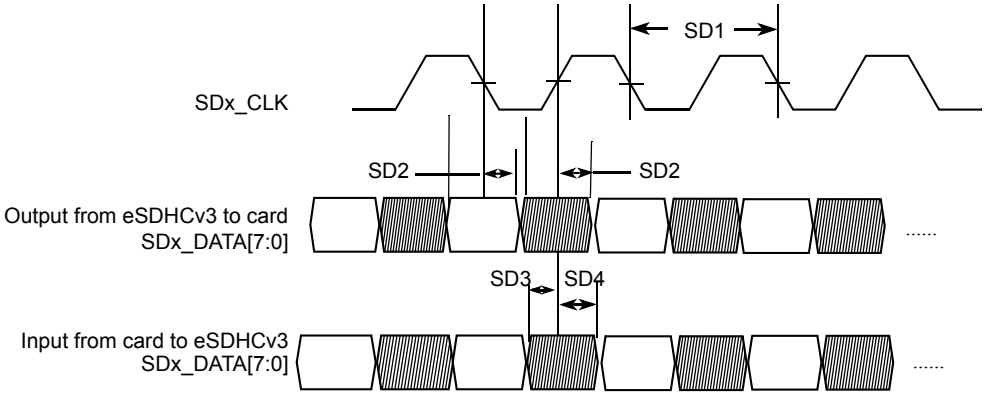

Figure 38. eMMC4.4/4.41 Timing

Table 49. eMMC4.4/4.41 Interface Timing Specification

ID	Parameter	Symbols	Min	Max	Unit
Card Input Clock					
SD1	Clock Frequency (eMMC4.4/4.41 DDR)	f_{PP}	0	52	MHz
SD1	Clock Frequency (SD3.0 DDR)	f_{PP}	0	50	MHz
uSDHC Output / Card Inputs SD_CMD, SDx_DATAx (Reference to CLK)					
SD2	uSDHC Output Delay	t_{OD}	2.5	7.1	ns
uSDHC Input / Card Outputs SD_CMD, SDx_DATAx (Reference to CLK)					
SD3	uSDHC Input Setup Time	t_{ISU}	1.7	—	ns
SD4	uSDHC Input Hold Time	t_{IH}	1.5	—	ns

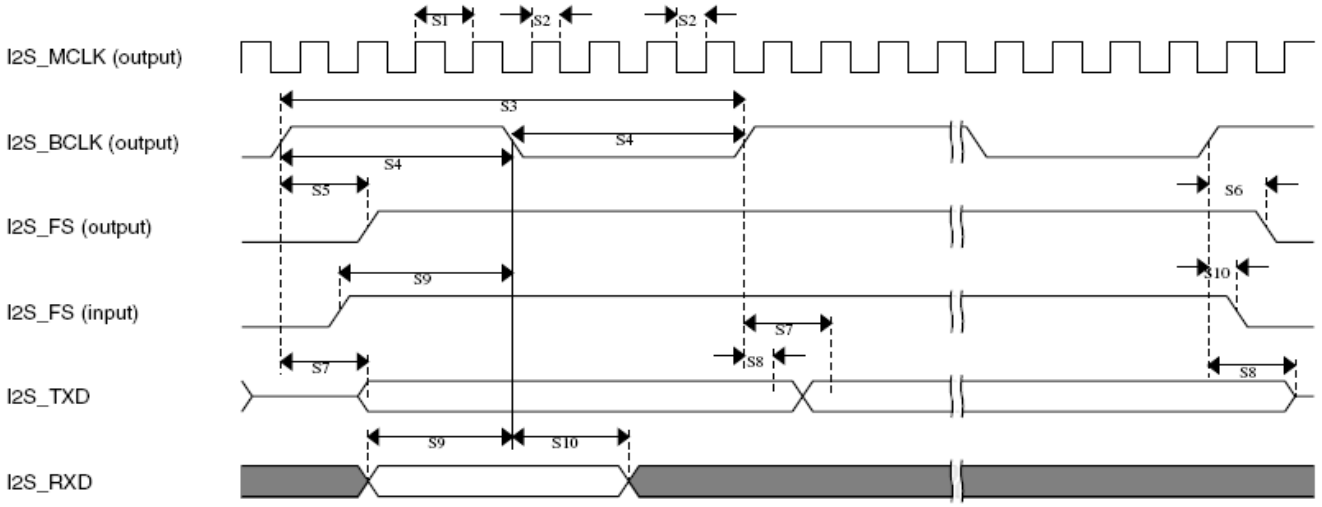

Figure 55. SAI Timing — Master Modes

Table 68. Master Mode SAI Timing

Num	Characteristic	Min	Max	Unit
S11	SAI_BCLK cycle time (input)	4 x t_{sys}	—	ns
S12	SAI_BCLK pulse width high/low (input)	40%	60%	BCLK period
S13	SAI_FS input setup before SAI_BCLK	10	—	ns
S14	SAI_FA input hold after SAI_BCLK	2	—	ns
S15	SAI_BCLK to SAI_TXD/SAI_FS output valid	—	20	ns
S16	SAI_BCLK to SAI_TXD/SAI_FS output invalid	0	—	ns
S17	SAI_RXD setup before SAI_BCLK	10	—	ns
S18	SAI_RXD hold after SAI_BCLK	2	—	ns

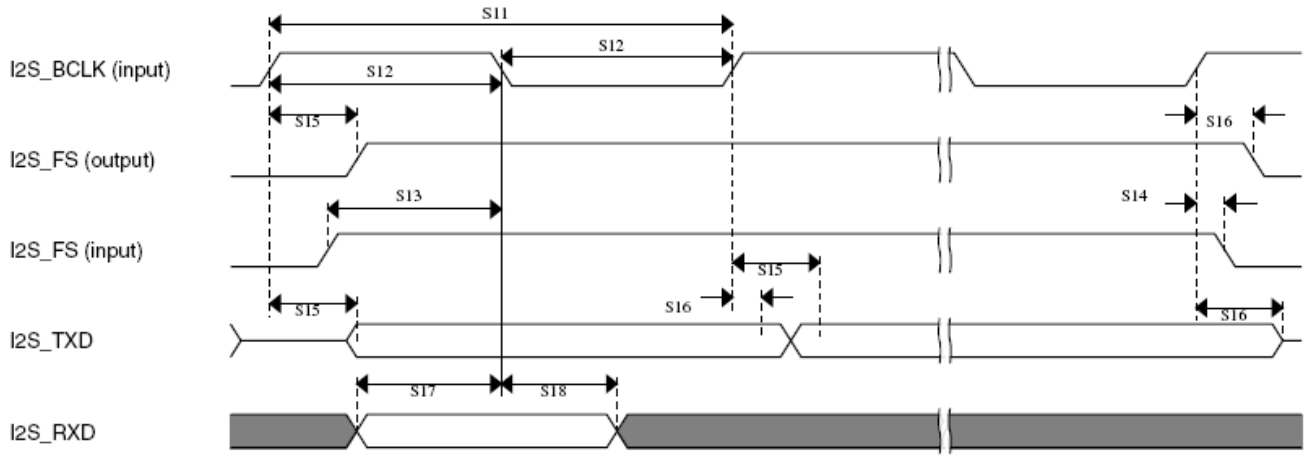

Figure 56. SAI Timing — Slave Modes

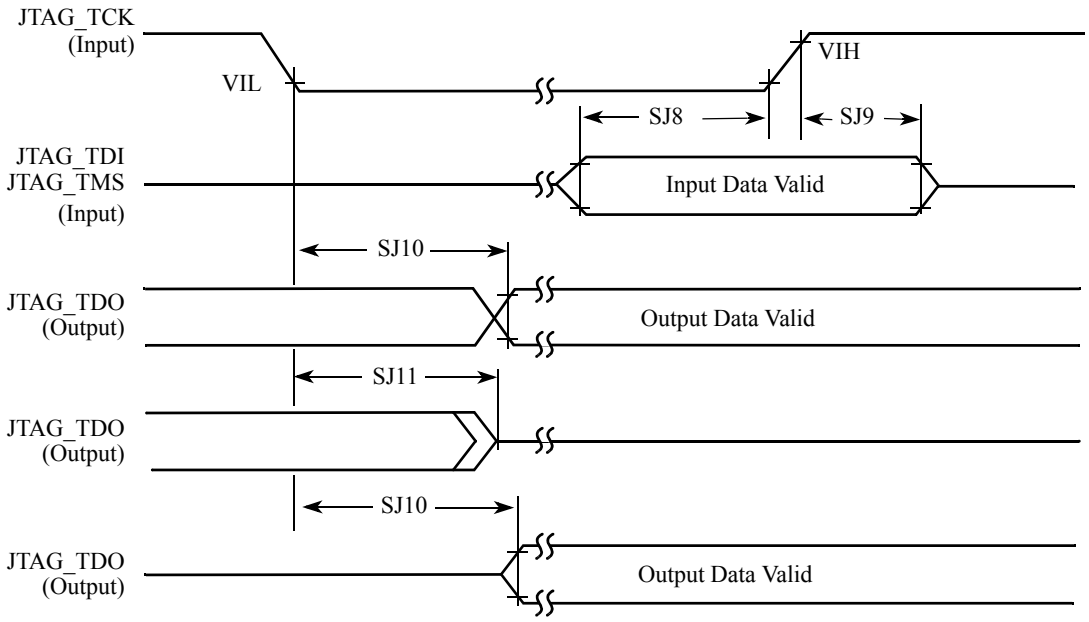

Figure 59. Test Access Port Timing Diagram

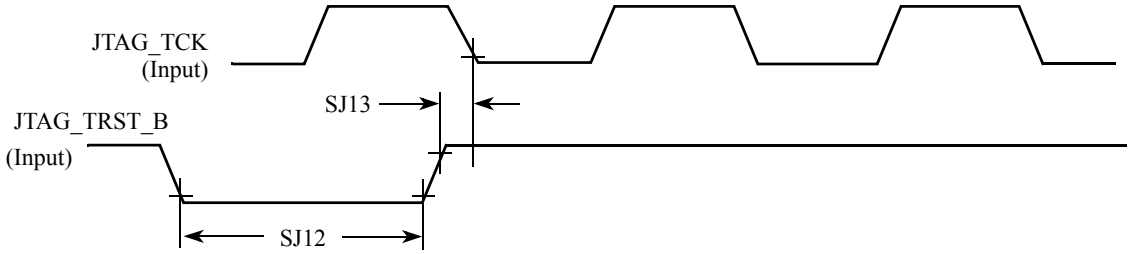

Figure 60. JTAG_TRST_B Timing Diagram

Table 69. JTAG Timing

ID	Parameter[1,2]	All Frequencies		Unit
		Min	Max	
SJ0	JTAG_TCK frequency of operation $1/(3 \bullet T_{DC})$[1]	0.001	22	MHz
SJ1	JTAG_TCK cycle time in crystal mode	45	—	ns
SJ2	JTAG_TCK clock pulse width measured at V_M[2]	22.5	—	ns
SJ3	JTAG_TCK rise and fall times	—	3	ns
SJ4	Boundary scan input data set-up time	5	—	ns
SJ5	Boundary scan input data hold time	24	—	ns
SJ6	JTAG_TCK low to output data valid	—	40	ns
SJ7	JTAG_TCK low to output high impedance	—	40	ns
SJ8	JTAG_TMS, JTAG_TDI data set-up time	5	—	ns

4.12.13.1.2 UART receiver

Figure 64 depicts the RS-232 serial mode receives timing with 8 data bit/1 stop bit format. Table 72 lists serial mode receive timing characteristics.

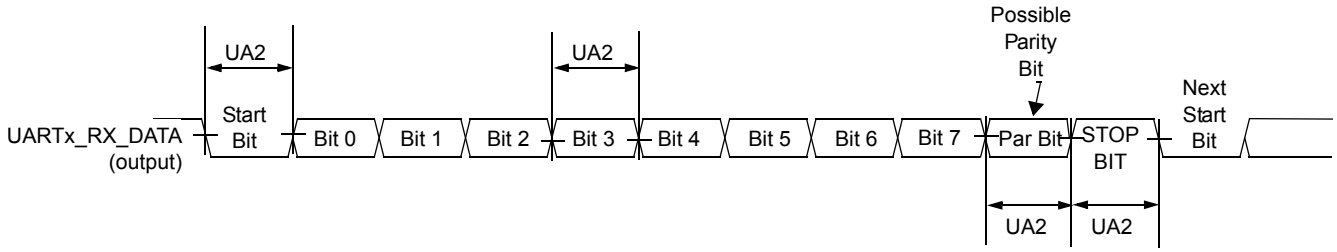

Figure 64. UART RS-232 Serial Mode Receive Timing Diagram

Table 72. RS-232 Serial Mode Receive Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
UA2	Receive Bit Time[1]	t_{Rbit}	$1/F_{baud\_rate}$[2] - $1/(16 \times F_{baud\_rate})$	$1/F_{baud\_rate} + 1/(16 \times F_{baud\_rate})$	—

[1] The UART receiver can tolerate $1/(16 \times F_{baud\_rate})$ tolerance in each bit. But accumulation tolerance in one frame must not exceed $3/(16 \times F_{baud\_rate})$.

[2] F_{baud_rate}: Baud rate frequency. The maximum baud rate the UART can support is (*ipg_perclk* frequency)/16.

4.12.13.1.3 UART IrDA mode timing

The following subsections give the UART transmit and receive timings in IrDA mode.

UART IrDA mode transmitter

Figure 65 depicts the UART IrDA mode transmit timing, with 8 data bit/1 stop bit format. Table 73 lists the transmit timing characteristics.

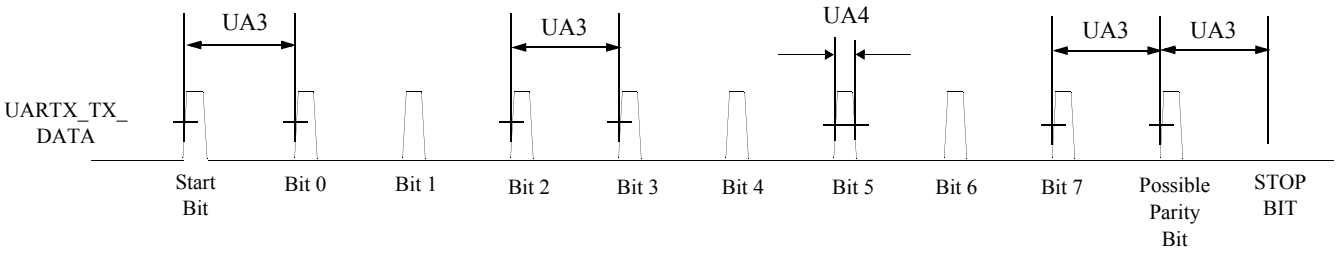

Figure 65. UART IrDA Mode Transmit Timing Diagram

Table 73. IrDA Mode Transmit Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
UA3	Transmit Bit Time in IrDA mode	t_{TIRbit}	$1/F_{baud\_rate}$[1] - T_{ref_clk}[2]	$1/F_{baud\_rate} + T_{ref\_clk}$	—
UA4	Transmit IR Pulse Duration	$t_{TIRpulse}$	$(3/16) \times (1/F_{baud\_rate}) - T_{ref\_clk}$	$(3/16) \times (1/F_{baud\_rate}) + T_{ref\_clk}$	—

[1] F_{baud_rate}: Baud rate frequency. The maximum baud rate the UART can support is (*ipg_perclk* frequency)/16.

5 Boot mode configuration

This section provides information on boot mode configuration pins allocation and boot devices interfaces allocation.

5.1 Boot mode configuration pins

Table 77 provides boot options, functionality, fuse values, and associated pins. Several input pins are also sampled at reset and can be used to override fuse values, depending on the value of BT_FUSE_SEL fuse. The boot option pins are in effect when BT_FUSE_SEL fuse is '0' (cleared, which is the case for an unblown fuse). For detailed boot mode options configured by the boot mode pins, see the i.MX 6UltraLite Fuse Map document and the System Boot chapter in *i.MX 6UltraLite Reference Manual (IMX6ULRM)*.

Table 77. Fuses and Associated Pins Used for Boot

Pin	Direction at reset	eFuse name	Details
BOOT_MODE0	Input with 100 K pull-down	N/A	Boot mode selection
BOOT_MODE1	Input with 100 K pull-down	N/A	Boot mode selection

6 Package information and contact assignments

This section includes the contact assignment information and mechanical package drawing.

6.1 14x14 mm package information

6.1.1 14x14 mm, 0.8 mm pitch, ball matrix

Figure 68 shows the top, bottom, and side views of the 14x14 mm BGA package.

Table 90. 14x14 mm Functional Contact Assignments (continued)

JTAG_MOD	P15	NVCC_GPIO	GPIO	ALT5	JTAG_MOD	Input	100 kΩ pull-up
JTAG_TCK	M14	NVCC_GPIO	GPIO	ALT5	JTAG_TCK	Input	47 kΩ pull-up
JTAG_TDI	N16	NVCC_GPIO	GPIO	ALT5	JTAG_TDI	Input	47 kΩ pull-up
JTAG_TDO	N15	NVCC_GPIO	GPIO	ALT5	JTAG_TDO	Output	Keeper
JTAG_TMS	P14	NVCC_GPIO	GPIO	ALT5	JTAG_TMS	Input	47 kΩ pull-up
JTAG_TRST_B	N14	NVCC_GPIO	GPIO	ALT5	JTAG_TRST_B	Input	47 kΩ pull-up
LCD_CLK	A8	NVCC_LCD	GPIO	ALT5	LCD_CLK	Input	Keeper
LCD_DATA00	B9	NVCC_LCD	GPIO	ALT5	LCD_DATA00	Input	Keeper
LCD_DATA01	A9	NVCC_LCD	GPIO	ALT5	LCD_DATA01	Input	Keeper
LCD_DATA02	E10	NVCC_LCD	GPIO	ALT5	LCD_DATA02	Input	Keeper
LCD_DATA03	D10	NVCC_LCD	GPIO	ALT5	LCD_DATA03	Input	Keeper
LCD_DATA04	C10	NVCC_LCD	GPIO	ALT5	LCD_DATA04	Input	Keeper
LCD_DATA05	B10	NVCC_LCD	GPIO	ALT5	LCD_DATA05	Input	Keeper
LCD_DATA06	A10	NVCC_LCD	GPIO	ALT5	LCD_DATA06	Input	Keeper
LCD_DATA07	D11	NVCC_LCD	GPIO	ALT5	LCD_DATA07	Input	Keeper
LCD_DATA08	B11	NVCC_LCD	GPIO	ALT5	LCD_DATA08	Input	Keeper
LCD_DATA09	A11	NVCC_LCD	GPIO	ALT5	LCD_DATA09	Input	Keeper
LCD_DATA10	E12	NVCC_LCD	GPIO	ALT5	LCD_DATA10	Input	Keeper
LCD_DATA11	D12	NVCC_LCD	GPIO	ALT5	LCD_DATA11	Input	Keeper
LCD_DATA12	C12	NVCC_LCD	GPIO	ALT5	LCD_DATA12	Input	Keeper
LCD_DATA13	B12	NVCC_LCD	GPIO	ALT5	LCD_DATA13	Input	Keeper
LCD_DATA14	A12	NVCC_LCD	GPIO	ALT5	LCD_DATA14	Input	Keeper
LCD_DATA15	D13	NVCC_LCD	GPIO	ALT5	LCD_DATA15	Input	Keeper
LCD_DATA16	C13	NVCC_LCD	GPIO	ALT5	LCD_DATA16	Input	Keeper
LCD_DATA17	B13	NVCC_LCD	GPIO	ALT5	LCD_DATA17	Input	Keeper
LCD_DATA18	A13	NVCC_LCD	GPIO	ALT5	LCD_DATA18	Input	Keeper
LCD_DATA19	D14	NVCC_LCD	GPIO	ALT5	LCD_DATA19	Input	Keeper
LCD_DATA20	C14	NVCC_LCD	GPIO	ALT5	LCD_DATA20	Input	Keeper
LCD_DATA21	B14	NVCC_LCD	GPIO	ALT5	LCD_DATA21	Input	Keeper
LCD_DATA22	A14	NVCC_LCD	GPIO	ALT5	LCD_DATA22	Input	Keeper
LCD_DATA23	B16	NVCC_LCD	GPIO	ALT5	LCD_DATA23	Input	Keeper

Table 90. 14x14 mm Functional Contact Assignments (continued)

LCD_ENABLE	B8	NVCC_LCD	GPIO	ALT5	LCD_ENABLE	Input	Keeper
LCD_HSYNC	D9	NVCC_LCD	GPIO	ALT5	LCD_HSYNC	Input	Keeper
LCD_RESET	E9	NVCC_LCD	GPIO	ALT5	LCD_RESET	Input	Keeper
LCD_VSYNC	C9	NVCC_LCD	GPIO	ALT5	LCD_VSYNC	Input	Keeper
NAND_ALE	B4	NVCC_NAND	GPIO	ALT5	VDDSOC	Input	Keeper
NAND_CE0_B	C5	NVCC_NAND	GPIO	ALT5	NAND_CE0_B	Input	Keeper
NAND_CE1_B	B5	NVCC_NAND	GPIO	ALT5	NAND_CE1_B	Input	Keeper
NAND_CLE	A4	NVCC_NAND	GPIO	ALT5	NAND_CLE	Input	Keeper
NAND_DATA00	D7	NVCC_NAND	GPIO	ALT5	NAND_DATA00	Input	Keeper
NAND_DATA01	B7	NVCC_NAND	GPIO	ALT5	NAND_DATA01	Input	Keeper
NAND_DATA02	A7	NVCC_NAND	GPIO	ALT5	NAND_DATA02	Input	Keeper
NAND_DATA03	D6	NVCC_NAND	GPIO	ALT5	NAND_DATA03	Input	Keeper
NAND_DATA04	C6	NVCC_NAND	GPIO	ALT5	NAND_DATA04	Input	Keeper
NAND_DATA05	B6	NVCC_NAND	GPIO	ALT5	NAND_DATA05	Input	Keeper
NAND_DATA06	A6	NVCC_NAND	GPIO	ALT5	NAND_DATA06	Input	Keeper
NAND_DATA07	A5	NVCC_NAND	GPIO	ALT5	NAND_DATA07	Input	Keeper
NAND_DQS	E6	NVCC_NAND	GPIO	ALT5	NAND_DQS	Input	Keeper
NAND_RE_B	D8	NVCC_NAND	GPIO	ALT5	NAND_RE_B	Input	Keeper
NAND_READY_B	A3	NVCC_NAND	GPIO	ALT5	NAND_READY_B	Input	Keeper
NAND_WE_B	C8	NVCC_NAND	GPIO	ALT5	NAND_WE_B	Input	Keeper
NAND_WP_B	D5	NVCC_NAND	GPIO	ALT5	NAND_WP_B	Input	Keeper
ONOFF	R8	VDD_SNVS_IN	GPIO	ALT0	ONOFF	Input	100 kΩ pull-up
POR_B	P8	VDD_SNVS_IN	GPIO	ALT0	POR_B	Input	100 kΩ pull-up
RTC_XTALI	T11	VDD_SNVS_CAP	ANALOG	—	RTC_XTALI	—	—
RTC_XTALO	U11	VDD_SNVS_CAP	ANALOG	—	RTC_XTALO	—	—
SD1_CLK	C1	NVCC_SD1	GPIO	ALT5	SD1_CLK	Input	Keeper
SD1_CMD	C2	NVCC_SD1	GPIO	ALT5	SD1_CMD	Input	Keeper
SD1_DATA0	B3	NVCC_SD1	GPIO	ALT5	SD1_DATA0	Input	Keeper
SD1_DATA1	B2	NVCC_SD1	GPIO	ALT5	SD1_DATA1	Input	Keeper
SD1_DATA2	B1	NVCC_SD1	GPIO	ALT5	SD1_DATA2	Input	Keeper
SD1_DATA3	A2	NVCC_SD1	GPIO	ALT5	SD1_DATA3	Input	Keeper
SNVS_PMIC_ON_REQ	T9	VDD_SNVS_IN	GPIO	ALT0	SNVS_PMIC_ON_REQ	Output	100 kΩ pull-up

Table 90. 14x14 mm Functional Contact Assignments (continued)

SNVS_TAMPER0	R10	VDD_SNVS_IN	GPIO	—	GPIO5_IO00/SNVS_TAMPER0	Input	Keeper[1]
SNVS_TAMPER1	R9	VDD_SNVS_IN	GPIO	—	GPIO5_IO01/SNVS_TAMPER1	Input	Keeper[1]
SNVS_TAMPER2	P11	VDD_SNVS_IN	GPIO	—	GPIO5_IO02/SNVS_TAMPER2	Input	Keeper[1]
SNVS_TAMPER3	P10	VDD_SNVS_IN	GPIO	—	GPIO5_IO03/SNVS_TAMPER3	Input	Keeper[1]
SNVS_TAMPER4	P9	VDD_SNVS_IN	GPIO	—	GPIO5_IO04/SNVS_TAMPER4	Input	Keeper[1]
SNVS_TAMPER5	N8	VDD_SNVS_IN	GPIO	—	GPIO5_IO05/SNVS_TAMPER5	Input	Keeper[1]
SNVS_TAMPER6	N11	VDD_SNVS_IN	GPIO	—	GPIO5_IO06/SNVS_TAMPER6	Input	Keeper[1]
SNVS_TAMPER7	N10	VDD_SNVS_IN	GPIO	—	GPIO5_IO07/SNVS_TAMPER7	Input	Keeper[1]
SNVS_TAMPER8	N9	VDD_SNVS_IN	GPIO	—	GPIO5_IO08/SNVS_TAMPER8	Input	Keeper[1]
SNVS_TAMPER9	R6	VDD_SNVS_IN	GPIO	—	GPIO5_IO09/SNVS_TAMPER9	Input	Keeper[1]
TEST_MODE	N7	VDD_SNVS_IN	GPIO	ALT0	TEST_MODE	Input	Keeper
UART1_CTS_B	K15	NVCC_UART	GPIO	ALT5	UART1_CTS_B	Input	Keeper
UART1_RTS_B	J14	NVCC_UART	GPIO	ALT5	UART1_RTS_B	Input	Keeper
UART1_RX_DATA	K16	NVCC_UART	GPIO	ALT5	UART1_RX_DATA	Input	Keeper
UART1_TX_DATA	K14	NVCC_UART	GPIO	ALT5	UART1_TX_DATA	Input	Keeper
UART2_CTS_B	J15	NVCC_UART	GPIO	ALT5	UART2_CTS_B	Input	Keeper
UART2_RTS_B	H14	NVCC_UART	GPIO	ALT5	UART2_RTS_B	Input	Keeper
UART2_RX_DATA	J16	NVCC_UART	GPIO	ALT5	UART2_RX_DATA	Input	Keeper
UART2_TX_DATA	J17	NVCC_UART	GPIO	ALT5	UART2_TX_DATA	Input	Keeper
UART3_CTS_B	H15	NVCC_UART	GPIO	ALT5	UART3_CTS_B	Input	Keeper
UART3_RTS_B	G14	NVCC_UART	GPIO	ALT5	UART3_RTS_B	Input	Keeper
UART3_RX_DATA	H16	NVCC_UART	GPIO	ALT5	UART3_RX_DATA	Input	Keeper
UART3_TX_DATA	H17	NVCC_UART	GPIO	ALT5	UART3_TX_DATA	Input	Keeper
UART4_RX_DATA	G16	NVCC_UART	GPIO	ALT5	UART4_RX_DATA	Input	Keeper
UART4_TX_DATA	G17	NVCC_UART	GPIO	ALT5	UART4_TX_DATA	Input	Keeper
UART5_RX_DATA	G13	NVCC_UART	GPIO	ALT5	UART5_RX_DATA	Input	Keeper
UART5_TX_DATA	F17	NVCC_UART	GPIO	ALT5	UART5_TX_DATA	Input	Keeper
USB_OTG1_CHD_B	U16	OPEN DRAIN	GPIO	—	USB_OTG1_CHD_B	—	—