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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-R5F
Core Size	32-Bit Single-Core
Speed	200MHz
Connectivity	CANbus, CSIO, I²C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	125
Program Memory Size	2.25MB (2.25M x 8)
Program Memory Type	FLASH
EEPROM Size	128K x 8
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	1.1V ~ 5.5V
Data Converters	A/D 40x12b; D/A 2x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	208-LQFP Exposed Pad
Supplier Device Package	208-TEQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb9df566maeeq-gtk5e1

MB9D560 Series

32-bit Microcontroller Traveo™ Family

MB9D560 series has Cypress 32-bit microcontrollers for automobile motor control. They use the ARM® Cortex-R5 MPCore™ CPU that is compatible with the ARM family.

Notes:

- ARM, Cortex, Thumb are the registered trademarks of ARM Limited in the EU and other countries.
- MPCore, CoreSight are the trademarks of ARM Limited in the EU and other countries.

Features

Technology

- CMOS 90nm technology

CPU

- ARM Cortex®-R5F
- 32-bit ARM architecture
- 2-instruction issuance super scalar
- 8-stage pipeline
- ARMv7 / Thumb®-2 instruction set
- Floating-Point Unit (FPU)
  - Double precision
- Memory protection Unit (MPU)
  - 16 area
- ECC support for the TCM port
  - 1-bit error correction, 2-bit error detection ECC (SEC-DED)
- TCM port
  - 2 TCM ports
- ATCM port
- BTCM 2 ports (B0TCM, B1TCM)
- VIC port
  - Low latency interrupt
- AXI master interface
  - 64-bit AXI interface (instruction / data access)
  - 32-bit AXI interface (I/O access)
- AXI slave interface
  - 64-bit AXI interface (accessible to TCM port)
- CPU configuration
  - 2 CPUs (AMP operation)
- Operating frequency
  - Maximum 200 MHz
- Trace with ETM-R5

Debugging

- ARM CoreSight™ Technology
  - Each CPU embedded Embedded Trace Macro (ETM), trace support of CPU operation
- Debugging interface
  - JTAG (5 pin)
  - Support clock : maximum 20 MHz
- Debugging security support
  - 128-bit security key (Device security key)
- Wakeup function on JTAG

Operation mode

- User mode
  - Normal mode (internal memory activation)
- Serial writer mode

Clock control

- Internal clock source
  - Fast-CR oscillation (8 MHz)
  - Slow-CR oscillation (100 kHz)
- External oscillation input
  - Main clock input
- Embedded PLL
  - Main PLL (Multiplying clock of main oscillation)
- Oscillator stabilized timer
  - Support oscillator stabilized timer for all clock source independently
  - After a lapse of oscillator stabilized time, it is able to use source clock timer (Except PLL for FlexRay/RDC)

1. Product Lineup

Memory Size

Parameter	MB9DF564	MB9DF565	MB9DF566
FLASH size (program)	(512KB+128KB)×2	(768KB+128KB)×2	(1024KB+128KB)×2
FLASH size (Work)	64KB×2	64KB×2	64KB×2
RAM size	64KB×2	96KB×2	128KB×2

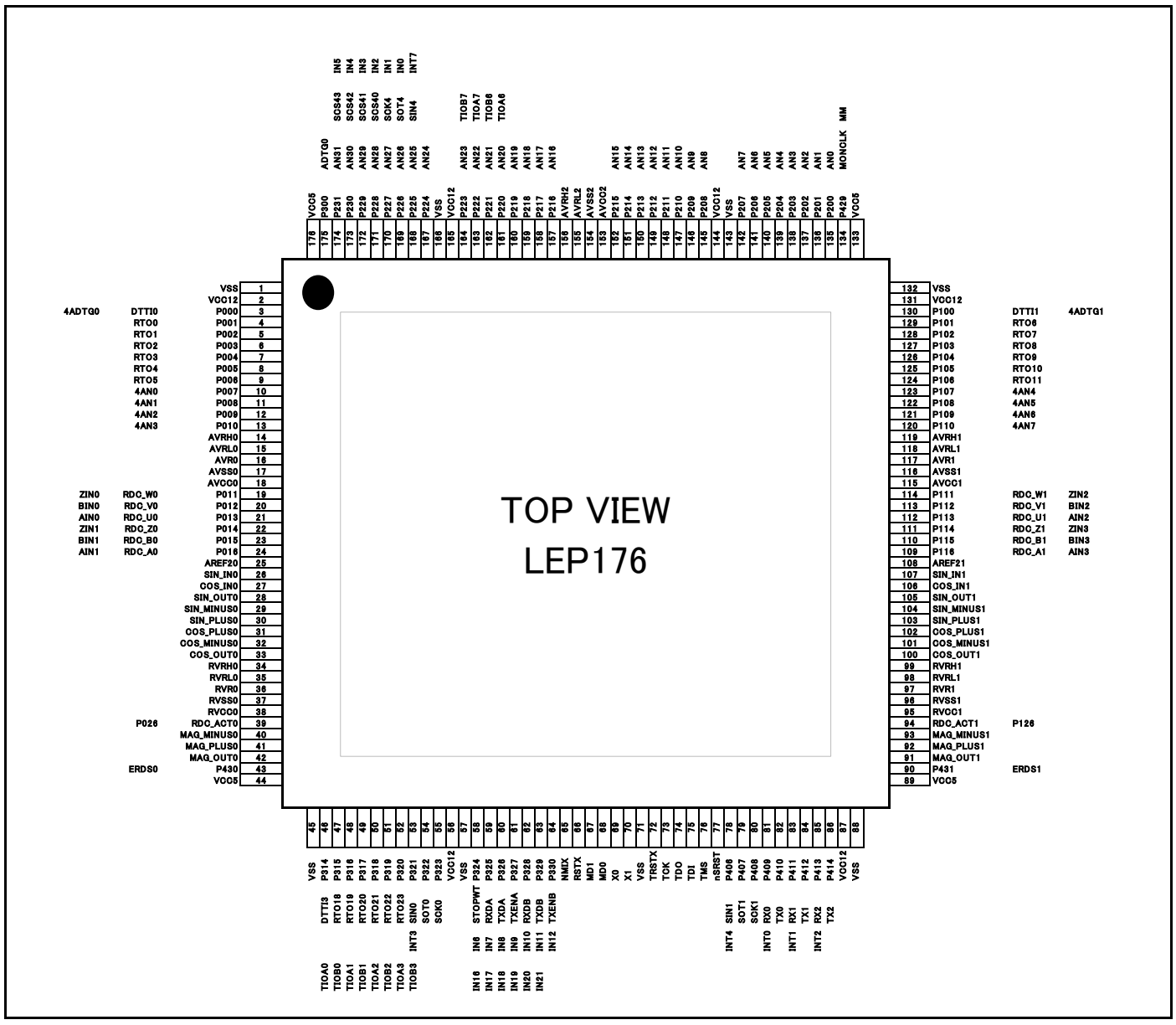
Functions

Pin number	208 pin	176 pin
System clock	On-chip PLL clock multiplication system Minimum instruction execution time :5 ns (200 MHz)	
CR oscillator (fast/slow)	Yes	
DMAC	16 channels	
Base timer	12 channels (0 to 11)	6 channels (0 to 3, 6, 7)
32-bit free-run timer	5 channels	
32-bit input capture	3 units (6 channels)	
16-bit free-run timer	20 channels*1	
16-bit input capture	8 units (0 to 7) (15 channels (0 to 14))	7 units (0 to 6) (13 channels (0 to 12))
16-bit output compare	12 units (0 to 11) (24 channels (0 to 23))	9 units (0 to 5, 9 to 11) (18 channels (0 to 11, 18 to 23))
Waveform generator	4 units (0 to 3) (24 channels (0 to 23))	3 units (0, 1, 3) (18 channels (0 to 11, 18 to 23))
External interrupt	8 channels (0 to 7)	6 channels (0 to 4, 7)
A/D converter	1 unit (32 channels)	
4ch sample-hold A/D converter	2 units (8 channels)	
R/D converter	2 units*2	
D/A converter	2 channels*2	
Up/Down counter	4 channels	
Motor vector operation accelerator	2 units	
Multi-function serial interface	5 channels (0 to 4)	3 channels (0, 1, 4)
CAN	3 channels	
FlexRay	128 msb x 1 unit (ch.A / ch.B)*2	
Inter-processor communications unit	Yes	
Exclusive access memory	Yes	
Software watchdog timer	Yes	
Hardware watchdog timer	Yes	
CRC	2 channels	
Internal power supply low-voltage detection	Yes	
External power supply low-voltage detection	Yes	
Key code	Yes*2	
Package	LER208	LEP176
Debugging interface	JTAG interface	

*1: 2 channels for motor control

*2: The function is different according to the part number. See “13. Part Number Option”.

176 Pin Part Number with RDC



Pin Number		Pin Name	I/O Circuit Type	Functions
208 pin	176 pin			
206	-	P303 TIOA11 FRCK6	E	General-purpose I/O port Base timer ch.11 TIOA I/O pin 16-bit free-run timer ch.6 external clock input pin
207	-	P304 TIOB11 FRCK7	E	General-purpose I/O port Base timer ch.11 TIOB input pin 16-bit free-run timer ch.7 external clock input pin
18	14	AVRH0	-	4ch sample-hold A/D converter unit0 upper limit reference voltage
19	15	AVRL0	-	4ch sample-hold A/D converter unit0 lower limit reference voltage
20	16	AVR0	-	4ch sample-hold A/D converter unit0 reference voltage
21	17	AVSS0	-	4ch sample-hold A/D converter unit0 analog GND
22	18	AVCC0	-	4ch sample-hold A/D converter unit0 analog power supply
134	115	AVCC1	-	4ch sample-hold A/D converter unit1 analog power supply
135	116	AVSS1	-	4ch sample-hold A/D converter unit1 analog GND
136	117	AVR1	-	4ch sample-hold A/D converter unit1 reference voltage
137	118	AVRL1	-	4ch sample-hold A/D converter unit1 lower limit reference voltage
138	119	AVRH1	-	4ch sample-hold A/D converter unit1 upper limit reference voltage
38	34	RVRH0	-	R/D converter unit0 upper limit reference voltage
39	35	RVRL0	-	R/D converter unit0 lower limit reference voltage
40	36	RVR0	-	R/D converter unit0 reference voltage
41	37	RVSS0	-	R/D converter unit0 analog GND
42	38	RVCC0	-	R/D converter unit0 analog power supply
114	95	RVCC1	-	R/D converter unit1 analog power supply
115	96	RVSS1	-	R/D converter unit1 analog GND
116	97	RVR1	-	R/D converter unit1 reference voltage
117	98	RVRL1	-	R/D converter unit1 lower limit reference voltage
118	99	RVRH1	-	R/D converter unit1 upper limit reference voltage
181	153	AVCC2	-	A/D converter analog power supply
182	154	AVSS2	-	A/D converter analog GND
183	155	AVRL2	-	A/D converter lower limit reference voltage
184	156	AVRH2	-	A/D converter upper limit reference voltage
2 54 68 103 155 172 193	2 56 87 131 144 165	VCC12	-	1.2V power supply
12 52 105 144 157 208	44 89 133 176	VCC5	-	5.0V power supply
1 13 53 69 83 104 143 156 171 194	1 45 57 71 88 132 143 166	VSS	-	GND

Pin Number		Pin Name	I/O Circuit Type	Functions
208pin	176pin			
153	-	P422 SOT3 FRCK9 IN13	E	General-purpose I/O port Multi -function serial interface ch.3 serial data output pin 16-bit free-run timer ch.9 external clock input pin 16-bit input capture ch.13 external pulse input pin
154	-	P423 SCK3 FRCK10 IN14	E	General-purpose I/O port Multi-function serial interface ch.3 clock I/O pin 16-bit free-run timer ch.10 external clock input pin 16-bit input capture ch.14 external pulse input pin
158	-	P425 TIOA8	E	General-purpose I/O port Base timer ch.8 TIOA output pin
159	-	P426 TIOB8	E	General-purpose I/O port Base timer ch.8 TIOB input pin
160	-	P427 TIOA9	E	General-purpose I/O port Base timer ch.9 TIOA I/O pin
161	-	P428 TIOB9	E	General-purpose I/O port Base timer ch.9 TIOB input pin
162	134	P429 MONCLK MM	E	General-purpose I/O port Clock monitor output pin Clock supervisor main clock error detection output pin
163	135	P200 AN0	F	General-purpose I/O port A/D converter analog 0 input pin
164	136	P201 AN1	F	General-purpose I/O port A/D converter analog 1 input pin
165	137	P202 AN2	F	General-purpose I/O port A/D converter analog 2 input pin
166	138	P203 AN3	F	General-purpose I/O port A/D converter analog 3 input pin
167	139	P204 AN4	F	General-purpose I/O port A/D converter analog 4 input pin
168	140	P205 AN5	F	General-purpose I/O port A/D converter analog 5 input pin
169	141	P206 AN6	F	General-purpose I/O port A/D converter analog 6 input pin
170	142	P207 AN7	F	General-purpose I/O port A/D converter analog 7 input pin
173	145	P208 AN8	F	General-purpose I/O port A/D converter analog 8 input pin
174	146	P209 AN9	F	General-purpose I/O port A/D converter analog 9 input pin
175	147	P210 AN10	F	General-purpose I/O port A/D converter analog 10 input pin
176	148	P211 AN11	F	General-purpose I/O port A/D converter analog 11 input pin
177	149	P212 AN12	F	General-purpose I/O port A/D converter analog 12 input pin
178	150	P213 AN13	F	General-purpose I/O port A/D converter analog 13 input pin
179	151	P214 AN14	F	General-purpose I/O port A/D converter analog 14 input pin
180	152	P215 AN15	F	General-purpose I/O port A/D converter analog 15 input pin
185	157	P216 AN16	F	General-purpose I/O port A/D converter analog 16 input pin
186	158	P217 AN17	F	General-purpose I/O port A/D converter analog 17 input pin
187	159	P218 AN18	F	General-purpose I/O port A/D converter analog 18 input pin
188	160	P219 AN19	F	General-purpose I/O port A/D converter analog 19 input pin

6. Handling Devices

For Latch-up Prevention

If a voltage higher than VCC5 or VCC12, or a voltage lower than VSS is applied to an I/O pin, or if a voltage exceeding the ratings is applied between VCC5 to VSS and VCC12 to VSS pins, a latch-up may occur in CMOS IC. If the latch-up occurs, the power supply current increases excessively and device elements may be damaged by heat. Take care to prevent any voltage from exceeding the maximum ratings in device application.

Also, the analog power supplies (AVCC0, AVCC1, AVCC2, AVRH0, AVRH1, AVRH2, RVCC0, RVCC1,

RVRH0, RVEH1) and analog input must not exceed the digital power supply (VCC5) when the power supply to the analog system is turned on or off.

In the correct power-on sequence, turn on the digital power supply voltage (VCC5, VCC12) and analog power supply voltages (AVCC0, AVCC1, AVCC2, AVRH0, AVRH1, AVRH2, RVCC0, RVCC1, RVRH0, RVRH1) simultaneously. Alternatively, turn on the digital power supply voltage (VCC5) first, and then turn on the analog power supplies (AVCC0, AVCC1, AVCC2, AVRH0, AVRH1, AVRH2, RVCC0, RVCC1,

RVRH0, RVRH1).

Treatment of Unused Pins

If unused input pins are left open, they may cause a permanent damage to the device due to device malfunction or latch-up. Connect a 2 kΩ or higher resistor to each of unused input pins for pull-up or pull-down processing.

Also, if I/O pins are not used, they must be set to the output state for releasing or they must be set to the input state and treated in the same way as for the input pins.

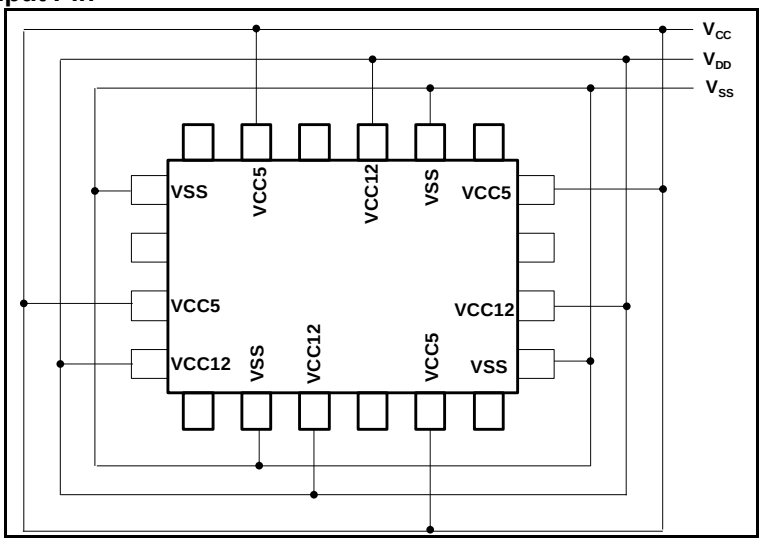
Power Supply Pins

The device is designed to ensure that if the device contains multiple VCC5, VCC12 and VSS pins, the pins that should be at the same potential are interconnected to prevent latch-up or other malfunctions.

Further, connect these pins to an external power supply or ground to reduce unwanted radiation, prevent strobe signals from malfunctioning due to a raised ground level, and fulfill the total output current standard, etc. As shown below, all VSS power supply pins must be treated in the similar way. If multiple VCC5 or

VCC12 or VSS systems are connected, the device cannot operate correctly even within the guaranteed operating range.

Power Supply Input Pin



The power supply pins should be connected to VCC5, VCC12 and VSS of this device at the low impedance from the power supply source.

In the area close to this device, a ceramic capacitor having the capacitance larger than the capacitor of C pin is recommended to use as a bypass capacitor between VCC5, VCC12 and VSS pins

Group

Group Name	Description
Core Group	CPU and TCM connected memory group
Debug Group	CoreSight of Debugging group
MCU Config Group	System control and supervision IP group
Memory & Config Group _	CPU related function and memory group
Common Peripheral Group	Common peripheral IP group for vehicle application
Application Specific Peripheral Group	Product specified peripheral group

Independent IP

Name	Description
HPM	Bus matrix of AXI Bus bridge (AXI-to-AHB, AHB-to-AXI)
DMAC	DMA controller
EAM	Exclusive access memory
Resource input configuration	Input selection circuit of MCU peripheral
Port MUX	Port MUX circuit
I/O	I/O circuit

Note:

- Each master connects to HPM. Each master has different transaction ID on AXI, Out-Of-Order for transaction completion.

8. Memory Map

Address		Block	
Start	**End**	**Overview**	**Function**
0x0000_0000	64KB: 0x0000_FFFF 96KB: 0x0001_7FFF 128KB: 0x0001_FFFF	Memory (Each CPU exclusive space)	TCRAM
0x0002_0000	0x007F_FFFF		Reserved
0x0080_0000	512KB: 0x0087_FFFF 768KB: 0x008B_FFFF 1024KB: 0x008F_FFFF		TCFLASH large sector area (TCM connection)
0x0090_0000	0x00FD_FFFF		Reserved
0x00FE_0000	0x00FF_FFFF		TCFLASH small sector area (TCM connection)
0x0100_0000	512KB: 0x0107_FFFF 768KB: 0x010B_FFFF 1024KB: 0x010F_FFFF		TCFLASH large sector area (AXI connection)
0x0110_0000	0x01FD_FFFF		Reserved
0x01FE_0000	0x01FF_FFFF		TCFLASH small sector area (AXI connection)
0x0200_0000	0x027F_FFFF	Memory (Common space)	Reserved
0x0280_0000	0x0280_0FFF		EAM
0x0280_1000	0x03FF_FFFF		Reserved
0x0400_0000	64KB: 0x0400_FFFF 96KB: 0x0401_7FFF 128KB: 0x0401_FFFF		CPU0 space TCRAM
0x0402_0000	0x047F_FFFF		Reserved
0x0480_0000	512KB: 0x0487_FFFF 768KB: 0x048B_FFFF 1024KB: 0x048F_FFFF		CPU0 space TCFLASH large sector area (TCM connection)
0x0490_0000	0x04FD_FFFF		Reserved
0x04FE_0000	0x04FF_FFFF		CPU0 space TCFLASH small sector area (TCM connection)
0x0500_0000	512KB: 0x0507_FFFF 768KB: 0x050B_FFFF 1024KB: 0x050F_FFFF		CPU0 space TCFLASH large sector area (AXI connection)
0x0510_0000	0x05FD_FFFF		Reserved
0x05FE_0000	0x05FF_FFFF		CPU0 space TCFLASH small sector area (AXI connection)
0x0600_0000	64KB: 0x0600_FFFF 96KB: 0x0601_7FFF 128KB: 0x0601_FFFF		CPU1 space TCRAM
0x0602_0000	0x067F_FFFF		Reserved
0x0680_0000	512KB: 0x0687_FFFF 768KB: 0x068B_FFFF 1024KB: 0x068F_FFFF		CPU1 space TCFLASH large sector area (TCM connection)
0x0690_0000	0x06FD_FFFF		Reserved

Notes:

- Each CPU exclusive space define memory space for each CPU specified. The other master cannot access (Reserved area). If the other master access to each CPU exclusive space, access from common space.
- Reserved area access cause bus error.
- However, following access of reserved area will be not bus error.
  0x0090_0000 to 0x00FD_FFFF

  0x0110_0000 to 0x01FD_FFFF

  0x0490_0000 to 0x04FD_FFFF

  0x0510_0000 to 0x05FD_FFFF

  0x0690_0000 to 0x06FD_FFFF

  0x0710_0000 to 0x07FD_FFFF

  0x1000_0000 to 0x1FFF_FFFF

  0x2000_0000 to 0x2FFF_FFFF
- The following area should be set device attribution or strongly ordered attribution as core access.
  1. I/O area

  2. Bit band alias area

  3. Error Config (BootROM area)

  4. WorkFLASH (when program)

  5. TCFLASH (when program)

  About device attribute and Strongly Ordered attribute, see "ARM® Architecture Reference Manual ARM® v7-A and ARM® v7-R edition (ARM DDI 0406B)".
- TCFLASH has a TCM-connected region and an AXI-connected region. AXI-connected region is dedicated for flash memory programming/erasing. When read operation in user mode, use TCM-connected region.

11.3 DC Characteristics

(T_A: Recommended operating conditions, V_{CC} = 5.0V±0.5V, V_{DD} = 1.2V±0.1V, V_{SS} = AV_{SS} = RV_{SS} = 0.0V)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
"H" level input voltage	V_{IH1}	P000 to P016, P026, P030 to P031, P100 to P116, P126, P131, P200 to P231, P300 toP306, P309 to P324, P406 to P423, P425 to P431	When CMOS schmitt input level is selected	0.7×V_{CC}	-	Vcc+0.3	V	
	V_{IH2}	P000 to P016, P026, P030 to P031, P100 to P116, P126, P131, P200 to P231, P300 to P306, P309 to P330, P406 to P423, P425 to P431	When automotive input level is selected	0.8×V_{CC}	-	Vcc+0.3	V	
	V_{IH3}	P325 to P330	When FlexRay input level is selected	0.7×V_{CC}	-	Vcc+0.3	V	
	V_{IH4}	RSTX, NMIX	-	0.7×V_{CC}	-	Vcc+0.3	V	
	V_{IH5}	MD0, MD1	-	0.7×V_{CC}	-	Vcc+0.3	V	
	V_{IH6}	TRSTX, TCK, TDI, TMS, nSRST	-	2.3	-	Vcc+0.3	V	

(T_A: Recommended operating conditions, V_{CC} = 5.0V±0.5V, V_{DD} = 1.2V±0.1V, V_{SS} = AV_{SS} = RV_{SS} = 0.0V)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
"L" level input voltage	V_{IL1}	P000 to P016, P026, P030 to P031, P100 to P116, P126, P131, P200 to P231, P300 toP306, P309 to P324, P406 to P423, P425 to P431	When CMOS schmitt input level is selected	V_{SS}-0.3	-	0.3×V_{CC}	V	
	V_{IL2}	P000 to P016, P026, P030 to P031, P100 to P116, P126, P131, P200 to P231, P300 to P306, P309 to P330, P406 to P423, P425 to P431	When automotive input level is selected	V_{SS}-0.3	-	0.5×V_{CC}	V	
	V_{IL3}	P325 to P330	When FlexRay input level is selected	V_{SS}-0.3	-	0.3×V_{CC}	V	
	V_{IL4}	RSTX, NMIX	-	V_{SS}-0.3	-	0.3×V_{CC}	V	
	V_{IL5}	MD0, MD1	-	V_{SS}-0.3	-	0.3×V_{CC}	V	
	V_{IL6}	TRSTX, TCK, TDI, TMS, nSRST	-	V_{SS}-0.3	-	0.8	V	

(T_A: Recommended operating conditions, V_{CC} = 5.0V±0.5V, V_{DD} = 1.2V±0.1V, V_{SS} = AVSS = RVSS = 0.0V)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current	I_{CCS12}	VCC12	CPU sleep mode 200MHz	-	220	410	mA	F_{CD0_CLK} = 200 MHz F_{CLK_CPUx} = 200 MHz, F_{CLK_TFCLKx} = 66 MHz, F_{CLK_HPMPD2} = 200 MHz, F_{CLK_DMA} = 200 MHz, F_{CLK_MEMC} = 100 MHz, F_{CLK_WFCLKx} = 200 MHz, $F_{CLK\_SYSCPD1}$ = 100 MHz, F_{CLK_PERIy} = 100 MHz, F_{CLK_PERIz} = 50 MHz x = 0, 1 y = 0, 4, 5 z = 1, 6, 7
			CPU sleep mode 160MHz	-	180	360	mA	F_{CD0_CLK} = 160 MHz F_{CLK_CPUx} = 160 MHz, F_{CLK_TFCLKx} = 80 MHz, F_{CLK_HPMPD2} = 160 MHz, F_{CLK_DMA} = 160 MHz, F_{CLK_MEMC} = 80 MHz, F_{CLK_WFCLKx} = 160 MHz, $F_{CLK\_SYSCPD1}$ = 80 MHz, F_{CLK_PERIy} = 80 MHz, F_{CLK_PERIz} = 40 MHz x = 0, 1 y = 0, 4, 5 z = 1, 6, 7
	I_{CCT12}		Watch mode, 4MHz source oscillation	-	1280	9730	µA	When using crystal T_A = 25°C
	I_{CCH12}		Stop mode	-	860	9530	µA	T_A = 25°C

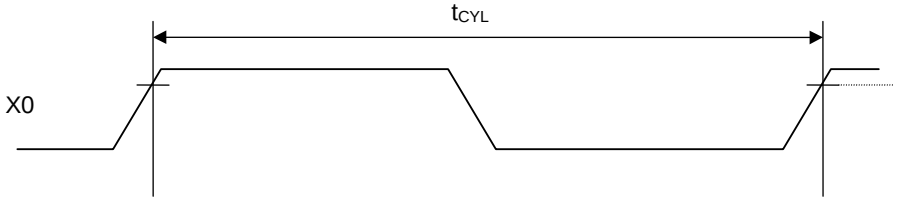
11.4 AC Characteristics

11.4.1 Source Clock Timing

(T_A: Recommended operating conditions, V_{CC} = 5.0V±0.5V, V_{DD} = 1.2V±0.1V, V_{SS} = AV_{SS} = RV_{SS} = 0.0V)

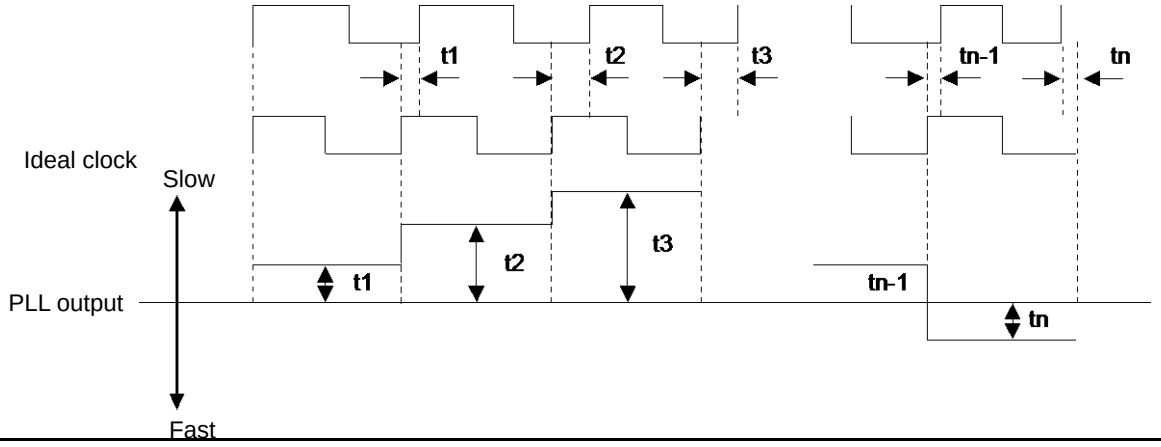
Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Source oscillation clock frequency	F_C	X0, X1	-	4	-	20	MHz	
Source oscillation clock cycle time	t_{CYL}	X0, X1	-	50	-	250	ns	
CAN PLL jitter (during lock)	t_{PJ}	-	-	-10	-	+10	ns	
Built-in slow-CR oscillation frequency	F_{CRS}	-	-	50	100	150	kHz	
Built-in fast-CR oscillation frequency	F_{CRF}	-	-	4	8	12	MHz	Without calibration
				7.2	8	8.8	MHz	With calibration

X0, X1 clock timing



CAN PLL jitter

Deviation time from the ideal clock is assured per cycle out of 20,000 cycles.



11.4.2 Internal Clock Timing

(T_A: Recommended operating conditions, V_{CC} = 5.0V±0.5V, V_{DD} = 1.2V±0.1V, V_{SS} = AV_{SS} = RV_{SS} = 0.0V)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Internal clock frequency	F_{CD0_CLK}	-	-	0	-	200	MHz	CD0_CLK
	F_{CD4_CLK}	-	-	0	-	200	MHz	CD4_CLK
	F_{CLK_CPU0}	-	-	0	-	200	MHz	CLK_CPU0
	F_{CLK_CPU1}	-	-	0	-	200	MHz	CLK_CPU1
	F_{CLK_TFCLK0}	-	-	0	-	80	MHz	CLK_TFCLK0
	F_{CLK_TFCLK1}	-	-	0	-	80	MHz	CLK_TFCLK1
	F_{CLK_ATB}	-	-	0	-	100	MHz	CLK_ATB
	F_{CLK_DBG}	-	-	0	-	50	MHz	CLK_DBG
	F_{CLK_HPMPD2}	-	-	0	-	200	MHz	CLK_HPMPD2
	F_{CLK_DMA}	-	-	0	-	200	MHz	CLK_DMA
	F_{CLK_MEMC}	-	-	0	-	200	MHz	CLK_MEMC
	F_{CLK_WFCLK0}	-	-	0	-	80	MHz	CLK_WFCLK0
	F_{CLK_WFCLK1}	-	-	0	-	80	MHz	CLK_WFCLK1
	$F_{CLK\_SYSCPD1}$	-	-	0	-	100	MHz	CLK_SYSCPD1
	F_{CLK_PERI0}	-	-	0	-	100	MHz	CLK_PERI0
	F_{CLK_PERI1}	-	-	0	-	50	MHz	CLK_PERI1
	F_{CLK_PERI4}	-	-	0	-	100	MHz	CLK_PERI4
	F_{CLK_PERI5}	-	-	0	-	100	MHz	CLK_PERI5
	F_{CLK_PERI6}	-	-	0	-	50	MHz	CLK_PERI6
	F_{CLK_PERI7}	-	-	0	-	50	MHz	CLK_PERI7
	F_{CLK_CLKO}	-	-	0	-	200	MHz	CLK_CLKO
Internal clock cycle time	t_{CD0_CLK}	-	-	5	-	-	ns	CD0_CLK
	t_{CD4_CLK}	-	-	5	-	-	ns	CD4_CLK
	t_{CLK_CPU0}	-	-	5	-	-	ns	CLK_CPU0
	t_{CLK_CPU1}	-	-	5	-	-	ns	CLK_CPU1
	t_{CLK_TFCLK0}	-	-	12.5	-	-	ns	CLK_TFCLK0
	t_{CLK_TFCLK1}	-	-	12.5	-	-	ns	CLK_TFCLK1
	t_{CLK_ATB}	-	-	10	-	-	ns	CLK_ATB
	t_{CLK_DBG}	-	-	20	-	-	ns	CLK_DBG
	t_{CLK_HPMPD2}	-	-	5	-	-	ns	CLK_HPMPD2
	t_{CLK_DMA}	-	-	5	-	-	ns	CLK_DMA
	t_{CLK_MEMC}	-	-	5	-	-	ns	CLK_MEMC
	t_{CLK_WFCLK0}	-	-	12.5	-	-	ns	CLK_WFCLK0
	t_{CLK_WFCLK1}	-	-	12.5	-	-	ns	CLK_WFCLK1
	$t_{CLK\_SYSCPD1}$	-	-	10	-	-	ns	CLK_SYSCPD1
	t_{CLK_PERI0}	-	-	10	-	-	ns	CLK_PERI0
	t_{CLK_PERI1}	-	-	20	-	-	ns	CLK_PERI1
	t_{CLK_PERI4}	-	-	10	-	-	ns	CLK_PERI4
	t_{CLK_PERI5}	-	-	10	-	-	ns	CLK_PERI5
	t_{CLK_PERI6}	-	-	20	-	-	ns	CLK_PERI6
	t_{CLK_PERI7}	-	-	20	-	-	ns	CLK_PERI7
	t_{CLK_CLKO}	-	-	5	-	-	ns	CLK_CLKO

11.4.5 Multi-Function Serial Interface

11.4.5.1 CSIO Timing (SMR: MD[2:0] = 0b010)

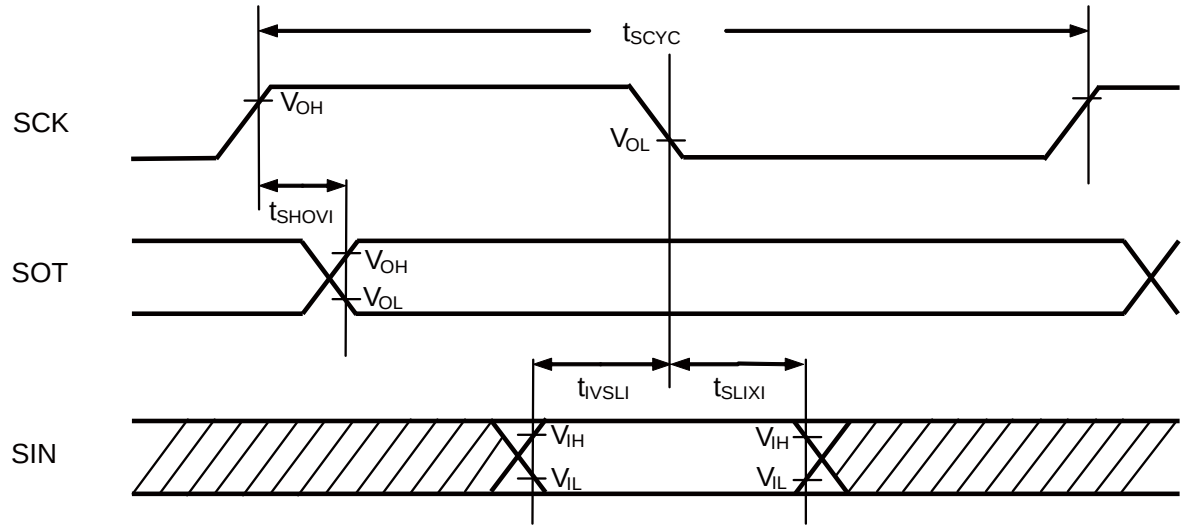
Normal Synchronous Transfer (SCR: SPI = 0) and Serial Clock Output Signal Detect Level "H"(SMR: SCINV = 0)

(T_A: Recommended operating conditions, V_{CC} = 5.0V±0.5V, V_{DD} = 1.2V±0.1V, V_{SS} = AV_{SS} = RV_{SS} = 0.0V)

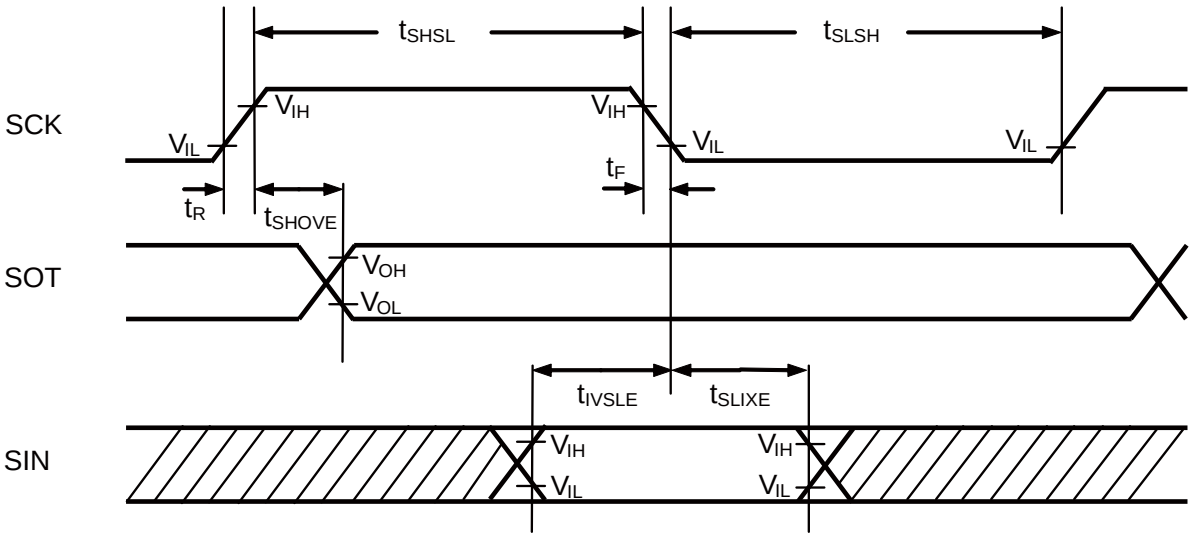
Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	t_{SCYC}	SCK0 to SCK4	Master mode (C_L = 50pF, I_{OL} = -2mA, I_{OH} = 2mA), (C_L = 20pF, I_{OL} = -1mA, I_{OH} = 1mA)	$4t_{CLK\_PERI1}$	-	ns	
SCK↓→SOT delay time	t_{SLOVI}	SCK0 to SCK4, SOT0 to SOT4		-30	+30	ns	
Valid SIN→SCK↑ setup time	t_{IVSHI}	SCK0 to SCK4, SIN0 to SIN4		30	-	ns	
SCK↑→Valid SIN hold time	t_{SHIXI}			0	-	ns	
Serial clock "H" pulse width	t_{SHSL}	SCK0 to SCK4	Slave mode (C_L = 50pF, I_{OL} = -2mA, I_{OH} = 2mA), (C_L = 20pF, I_{OL} = -1mA, I_{OH} = 1mA)	t_{CLK_PERI1}+10	-	ns	
Serial clock "L" pulse width	t_{SLSH}			$2t_{CLK\_PERI1}$-10	-	ns	
SCK↓→SOT delay time	t_{SLOVE}	SCK0 to SCK4, SOT0 to SOT4		-	30	ns	
Valid SIN→SCK↑ setup time	t_{IVSHE}	SCK0 to SCK4, SIN0 to SIN4		10	-	ns	
SCK↑→Valid SIN hold time	t_{SHIXE}			20	-	ns	
SCK fall time	t_F	SCK0 to SCK4		-	5	ns	
SCK rise time	t_R	SCK0 to SCK4		-	5	ns	
Transfer speed	-	-	C_L = 50pF, I_{OL} = -2mA, I_{OH} = 2mA	-	5	Mbps	
	-	-	C_L = 20pF, I_{OL} = -1mA, I_{OH} = 1mA	-	6	Mbps	

Notes:

- This is the AC characteristic in CLK synchronized mode.
- C_L is the load capacitance applied to pins during testing.
- The maximum baud rate is limited by the internal operation clock used and other parameters. See Hardware Manual for details.



Master mode



Slave mode

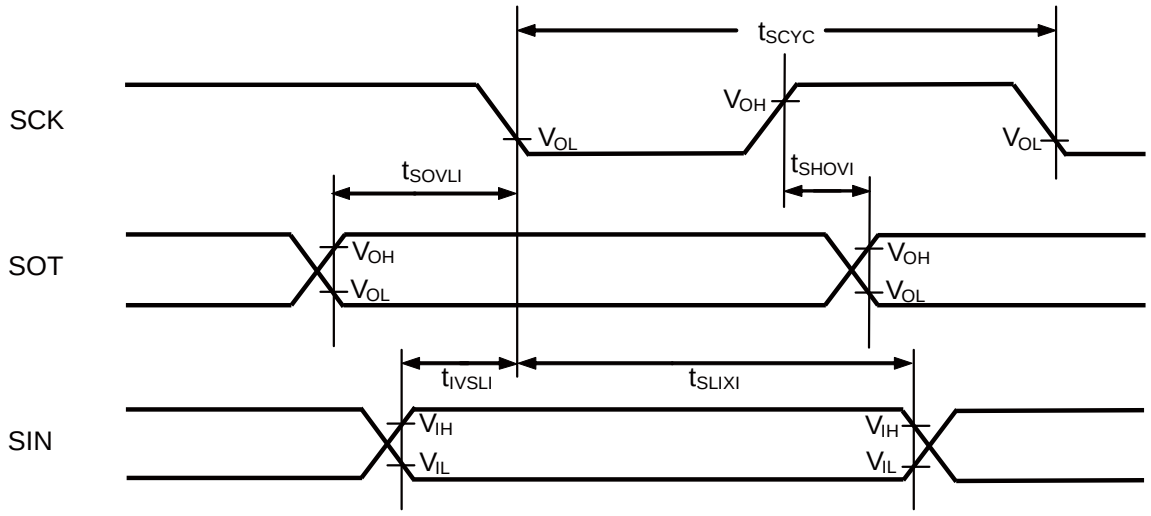
SPI Compatible (SCR: SPI = 1) and Serial Clock Output Signal Detect Level "H" (SMR: SCINV = 0)

(T_A: Recommended operating conditions, V_{CC} = 5.0V±0.5V, V_{DD} = 1.2V±0.1V, V_{SS} = AV_{SS} = RV_{SS} = 0.0V)

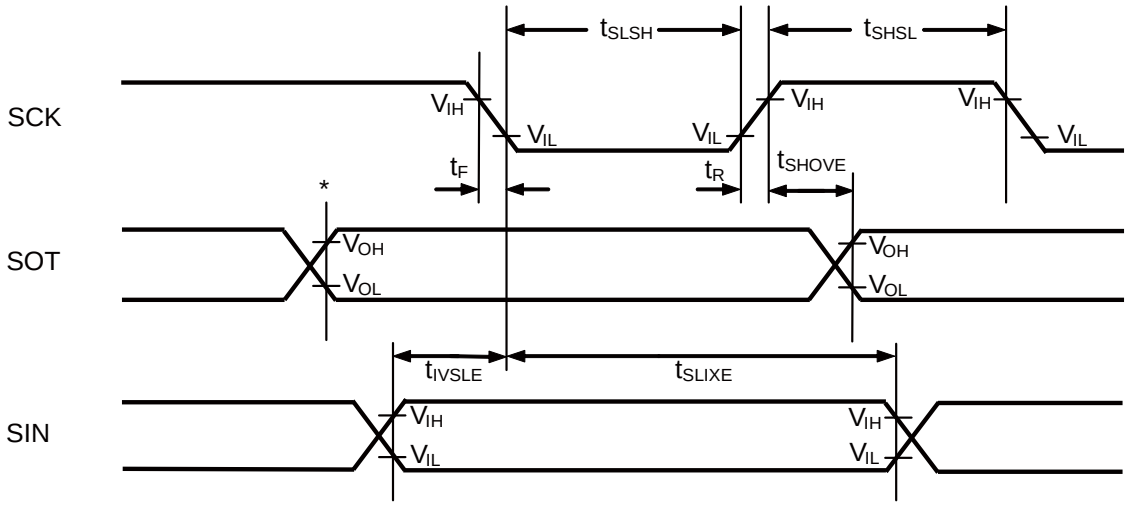
Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	t_{SCYC}	SCK0 to SCK4	Master mode (C_L = 50pF, I_{OL} = -2mA, I_{OH} = 2mA), (C_L = 20pF, I_{OL} = -1mA, I_{OH} = 1mA)	$4t_{CLK\_PERI1}$	-	ns	
SCK↑→SOT delay time	t_{SHOVI}	SCK0 to SCK4, SOT0 to SOT4		-30	+30	ns	
Valid SIN→SCK↓ setup time	t_{IVSLI}	SCK0 to SCK4, SIN0 to SIN4		30	-	ns	
SCK↓→valid SIN hold time	t_{SLIXI}			0	-	ns	
SOT→SCK↓ delay time	t_{SOVLI}	SCK0 to SCK4, SOT0 to SOT4		$2t_{CLK\_PERI1}$-30	-	ns	
Serial clock "H" pulse width	t_{SHSL}	SCK0 to SCK4	Slave mode (C_L = 50pF, I_{OL} = -2mA, I_{OH} = 2mA), (C_L = 20pF, I_{OL} = -1mA, I_{OH} = 1mA)	t_{CLK_PERI1}+10	-	ns	
Serial clock "L" pulse width	t_{SLSH}			$2t_{CLK\_PERI1}$-10	-	ns	
SCK↑→SOT delay time	t_{SHOVE}	SCK0 to SCK4, SOT0 to SOT4		-	30	ns	
valid SIN→SCK↓ setup time	t_{IVSLE}	SCK0 to SCK4, SIN0 to SIN4		10	-	ns	
SCK↓→valid SIN hold time	t_{SLIXE}			20	-	ns	
SCK fall time	t_F	SCK0 to SCK4		-	5	ns	
SCK rise time	t_R	SCK0 to SCK4		-	5	ns	
Transfer speed	-	-	C_L = 50pF, I_{OL} = -2mA, I_{OH} = 2mA	-	5	Mbps	
	-	-	C_L = 20pF, I_{OL} = -1mA, I_{OH} = 1mA	-	6	Mbps	

Notes:

- This is the AC characteristic in CLK synchronized mode.
- C_L is the load capacitance applied to pins during testing.
- The maximum baud rate is limited by the internal operation clock used and other parameters. See Hardware Manual for details.



Master mode



*: Changes when writing to TDR register

Slave mode

SPI Compatible (SCR: SPI = 1) and Serial Clock Output Signal Detect Level "L" (SMR: SCINV = 1)

(T_A: Recommended operating conditions, V_{CC} = 5.0V±0.5V, V_{DD} = 1.2V±0.1V, V_{SS} = AV_{SS} = RV_{SS} = 0.0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	t_{SCYC}	SCK0 to SCK4	Master mode (C_L = 50pF, I_{OL} = -2mA, I_{OH} = 2mA), (C_L = 20pF, I_{OL} = -1mA, I_{OH} = 1mA)	$4t_{CLK\_PERI1}$	-	ns	
SCK↓→SOT delay time	t_{SLOVI}	SCK0 to SCK4, SOT0 to SOT4		-30	+30	ns	
Valid SIN→SCK↑ setup time	t_{IVSHI}	SCK0 to SCK4, SIN0 to SIN4		30	-	ns	
SCK↑→valid SIN hold time	t_{SHIXI}			0	-	ns	
SOT→SCK↑ Delay time	t_{SOVHI}	SCK0 to SCK4, SOT0 to SOT4		$2t_{CLK\_PERI1}$-30	-	ns	
Serial clock "H" pulse width	t_{SHSL}	SCK0 to SCK4, SOT0 to SOT4	Slave mode (C_L = 50pF, I_{OL} = -2mA, I_{OH} = 2mA), (C_L = 20pF, I_{OL} = -1mA, I_{OH} = 1mA)	t_{CLK_PERI1}+10	-	ns	
Serial clock "L" pulse width	t_{SLSH}			$2t_{CLK\_PERI1}$-10	-	ns	
SCK↓→SOT delay time	t_{SLOVE}	SCK0 to SCK4, SOT0 to SOT4		-	30	ns	
valid SIN→SCK↑ setup time	t_{IVSHE}	SCK0 to SCK4, SIN0 to SIN4		10	-	ns	
SCK↑→valid SIN hold time	t_{SHIXE}			20	-	ns	
SCK fall time	t_F	SCK0 to SCK4		-	5	ns	
SCK rise time	t_R	SCK0 to SCK4		-	5	ns	
Transfer speed	-	-	C_L = 50pF, I_{OL} = -2mA, I_{OH} = 2mA	-	5	Mbps	
	-	-	C_L = 20pF, I_{OL} = -1mA, I_{OH} = 1mA	-	6	Mbps	

Notes:

- This is the AC characteristic in CLK synchronized mode.
- C_L is the load capacitance applied to pins during testing.
- The maximum baud rate is limited by the internal operation clock used and other parameters. See Hardware Manual for details.

When the Serial Chip Select is Used (SCSCR: CSEN = 1)

■Serial clock output signal detect level "L"(SMR, SCSFR: SCINV = 1)

■Serial Chip select inactive level "L"(SCSCR, SCSFR: CSLVL = 0)

(T_A: Recommended operating conditions, V_{CC} = 5.0V±0.5V, V_{DD} = 1.2V±0.1V, V_{SS} = AV_{SS} = RV_{SS} = 0.0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
SCS↑→SCK↑ setup time	t_{CSSI}	SCK4, SCS40 to SCS43	Master mode (C_L = 50pF, I_{OL} = -2mA, I_{OH} = 2mA), (C_L = 20pF, I_{OL} = -1mA, I_{OH} = 1mA)	t_{CSSU} *1-50	-	ns	
SCK↓→SCS↓ hold time	t_{CSHI}			t_{CSHD} *2+0	-	ns	
SCS deselect t time	t_{CSDI}	SCS40 to SCS43		t_{CSDS} *3-50 +5t_{CLK_PERI1}	-	ns	
SCS↑→SCK↑ setup time	t_{CSSE}	SCK4, SCS40 to SCS43	Slave mode (C_L = 50pF, I_{OL} = -2mA, I_{OH} = 2mA), (C_L = 20pF, I_{OL} = -1mA, I_{OH} = 1mA)	3t_{CLK_PERI1}+30	-	ns	
SCK↓→SCS↓ hold time	t_{CSHE}			0	-	ns	
SCS deselect time	t_{CSDE}	SCS40 to SCS43		3t_{CLK_PERI1}+30	-	ns	
SCS↑→SOT delay time	t_{DSE}	SCS40 to SCS43, SOT4		-	40	ns	
SCS↓→SOT delay time	t_{DEE}			0	-	ns	
SCK↑→SCS↑ clock switch time	t_{SCC}	SCK4, SCS40 to SCS43	Master mode, Round operation (C_L = 50pF, I_{OL} = -2mA,I_{OH} = 2mA), (C_L = 20pF, I_{OL} = -1mA, I_{OH} = 1mA)	3t_{CLK_PERI1}+0	3t_{CLK_PERI1} +50	ns	
Transfer speed	-	-	C_L = 50pF, I_{OL} = -2mA, I_{OH} = 2mA	-	5	Mbps	
	-	-	C_L = 20pF, I_{OL} = -1mA, I_{OH} = 1mA	-	6	Mbps	

*1: t_{CSSU} = SCSTR:CSSU[7:0] × serial chip select timing operation clock

*2: t_{CSHD} = SCSTR:CSHD[7:0] × serial chip select timing operation clock

*3: t_{CSDS} = SCSTR:CSDS[15:0] × serial chip select timing operation clock

For details of *1, *2 and *3 above, see Hardware Manual.

Notes:

- This is the AC characteristic in CLK synchronized mode.
- C_L is the load capacitance applied to pins during testing.
- The maximum baud rate is limited by the internal operation clock used and other parameters. See Hardware Manual for details.

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