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### Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

Product Status	Obsolete
Number of LABs/CLBs	64
Number of Logic Elements/Cells	-
Total RAM Bits	14779
Number of I/O	64
Number of Gates	1500
Voltage - Supply	4.75V ~ 5.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	84-LCC (J-Lead)
Supplier Device Package	84-PLCC (29.31x29.31)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/xilinx/xc3020a-7pc84c">https://www.e-xfl.com/product-detail/xilinx/xc3020a-7pc84c</a>

### ***Improvements in the XC3000A and XC3000L Families***

The XC3000A and XC3000L families offer the following enhancements over the popular XC3000 family:

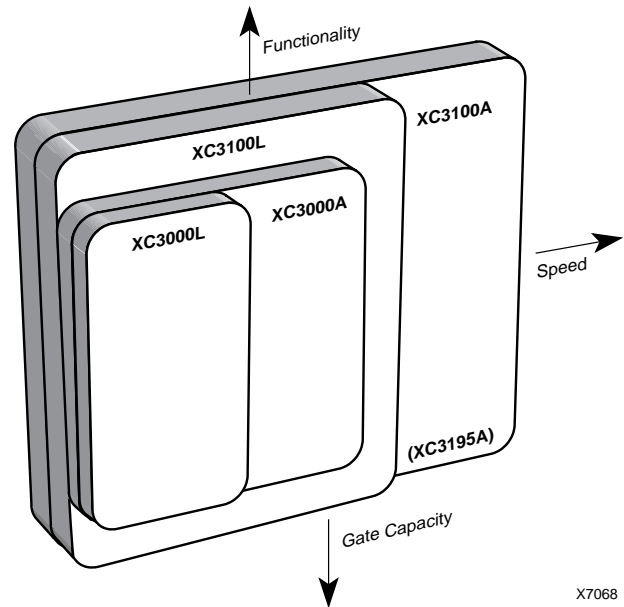
The XC3000A and XC3000L families have additional interconnect resources to drive the I-inputs of TBUFs driving horizontal Longlines. The CLB Clock Enable input can be driven from a second vertical Longline. These two additions result in more efficient and faster designs when horizontal Longlines are used for data bussing.

During configuration, the XC3000A and XC3000L devices check the bit-stream format for stop bits in the appropriate positions. Any error terminates the configuration and pulls INIT Low.

When the configuration process is finished and the device starts up in user mode, the first activation of the outputs is automatically slew-rate limited. This feature, called Soft Startup, avoids the potential ground bounce when all out-puts are turned on simultaneously. After start-up, the slew rate of the individual outputs is, as in the XC3000 family, determined by the individual configuration option.

### ***Improvements in the XC3100A and XC3100L Families***

Based on a more advanced CMOS process, the XC3100A and XC3100L families are architecturally-identical, performance-optimized relatives of the XC3000A and XC3000L families. While all families are footprint compatible, the XC3100A family extends achievable system performance beyond 85 MHz.



**Figure 1: XC3000 FPGA Families**



The input-buffer portion of each IOB provides threshold detection to translate external signals applied to the package pin to internal logic levels. The global input-buffer threshold of the IOBs can be programmed to be compatible with either TTL or CMOS levels. The buffered input signal drives the data input of a storage element, which may be configured as either a flip-flop or a latch. The clocking polarity (rising/falling edge-triggered flip-flop, High/Low transparent latch) is programmable for each of the two clock lines on each of the four die edges. Note that a clock line driving a *rising* edge-triggered flip-flop makes any latch driven by the same line on the same edge Low-level transparent and vice versa (*falling* edge, *High* transparent). All Xilinx primitives in the supported schematic-entry packages, however, are positive edge-triggered flip-flops or High transparent latches. When one clock line must drive flip-flops as well as latches, it is necessary to compensate for the difference in clocking polarities with an additional inverter either in the flip-flop clock input or the latch-enable input. I/O storage elements are reset during configuration or by the active-Low chip RESET input. Both direct input (from IOB pin I) and registered input (from IOB pin Q) signals are available for interconnect.

For reliable operation, inputs should have transition times of less than 100 ns and should not be left floating. Floating CMOS input-pin circuits might be at threshold and produce oscillations. This can produce additional power dissipation and system noise. A typical hysteresis of about 300 mV reduces sensitivity to input noise. Each user IOB includes a programmable high-impedance pull-up resistor, which may be selected by the program to provide a constant High for otherwise undriven package pins. Although the Field Programmable Gate Array provides circuitry to provide input protection for electrostatic discharge, normal CMOS handling precautions should be observed.

Flip-flop loop delays for the IOB and logic-block flip-flops are short, providing good performance under asynchronous clock and data conditions. Short loop delays minimize the probability of a metastable condition that can result from assertion of the clock during data transitions. Because of the short-loop-delay characteristic in the Field Programmable Gate Array, the IOB flip-flops can be used to synchronize external signals applied to the device. Once synchronized in the IOB, the signals can be used internally without further consideration of their clock relative timing, except as it applies to the internal logic and routing-path delays.

IOB output buffers provide CMOS-compatible 4-mA source-or-sink drive for high fan-out CMOS or TTL-compatible signal levels (8 mA in the XC3100A family). The network driving IOB pin O becomes the registered or direct data source for the output buffer. The 3-state control signal (IOB) pin T can control output activity. An open-drain output may be obtained by using the same signal for driving the

output and 3-state signal nets so that the buffer output is enabled only for a Low.

Configuration program bits for each IOB control features such as optional output register, logic signal inversion, and 3-state and slew-rate control of the output.

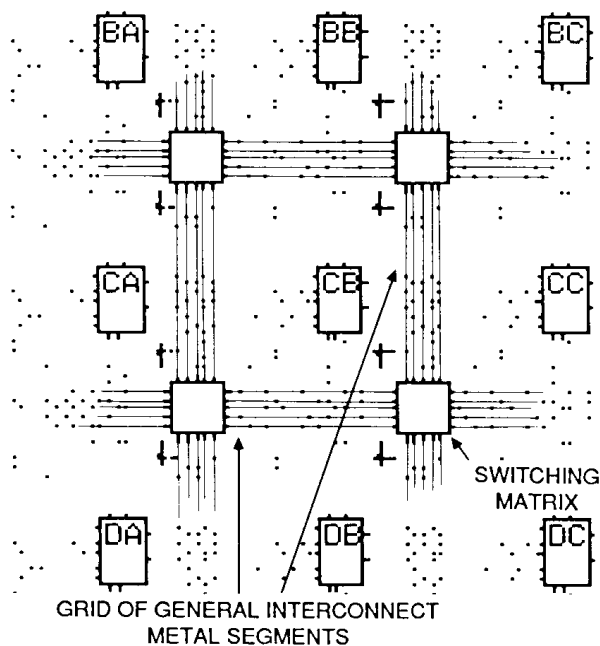
The program-controlled memory cells of [Figure 4](#) control the following options.

- Logic inversion of the output is controlled by one configuration program bit per IOB.
- Logic 3-state control of each IOB output buffer is determined by the states of configuration program bits that turn the buffer on, or off, or select the output buffer 3-state control interconnection (IOB pin T). When this IOB output control signal is High, a logic one, the buffer is disabled and the package pin is high impedance. When this IOB output control signal is Low, a logic zero, the buffer is enabled and the package pin is active. Inversion of the buffer 3-state control-logic sense (output enable) is controlled by an additional configuration program bit.
- Direct or registered output is selectable for each IOB. The register uses a positive-edge, clocked flip-flop. The clock source may be supplied (IOB pin OK) by either of two metal lines available along each die edge. Each of these lines is driven by an invertible buffer.
- Increased output transition speed can be selected to improve critical timing. Slower transitions reduce capacitive-load peak currents of non-critical outputs and minimize system noise.
- An internal high-impedance pull-up resistor (active by default) prevents unconnected inputs from floating.

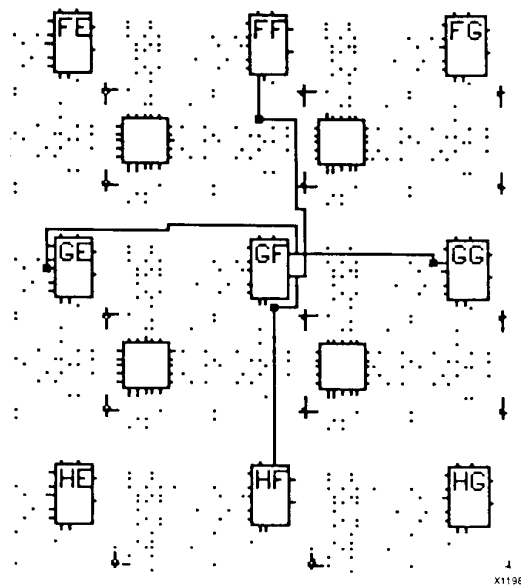
Unlike the original XC3000 series, the XC3000A, XC3000L, XC3100A, and XC3100L families include the Soft Startup feature. When the configuration process is finished and the device starts up in user mode, the first activation of the outputs is automatically slew-rate limited. This feature avoids potential ground bounce when all outputs are turned on simultaneously. After start-up, the slew rate of the individual outputs is determined by the individual configuration option.

### Summary of I/O Options

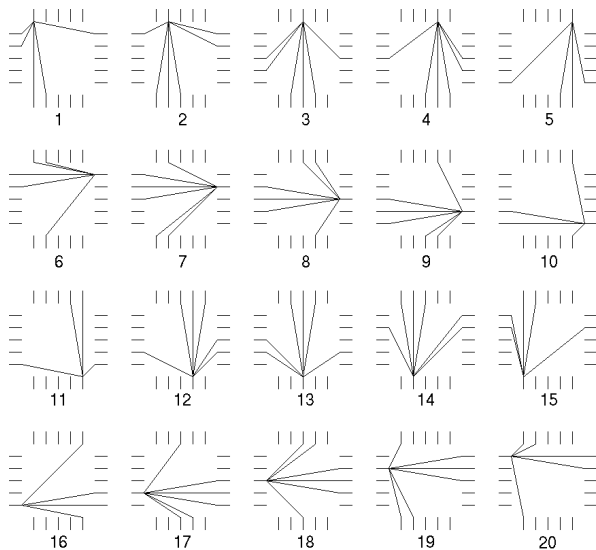
- Inputs
  - Direct
  - Flip-flop/latch
  - CMOS/TTL threshold (chip inputs)
  - Pull-up resistor/open circuit
- Outputs
  - Direct/registered
  - Inverted/not
  - 3-state/on/off
  - Full speed/slew limited
  - 3-state/output enable (inverse)



**Figure 10: FPGA General-Purpose Interconnect.**  
Composed of a grid of metal segments that may be inter-connected through switch matrices to form networks for CLB and IOB inputs and outputs.

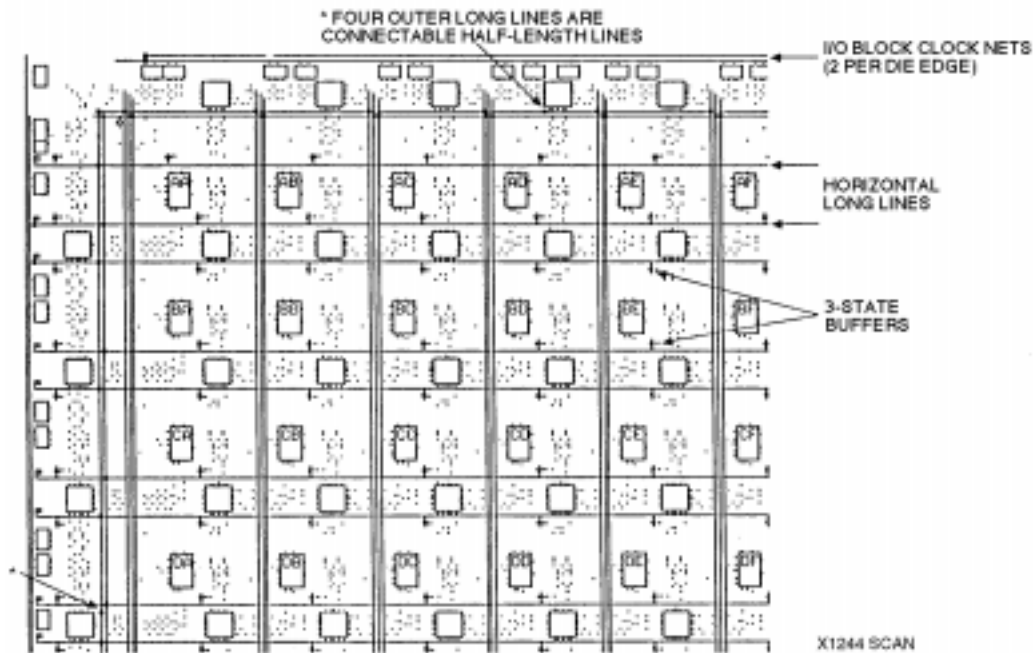


**Figure 12: CLB X and Y Outputs.**  
The X and Y outputs of each CLB have single contact, direct access to inputs of adjacent CLBs

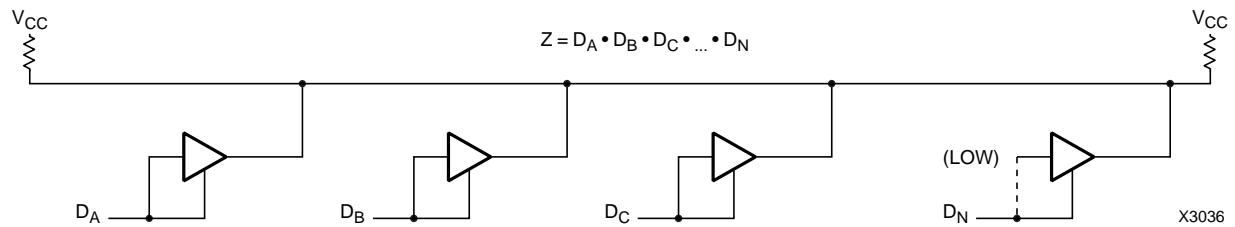


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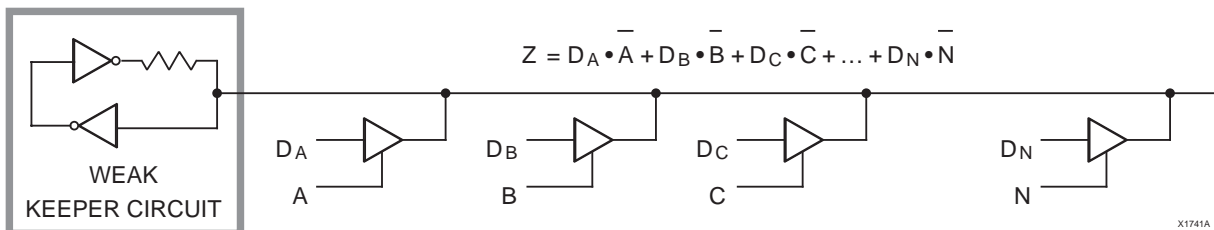
**Figure 11: Switch Matrix Interconnection Options for Each Pin.**  
Switch matrices on the edges are different.



**Figure 15: Programmable Interconnection of Longlines.** This is provided at the edges of the routing area. Three-state buffers allow the use of horizontal Longlines to form on-chip wired AND and multiplexed buses. The left two non-clock vertical Longlines per column (except XC3020A) and the outer perimeter Longlines may be programmed as connectable half-length lines.



**Figure 16: 3-State Buffers Implement a Wired-AND Function.** When all the buffer 3-state lines are High, (high impedance), the pull-up resistor(s) provide the High output. The buffer inputs are driven by the control signals or a Low.



**Figure 17: 3-State Buffers Implement a Multiplexer.** The selection is accomplished by the buffer 3-state signal.

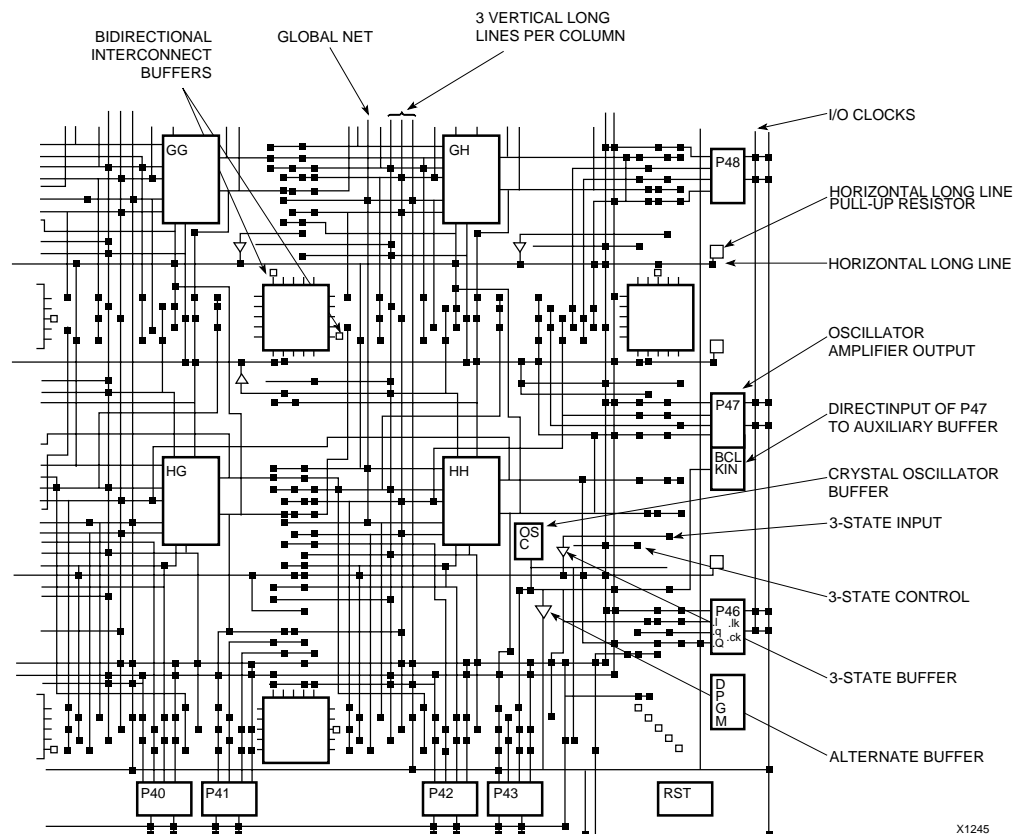
A buffer in the upper left corner of the FPGA chip drives a global net which is available to all K inputs of logic blocks. Using the global buffer for a clock signal provides a skew-free, high fan-out, synchronized clock for use at any or all of the IOBs and CLBs. Configuration bits for the K input to each logic block can select this global line or another routing resource as the clock source for its flip-flops. This net may also be programmed to drive the die edge clock lines for IOB use. An enhanced speed, CMOS threshold, direct access to this buffer is available at the second pad from the top of the left die edge.

A buffer in the lower right corner of the array drives a horizontal Longline that can drive programmed connections to a vertical Longline in each interconnection column. This alternate buffer also has low skew and high fan-out. The network formed by this alternate buffer's Longlines can be selected to drive the K inputs of the CLBs. CMOS threshold, high speed access to this buffer is available from the third pad from the bottom of the right die edge.

### Internal Busses

A pair of 3-state buffers, located adjacent to each CLB, permits logic to drive the horizontal Longlines. Logic operation

of the 3-state buffer controls allows them to implement wide multiplexing functions. Any 3-state buffer input can be selected as drive for the horizontal long-line bus by applying a Low logic level on its 3-state control line. See [Figure 16](#). The user is required to avoid contention which can result from multiple drivers with opposing logic levels. Control of the 3-state input by the same signal that drives the buffer input, creates an open-drain wired-AND function. A logic High on both buffer inputs creates a high impedance, which represents no contention. A logic Low enables the buffer to drive the Longline Low. See [Figure 17](#). Pull-up resistors are available at each end of the Longline to provide a High output when all connected buffers are non-conducting. This forms fast, wide gating functions. When data drives the inputs, and separate signals drive the 3-state control lines, these buffers form multiplexers (3-state buses). In this case, care must be used to prevent contention through multiple active buffers of conflicting levels on a common line. Each horizontal Longline is also driven by a weak keeper circuit that prevents undefined floating levels by maintaining the previous logic level when the line is not driven by an active buffer or a pull-up resistor. [Figure 18](#) shows 3-state buffers, Longlines and pull-up resistors.



**Figure 18: Design Editor.**

An extra large view of possible interconnections in the lower right corner of the XC3020A.



### **RESET Timing**

As with DONE timing, the timing of the release of the internal reset can be controlled to occur either a CCLK cycle before, or after, the outputs going active. See [Figure 22](#). This reset keeps all user programmable flip-flops and latches in a zero state during configuration.

### **Crystal Oscillator Division**

A selection allows the user to incorporate a dedicated divide-by-two flip-flop between the crystal oscillator and the alternate clock line. This guarantees a symmetrical clock signal. Although the frequency stability of a crystal oscillator is very good, the symmetry of its waveform can be affected by bias or feedback drive.

### **Bitstream Error Checking**

**Bitstream error checking** protects against erroneous configuration.

Each Xilinx FPGA bitstream consists of a 40-bit preamble, followed by a device-specific number of data frames. The number of bits per frame is also device-specific; however, each frame ends with three stop bits (111) followed by a start bit for the next frame (0).

All devices in all XC3000 families start reading in a new frame when they find the first 0 after the end of the previous frame. An original XC3000 device does not check for the correct stop bits, but XC3000A, XC3100A, XC3000L, and XC3100L devices check that the last three bits of any frame are actually 111.

Under normal circumstances, all these FPGAs behave the same way; however, if the bitstream is corrupted, an XC3000 device will always start a new frame as soon as it finds the first 0 after the end of the previous frame, even if the data is completely wrong or out-of-sync. Given sufficient zeros in the data stream, the device will also go Done,

but with incorrect configuration and the possibility of internal contention.

An XC3000A/XC3100A/XC3000L/XC3100L device starts any new frame only if the three preceding bits are all ones. If this check fails, it pulls INIT Low and stops the internal configuration, although the Master CCLK keeps running. The user must then start a new configuration by applying a  $>6\ \mu\text{s}$  Low level on RESET.

This simple check does not protect against random bit errors, but it offers almost 100 percent protection against erroneous configuration files, defective configuration data sources, synchronization errors between configuration source and FPGA, or PC-board level defects, such as broken lines or solder-bridges.

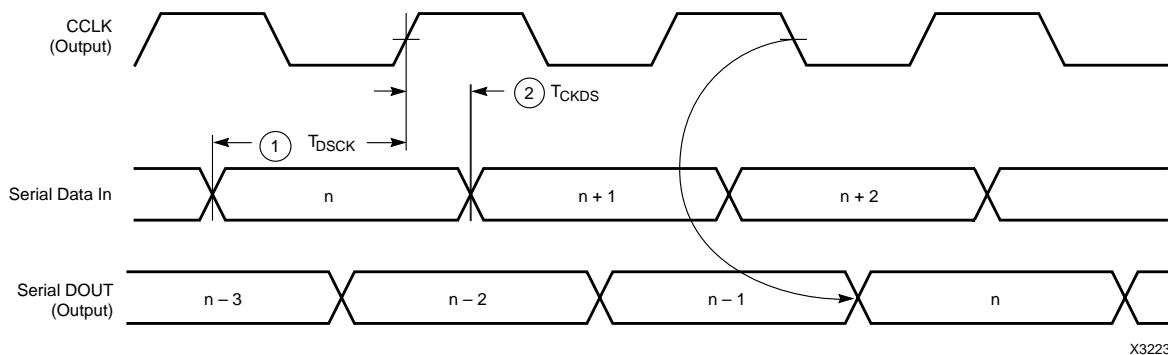
### **Reset Spike Protection**

A separate modification slows down the RESET input before configuration by using a two-stage shift register driven from the internal clock. It tolerates submicrosecond High spikes on RESET before configuration. The XC3000 master can be connected like an XC4000 master, but with its RESET input used instead of INIT. (On XC3000, INIT is output only).

### **Soft Start-up**

After configuration, the outputs of all FPGAs in a daisy-chain become active simultaneously, as a result of the same CCLK edge. In the original XC3000/3100 devices, each output becomes active in either fast or slew-rate limited mode, depending on the way it is configured. This can lead to large ground-bounce signals. In XC3000A, XC3000L, XC3100A, and XC3100L devices, all outputs become active first in slew-rate limited mode, reducing the ground bounce. After this soft start-up, each individual output slew rate is again controlled by the respective configuration bit.



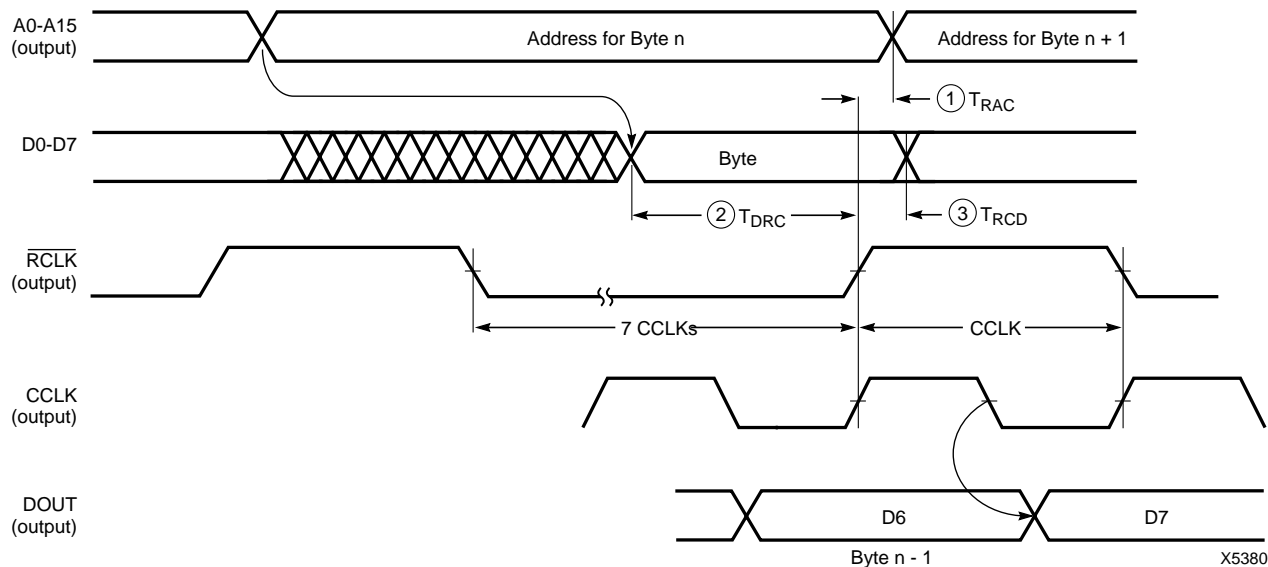


X3223

	Description		Symbol	Min	Max	Units
CCLK	Data In setup	1	$T_{DSCK}$	60		ns
	Data In hold	2	$C_{KDS}$	0		ns

- Notes:
1. At power-up,  $V_{CC}$  must rise from 2.0 V to  $V_{CC}$  min in less than 25 ms. If this is not possible, configuration can be delayed by holding RESET Low until  $V_{CC}$  has reached 4.0 V (2.5 V for the XC3000L). A very long  $V_{CC}$  rise time of >100 ms, or a non-monotonically rising  $V_{CC}$  may require >6- $\mu$ s High level on RESET, followed by a >6- $\mu$ s Low level on RESET and D/ $\bar{P}$  after  $V_{CC}$  has reached 4.0 V (2.5 V for the XC3000L).
  2. Configuration can be controlled by holding RESET Low with or until after the  $\overline{INIT}$  of all daisy-chain slave-mode devices is High.
  3. Master-serial-mode timing is based on slave-mode testing.

**Figure 24: Master Serial Mode Programming Switching Characteristics**



	Description	Symbol	Min	Max	Units
RCLK	To address valid	1 T <sub>RAC</sub>	0	200	ns
	To data setup	2 T <sub>DRC</sub>	60		ns
	To data hold	3 T <sub>RCD</sub>	0		ns
	RCLK High	T <sub>RCH</sub>	600		ns
	RCLK Low	T <sub>RCL</sub>	4.0		μs

- Notes:
1. At power-up, V<sub>CC</sub> must rise from 2.0 V to V<sub>CC</sub> min in less than 25 ms. If this is not possible, configuration can be delayed by holding RESET Low until V<sub>CC</sub> has reached 4.0 V (2.5 V for the XC3000L). A very long V<sub>CC</sub> rise time of >100 ms, or a non-monotonically rising V<sub>CC</sub> may require a >6-μs High level on RESET, followed by a >6-μs Low level on RESET and D/P after V<sub>CC</sub> has reached 4.0 V (2.5 V for the XC3000L).
  2. Configuration can be controlled by holding RESET Low with or until after the INIT of all daisy-chain slave-mode devices is High.

*This timing diagram shows that the EPROM requirements are extremely relaxed:  
EPROM access time can be longer than 4000 ns. EPROM data output has no hold time requirements.*

Figure 26: Master Parallel Mode Programming Switching Characteristics

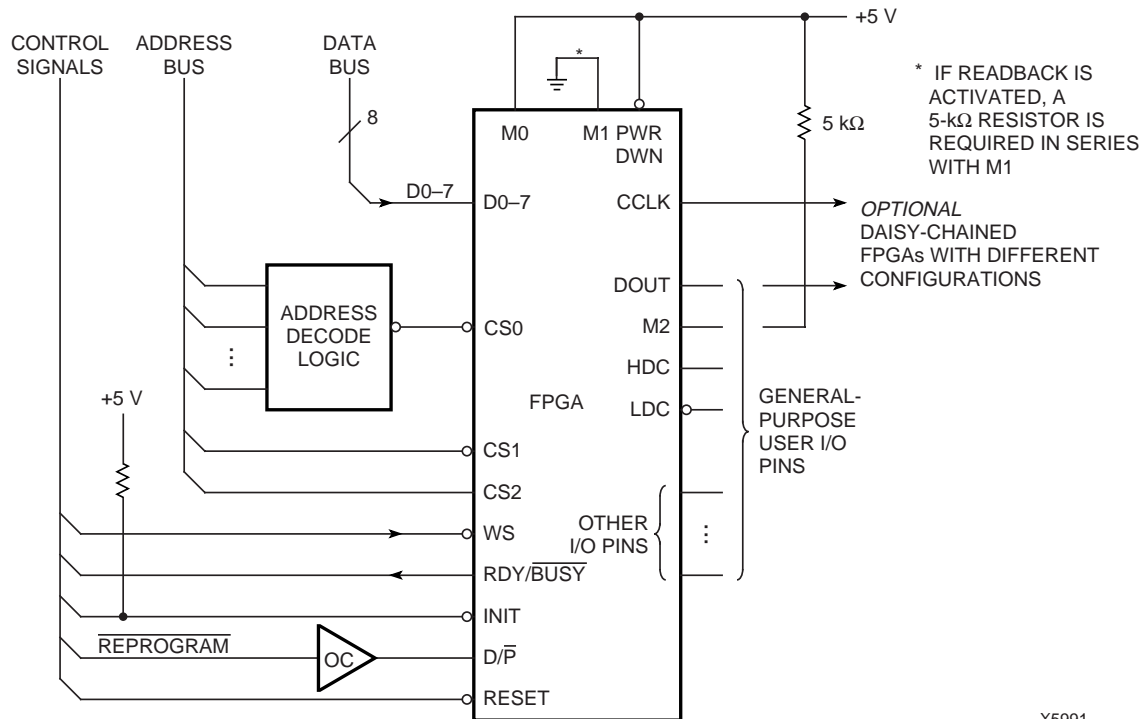
### Peripheral Mode

Peripheral mode uses the trailing edge of the logic AND condition of the  $\overline{CS0}$ ,  $\overline{CS1}$ ,  $\overline{CS2}$ , and  $\overline{WS}$  inputs to accept byte-wide data from a microprocessor bus. In the lead FPGA, this data is loaded into a double-buffered UART-like parallel-to-serial converter and is serially shifted into the internal logic. The lead FPGA presents the preamble data (and all data that overflows the lead device) on the DOUT pin.

The Ready/Busy output from the lead device acts as a handshake signal to the microprocessor.  $\overline{RDY/BUSY}$  goes Low when a byte has been received, and goes High again

when the byte-wide input buffer has transferred its information into the shift register, and the buffer is ready to receive new data. The length of the  $\overline{BUSY}$  signal depends on the activity in the UART. If the shift register had been empty when the new byte was received, the  $\overline{BUSY}$  signal lasts for only two CCLK periods. If the shift register was still full when the new byte was received, the  $\overline{BUSY}$  signal can be as long as nine CCLK periods.

Note that after the last byte has been entered, only seven of its bits are shifted out. CCLK remains High with DOUT equal to bit 6 (the next-to-last bit) of the last byte entered.



**Figure 27: Peripheral Mode Circuit Diagram**

### Device Performance

The XC3000 families of FPGAs can achieve very high performance. This is the result of

- A sub-micron manufacturing process, developed and continuously being enhanced for the production of state-of-the-art CMOS SRAMs.
- Careful optimization of transistor geometries, circuit design, and lay-out, based on years of experience with the XC3000 family.
- A look-up table based, coarse-grained architecture that can collapse multiple-layer combinatorial logic into a single function generator. One CLB can implement up to four layers of conventional logic in as little as 1.5 ns.

Actual system performance is determined by the timing of critical paths, including the delay through the combinatorial and sequential logic elements within CLBs and IOBs, plus the delay in the interconnect routing. The AC-timing specifications state the worst-case timing parameters for the various logic resources available in the XC3000-families architecture. **Figure 31** shows a variety of elements involved in determining system performance.

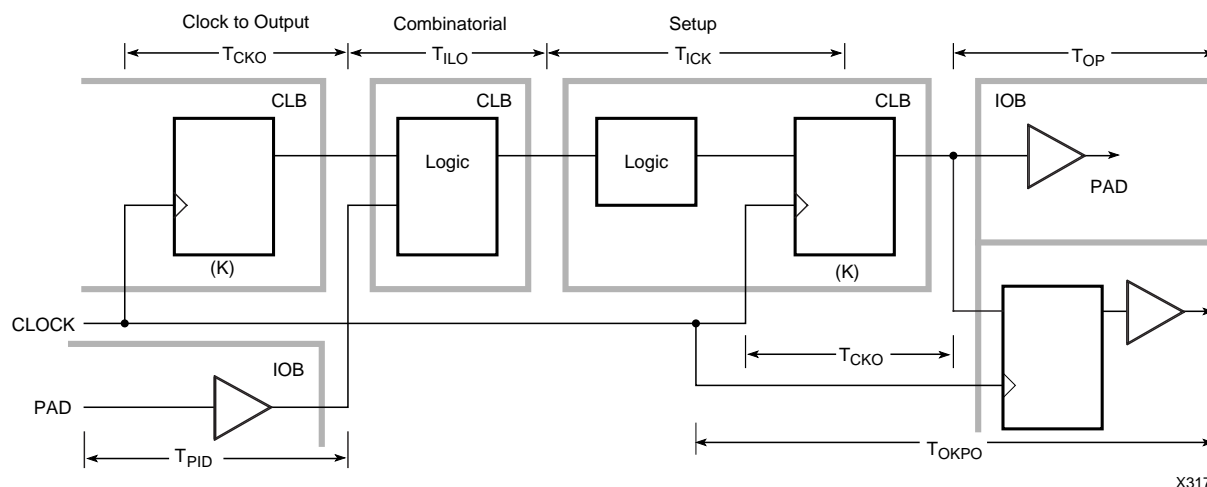
Logic block performance is expressed as the propagation time from the interconnect point at the input to the block to the output of the block in the interconnect area. Since combinatorial logic is implemented with a memory lookup table within a CLB, the combinatorial delay through the CLB, called  $T_{ILO}$ , is always the same, regardless of the function being implemented. For the combinatorial logic function driving the data input of the storage element, the critical timing is data set-up relative to the clock edge provided to the flip-flop element. The delay from the clock source to the output of the logic block is critical in the timing signals pro-

duced by storage elements. Loading of a logic-block output is limited only by the resulting propagation delay of the larger interconnect network. Speed performance of the logic block is a function of supply voltage and temperature. See **Figure 32**.

Interconnect performance depends on the routing resources used to implement the signal path. Direct interconnects to the neighboring CLB provide an extremely fast path. Local interconnects go through switch matrices (magic boxes) and suffer an RC delay, equal to the resistance of the pass transistor multiplied by the capacitance of the driven metal line. Longlines carry the signal across the length or breadth of the chip with only one access delay. Generous on-chip signal buffering makes performance relatively insensitive to signal fan-out; increasing fan-out from 1 to 8 changes the CLB delay by only 10%. Clocks can be distributed with two low-skew clock distribution networks.

The tools in the Development System used to place and route a design in an XC3000 FPGA automatically calculate the actual maximum worst-case delays along each signal path. This timing information can be back-annotated to the design's netlist for use in timing simulation or examined with, a static timing analyzer.

Actual system performance is applications dependent. The maximum clock rate that can be used in a system is determined by the critical path delays within that system. These delays are combinations of incremental logic and routing delays, and vary from design to design. In a synchronous system, the maximum clock rate depends on the number of combinatorial logic layers between re-synchronizing flip-flops. **Figure 33** shows the achievable clock rate as a function of the number of CLB layers.



X3178

**Figure 31: Primary Block Speed Factors.** Actual timing is a function of various block factors combined with routing factors. Overall performance can be evaluated with the timing calculator or by an optional simulation.

### XC3000L Absolute Maximum Ratings

Symbol	Description		Units
$V_{CC}$	Supply voltage relative to GND	-0.5 to +7.0	V
$V_{IN}$	Input voltage with respect to GND	-0.5 to $V_{CC} + 0.5$	V
$V_{TS}$	Voltage applied to 3-state output	-0.5 to $V_{CC} + 0.5$	V
$T_{STG}$	Storage temperature (ambient)	-65 to +150	°C
$T_{SOL}$	Maximum soldering temperature (10 s @ 1/16 in.)	+260	°C
$T_J$	Junction temperature plastic	+125	°C
	Junction temperature ceramic	+150	°C

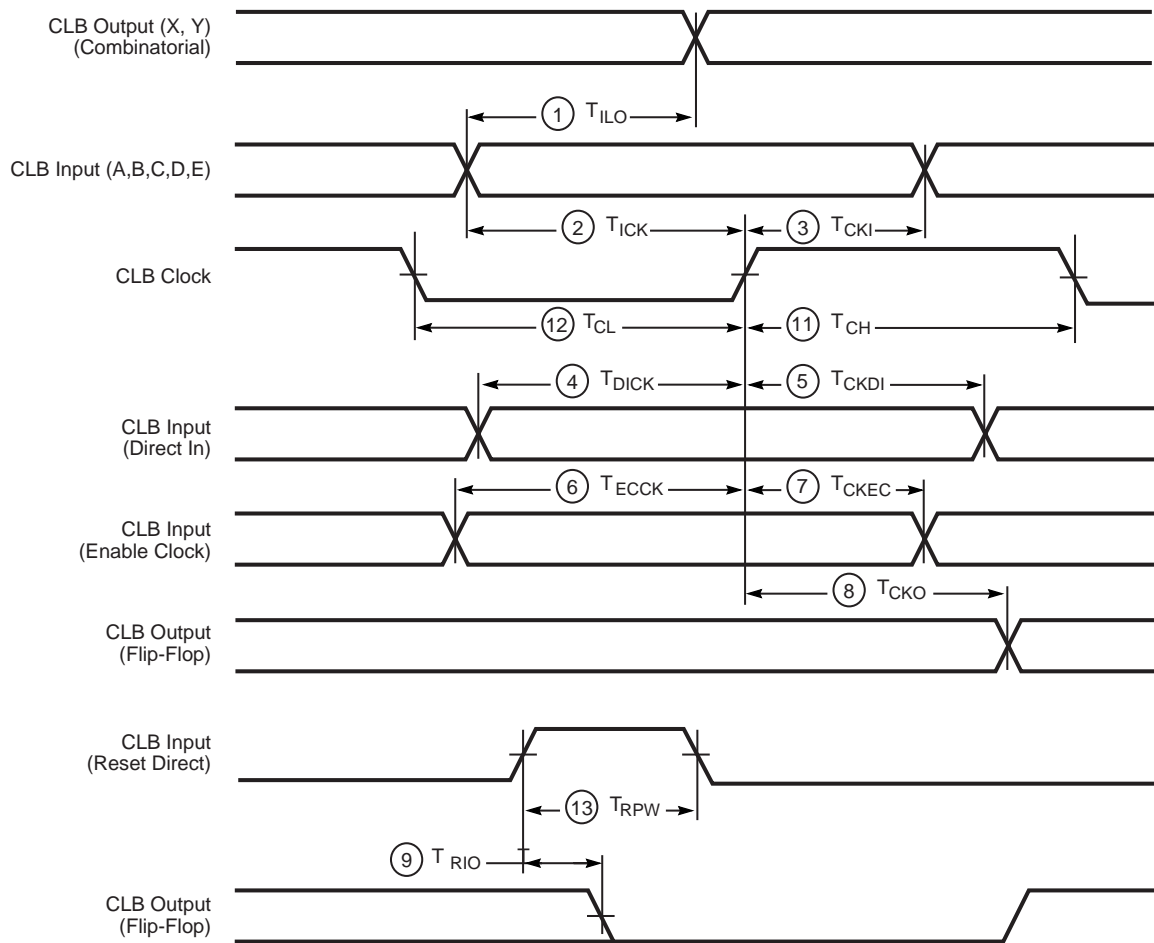
**Note:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

### XC3000L Global Buffer Switching Characteristics Guidelines

		Speed Grade	-8	
Description	Symbol	Max	Units	
Global and Alternate Clock Distribution <sup>1</sup> Either: <b>Normal</b> IOB input pad through clock buffer to any CLB or IOB clock input Or: <b>Fast</b> (CMOS only) input pad through clock buffer to any CLB or IOB clock input	$T_{PID}$	9.0	ns	
	$T_{PIDC}$	7.0	ns	
<b>TBUF</b> driving a Horizontal Longline (L.L.) <sup>1</sup> I to L.L. while T is Low (buffer active) $T \downarrow$ to L.L. active and valid with single pull-up resistor $T \uparrow$ to L.L. High with single pull-up resistor	$T_{IO}$	5.0	ns	
	$T_{ON}$	12.0	ns	
	$T_{PUS}$	24.0	ns	
<b>BIDI</b> Bidirectional buffer delay	$T_{BIDI}$	2.0	ns	

**Notes:** 1. Timing is based on the XC3042A, for other devices see timing calculator.  
2. The use of two pull-up resistors per Longline, available on other XC3000 devices, is not a valid option for XC3000L devices.

XC3000L CLB Switching Characteristics Guidelines (continued)



X5424

### XC3000L IOB Switching Characteristics Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Since many internal timing parameters cannot be measured directly, they are derived from benchmark timing patterns. The following guidelines reflect worst-case values over the recommended operating conditions. For more detailed, more precise, and more up-to-date timing information, use the values provided by the timing calculator and used in the simulator.

Description	Speed Grade		-8		Units
	Symbol		Min	Max	
Propagation Delays (Input)					
Pad to Direct In (I)	3	$T_{PID}$		5.0	ns
Pad to Registered In (Q) with latch transparent		$T_{PTG}$		24.0	ns
Clock (IK) to Registered In (Q)	4	$T_{IKRI}$		6.0	ns
Set-up Time (Input)					
Pad to Clock (IK) set-up time	1	$T_{PICK}$	22.0		ns
Propagation Delays (Output)					
Clock (OK) to Pad (fast)	7	$T_{OKPO}$		12.0	ns
same (slew rate limited)	7	$T_{OKPO}$		28.0	ns
Output (O) to Pad (fast)	10	$T_{OPF}$		9.0	ns
same (slew-rate limited)	10	$T_{OPS}$		25.0	ns
3-state to Pad begin hi-Z (fast)	9	$T_{TSHZ}$		12.0	ns
same (slew-rate limited)	9	$T_{TSHZ}$		28.0	ns
3-state to Pad active and valid (fast)	8	$T_{TSOIN}$		16.0	ns
same (slew -rate limited)	8	$T_{TSOIN}$		32.0	ns
Set-up and Hold Times (Output)					
Output (O) to clock (OK) set-up time	5	$T_{OOK}$	12.0		ns
Output (O) to clock (OK) hold time	6	$T_{OKO}$	0		ns
Clock					
Clock High time	11	$T_{IOH}$	5.0		ns
Clock Low time	12	$T_{IOL}$	5.0		ns
Max. flip-flop toggle rate		$F_{CLK}$	80.0		MHz
Global Reset Delays (based on XC3042L)					
$\overline{RESET}$ Pad to Registered In (Q)	13	$T_{RRI}$		25.0	ns
$\overline{RESET}$ Pad to output pad (fast)	15	$T_{RPO}$		35.0	ns
(slew-rate limited)	15	$T_{RPO}$		51.0	ns

- Notes:**
1. Timing is measured at pin threshold, with 50 pF external capacitive loads (incl. test fixture). Typical slew rate limited output rise/fall times are approximately four times longer.
  2. Voltage levels of unused (bonded and unbonded) pads must be valid logic levels. Each can be configured with the internal pull-up resistor or alternatively configured as a driven output or driven from an external source.
  3. Input pad set-up time is specified with respect to the internal clock (ik). In order to calculate system set-up time, subtract clock delay (pad to ik) from the input pad set-up time value. Input pad holdtime with respect to the internal clock (ik) is negative. This means that pad level changes immediately before the internal clock edge (ik) will not be recognized.
  4.  $T_{PID}$ ,  $T_{PTG}$ , and  $T_{PICK}$  are 3 ns higher for XTL2 when the pin is configured as a user input.



### XC3100A Switching Characteristics

Xilinx maintains test specifications for each product as controlled documents. To insure the use of the most recently released device performance parameters, please request a copy of the current test-specification revision.

### XC3100A Operating Conditions

Symbol	Description	Min	Max	Units
$V_{CC}$	Supply voltage relative to GND Commercial 0°C to +85°C junction	4.25	5.25	V
	Supply voltage relative to GND Industrial -40°C to +100°C junction	4.5	5.5	V
$V_{IHT}$	High-level input voltage — TTL configuration	2.0	$V_{CC}$	V
$V_{ILT}$	Low-level input voltage — TTL configuration	0	0.8	V
$V_{IHC}$	High-level input voltage — CMOS configuration	70%	100%	$V_{CC}$
$V_{ILC}$	Low-level input voltage — CMOS configuration	0	20%	$V_{CC}$
$T_{IN}$	Input signal transition time		250	ns

**Note:** At junction temperatures above those listed as Operating Conditions, all delay parameters increase by 0.3% per °C.

### XC3100A DC Characteristics Over Operating Conditions

Symbol	Description	Min	Max	Units
$V_{OH}$	High-level output voltage (@ $I_{OH} = -8.0$ mA, $V_{CC}$ min)	3.86		V
$V_{OL}$	Low-level output voltage (@ $I_{OL} = 8.0$ mA, $V_{CC}$ min)		0.40	V
$V_{OH}$	High-level output voltage (@ $I_{OH} = -8.0$ mA, $V_{CC}$ min)	3.76		V
$V_{OL}$	Low-level output voltage (@ $I_{OL} = 8.0$ mA, $V_{CC}$ min)		0.40	V
$V_{CCPD}$	Power-down supply voltage (PWRDWN must be Low)	2.30		V
$I_{CCO}$	Quiescent LCA supply current in addition to $I_{CCPD}^1$		8	mA
	Chip thresholds programmed as CMOS levels		14	mA
	Chip thresholds programmed as TTL levels			
$I_{IL}$	Input Leakage Current	-10	+10	μA
$C_{IN}$	Input capacitance, all packages except PGA175 (sample tested)		10	pF
	All Pins except XTL1 and XTL2		15	pF
	XTL1 and XTL2			
	Input capacitance, PGA 175 (sample tested)		15	pF
	All Pins except XTL1 and XTL2		20	pF
	XTL1 and XTL2			
$I_{RIN}$	Pad pull-up (when selected) @ $V_{IN} = 0$ V <sup>3</sup>	0.02	0.17	mA
$I_{RLL}$	Horizontal Longline pull-up (when selected) @ logic Low	0.20	2.80	mA

- Notes:**
1. With no output current loads, no active input or Longline pull-up resistors, all package pins at  $V_{CC}$  or GND, and the LCA device configured with a tie option.
  2. Total continuous output sink current may not exceed 100 mA per ground pin. The number of ground pins varies from two for the XC3120A in the PC84 package, to eight for the XC3195A in the PQ208 package.
  3. Not tested. Allows an undriven pin to float High. For any other purpose, use an external pull-up.

### XC3100L IOB Switching Characteristics Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Since many internal timing parameters cannot be measured directly, they are derived from benchmark timing patterns. The following guidelines reflect worst-case values over the recommended operating conditions. For more detailed, more precise, and more up-to-date timing information, use the values provided by the timing calculator and used in the simulator.

		Speed Grade	-3		-2		
Description	Symbol		Min	Max	Min	Max	Units
Propagation Delays (Input)							
Pad to Direct In (I)	3	$T_{PID}$		2.2		2.0	ns
Pad to Registered In (Q) with latch (XC3100L) transparent		$T_{PTG}$		11.0		11.0	ns
Clock (IK) to Registered In (Q)	4	$T_{IKRI}$		2.2		1.9	ns
Set-up Time (Input)							
Pad to Clock (IK) set-up time	1	$T_{PICK}$					
XC3142L			9.5		9.0		ns
XC3190L			9.9		9.4		ns
Propagation Delays (Output)							
Clock (OK) to Pad (fast)	7	$T_{OKPO}$		4.4		4.0	ns
same (slew rate limited)	7	$T_{PO}$		10.0		9.7	ns
Output (O) to Pad (fast)	10	$T_{OPF}$		3.3		3.0	ns
same (slew-rate limited)(XC3100L)	10	$T_{OPF}$		9.0		8.7	ns
3-state to Pad begin hi-Z (fast)	9	$T_{TSHZ}$		5.5		5.0	ns
same (slew-rate limited)	9	$T_{TSHZ}$		5.5		5.0	ns
3-state to Pad active and valid (fast)(XC3100L)	8	$T_{TSOIN}$		9.0		8.5	ns
same (slew -rate limited)	8	$T_{TSOIN}$		15.0		14.2	ns
Set-up and Hold Times (Output)							
Output (O) to clock (OK) set-up time (XC3100L)	5	$T_{OOK}$	4.0		3.6		ns
Output (O) to clock (OK) hold time	6	$T_{OKO}$	0		0		ns
Clock							
Clock High time	11	$T_{IOH}$	1.6		1.3		ns
Clock Low time	12	$T_{IOL}$	1.6		1.3		ns
Export Control Maximum flip-flop toggle rate		$F_{TOG}$	270		325		MHz
Global Reset Delays							
RESET Pad to Registered In (Q)							
(XC3142L)	13	$T_{RRI}$		16.0		16.0	ns
(XC3190L)				21.0		21.0	ns
RESET Pad to output pad (fast)	15	$T_{RPO}$		17.0		17.0	ns
(slew-rate limited)	15	$T_{RPO}$		23.0		23.0	ns
Advance							

- Notes:**
1. Timing is measured at pin threshold, with 50 pF external capacitive loads (incl. test fixture). Typical slew rate limited output rise/fall times are approximately four times longer.
  2. Voltage levels of unused (bonded and unbonded) pads must be valid logic levels. Each can be configured with the internal pull-up resistor or alternatively configured as a driven output or driven from an external source.
  3. Input pad set-up time is specified with respect to the internal clock (IK). In order to calculate system set-up time, subtract clock delay (pad to ik) from the input pad set-up time value. Input pad holdtime with respect to the internal clock (IK) is negative. This means that pad level changes immediately before the internal clock edge (IK) will not be recognized.

# Product Obsolete or Under Obsolescence



## XC3000 Series Field Programmable Gate Arrays

### XC3000 Series 68-Pin PLCC, 84-Pin PLCC and PGA Pinouts

XC3000A, XC3000L, XC3100A, and XC3100L families have identical pinouts

68 PLCC		XC3020A, XC3030A, XC3042A	84 PLCC
XC3030A	XC3020A		
10	10	PWRDN	12
11	11	TCLKIN-I/O	13
12	—	I/O*	14
13	12	I/O	15
14	13	I/O	16
—	—	I/O	17
15	14	I/O	18
16	15	I/O	19
—	16	I/O	20
17	17	I/O	21
18	18	VCC	22
19	19	I/O	23
—	—	I/O	24
20	20	I/O	25
—	21	I/O	26
21	22	I/O	27
22	—	I/O	28
23	23	I/O	29
24	24	I/O	30
25	25	M1-RDATA	31
26	26	M0-RTRIG	32
27	27	M2-I/O	33
28	28	HDC-I/O	34
29	29	I/O	35
30	30	LDC-I/O	36
—	31	I/O	37
—	—	I/O*	38
31	32	I/O	39
32	33	I/O	40
33	—	I/O*	41
34	34	INIT-I/O	42
35	35	GND	43
36	36	I/O	44
37	37	I/O	45
38	38	I/O	46
39	39	I/O	47
—	40	I/O	48
—	41	I/O	49
40	—	I/O*	50
41	—	I/O*	51
42	42	I/O	52
43	43	XTL2(IN)-I/O	53

68 PLCC		XC3020A, XC3030A, XC3042A	84 PLCC
XC3030A	XC3020A		
44	44	RESET	54
45	45	DONE-PG	55
46	46	D7-I/O	56
47	47	XTL1(OUT)-BCLKIN-I/O	57
48	48	D6-I/O	58
—	—	I/O	59
49	49	D5-I/O	60
50	50	CS0-I/O	61
51	51	D4-I/O	62
—	—	I/O	63
52	52	VCC	64
53	53	D3-I/O	65
54	54	CS1-I/O	66
55	55	D2-I/O	67
—	—	I/O	68
—	—	I/O*	69
56	56	D1-I/O	70
57	57	RDY/BUSY-RCLK-I/O	71
58	58	D0-DIN-I/O	72
59	59	DOUT-I/O	73
60	60	CCLK	74
61	61	A0-WS-I/O	75
62	62	A1-CS2-I/O	76
63	63	A2-I/O	77
64	64	A3-I/O	78
—	—	I/O*	79
—	—	I/O*	80
65	65	A15-I/O	81
66	66	A4-I/O	82
67	67	A14-I/O	83
68	68	A5-I/O	84
1	1	GND	1
2	2	A13-I/O	2
3	3	A6-I/O	3
4	4	A12-I/O	4
5	5	A7-I/O	5
—	—	I/O*	6
—	—	I/O*	7
6	6	A11-I/O	8
7	7	A8-I/O	9
8	8	A10-I/O	10
9	9	A9-I/O	11

Unprogrammed IOBs have a default pull-up. This prevents an undefined pad level for unbonded or unused IOBs. Programmed outputs are default slew-rate limited.

This table describes the pinouts of three different chips in three different packages. The pin-description column lists 84 of the 118 pads on the XC3042A (and 84 of the 98 pads on the XC3030A) that are connected to the 84 package pins. Ten pads, indicated by an asterisk, do not exist on the XC3020A, which has 74 pads; therefore the corresponding pins on the 84-pin packages have no connections to an XC3020A. Six pads on the XC3020A and 16 pads on the XC3030A, indicated by a dash (—) in the 68 PLCC column, have no connection to the 68 PLCC, but are connected to the 84-pin packages.

# Product Obsolete or Under Obsolescence

## XC3000 Series Field Programmable Gate Arrays



### XC3000 Series 160-Pin PQFP Pinouts

XC3000A, XC3000L, XC3100A, and XC3100L families have identical pinouts

PQFP Pin Number	XC3064A, XC3090A, XC3195A	PQFP Pin Number	XC3064A, XC3090A, XC3195A	PQFP Pin Number	XC3064A, XC3090A, XC3195A	PQFP Pin Number	XC3064A, XC3090A, XC3195A
1	I/O*	41	GND	81	D7-I/O	121	CCLK
2	I/O*	42	M0-RTRIG	82	XTL1-I/O-BCLKIN	122	VCC
3	I/O*	43	VCC	83	I/O*	123	GND
4	I/O	44	M2-I/O	84	I/O	124	A0-WS-I/O
5	I/O	45	HDC-I/O	85	I/O	125	A1-CS2-I/O
6	I/O	46	I/O	86	D6-I/O	126	I/O
7	I/O	47	I/O	87	I/O	127	I/O
8	I/O	48	I/O	88	I/O	128	A2-I/O
9	I/O	49	LDC-I/O	89	I/O	129	A3-I/O
10	I/O	50	I/O*	90	I/O	130	I/O
11	I/O	51	I/O*	91	I/O	131	I/O
12	I/O	52	I/O	92	D5-I/O	132	A15-I/O
13	I/O	53	I/O	93	CS0-I/O	133	A4-I/O
14	I/O	54	I/O	94	I/O*	134	I/O
15	I/O	55	I/O	95	I/O*	135	I/O
16	I/O	56	I/O	96	I/O	136	A14-I/O
17	I/O	57	I/O	97	I/O	137	A5-I/O
18	I/O	58	I/O	98	D4-I/O	138	I/O*
19	GND	59	INIT-I/O	99	I/O	139	GND
20	VCC	60	VCC	100	VCC	140	VCC
21	I/O*	61	GND	101	GND	141	A13-I/O
22	I/O	62	I/O	102	D3-I/O	142	A6-I/O
23	I/O	63	I/O	103	CS1-I/O	143	I/O*
24	I/O	64	I/O	104	I/O	144	I/O*
25	I/O	65	I/O	105	I/O	145	I/O
26	I/O	66	I/O	106	I/O*	146	I/O
27	I/O	67	I/O	107	I/O*	147	A12-I/O
28	I/O	68	I/O	108	D2-I/O	148	A7-I/O
29	I/O	69	I/O	109	I/O	149	I/O
30	I/O	70	I/O	110	I/O	150	I/O
31	I/O	71	I/O	111	I/O	151	A11-I/O
32	I/O	72	I/O	112	I/O	152	A8-I/O
33	I/O	73	I/O	113	I/O	153	I/O
34	I/O	74	I/O	114	D1-I/O	154	I/O
35	I/O	75	I/O*	115	RDY/BUSY-RCLK-I/O	155	A10-I/O
36	I/O	76	XTL2-I/O	116	I/O	156	A9-I/O
37	I/O	77	GND	117	I/O	157	VCC
38	I/O*	78	RESET	118	I/O*	158	GND
39	I/O*	79	VCC	119	D0-DIN-I/O	159	PWRDWN
40	M1-RDATA	80	DONE/PG	120	DOUT-I/O	160	TCLKIN-I/O

Unprogrammed IOBs have a default pull-up. This prevents an undefined pad level for unbonded or unused IOBs. Programmed IOBs are default slew-rate limited.

\* Indicates unconnected package pins (18) for the XC3064A.

# Product Obsolete or Under Obsolescence

## XC3000 Series Field Programmable Gate Arrays



### XC3195A PQ208 Pinouts

Pin Description	PQ208	Pin Description	PQ208	Pin Description	PQ208	Pin Description	PQ208
A9-I/O	206	D0-DIN-I/O	154	I/O	102	I/O	48
A10-I/O	205	I/O	153	I/O	101	I/O	47
I/O	204	I/O	152	I/O	100	I/O	46
I/O	203	I/O	151	I/O	99	I/O	45
I/O	202	I/O	150	I/O	98	I/O	44
I/O	201	RDY/BUSY-RCLK-I/O	149	I/O	97	I/O	43
A8-I/O	200	D1-I/O	148	I/O	96	I/O	42
A11-I/O	199	I/O	147	I/O	95	I/O	41
I/O	198	I/O	146	I/O	94	I/O	40
I/O	197	I/O	145	I/O	93	I/O	39
I/O	196	I/O	144	I/O	92	I/O	38
I/O	194	I/O	141	I/O	89	I/O	37
A7-I/O	193	I/O	140	I/O	88	I/O	36
A12-I/O	192	I/O	139	I/O	87	I/O	35
I/O	191	D2-I/O	138	I/O	86	I/O	34
I/O	190	I/O	137	I/O	85	I/O	33
I/O	189	I/O	136	I/O	84	I/O	32
I/O	188	I/O	135	I/O	83	I/O	31
I/O	187	I/O	134	I/O	82	I/O	30
I/O	186	CS1-I/O	133	I/O	81	I/O	29
A6-I/O	185	D3-I/O	132	I/O	80	I/O	28
A13-I/O	184	GND	131	GND	79	VCC	27
VCC	183	VCC	130	VCC	78	GND	26
GND	182	I/O	129	INIT	77	I/O	25
I/O	181	D4-I/O	128	I/O	76	I/O	24
I/O	180	I/O	127	I/O	75	I/O	23
A5-I/O	179	I/O	126	I/O	74	I/O	22
A14-I/O	178	I/O	125	I/O	73	I/O	21
I/O	177	I/O	124	I/O	72	I/O	20
I/O	176	CS0-I/O	123	I/O	71	I/O	19
I/O	175	D5-I/O	122	I/O	70	I/O	18
I/O	174	I/O	121	I/O	69	I/O	17
A4-I/O	173	I/O	120	I/O	68	I/O	14
A15-I/O	172	I/O	119	I/O	67	I/O	13
I/O	171	I/O	118	I/O	66	I/O	12
I/O	169	I/O	117	I/O	63	I/O	11
I/O	168	I/O	116	I/O	62	I/O	10
I/O	167	I/O	115	I/O	61	I/O	9
A3-I/O	166	D6-I/O	114	I/O	60	I/O	8
A2-I/O	165	I/O	113	LDC-I/O	59	I/O	7
I/O	164	I/O	112	I/O	58	I/O	6
I/O	163	I/O	111	I/O	57	I/O	5
I/O	162	I/O	110	I/O	56	I/O	4
I/O	161	XTLX1(OUT)BCLKN-I/O	109	HDC-I/O	55	I/O	3
A1-CS2-I/O	160	D7-I/O	108	M2-I/O	54	TCLKIN-I/O	2
A0-WS-I/O	159	D/P	107	VCC	53	PWRDN	1
GND	158	VCC	106	M0-RTIG	52	GND	208
VCC	157	RESET	105	GND	51	VCC	207
CCLK	156	GND	104	M1/RDATA	50		
DOUT-I/O	155	XTL2(IN)-I/O	103	I/O	49		

Unprogrammed IOBs have a default pull-up. This prevents an undefined pad level for unbonded or unused IOBs. Programmed outputs are default slew-rate limited.

In the PQ208 package, pins 15, 16, 64, 65, 90, 91, 142, 143, 170 and 195 are not connected.

\* In PQ208, XC3090A and XC3195A have different pinouts.

# Product Obsolete or Under Obsolescence

## XC3000 Series Field Programmable Gate Arrays



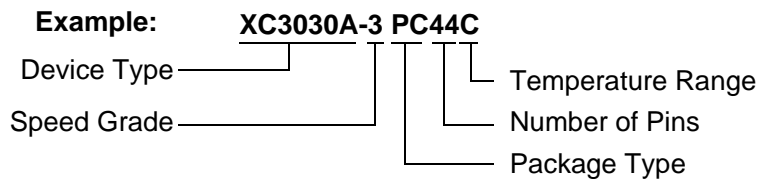
Pins		44	64	68	84		100			132		144	160	175		176	208
Type		Plast. PLCC	Plast. VQFP	Plast. PLCC	Plast. PLCC	Cer. PGA	Plast. PQFP	Plast. TQFP	Plast. VQFP	Plast. PGA	Cer. PGA	Plast. TQFP	Plast. PQFP	Plast. PGA	Cer. PGA	Plast. TQFP	Plast. PQFP
Code		PC44	VQ64	PC68	PC84	PG84	PQ100	TQ100	VQ100	PP132	PG132	TQ144	PQ160	PP175	PG175	TQ176	PQ208
XC3142L					C				C			C					
					C				C			C					
XC3190L					C							C				C	
					C							C				C	

Notes: C = Commercial, T<sub>J</sub> = 0° to +85°C I = Industrial, T<sub>J</sub> = -40° to +100°C

## Number of Available I/O Pins

	Max I/O	Number of Package Pins										
		44	64	68	84	100	132	144	160	175	176	208
XC3020A/XC3120A	64			58	64	64						
XC3030A/XC3130A	80	34	54	58	74	80						
XC3042A/3142A	96				74	82	96	96				
XC2064A/XC3164A	120				70		110	120	120			
XC3090A/XC3190A	144				70			122	138	144	144	144
XC3195A	176				70				138	144		176

## Ordering Information



## Revision History

Date	Revision
11/98	Revised version number to 3.1, removed XC3100A-5 obsolete packages.