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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	100
Number of Logic Elements/Cells	-
Total RAM Bits	22176
Number of I/O	74
Number of Gates	2000
Voltage - Supply	4.75V ~ 5.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	84-LCC (J-Lead)
Supplier Device Package	84-PLCC (29.31x29.31)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc3030a-7pc84c

Flexible routing allows use of common or individual CLB clocking.

The combinatorial-logic portion of the CLB uses a 32 by 1 look-up table to implement Boolean functions. Variables selected from the five logic inputs and two internal block flip-flops are used as table address inputs. The combinatorial propagation delay through the network is independent of the logic function generated and is spike free for single input variable changes. This technique can generate two independent logic functions of up to four variables each as shown in Figure 6a, or a single function of five variables as shown in Figure 6b, or some functions of seven variables as shown in Figure 6c. Figure 7 shows a modulo-8 binary counter with parallel enable. It uses one CLB of each type. The partial functions of six or seven variables are implemented using the input variable (E) to dynamically select between two functions of four different variables. For the two functions of four variables each, the independent results (F and G) may be used as data inputs to either flip-flop or either logic block output. For the single function of five variables and merged functions of six or seven variables, the F and G outputs are identical. Symmetry of the F and G functions and the flip-flops allows the interchange of CLB outputs to optimize routing efficiencies of the networks interconnecting the CLBs and IOBs.

Programmable Interconnect

Programmable-interconnection resources in the Field Programmable Gate Array provide routing paths to connect inputs and outputs of the IOBs and CLBs into logic networks. Interconnections between blocks are composed of a two-layer grid of metal segments. Specially designed pass transistors, each controlled by a configuration bit, form programmable interconnect points (PIPs) and switching matrices used to implement the necessary connections between selected metal segments and block pins. Figure 8 is an example of a routed net. The development system provides automatic routing of these interconnections. Interactive routing is also available for design optimization. The inputs of the CLBs or IOBs are multiplexers which can be programmed to select an input network from the adjacent interconnect segments. ***Since the switch connections to block inputs are unidirectional, as are block outputs, they are usable only for block input connection and not for routing.*** Figure 9 illustrates routing access to logic block input variables, control inputs and block outputs. Three types of metal resources are provided to accommodate various network interconnect requirements.

- General Purpose Interconnect
- Direct Connection
- Longlines (multiplexed busses and wide AND gates)

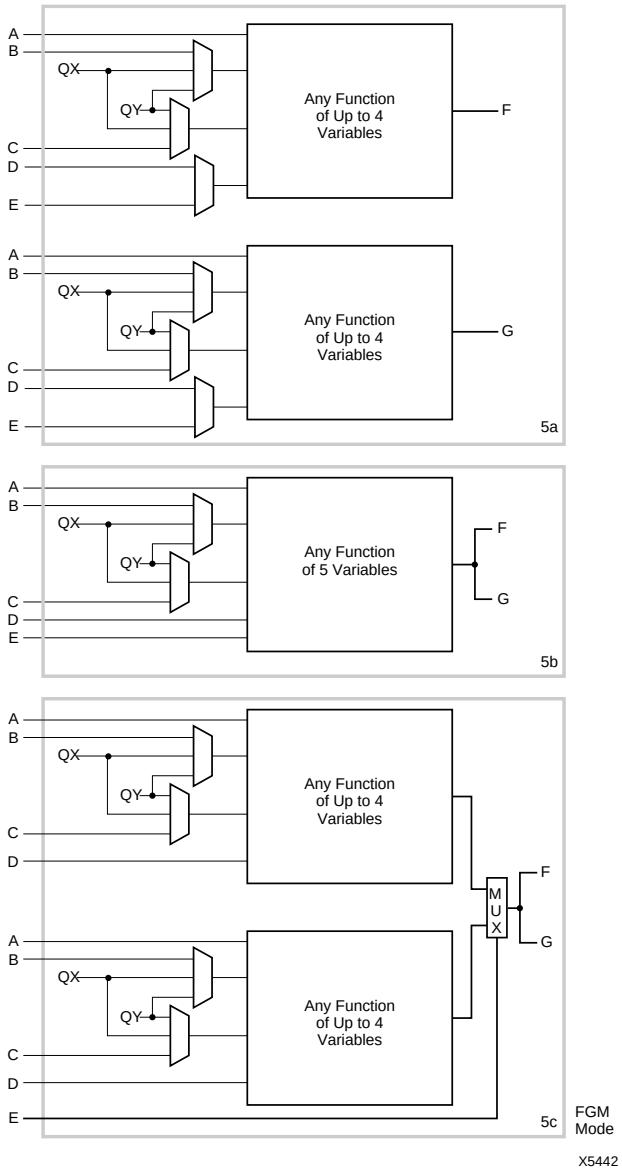

Figure 6: Combinational Logic Options

6a. Combinatorial Logic Option FG generates two functions of four variables each. One variable, A, must be common to both functions. The second and third variable can be any choice of B, C, QX and QY. The fourth variable can be any choice of D or E.

6b. Combinatorial Logic Option F generates any function of five variables: A, D, E and two choices out of B, C, QX, QY.

6c. Combinatorial Logic Option FGM allows variable E to select between two functions of four variables: Both have common inputs A and D and any choice out of B, C, QX and QY for the remaining two variables. Option 3 can then implement some functions of six or seven variables.

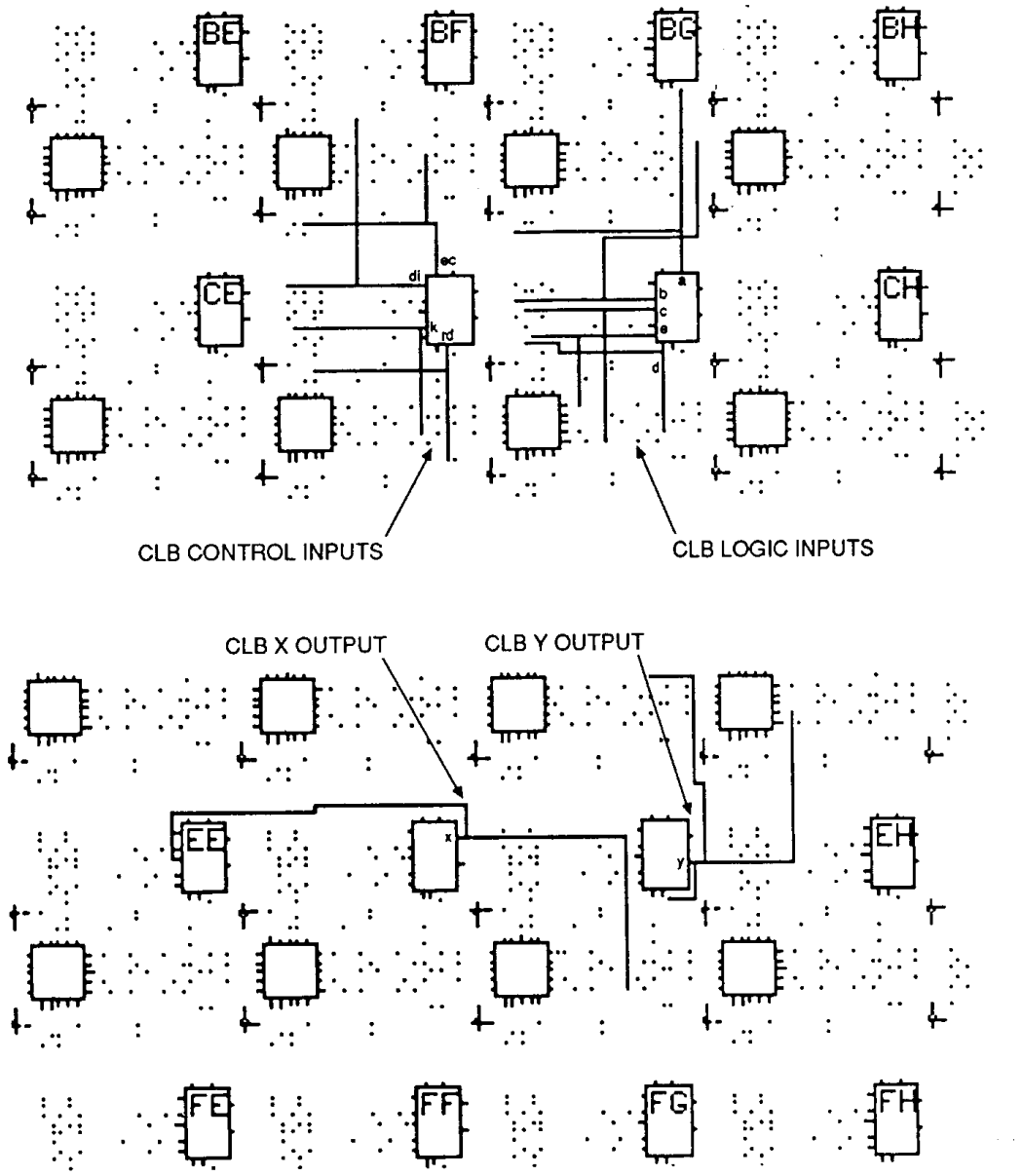

Figure 9: Design Editor Locations of interconnect access, CLB control inputs, logic inputs and outputs. The dot pattern represents the available programmable interconnection points (PIPs).

Some of the interconnect PIPs are directional.

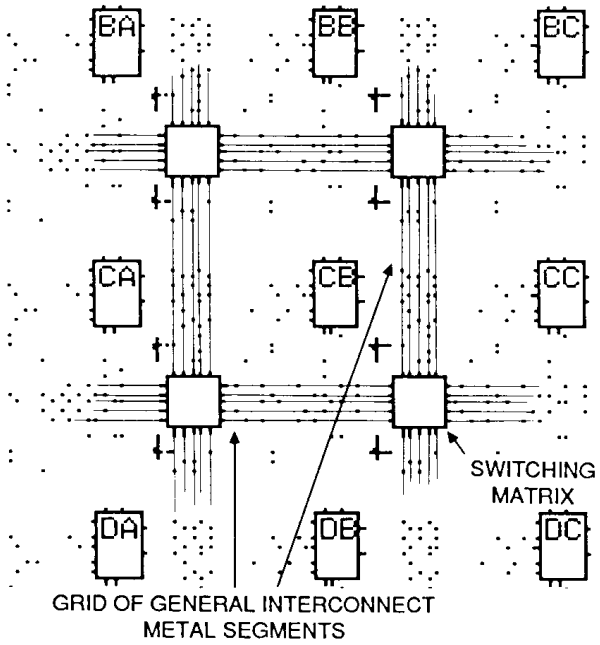

Figure 10: FPGA General-Purpose Interconnect.
Composed of a grid of metal segments that may be interconnected through switch matrices to form networks for CLB and IOB inputs and outputs.

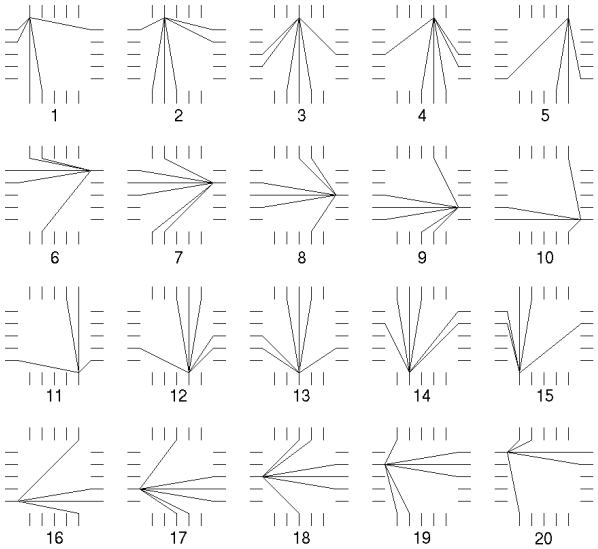

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Figure 11: Switch Matrix Interconnection Options for Each Pin.
Switch matrices on the edges are different.

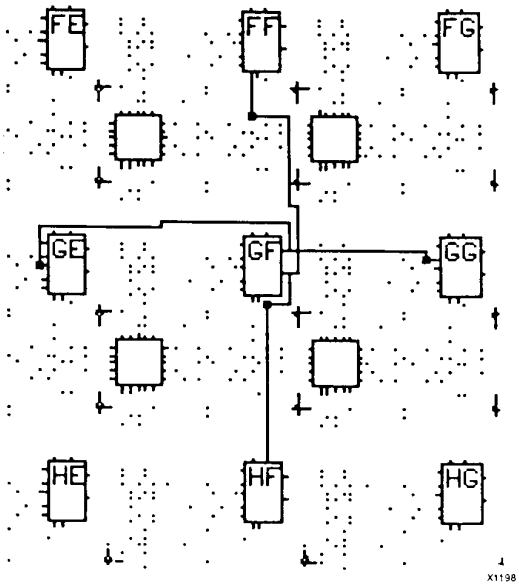

Figure 12: CLB X and Y Outputs.
The X and Y outputs of each CLB have single contact, direct access to inputs of adjacent CLBs

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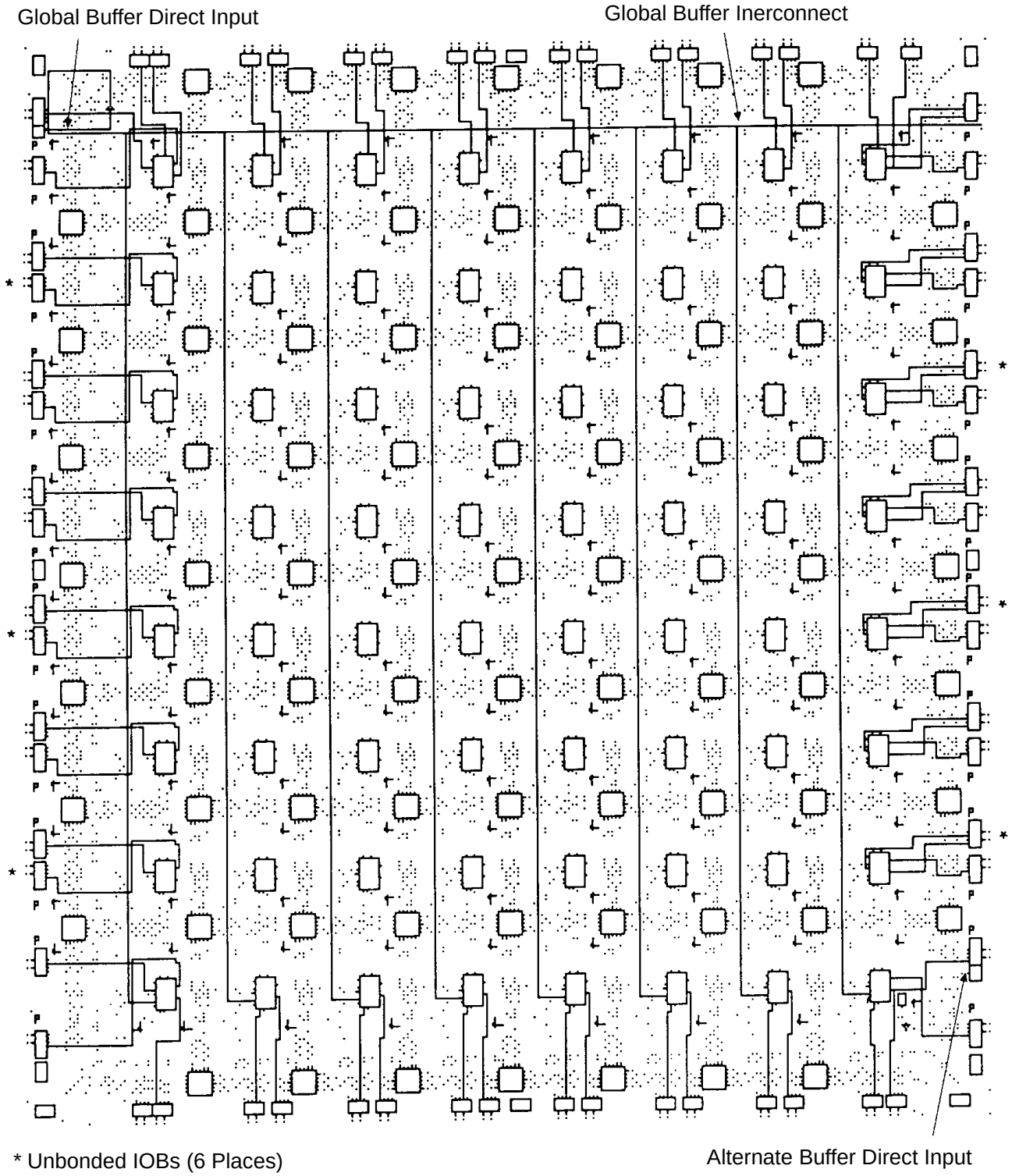
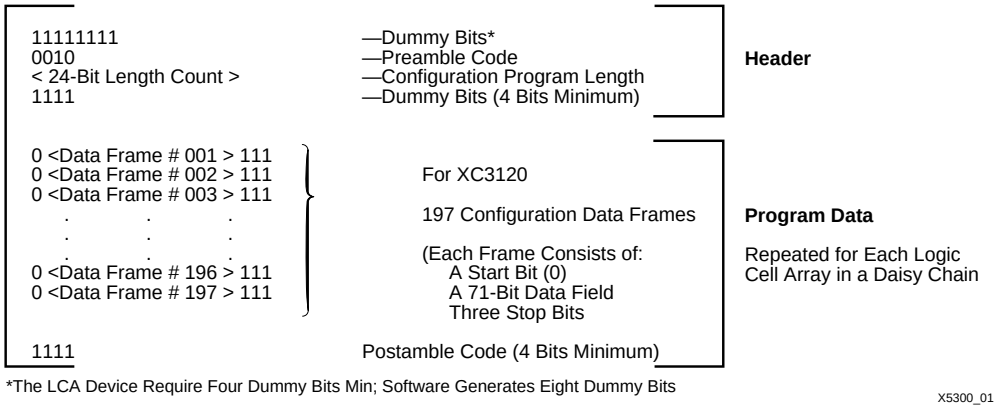


Figure 13: XC3020A Die-Edge IOBs. The XC3020A die-edge IOBs are provided with direct access to adjacent CLBs.

A re-program is initiated.when a configured XC3000 series device senses a High-to-Low transition and subsequent >6 µs Low level on the DONE/PROG package pin, or, if this pin is externally held permanently Low, a High-to-Low transition and subsequent >6 µs Low time on the RESET package pin.

The device returns to the Clear state where the configuration memory is cleared and mode lines re-sampled, as for an aborted configuration. The complete configuration program is cleared and loaded during each configuration program cycle.

Length count control allows a system of multiple Field Programmable Gate Arrays, of assorted sizes, to begin operation in a synchronized fashion. The configuration program generated by the development system begins with a preamble of 111111110010 followed by a 24-bit length count representing the total number of configuration clocks needed to complete loading of the configuration program(s). The data framing is shown in Figure 21. All FPGAs connected in series read and shift preamble and length count in on positive and out on negative configuration clock edges. A device which has received the preamble and length count then presents a High Data Out until it has intercepted the appropriate number of data frames. When the configuration program memory of an FPGA is full and the length count does not yet compare, the device shifts any additional data through, as it did for preamble and length count. When the FPGA configuration memory is full and the length count compares, the device will execute



Device	XC3020A XC3020L XC3120A	XC3030A XC3030L XC3130A	XC3042A XC3042L XC3142A XC3142L	XC3064A XC3064L XC3164A	XC3090A XC3090L XC3190A XC3190L	XC3195A
Gates	1,000 to 1,500	1,500 to 2,000	2,000 to 3,000	3,500 to 4,500	5,000 to 6,000	6,500 to 7,500
CLBs	64	100	144	224	320	484
Row x Col	(8 x 8)	(10 x 10)	(12 x 12)	(16 x 14)	(20 x 16)	(22 x 22)
IOBs	64	80	96	120	144	176
Flip-flops	256	360	480	688	928	1,320
Horizontal Longlines	16	20	24	32	40	44
TBUFs/Horizontal LL	9	11	13	15	17	23
Bits per Frame (including1 start and 3 stop bits)	75	92	108	140	172	188
Frames	197	241	285	329	373	505
Program Data = Bits x Frames + 4 bits (excludes header)	14,779	22,176	30,784	46,064	64,160	94,944
PROM size (bits) = Program Data + 40-bit Header	14,819	22,216	30,824	46,104	64,200	94,984

Figure 21: Internal Configuration Data Structure for an FPGA. This shows the preamble, length count and data frames generated by the Development System.

The Length Count produced by the program = [(40-bit preamble + sum of program data + 1 per daisy chain device) rounded up to multiple of 8] – ($2 \le K \le 4$) where K is a function of DONE and RESET timing selected. An additional 8 is added if roundup increment is less than K. K additional clocks are needed to complete start-up after length count is reached.

Special Configuration Functions

The configuration data includes control over several special functions in addition to the normal user logic functions and interconnect.

- Input thresholds
- Readback disable
- DONE pull-up resistor
- DONE timing
- RESET timing
- Oscillator frequency divided by two

Each of these functions is controlled by configuration data bits which are selected as part of the normal development system bitstream generation process.

Input Thresholds

Prior to the completion of configuration all FPGA input thresholds are TTL compatible. Upon completion of configuration, the input thresholds become either TTL or CMOS compatible as programmed. The use of the TTL threshold option requires some additional supply current for threshold shifting. The exception is the threshold of the PWRDWN input and direct clocks which always have a CMOS input. Prior to the completion of configuration the user I/O pins each have a high impedance pull-up. The configuration program can be used to enable the IOB pull-up resistors in the Operational mode to act either as an input load or to avoid a floating input on an otherwise unused pin.

Readback

The contents of a Field Programmable Gate Array may be read back if it has been programmed with a bitstream in which the Readback option has been enabled. Readback may be used for verification of configuration and as a method of determining the state of internal logic nodes during debugging. There are three options in generating the configuration bitstream.

- “Never” inhibits the Readback capability.
- “One-time,” inhibits Readback after one Readback has been executed to verify the configuration.
- “On-command” allows unrestricted use of Readback.

Readback is accomplished without the use of any of the user I/O pins; only M0, M1 and CCLK are used. The initiation of Readback is produced by a Low to High transition of the M0/RTRIG (Read Trigger) pin. The CCLK input must then be driven by external logic to read back the configuration data. The first three Low-to-High CCLK transitions clock out dummy data. The subsequent Low-to-High CCLK transitions shift the data frame information out on the M1/RDATA (Read Data) pin. Note that the logic polarity is always inverted, a zero in configuration becomes a one in Readback, and vice versa. Note also that each Readback frame has one Start bit (read back as a one) but, unlike in configuration, each Readback frame has only one Stop bit (read back as a zero). The third leading dummy bit mentioned above can be considered the Start bit of the first frame. All data frames must be read back to complete the process and return the Mode Select and CCLK pins to their normal functions.

Readback data includes the current state of each CLB flip-flop, each input flip-flop or latch, and each device pad. These data are imbedded into unused configuration bit positions during Readback. This state information is used by the development system In-Circuit Verifier to provide visibility into the internal operation of the logic while the system is operating. To readback a uniform time-sample of all storage elements, it may be necessary to inhibit the system clock.

Reprogram

To initiate a re-programming cycle, the dual-function pin DONE/PROG must be given a High-to-Low transition. To reduce sensitivity to noise, the input signal is filtered for two cycles of the FPGA internal timing generator. When reprogram begins, the user-programmable I/O output buffers are disabled and high-impedance pull-ups are provided for the package pins. The device returns to the Clear state and clears the configuration memory before it indicates ‘initialized’. Since this Clear operation uses chip-individual internal timing, the master might complete the Clear operation and then start configuration before the slave has completed the Clear operation. To avoid this problem, the slave INIT pins must be AND-wired and used to force a RESET on the master (see Figure 25). Reprogram control is often implemented using an external open-collector driver which pulls DONE/PROG Low. Once a stable request is recognized, the DONE/PROG pin is held Low until the new configuration has been completed. Even if the re-program request is externally held Low beyond the configuration period, the FPGA will begin operation upon completion of configuration.

DONE Pull-up

DONE/PROG is an open-drain I/O pin that indicates the FPGA is in the operational state. An optional internal pull-up resistor can be enabled by the user of the development system. The DONE/PROG pins of multiple FPGAs in a daisy-chain may be connected together to indicate all are DONE or to direct them all to reprogram.

DONE Timing

The timing of the DONE status signal can be controlled by a selection to occur either a CCLK cycle before, or after, the outputs going active. See Figure 22. This facilitates control of external functions such as a PROM enable or holding a system in a wait state.

Configuration Timing

This section describes the configuration modes in detail.

Master Serial Mode

In Master Serial mode, the CCLK output of the lead FPGA drives a Xilinx Serial PROM that feeds the DIN input. Each rising edge of the CCLK output increments the Serial PROM internal address counter. This puts the next data bit on the SPROM data output, connected to the DIN pin. The lead FPGA accepts this data on the subsequent rising CCLK edge.

The lead FPGA then presents the preamble data (and all data that overflows the lead device) on its DOUT pin. There is an internal delay of 1.5 CCLK periods, which means that DOUT changes on the falling CCLK edge, and the next device in the daisy-chain accepts data on the subsequent rising CCLK edge.

The SPROM $\overline{CE}$ input can be driven from either $\overline{LDC}$ or DONE. Using $\overline{LDC}$ avoids potential contention on the DIN pin, if this pin is configured as user-I/O, but $\overline{LDC}$ is then restricted to be a permanently High user output. Using DONE also avoids contention on DIN, provided the early DONE option is invoked.

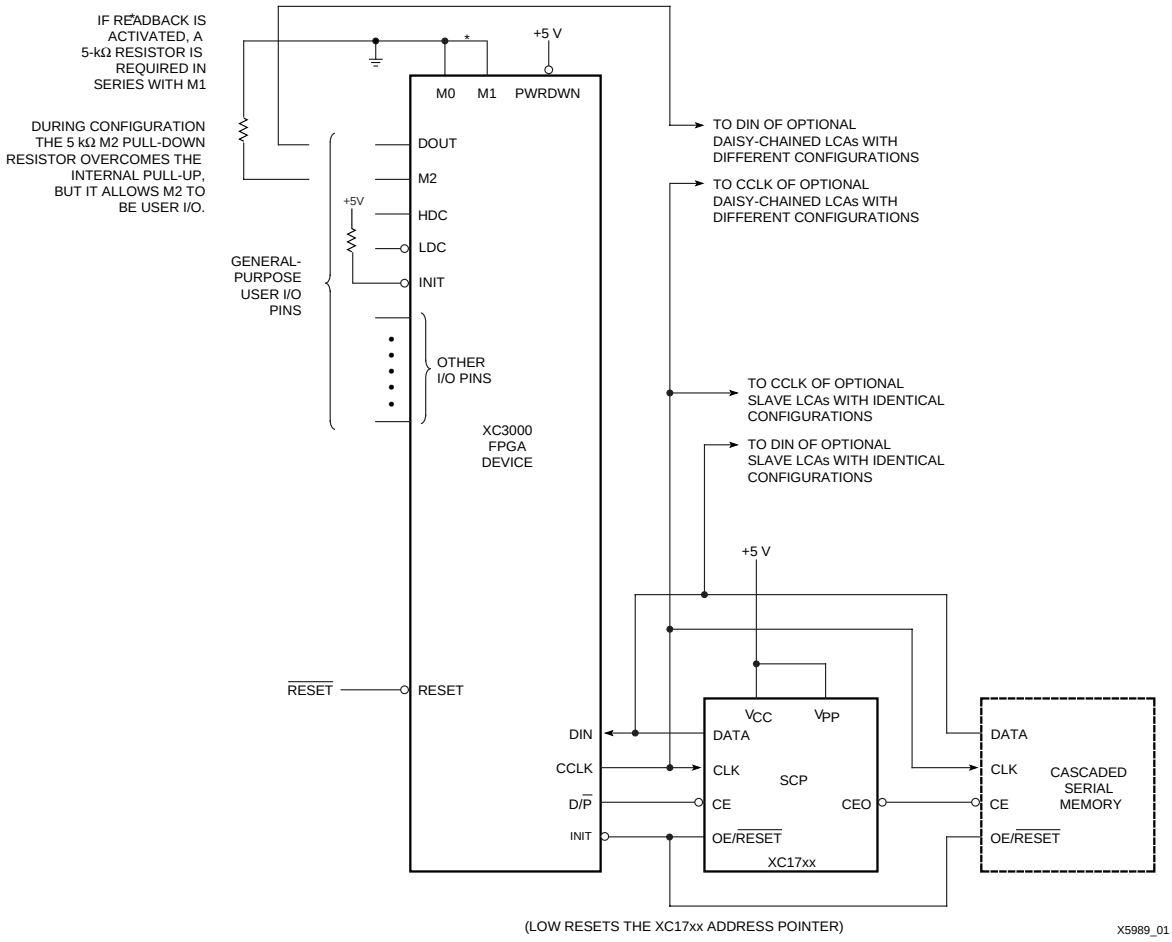


Figure 23: Master Serial Mode Circuit Diagram

Pin Descriptions

Permanently Dedicated Pins

V_{CC}

Two to eight (depending on package type) connections to the positive V supply voltage. All must be connected.

GND

Two to eight (depending on package type) connections to ground. All must be connected.

$\overline{\text{PWRDWN}}$

A Low on this CMOS-compatible input stops all internal activity, but retains configuration. All flip-flops and latches are reset, all outputs are 3-stated, and all inputs are interpreted as High, independent of their actual level. When $\overline{\text{PWDWN}}$ returns High, the FPGA becomes operational with DONE Low for two cycles of the internal 1-MHz clock. Before and during configuration, $\overline{\text{PWRDWN}}$ must be High. If not used, $\overline{\text{PWRDWN}}$ must be tied to V_{CC}.

$\overline{\text{RESET}}$

This is an active Low input which has three functions.

Prior to the start of configuration, a Low input will delay the start of the configuration process. An internal circuit senses the application of power and begins a minimal time-out cycle. When the time-out and $\overline{\text{RESET}}$ are complete, the levels of the M lines are sampled and configuration begins.

If $\overline{\text{RESET}}$ is asserted during a configuration, the FPGA is re-initialized and restarts the configuration at the termination of $\overline{\text{RESET}}$.

If $\overline{\text{RESET}}$ is asserted after configuration is complete, it provides a global asynchronous $\overline{\text{RESET}}$ of all IOB and CLB storage elements of the FPGA.

CCLK

During configuration, Configuration Clock is an output of an FPGA in Master mode or Peripheral mode, but an input in Slave mode. During Readback, CCLK is a clock input for shifting configuration data out of the FPGA.

CCLK drives dynamic circuitry inside the FPGA. The Low time may, therefore, not exceed a few microseconds. When used as an input, CCLK must be “parked High”. An internal pull-up resistor maintains High when the pin is not being driven.

DONE/$\overline{\text{PROG}}$ (D/$\overline{\text{P}}$)

DONE is an open-drain output, configurable with or without an internal pull-up resistor of 2 to 8 k Ω. At the completion of configuration, the FPGA circuitry becomes active in a synchronous order; DONE is programmed to go active High one cycle either before or after the outputs go active.

Once configuration is done, a High-to-Low transition of this pin will cause an initialization of the FPGA and start a reconfiguration.

M0/RTRIG

As Mode 0, this input is sampled on power-on to determine the power-on delay (2^{14} cycles if M0 is High, 2^{16} cycles if M0 is Low). Before the start of configuration, this input is again sampled together with M1, M2 to determine the configuration mode to be used.

A Low-to-High input transition, after configuration is complete, acts as a Read Trigger and initiates a Readback of configuration and storage-element data clocked by CCLK. By selecting the appropriate Readback option when generating the bitstream, this operation may be limited to a single Readback, or be inhibited altogether.

M1/$\overline{\text{RDATA}}$

As Mode 1, this input and M0, M2 are sampled before the start of configuration to establish the configuration mode to be used. If Readback is never used, M1 can be tied directly to ground or V_{CC}. If Readback is ever used, M1 must use a 5-kΩ resistor to ground or V_{CC}, to accommodate the RDATA output.

As an active-Low Read Data, after configuration is complete, this pin is the output of the Readback data.

User I/O Pins That Can Have Special Functions

M2

During configuration, this input has a weak pull-up resistor. Together with M0 and M1, it is sampled before the start of configuration to establish the configuration mode to be used. After configuration, this pin is a user-programmable I/O pin.

HDC

During configuration, this output is held at a High level to indicate that configuration is not yet complete. After configuration, this pin is a user-programmable I/O pin.

$\overline{\text{LDC}}$

During Configuration, this output is held at a Low level to indicate that the configuration is not yet complete. After configuration, this pin is a user-programmable I/O pin. $\overline{\text{LDC}}$ is particularly useful in Master mode as a Low enable for an EPROM, but it must then be programmed as a High after configuration.

$\overline{\text{INIT}}$

This is an active Low open-drain output with a weak pull-up and is held Low during the power stabilization and internal clearing of the configuration memory. It can be used to indicate status to a configuring microprocessor or, as a wired

Pin Functions During Configuration

Configuration Mode <M2:M1:M0>					***		**										****	
SLAVE SERIAL <1:1:1>	MASTER-SERIAL <0:0:0>	PERIPH <1:0:1>	MASTER-HIGH <1:1:0>	MASTER-LOW <1:0:0>	44 PLCC	64 VQFP	68 PLCC	84 PLCC	84 PGA	100 PQFP	100 VQFP TQFP	132 PGA	144 TQFP	160 PQFP	175 PGA	176 TQFP	208 PQFP	User Function
POWR DWN (I)	POWER DWN (I)	POWER DWN (I)	POWER DWN (I)	POWER DWN (I)	7	17	10	12	B2	29	26	A1	1	159	B2	1	3	POWER DWN (1)
M1 (HIGH) (I)	M1 (LOW) (I)	M1 (LOW) (I)	M1 (HIGH) (I)	M1 (LOW) (I)	16	31	25	31	J2	52	49	B13	36	40	B14	45	48	RDATA
M0 (HIGH) (I)	M0 (LOW) (I)	M0 (HIGH) (I)	M0 (LOW) (I)	M0 (LOW) (I)	17	32	26	32	L1	54	51	A14	38	42	B15	47	50	RTRIG (I)
M2 (HIGH) (I)	M2 (LOW) (I)	M2 (HIGH) (I)	M2 (HIGH) (I)	M2 (HIGH) (I)	18	33	27	33	K2	56	53	C13	40	44	C15	49	56	I/O
HDC (HIGH)	HDC (HIGH)	HDC (HIGH)	HDC (HIGH)	HDC (HIGH)	19	34	28	34	K3	57	54	B14	41	45	E14	50	57	I/O
LDC (LOW)	LDC (LOW)	LDC (LOW)	LDC (LOW)	LDC (LOW)	20	36	30	36	L3	59	56	D14	45	49	D16	54	61	I/O
INIT*	INIT*	INIT*	INIT*	INIT*	22	40	34	42	K6	65	62	G14	53	59	H15	65	77	I/O
GND	GND	GND	GND	GND	23	41	35	43	J6	66	63	H12	55	61	J14	67	79	GND
					26	47	43	53	L11	76	73	M13	69	76	P15	85	100	XTL2 OR I/O
RESET (I)	RESET (I)	RESET (I)	RESET (I)	RESET (I)	27	48	44	54	K10	78	75	P14	71	78	R15	87	102	RESET (I)
DONE	DONE	DONE	DONE	DONE	28	49	45	55	J10	80	77	N13	73	80	R14	89	107	PROGRAM (I)
		DATA 7 (I)	DATA 7 (I)	DATA 7 (I)		50	46	56	K11	81	78	M12	74	81	N13	90	109	I/O
					30	51	47	57	J11	82	79	P13	75	82	T14	91	110	XTL1 OR I/O
		DATA 6 (I)	DATA 6 (I)	DATA 6 (I)		52	48	58	H10	83	80	N11	78	86	P12	96	115	I/O
		DATA 5 (I)	DATA 5 (I)	DATA 5 (I)		53	49	60	F10	87	84	M9	84	92	T11	102	122	I/O
		CS0 (I)				54	50	61	G10	88	85	N9	85	93	R10	103	123	I/O
		DATA 4 (I)	DATA 4 (I)	DATA 4 (I)		55	51	62	G11	89	86	N8	88	96	R9	108	128	I/O
		DATA 3 (I)	DATA 3 (I)	DATA 3 (I)		57	53	65	F11	92	89	N7	92	102	P8	112	132	I/O
		CS1 (I)				58	54	66	E11	93	90	P6	93	103	R8	113	133	I/O
		DATA 2 (I)	DATA 2 (I)	DATA 2 (I)		59	55	67	E10	94	91	M6	96	106	R7	118	138	I/O
		DATA 1 (I)	DATA 1 (I)	DATA 1 (I)		60	56	70	D10	98	95	M5	102	114	R5	124	145	I/O
		RDY/BUSY	$\overline{\text{RCLK}}$	$\overline{\text{RCLK}}$		61	57	71	C11	99	96	N4	103	115	P5	125	146	I/O
DIN (I)	DIN (I)	DATA 0 (I)	DATA 0 (I)	DATA 0 (I)	38	62	58	72	B11	100	97	N2	106	119	R3	130	151	I/O
DOUT	DOUT	DOUT	DOUT	DOUT	39	63	59	73	C10	1	98	M3	107	120	N4	131	152	I/O
CCLK (I)	CCLK (O)	CCLK (O)	CCLK (O)	CCLK (O)	40	64	60	74	A11	2	99	P1	108	121	R2	132	153	CCLK (I)
		WS (I)	A0	A0		1	61	75	B10	5	2	M2	111	124	P2	135	161	I/O
		CS2 (I)	A1	A1		2	62	76	B9	6	3	N1	112	125	M3	136	162	I/O
			A2	A2		3	63	77	A10	8	5	L2	115	128	P1	140	165	I/O
			A3	A3		4	64	78	A9	9	6	L1	116	129	N1	141	166	I/O
			A15	A15			65	81	B6	12	9	K1	119	132	M1	146	172	5
			A4	A4		5	66	82	B7	13	10	J2	120	133	L2	147	173	I/O
			A14	A14		6	67	83	A7	14	11	H1	123	136	K2	150	178	I/O
			A5	A5		7	68	84	C7	15	12	H2	124	137	K1	151	179	I/O
			A13	A13		9	2	2	A6	17	14	G2	128	141	H2	156	184	I/O
			A6	A6		10	3	3	A5	18	15	G1	129	142	H1	157	185	I/O
			A12	A12		11	4	4	B5	19	16	F2	133	147	F2	164	192	I/O
			A7	A7		12	5	5	C5	20	17	E1	134	148	E1	165	193	I/O
			A11	A11		13	6	8	A3	23	20	D1	137	151	D1	169	199	I/O
			A8	A8		14	7	9	A2	24	21	D2	138	152	C1	170	200	I/O
			A10	A10		15	8	10	B3	25	22	B1	141	155	E3	173	203	I/O
			A9	A9		16	9	11	A1	26	26	C2	142	156	C2	174	204	I/O
																		All Others
							X	X	X	X								XC3x20A etc.
					X	X	X	X	X	X	X							XC3x30A etc.
								X	X	X	X	X	X					XC3x42A etc.
								X**				X	X					XC3x64A etc.
								X**					X	X	X	X	X	XC3x90A etc.
								X**						X	X		X	XC3195A

Notes:

Generic I/O pins are not shown.
For a detailed description of the configuration modes, see page 25 through page 34.
For pinout details, see page 65 through page 76.
Represents a weak pull-up before and during configuration.
* INIT is an open drain output during configuration.
(I) Represents an input.
** Pin assignment for the XC3064A/XC3090A and XC3195A differ from those shown.
*** Peripheral mode and master parallel mode are not supported in the PC44 package.
**** Pin assignments for the XC3195A PQ208 differ from those shown.
Pin assignments of PGA Footprint PLCC sockets and PGA packages are not identical.
The information on this page is provided as a convenient summary. For detailed pin descriptions, see the preceding two pages.

Note: Before and during configuration, all outputs that are not used for the configuration process are 3-stated with a weak pull-up resistor.

XC3000A CLB Switching Characteristics Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Since many internal timing parameters cannot be measured directly, they are derived from benchmark timing patterns. The following guidelines reflect worst-case values over the recommended operating conditions. For more detailed, more precise, and more up-to-date timing information, use the values provided by the timing calculator and used in the simulator.

		Speed Grade		-7		-6		
Description		**Symbol**		**Min**	**Max**	**Min**	**Max**	**Units**
Combinatorial Delay								
Logic Variables	A, B, C, D, E, to outputs X or Y							
	FG Mode	1	T_{ILO}		5.1		4.1	ns
	F and FGM Mode				5.6		4.6	ns
Sequential delay								
Clock k to outputs X or Y		8	T_{CKO}		4.5		4.0	ns
Clock k to outputs X or Y when Q is returned through function generators F or G to drive X or Y								
	FG Mode		T_{QLO}		9.5		8.0	ns
	F and FGM Mode				10.0		8.5	ns
Set-up time before clock K								
Logic Variables	A, B, C, D, E							
	FG Mode	2	T_{ICK}	4.5		3.5		ns
	F and FGM Mode			5.0		4.0		ns
Data In	DI	4	T_{DICK}	4.0		3.0		ns
Enable Clock	EC	6	T_{ECCK}	4.5		4.0		ns
Hold Time after clock K								
Logic Variables	A, B, C, D, E	3	T_{CKI}	0		0		ns
Data In	DI[2]	5	T_{CKDI}	1.0		1.0		ns
Enable Clock	EC	7	T_{CKEC}	2.0		2.0		ns
Clock								
Clock High time		11	T_{CH}	4.0		3.5		ns
Clock Low time		12	T_{CL}	4.0		3.5		ns
Max. flip-flop toggle rate			F_{CLK}	113.0		135.0		MHz
Reset Direct (RD)								
RD width		13	T_{RPW}	6.0		5.0		ns
delay from RD to outputs X or Y		9	T_{RIO}		6.0		5.0	ns
Global Reset ($\overline{\text{RESET}}$ Pad)[1]								
$\overline{\text{RESET}}$ width (Low)			T_{MRW}	16.0		14.0		ns
delay from $\overline{\text{RESET}}$ pad to outputs X or Y			T_{MRQ}		19.0		17.0	ns

Notes: 1. Timing is based on the XC3042A, for other devices see timing calculator.
2. The CLB K to Q output delay (T_{CKO}, #8) of any CLB, plus the shortest possible interconnect delay, is always longer than the Data In hold time requirement (T_{CKDI}, #5) of any CLB on the same die.

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XC3000L Absolute Maximum Ratings

Symbol	Description		Units
V_{CC}	Supply voltage relative to GND	–0.5 to +7.0	V
V_{IN}	Input voltage with respect to GND	–0.5 to V_{CC} +0.5	V
V_{TS}	Voltage applied to 3-state output	–0.5 to V_{CC} +0.5	V
T_{STG}	Storage temperature (ambient)	–65 to +150	°C
T_{SOL}	Maximum soldering temperature (10 s @ 1/16 in.)	+260	°C
T_J	Junction temperature plastic	+125	°C
	Junction temperature ceramic	+150	°C

Note: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

XC3000L Global Buffer Switching Characteristics Guidelines

	Speed Grade	-8	
Description	**Symbol**	**Max**	**Units**
Global and Alternate Clock Distribution[1]			
Either: **Normal** IOB input pad through clock buffer to any CLB or IOB clock input	T_{PID}	9.0	ns
Or: **Fast** (CMOS only) input pad through clock buffer to any CLB or IOB clock input	T_{PIDC}	7.0	ns
TBUF driving a Horizontal Longline (L.L.)[1]			
I to L.L. while T is Low (buffer active)	T_{IO}	5.0	ns
T↓ to L.L. active and valid with single pull-up resistor	T_{ON}	12.0	ns
T↑ to L.L. High with single pull-up resistor	T_{PUS}	24.0	ns
BIDI			
Bidirectional buffer delay	T_{BIDI}	2.0	ns

Notes: 1. Timing is based on the XC3042A, for other devices see timing calculator.
2. The use of two pull-up resistors per Longline, available on other XC3000 devices, is not a valid option for XC3000L devices.

XC3000L CLB Switching Characteristics Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Since many internal timing parameters cannot be measured directly, they are derived from benchmark timing patterns. The following guidelines reflect worst-case values over the recommended operating conditions. For more detailed, more precise, and more up-to-date timing information, use the values provided by the timing calculator and used in the simulator.

		Speed Grade		-8		
Description		**Symbol**		**Min**	**Max**	**Units**
Combinatorial Delay						
Logic Variables	A, B, C, D, E, to outputs X or Y					
	FG Mode	1	T_{ILO}		6.7	ns
	F and FGM Mode				7.5	ns
Sequential delay						
Clock k to outputs X or Y		8	T_{CKO}		7.5	ns
Clock k to outputs X or Y when Q is returned through function generators F or G to drive X or Y			T_{QLO}			
	FG Mode				14.0	ns
	F and FGM Mode				14.8	ns
Set-up time before clock K						
Logic Variables	A, B, C, D, E					
	FG Mode	2	T_{ICK}	5.0		ns
	F and FGM Mode			5.8		ns
Data In	DI	4	T_{DICK}	5.0		ns
Enable Clock	EC	6	T_{ECCK}	6.0		ns
Hold Time after clock K						
Logic Variables	A, B, C, D, E	3	T_{CKI}	0		ns
Data In	DI[2]	5	T_{CKDI}	2.0		ns
Enable Clock	EC	7	T_{CKEC}	2.0		ns
Clock						
Clock High time		11	T_{CH}	5.0		ns
Clock Low time		12	T_{CL}	5.0		ns
Max. flip-flop toggle rate			F_{CLK}	80.0		MHz
Reset Direct (RD)						
RD width		13	T_{RPW}	7.0		ns
delay from RD to outputs X or Y		9	T_{RIO}	7.0		ns
Global Reset ($\overline{\text{RESET}}$ Pad)[1]						
$\overline{\text{RESET}}$ width (Low)			T_{MRW}	16.0		ns
delay from $\overline{\text{RESET}}$ pad to outputs X or Y			T_{MRQ}		23.0	ns

Notes: 1. Timing is based on the XC3042L, for other devices see timing calculator.
2. The CLB K to Q output delay (T_{CKO}, #8) of any CLB, plus the shortest possible interconnect delay, is always longer than the Data In hold time requirement (T_{CKDI}, #5) of any CLB on the same die.

XC3000L IOB Switching Characteristics Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Since many internal timing parameters cannot be measured directly, they are derived from benchmark timing patterns. The following guidelines reflect worst-case values over the recommended operating conditions. For more detailed, more precise, and more up-to-date timing information, use the values provided by the timing calculator and used in the simulator.

		Speed Grade	-8		
Description		**Symbol**		**Min**	**Max**	**Units**
Propagation Delays (Input)						
Pad to Direct In (I)		3	T_{PID}		5.0	ns
Pad to Registered In (Q) with latch transparent			T_{PTG}		24.0	ns
Clock (IK) to Registered In (Q)		4	T_{IKRI}		6.0	ns
Set-up Time (Input)						
Pad to Clock (IK) set-up time		1	T_{PICK}	22.0		ns
Propagation Delays (Output)						
Clock (OK) to Pad	(fast)	7	T_{OKPO}		12.0	ns
same	(slew rate limited)	7	T_{OKPO}		28.0	ns
Output (O) to Pad	(fast)	10	T_{OPF}		9.0	ns
same	(slew-rate limited)	10	T_{OPS}		25.0	ns
3-state to Pad begin hi-Z	(fast)	9	T_{TSHZ}		12.0	ns
same	(slew-rate limited)	9	T_{TSHZ}		28.0	ns
3-state to Pad active and valid	(fast)	8	T_{TSON}		16.0	ns
same	(slew -rate limited)	8	T_{TSON}		32.0	ns
Set-up and Hold Times (Output)						
Output (O) to clock (OK) set-up time		5	T_{OOK}	12.0		ns
Output (O) to clock (OK) hold time		6	T_{OKO}	0		ns
Clock						
Clock High time		11	T_{IOH}	5.0		ns
Clock Low time		12	T_{IOL}	5.0		ns
Max. flip-flop toggle rate			F_{CLK}	80.0		MHz
Global Reset Delays (based on XC3042L)						
$\overline{\text{RESET}}$ Pad to Registered In	(Q)	13	T_{RRI}		25.0	ns
$\overline{\text{RESET}}$ Pad to output pad	(fast)	15	T_{RPO}		35.0	ns
	(slew-rate limited)	15	T_{RPO}		51.0	ns

Notes: 1. Timing is measured at pin threshold, with 50 pF external capacitive loads (incl. test fixture). Typical slew rate limited output rise/fall times are approximately four times longer.
2. Voltage levels of unused (bonded and unbonded) pads must be valid logic levels. Each can be configured with the internal pull-up resistor or alternatively configured as a driven output or driven from an external source.
3. Input pad set-up time is specified with respect to the internal clock (ik). In order to calculate system set-up time, subtract clock delay (pad to ik) from the input pad set-up time value. Input pad holdtime with respect to the internal clock (ik) is negative. This means that pad level changes immediately before the internal clock edge (ik) will not be recognized.
4. T_{PID}, T_{PTG}, and T_{PICK} are 3 ns higher for XTL2 when the pin is configured as a user input.

XC3100A Switching Characteristics

Xilinx maintains test specifications for each product as controlled documents. To insure the use of the most recently released device performance parameters, please request a copy of the current test-specification revision.

XC3100A Operating Conditions

Symbol	Description	Min	Max	Units
V_{CC}	Supply voltage relative to GND Commercial 0°C to +85°C junction	4.25	5.25	V
	Supply voltage relative to GND Industrial -40°C to +100°C junction	4.5	5.5	V
V_{IHT}	High-level input voltage — TTL configuration	2.0	V_{CC}	V
V_{ILT}	Low-level input voltage — TTL configuration	0	0.8	V
V_{IHC}	High-level input voltage — CMOS configuration	70%	100%	V_{CC}
V_{ILC}	Low-level input voltage — CMOS configuration	0	20%	V_{CC}
T_{IN}	Input signal transition time		250	ns

Note: At junction temperatures above those listed as Operating Conditions, all delay parameters increase by 0.3% per °C.

XC3100A DC Characteristics Over Operating Conditions

Symbol	Description		Min	Max	Units
V_{OH}	High-level output voltage (@ I_{OH} = –8.0 mA, V_{CC} min)	Commercial	3.86		V
V_{OL}	Low-level output voltage (@ I_{OL} = 8.0 mA, V_{CC} min)			0.40	V
V_{OH}	High-level output voltage (@ I_{OH} = –8.0 mA, V_{CC} min)	Industrial	3.76		V
V_{OL}	Low-level output voltage (@ I_{OL} = 8.0 mA, V_{CC} min)			0.40	V
V_{CCPD}	Power-down supply voltage (PWRDWN must be Low)		2.30		V
I_{CCO}	Quiescent LCA supply current in addition to I_{CCPD}[1] Chip thresholds programmed as CMOS levels Chip thresholds programmed as TTL levels			 8 14	 mA mA
I_{IL}	Input Leakage Current		–10	+10	µA
C_{IN}	Input capacitance, all packages except PGA175 (sample tested) All Pins except XTL1 and XTL2 XTL1 and XTL2			 10 15	 pF pF
	Input capacitance, PGA 175 (sample tested) All Pins except XTL1 and XTL2 XTL1 and XTL2			 15 20	 pF pF
I_{RIN}	Pad pull-up (when selected) @ V_{IN} = 0 V[3]		0.02	0.17	mA
I_{RLL}	Horizontal Longline pull-up (when selected) @ logic Low		0.20	2.80	mA

Notes: 1. With no output current loads, no active input or Longline pull-up resistors, all package pins at V_{CC} or GND, and the LCA device configured with a tie option.
2. Total continuous output sink current may not exceed 100 mA per ground pin. The number of ground pins varies from two for the XC3120A in the PC84 package, to eight for the XC3195A in the PQ208 package.
3. Not tested. Allows an undriven pin to float High. For any other purpose, use an external pull-up.

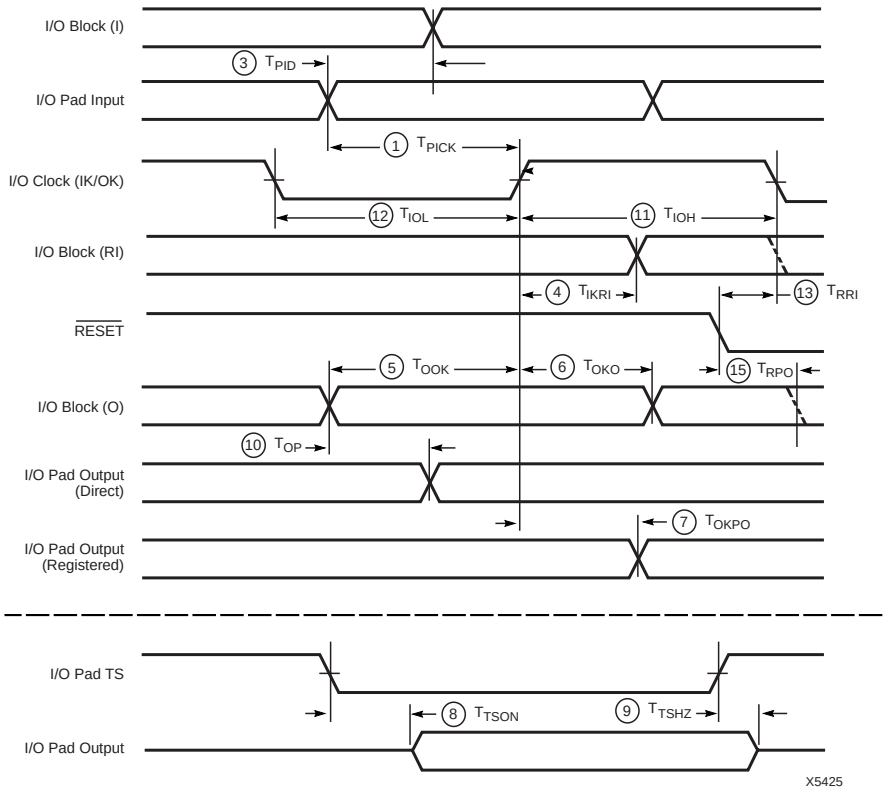
XC3100A IOB Switching Characteristics Guidelines

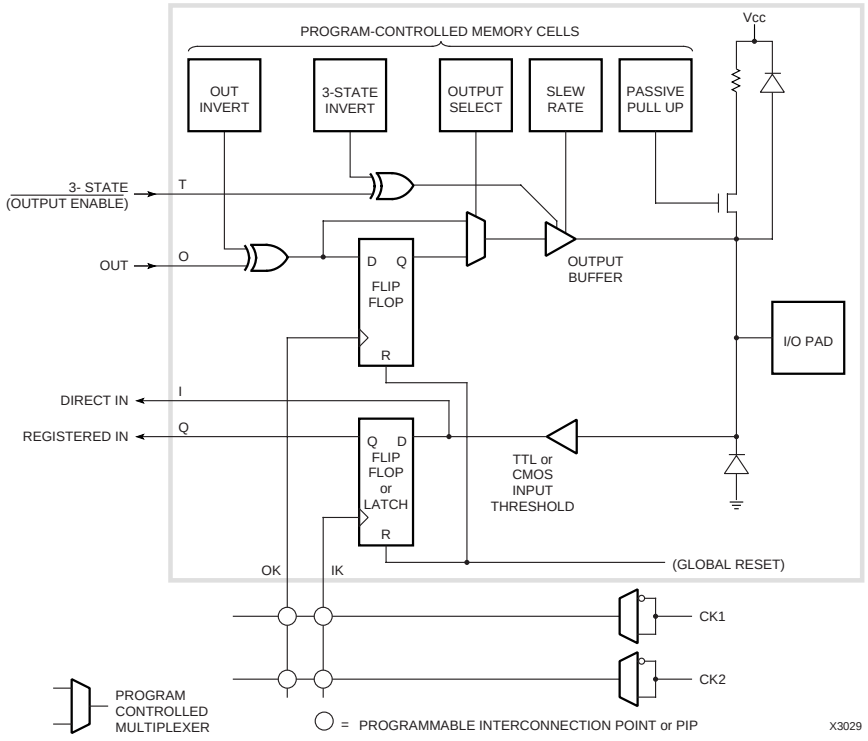
Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Since many internal timing parameters cannot be measured directly, they are derived from benchmark timing patterns. The following guidelines reflect worst-case values over the recommended operating conditions. For more detailed, more precise, and more up-to-date timing information, use the values provided by the timing calculator and used in the simulator.

Speed Grade			-4		-3		-2		-1		-09		
Description	**Symbol**		**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**
Propagation Delays (Input)													
Pad to Direct In (I)	3	T_{PID}		2.5		2.2		2.0		1.7		1.55	ns
Pad to Registered In (Q)													
with latch transparent(XC3100A)Clock (IK)		T_{PTG}		12.0		11.0		11.0		10.0		9.2	ns
to Registered In (Q)	4	T_{IKRI}		2.5		2.2		1.9		1.7		1.55	ns
Set-up Time (Input)													
Pad to Clock (IK) set-up time													
XC3120A, XC3130A	1	T_{PICK}	10.6		9.4		8.9		8.0		7.2		ns
XC3142A			10.7		9.5		9.0		8.1		7.3		ns
XC3164A			11.0		9.7		9.2		8.3		7.5		ns
XC3190A			11.2		9.9		9.4		8.5		7.7		ns
XC3195A			11.6		10.3		9.8		8.9		8.1		ns
Propagation Delays (Output)													
Clock (OK) to Pad (fast)	7	T_{OKPO}		5.0		4.4		3.7		3.4		3.3	ns
same (slew rate limited)	7	T_{OKPO}		12.0		10.0		9.7		8.4		6.9	ns
Output (O) to Pad (fast)	10	T_{OPF}		3.7		3.3		3.0		3.0		2.9	ns
same (slew-rate limited)													ns
(XC3100A)	10	T_{OPS}		11.0		9.0		8.7		8.0		6.5	ns
3-state to Pad													
begin hi-Z (fast)	9	T_{TSHZ}		6.2		5.5		5.0		4.5		4.05	ns
same (slew-rate limited)	9	T_{TSHZ}		6.2		5.5		5.0		4.5		4.05	ns
3-state to Pad													
active and valid (fast) (XC3100A)	8	T_{TSON}		10.0		9.0		8.5		6.5		5.0	ns
same (slew -rate limited)	8	T_{TSON}		17.0		15.0		14.2		11.5		8.6	ns
Set-up and Hold Times (Output)													
Output (O) to clock (OK) set-up time													
(XC3100A)	5	T_{OOK}	4.5				3.6		3.2		2.9		ns
Output (O) to clock (OK) hold time	6	T_{OKO}	0				0		0				ns
Clock													
Clock High time	11	T_{IOH}	2.0		1.6		1.3		1.3		1.3		ns
Clock Low time	12	T_{IOL}	2.0		1.6		1.3		1.3		1.3		ns
Max. flip-flop toggle rate		F_{CLK}	227		270		323		323		370		MHz
Global Reset Delays													
RESET Pad to Registered In (Q)													
(XC3142A)	13	T_{RRI}		15.0		13.0		13.0		13.0		14.4	ns
(XC3190A)				25.5		21.0		21.0		21.0		21.0	ns
RESET Pad to output pad (fast)	15	T_{RPO}		20.0		17.0		17.0		17.0		17.0	ns
(slew-rate limited)	15	T_{RPO}		27.0		23.0		23.0		22.0		21.0	ns
											Preliminary		

Notes: 1. Timing is measured at pin threshold, with 50 pF external capacitive loads (incl. test fixture). For larger capacitive loads, see XAPP024. Typical slew rate limited output rise/fall times are approximately four times longer.
2. Voltage levels of unused (bonded and unbonded) pads must be valid logic levels. Each can be configured with the internal pull-up resistor or alternatively configured as a driven output or driven from an external source.
3. Input pad set-up time is specified with respect to the internal clock (ik). In order to calculate system set-up time, subtract clock delay (pad to ik) from the input pad set-up time value. Input pad holdtime with respect to the internal clock (ik) is negative. This means that pad level changes immediately before the internal clock edge (ik) will not be recognized.
4. T_{PID}, T_{PTG}, and T_{PICK} are 3 ns higher for XTL2 when the pin is configured as a user input.

XC3100L IOB Switching Characteristics Guidelines (continued)





XC3000 Series Pin Assignments

Xilinx offers the six different array sizes in the XC3000 families in a variety of surface-mount and through-hole package types, with pin counts from 44 to 208.

Each chip is offered in several package types to accommodate the available PC board space and manufacturing technology. Most package types are also offered with different chips to accommodate design changes without the need for PC board changes.

Note that there is no perfect match between the number of bonding pads on the chip and the number of pins on a package. In some cases, the chip has more pads than there are pins on the package, as indicated by the information (“unused” pads) below the line in the following table. The IOBs of the unconnected pads can still be used as storage elements if the specified propagation delays and set-up times are acceptable.

In other cases, the chip has fewer pads than there are pins on the package; therefore, some package pins are not connected (n.c.), as shown above the line in the following table.

XC3000 Series 44-Pin PLCC Pinouts

XC3000A, XC3000L, and XC3100A families have identical pinouts

Pin No.	XC3030A
1	GND
2	I/O
3	I/O
4	I/O
5	I/O
6	I/O
7	PWRDWN
8	TCLKIN-I/O
9	I/O
10	I/O
11	I/O
12	VCC
13	I/O
14	I/O
15	I/O
16	M1-RDATA
17	M0-RTRIG
18	M2-I/O
19	HDC-I/O
20	LDC-I/O
21	I/O
22	$\overline{\text{INIT}}$-I/O

Pin No.	XC3030A
23	GND
24	I/O
25	I/O
26	XTL2(IN)-I/O
27	RESET
28	DONE-PGM
29	I/O
30	XTL1(OUT)-BCLK-I/O
31	I/O
32	I/O
33	I/O
34	**VCC**
35	I/O
36	I/O
37	I/O
38	DIN-I/O
39	DOUT-I/O
40	CCLK
41	I/O
42	I/O
43	I/O
44	I/O

Peripheral mode and Master Parallel mode are not supported in the PC44 package

XC3000 Series 68-Pin PLCC, 84-Pin PLCC and PGA Pinouts

XC3000A, XC3000L, XC3100A, and XC3100L families have identical pinouts

68 PLCC		XC3020A, XC3030A, XC3042A	84 PLCC
XC3030A	XC3020A		
10	10	$\overline{\text{PWRDN}}$	12
11	11	TCLKIN-I/O	13
12	—	I/O*	14
13	12	I/O	15
14	13	I/O	16
—	—	I/O	17
15	14	I/O	18
16	15	I/O	19
—	16	I/O	20
17	17	I/O	21
18	18	VCC	22
19	19	I/O	23
—	—	I/O	24
20	20	I/O	25
—	21	I/O	26
21	22	I/O	27
22	—	I/O	28
23	23	I/O	29
24	24	I/O	30
25	25	M1-$\overline{\text{RDATA}}$	31
26	26	M0-RTRIG	32
27	27	M2-I/O	33
28	28	HDC-I/O	34
29	29	I/O	35
30	30	$\overline{\text{LDC}}$-I/O	36
—	31	I/O	37
—		I/O*	38
31	32	I/O	39
32	33	I/O	40
33	—	I/O*	41
34	34	$\overline{\text{INIT}}$-I/O	42
35	35	GND	43
36	36	I/O	44
37	37	I/O	45
38	38	I/O	46
39	39	I/O	47
—	40	I/O	48
—	41	I/O	49
40		I/O*	50
41		I/O*	51
42	42	I/O	52
43	43	XTL2(IN)-I/O	53

68 PLCC		XC3020A, XC3030A, XC3042A	84 PLCC
XC3030A	XC3020A		
44	44	$\overline{\text{RESET}}$	54
45	45	DONE-$\overline{\text{PG}}$	55
46	46	D7-I/O	56
47	47	XTL1(OUT)-BCLKIN-I/O	57
48	48	D6-I/O	58
—	—	I/O	59
49	49	D5-I/O	60
50	50	$\overline{\text{CS0}}$-I/O	61
51	51	D4-I/O	62
—	—	I/O	63
52	52	VCC	64
53	53	D3-I/O	65
54	54	$\overline{\text{CS1}}$-I/O	66
55	55	D2-I/O	67
—	—	I/O	68
—	—	I/O*	69
56	56	D1-I/O	70
57	57	RDY/$\overline{\text{BUSY}}$-$\overline{\text{RCLK}}$-I/O	71
58	58	D0-DIN-I/O	72
59	59	DOUT-I/O	73
60	60	CCLK	74
61	61	A0-$\overline{\text{WS}}$-I/O	75
62	62	A1-CS2-I/O	76
63	63	A2-I/O	77
64	64	A3-I/O	78
—	—	I/O*	79
—	—	I/O*	80
65	65	A15-I/O	81
66	66	A4-I/O	82
67	67	A14-I/O	83
68	68	A5-I/O	84
1	1	GND	1
2	2	A13-I/O	2
3	3	A6-I/O	3
4	4	A12-I/O	4
5	5	A7-I/O	5
—	—	I/O*	6
—	—	I/O*	7
6	6	A11-I/O	8
7	7	A8-I/O	9
8	8	A10-I/O	10
9	9	A9-I/O	11

Unprogrammed IOBs have a default pull-up. This prevents an undefined pad level for unbonded or unused IOBs. Programmed outputs are default slew-rate limited.

This table describes the pinouts of three different chips in three different packages. The pin-description column lists 84 of the 118 pads on the XC3042A (and 84 of the 98 pads on the XC3030A) that are connected to the 84 package pins. Ten pads, indicated by an asterisk, do not exist on the XC3020A, which has 74 pads; therefore the corresponding pins on the 84-pin packages have no connections to an XC3020A. Six pads on the XC3020A and 16 pads on the XC3030A, indicated by a dash (—) in the 68 PLCC column, have no connection to the 68 PLCC, but are connected to the 84-pin packages.

XC3000 Series 160-Pin PQFP Pinouts

XC3000A, XC3000L, XC3100A, and XC3100L families have identical pinouts

PQFP Pin Number	XC3064A, XC3090A, XC3195A
1	I/O*
2	I/O*
3	I/O*
4	I/O
5	I/O
6	I/O
7	I/O
8	I/O
9	I/O
10	I/O
11	I/O
12	I/O
13	I/O
14	I/O
15	I/O
16	I/O
17	I/O
18	I/O
19	GND
20	VCC
21	I/O*
22	I/O
23	I/O
24	I/O
25	I/O
26	I/O
27	I/O
28	I/O
29	I/O
30	I/O
31	I/O
32	I/O
33	I/O
34	I/O
35	I/O
36	I/O
37	I/O
38	I/O*
39	I/O*
40	M1-$\overline{\text{RDATA}}$

PQFP Pin Number	XC3064A, XC3090A, XC3195A
41	GND
42	M0–RTRIG
43	VCC
44	M2-I/O
45	HDC-I/O
46	I/O
47	I/O
48	I/O
49	$\overline{\text{LDC}}$-I/O
50	I/O*
51	I/O*
52	I/O
53	I/O
54	I/O
55	I/O
56	I/O
57	I/O
58	I/O
59	$\overline{\text{INIT}}$-I/O
60	VCC
61	GND
62	I/O
63	I/O
64	I/O
65	I/O
66	I/O
67	I/O
68	I/O
69	I/O
70	I/O
71	I/O
72	I/O
73	I/O
74	I/O
75	I/O*
76	XTL2-I/O
77	GND
78	$\overline{\text{RESET}}$
79	VCC
80	DONE/$\overline{\text{PG}}$

PQFP Pin Number	XC3064A, XC3090A, XC3195A
81	D7-I/O
82	XTL1-I/O-BCLKIN
83	I/O*
84	I/O
85	I/O
86	D6-I/O
87	I/O
88	I/O
89	I/O
90	I/O
91	I/O
92	D5-I/O
93	$\overline{\text{CS0}}$-I/O
94	I/O*
95	I/O*
96	I/O
97	I/O
98	D4-I/O
99	I/O
100	VCC
101	GND
102	D3-I/O
103	$\overline{\text{CS1}}$-I/O
104	I/O
105	I/O
106	I/O*
107	I/O*
108	D2-I/O
109	I/O
110	I/O
111	I/O
112	I/O
113	I/O
114	D1-I/O
115	RDY/$\overline{\text{BUSY}}$-$\overline{\text{RCLK}}$-I/O
116	I/O
117	I/O
118	I/O*
119	D0-DIN-I/O
120	DOUT-I/O

PQFP Pin Number	XC3064A, XC3090A, XC3195A
121	CCLK
122	VCC
123	GND
124	A0-$\overline{\text{WS}}$-I/O
125	A1-CS2-I/O
126	I/O
127	I/O
128	A2-I/O
129	A3-I/O
130	I/O
131	I/O
132	A15-I/O
133	A4-I/O
134	I/O
135	I/O
136	A14-I/O
137	A5-I/O
138	I/O*
139	GND
140	VCC
141	A13-I/O
142	A6-I/O
143	I/O*
144	I/O*
145	I/O
146	I/O
147	A12-I/O
148	A7-I/O
149	I/O
150	I/O
151	A11-I/O
152	A8-I/O
153	I/O
154	I/O
155	A10-I/O
156	A9-I/O
157	VCC
158	GND
159	$\overline{\text{PWRDWN}}$
160	TCLKIN-I/O

Unprogrammed IOBs have a default pull-up. This prevents an undefined pad level for unbonded or unused IOBs. Programmed IOBs are default slew-rate limited.

* Indicates unconnected package pins (18) for the XC3064A.

XC3195A PQ208 Pinouts

Pin Description	PQ208
A9-I/O	206
A10-I/O	205
I/O	204
I/O	203
I/O	202
I/O	201
A8-I/O	200
A11-I/O	199
I/O	198
I/O	197
I/O	196
I/O	194
A7-I/O	193
A12-I/O	192
I/O	191
I/O	190
I/O	189
I/O	188
I/O	187
I/O	186
A6-I/O	185
A13-I/O	184
VCC	183
GND	182
I/O	181
I/O	180
A5-I/O	179
A14-I/O	178
I/O	177
I/O	176
I/O	175
I/O	174
A4-I/O	173
A15-I/O	172
I/O	171
I/O	169
I/O	168
I/O	167
A3-I/O	166
A2-I/O	165
I/O	164
I/O	163
I/O	162
I/O	161
A1-CS2-I/O	160
A0-$\overline{WS}$-I/O	159
GND	158
VCC	157
CCLK	156
DOUT-I/O	155

Pin Description	PQ208
D0-DIN-I/O	154
I/O	153
I/O	152
I/O	151
I/O	150
RDY/BUSY-RCLK-I/O	149
D1-I/O	148
I/O	147
I/O	146
I/O	145
I/O	144
I/O	141
I/O	140
I/O	139
D2-I/O	138
I/O	137
I/O	136
I/O	135
I/O	134
$\overline{CS1}$-I/O	133
D3-I/O	132
GND	131
VCC	130
I/O	129
D4-I/O	128
I/O	127
I/O	126
I/O	125
I/O	124
$\overline{CS0}$-I/O	123
D5-I/O	122
I/O	121
I/O	120
I/O	119
I/O	118
I/O	117
I/O	116
I/O	115
D6-I/O	114
I/O	113
I/O	112
I/O	111
I/O	110
XTLX1(OUT)BCLKN-I/O	109
D7-I/O	108
D/$\overline{P}$	107
VCC	106
$\overline{RESET}$	105
GND	104
XTL2(IN)-I/O	103

Pin Description	PQ208
I/O	102
I/O	101
I/O	100
I/O	99
I/O	98
I/O	97
I/O	96
I/O	95
I/O	94
I/O	93
I/O	92
I/O	89
I/O	88
I/O	87
I/O	86
I/O	85
I/O	84
I/O	83
I/O	82
I/O	81
I/O	80
GND	79
VCC	78
$\overline{INIT}$	77
I/O	76
I/O	75
I/O	74
I/O	73
I/O	72
I/O	71
I/O	70
I/O	69
I/O	68
I/O	67
I/O	66
I/O	63
I/O	62
I/O	61
I/O	60
$\overline{LDC}$-I/O	59
I/O	58
I/O	57
I/O	56
HDC-I/O	55
M2-I/O	54
VCC	53
M0-RTIG	52
GND	51
M1/$\overline{RDATA}$	50
I/O	49

Pin Description	PQ208
I/O	48
I/O	47
I/O	46
I/O	45
I/O	44
I/O	43
I/O	42
I/O	41
I/O	40
I/O	39
I/O	38
I/O	37
I/O	36
I/O	35
I/O	34
I/O	33
I/O	32
I/O	31
I/O	30
I/O	29
I/O	28
VCC	27
GND	26
I/O	25
I/O	24
I/O	23
I/O	22
I/O	21
I/O	20
I/O	19
I/O	18
I/O	17
I/O	14
I/O	13
I/O	12
I/O	11
I/O	10
I/O	9
I/O	8
I/O	7
I/O	6
I/O	5
I/O	4
I/O	3
TCLKIN-I/O	2
$\overline{PWRDN}$	1
GND	208
VCC	207

Unprogrammed IOBs have a default pull-up. This prevents an undefined pad level for unbonded or unused IOBs. Programmed outputs are default slew-rate limited.
In the PQ208 package, pins 15, 16, 64, 65, 90, 91, 142, 143, 170 and 195 are not connected.
* In PQ208, XC3090A and XC3195A have different pinouts.