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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	100
Number of Logic Elements/Cells	-
Total RAM Bits	22176
Number of I/O	80
Number of Gates	2000
Voltage - Supply	4.75V ~ 5.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	100-BQFP
Supplier Device Package	100-PQFP (20x14)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc3030a-7pq100c

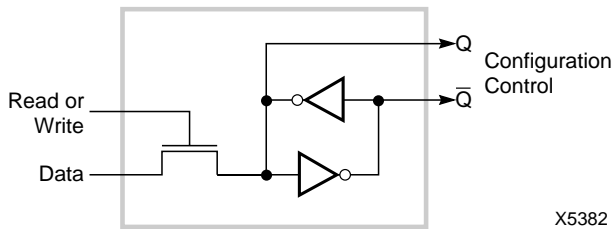


Figure 3: Static Configuration Memory Cell.

It is loaded with one bit of configuration program and controls one program selection in the Field Programmable Gate Array.

The memory cell outputs Q and \bar{Q} use ground and V_{CC} levels and provide continuous, direct control. The additional capacitive load together with the absence of address decoding and sense amplifiers provide high stability to the cell. Due to the structure of the configuration memory cells, they are not affected by extreme power-supply excursions or very high levels of alpha particle radiation. In reliability

testing, no soft errors have been observed even in the presence of very high doses of alpha radiation.

The method of loading the configuration data is selectable. Two methods use serial data, while three use byte-wide data. The internal configuration logic utilizes framing information, embedded in the program data by the development system, to direct memory-cell loading. The serial-data framing and length-count preamble provide programming compatibility for mixes of various FPGA device devices in a synchronous, serial, daisy-chain fashion.

I/O Block

Each user-configurable IOB shown in **Figure 4**, provides an interface between the external package pin of the device and the internal user logic. Each IOB includes both registered and direct input paths. Each IOB provides a programmable 3-state output buffer, which may be driven by a registered or direct output signal. Configuration options allow each IOB an inversion, a controlled slew rate and a high impedance pull-up. Each input circuit also provides input clamping diodes to provide electrostatic protection, and circuits to inhibit latch-up produced by input currents.

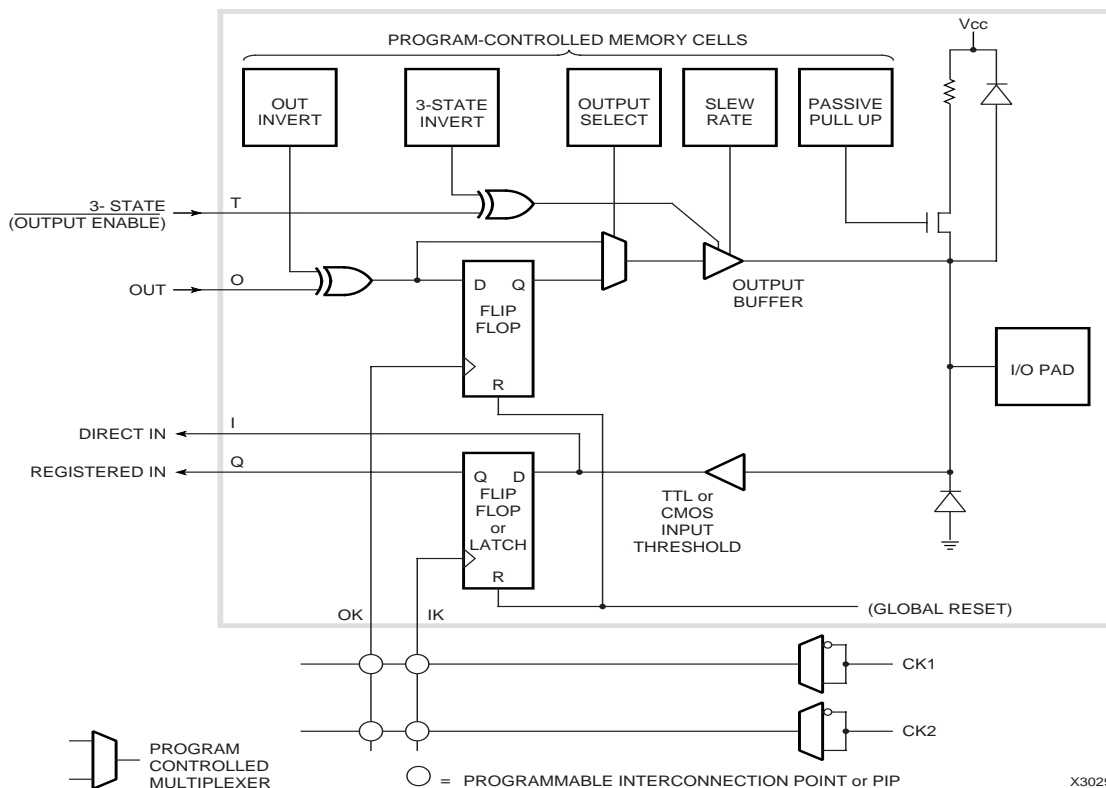


Figure 4: Input/Output Block.

Each IOB includes input and output storage elements and I/O options selected by configuration memory cells. A choice of two clocks is available on each die edge. The polarity of each clock line (not each flip-flop or latch) is programmable. A clock line that triggers the flip-flop on the rising edge is an active Low Latch Enable (Latch transparent) signal and vice versa. Passive pull-up can only be enabled on inputs, not on outputs. All user inputs are programmed for TTL or CMOS thresholds.

Flexible routing allows use of common or individual CLB clocking.

The combinatorial-logic portion of the CLB uses a 32 by 1 look-up table to implement Boolean functions. Variables selected from the five logic inputs and two internal block flip-flops are used as table address inputs. The combinatorial propagation delay through the network is independent of the logic function generated and is spike free for single input variable changes. This technique can generate two independent logic functions of up to four variables each as shown in Figure 6a, or a single function of five variables as shown in Figure 6b, or some functions of seven variables as shown in Figure 6c. **Figure 7** shows a modulo-8 binary counter with parallel enable. It uses one CLB of each type. The partial functions of six or seven variables are implemented using the input variable (E) to dynamically select between two functions of four different variables. For the two functions of four variables each, the independent results (F and G) may be used as data inputs to either flip-flop or either logic block output. For the single function of five variables and merged functions of six or seven variables, the F and G outputs are identical. Symmetry of the F and G functions and the flip-flops allows the interchange of CLB outputs to optimize routing efficiencies of the networks interconnecting the CLBs and IOBs.

Programmable Interconnect

Programmable-interconnection resources in the Field Programmable Gate Array provide routing paths to connect inputs and outputs of the IOBs and CLBs into logic networks. Interconnections between blocks are composed of a two-layer grid of metal segments. Specially designed pass transistors, each controlled by a configuration bit, form programmable interconnect points (PIPs) and switching matrices used to implement the necessary connections between selected metal segments and block pins. **Figure 8** is an example of a routed net. The development system provides automatic routing of these interconnections. Interactive routing is also available for design optimization. The inputs of the CLBs or IOBs are multiplexers which can be programmed to select an input network from the adjacent interconnect segments. **Since the switch connections to block inputs are unidirectional, as are block outputs, they are usable only for block input connection and not for routing.** **Figure 9** illustrates routing access to logic block input variables, control inputs and block outputs. Three types of metal resources are provided to accommodate various network interconnect requirements.

- General Purpose Interconnect
- Direct Connection
- Longlines (multiplexed busses and wide AND gates)

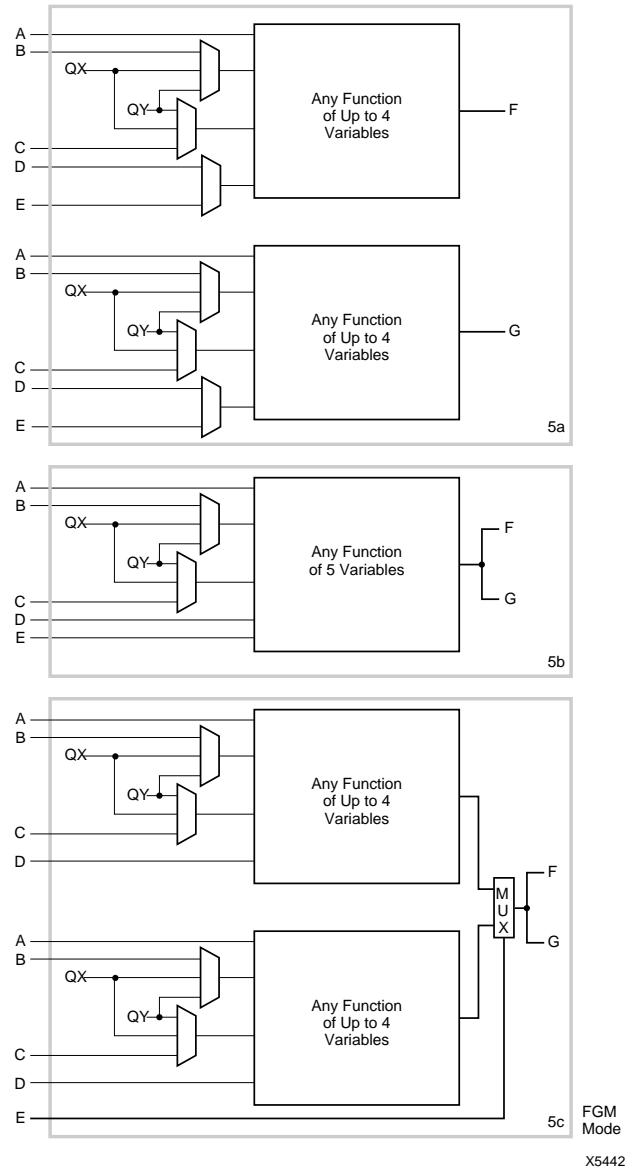


Figure 6: Combinational Logic Options

6a. Combinatorial Logic Option FG generates two functions of four variables each. One variable, A, must be common to both functions. The second and third variable can be any choice of B, C, QX and QY. The fourth variable can be any choice of D or E.

6b. Combinatorial Logic Option F generates any function of five variables: A, D, E and two choices out of B, C, QX, QY.

6c. Combinatorial Logic Option FGM allows variable E to select between two functions of four variables: Both have common inputs A and D and any choice out of B, C, QX and QY for the remaining two variables. Option 3 can then implement some functions of six or seven variables.

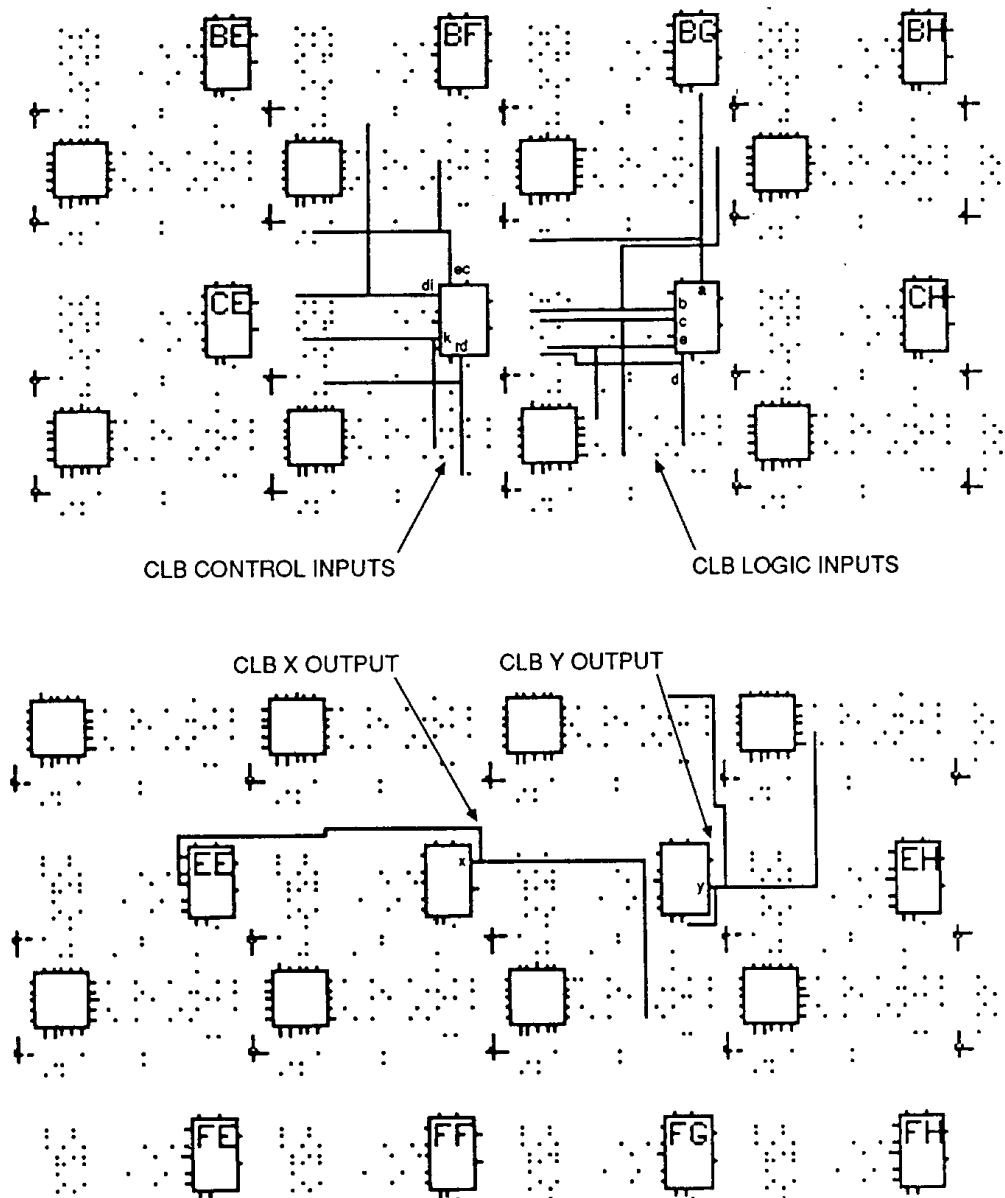


Figure 9: Design Editor Locations of interconnect access, CLB control inputs, logic inputs and outputs. The dot pattern represents the available programmable interconnection points (PIPs).

Some of the interconnect PIPs are directional.

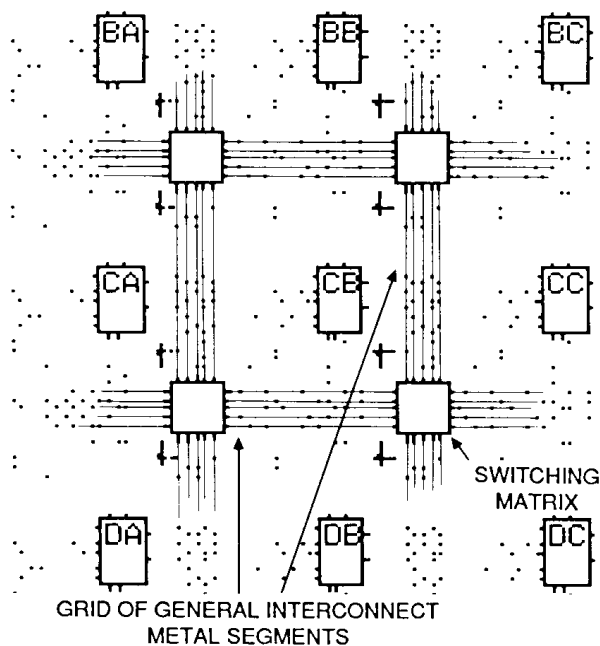


Figure 10: FPGA General-Purpose Interconnect.
Composed of a grid of metal segments that may be inter-connected through switch matrices to form networks for CLB and IOB inputs and outputs.

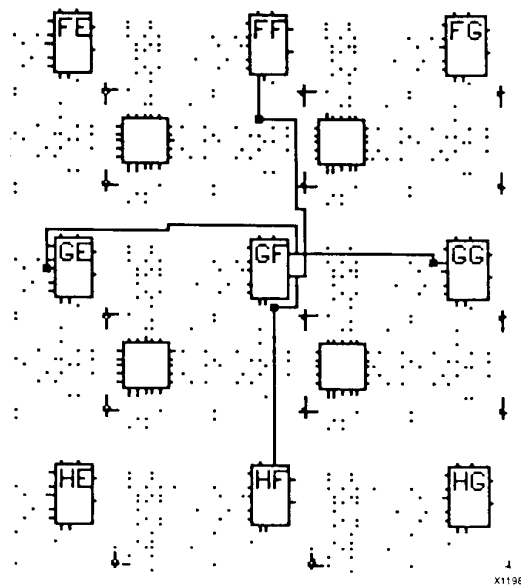
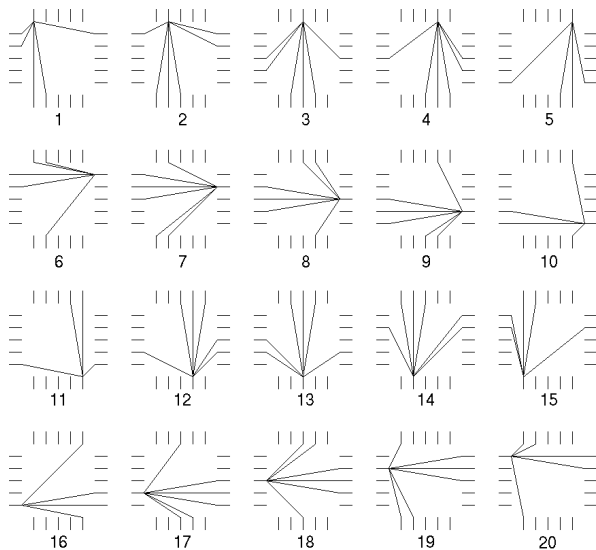


Figure 12: CLB X and Y Outputs.
The X and Y outputs of each CLB have single contact, direct access to inputs of adjacent CLBs



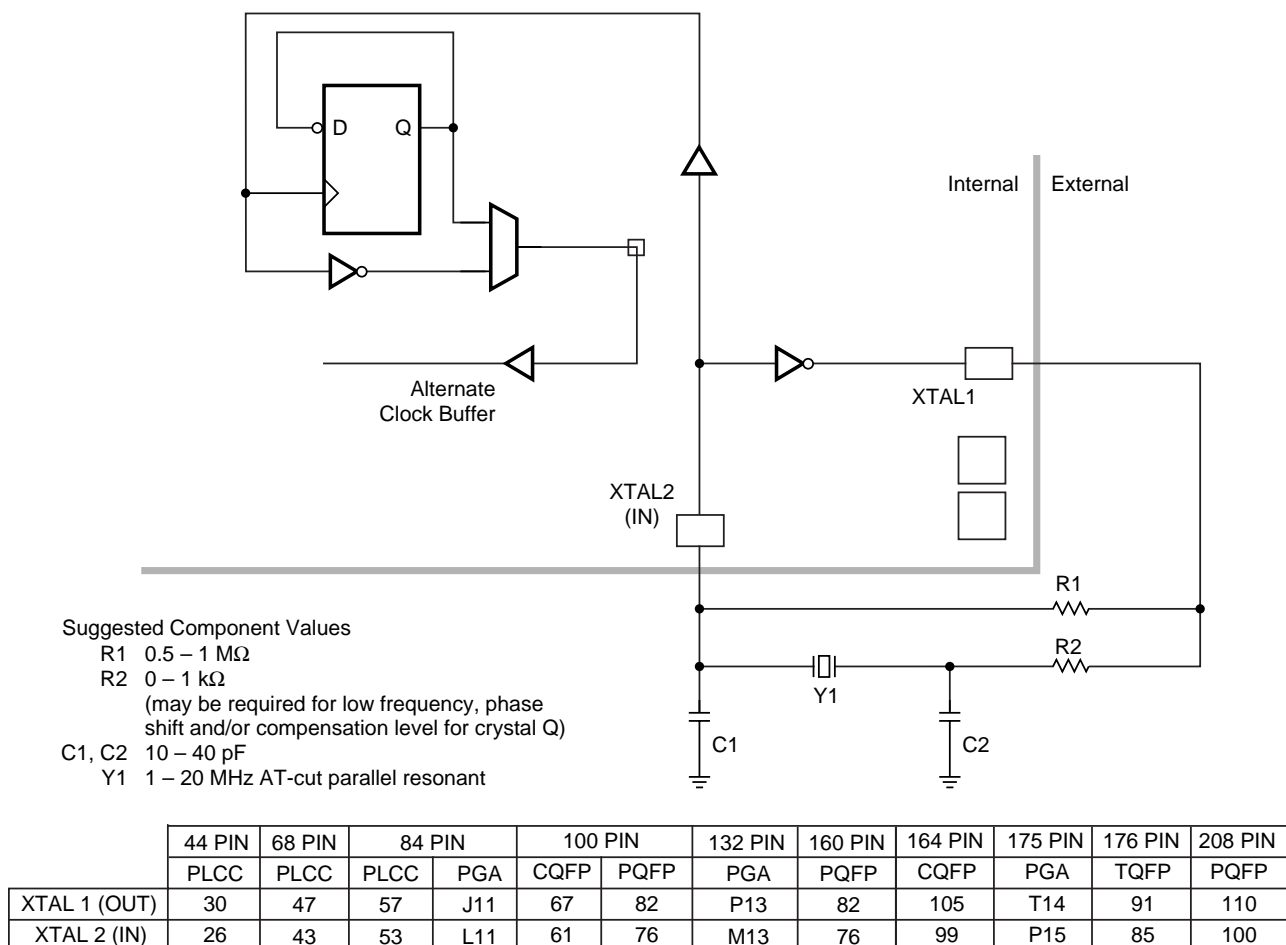
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Figure 11: Switch Matrix Interconnection Options for Each Pin.
Switch matrices on the edges are different.

Crystal Oscillator

Figure 18 also shows the location of an internal high speed inverting amplifier that may be used to implement an on-chip crystal oscillator. It is associated with the auxiliary buffer in the lower right corner of the die. When the oscillator is configured and connected as a signal source, two special user IOBs are also configured to connect the oscillator amplifier with external crystal oscillator components as shown in Figure 19. A divide by two option is available to assure symmetry. The oscillator circuit becomes active early in the configuration process to allow the oscillator to stabilize. Actual internal connection is delayed until completion of configuration. In Figure 19 the feedback resistor R1, between the output and input, biases the amplifier at threshold. The inversion of the amplifier, together with the R-C networks and an AT-cut series resonant crystal, produce the 360-degree phase shift of the Pierce oscillator. A

series resistor R2 may be included to add to the amplifier output impedance when needed for phase-shift control, crystal resistance matching, or to limit the amplifier input swing to control clipping at large amplitudes. Excess feedback voltage may be corrected by the ratio of C2/C1. The amplifier is designed to be used from 1 MHz to about one-half the specified CLB toggle frequency. Use at frequencies below 1 MHz may require individual characterization with respect to a series resistance. Crystal oscillators above 20 MHz generally require a crystal which operates in a third overtone mode, where the fundamental frequency must be suppressed by an inductor across C2, turning this parallel resonant circuit to double the fundamental crystal frequency, i.e., 2/3 of the desired third harmonic frequency. When the oscillator inverter is not used, these IOBs and their package pins are available for general user I/O.



X7064

Figure 19: Crystal Oscillator Inverter. When activated, and by selecting an output network for its buffer, the crystal oscillator inverter uses two unconfigured package pins and external components to implement an oscillator. An optional divide-by-two mode is available to assure symmetry.

Configuration

Initialization Phase

An internal power-on-reset circuit is triggered when power is applied. When V_{CC} reaches the voltage at which portions of the FPGA device begin to operate (nominally 2.5 to 3 V), the programmable I/O output buffers are 3-stated and a high-impedance pull-up resistor is provided for the user I/O pins. A time-out delay is initiated to allow the power supply voltage to stabilize. During this time the power-down mode is inhibited. The Initialization state time-out (about 11 to 33 ms) is determined by a 14-bit counter driven by a self-generated internal timer. This nominal 1-MHz timer is subject to variations with process, temperature and power supply. As shown in Table 1, five configuration mode choices are available as determined by the input levels of three mode pins; M0, M1 and M2.

Table 1: Configuration Mode Choices

M0	M1	M2	CCLK	Mode	Data
0	0	0	output	Master	Bit Serial
0	0	1	output	Master	Byte Wide Addr. = 0000 up
0	1	0	—	reserved	—
0	1	1	output	Master	Byte Wide Addr. = FFFF down
1	0	0	—	reserved	—
1	0	1	output	Peripheral	Byte Wide
1	1	0	—	reserved	—
1	1	1	input	Slave	Bit Serial

In Master configuration modes, the device becomes the source of the Configuration Clock (CCLK). The beginning of configuration of devices using Peripheral or Slave modes must be delayed long enough for their initialization to be completed. An FPGA with mode lines selecting a Master configuration mode extends its initialization state using four times the delay (43 to 130 ms) to assure that all daisy-chained slave devices, which it may be driving, will be ready even if the master is very fast, and the slave(s) very slow. Figure 20 shows the state sequences. At the end of Initialization, the device enters the Clear state where it clears the configuration memory. The active Low, open-drain initialization signal \overline{INIT} indicates when the Initialization and Clear states are complete. The FPGA tests for the absence of an external active Low \overline{RESET} before it makes a final sample of the mode lines and enters the Configuration state. An external wired-AND of one or more \overline{INIT} pins can be used to control configuration by the assertion of the active-Low \overline{RESET} of a master mode device or to signal a processor that the FPGAs are not yet initialized.

If a configuration has begun, a re-assertion of \overline{RESET} for a minimum of three internal timer cycles will be recognized and the FPGA will initiate an abort, returning to the Clear state to clear the partially loaded configuration memory words. The FPGA will then resample \overline{RESET} and the mode lines before re-entering the Configuration state.

During configuration, the XC3000A, XC3000L, XC3100A, and XC3100L devices check the bit-stream format for stop bits in the appropriate positions. Any error terminates the configuration and pulls \overline{INIT} Low.

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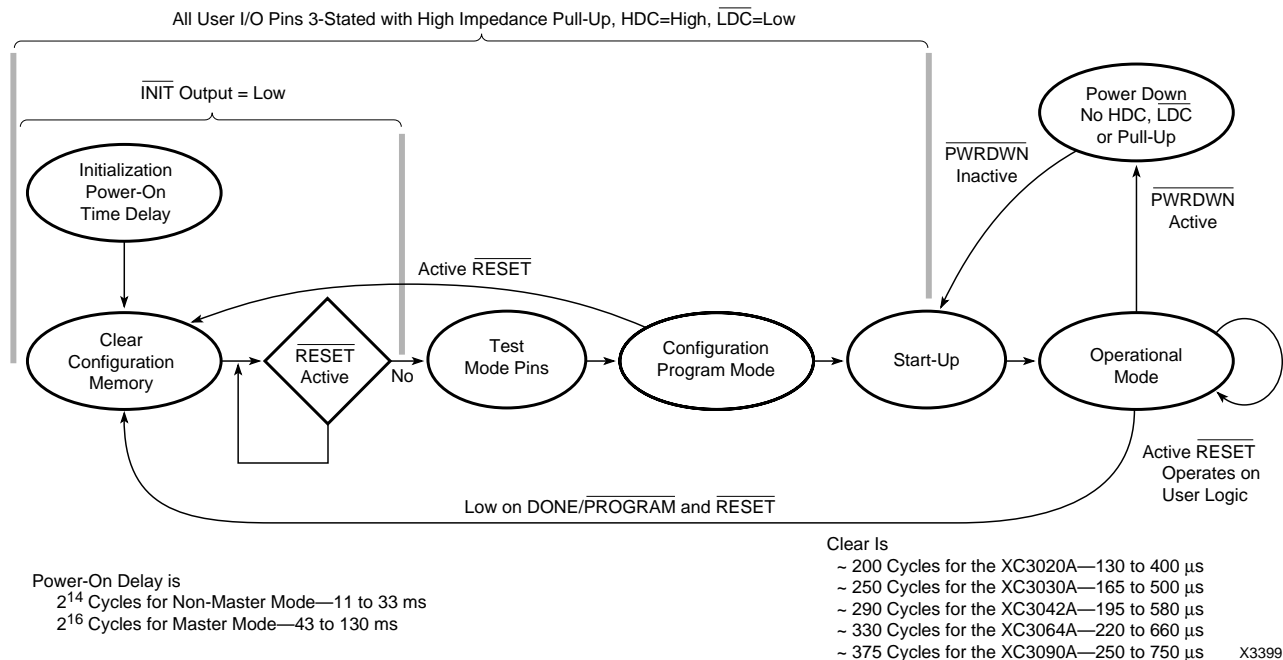


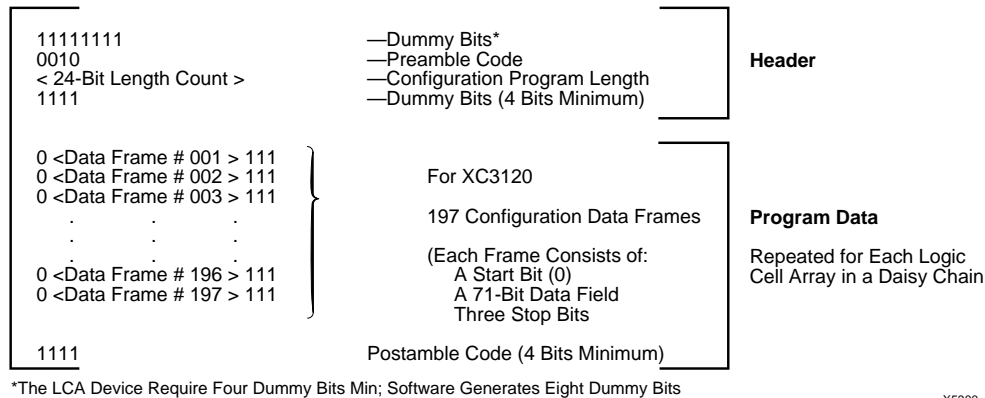
Figure 20: A State Diagram of the Configuration Process for Power-up and Reprogram.

A re-program is initiated when a configured XC3000 series device senses a High-to-Low transition and subsequent >6 μ s Low level on the DONE/ $\overline{\text{PROG}}$ package pin, or, if this pin is externally held permanently Low, a High-to-Low transition and subsequent >6 μ s Low time on the RESET package pin.

The device returns to the Clear state where the configuration memory is cleared and mode lines re-sampled, as for an aborted configuration. The complete configuration program is cleared and loaded during each configuration program cycle.

Length count control allows a system of multiple Field Programmable Gate Arrays, of assorted sizes, to begin operation in a synchronized fashion. The configuration program

generated by the development system begins with a preamble of 11111110010 followed by a 24-bit length count representing the total number of configuration clocks needed to complete loading of the configuration program(s). The data framing is shown in Figure 21. All FPGAs connected in series read and shift preamble and length count in on positive and out on negative configuration clock edges. A device which has received the preamble and length count then presents a High Data Out until it has intercepted the appropriate number of data frames. When the configuration program memory of an FPGA is full and the length count does not yet compare, the device shifts any additional data through, as it did for preamble and length count. When the FPGA configuration memory is full and the length count compares, the device will execute



Device	XC3020A XC3020L XC3120A	XC3030A XC3030L XC3130A	XC3042A XC3042L XC3142A XC3142L	XC3064A XC3064L XC3164A	XC3090A XC3090L XC3190A XC3190L	XC3195A
Gates	1,000 to 1,500	1,500 to 2,000	2,000 to 3,000	3,500 to 4,500	5,000 to 6,000	6,500 to 7,500
CLBs	64	100	144	224	320	484
Row x Col	(8 x 8)	(10 x 10)	(12 x 12)	(16 x 14)	(20 x 16)	(22 x 22)
IOBs	64	80	96	120	144	176
Flip-flops	256	360	480	688	928	1,320
Horizontal Longlines	16	20	24	32	40	44
TBUFs/Horizontal LL	9	11	13	15	17	23
Bits per Frame (including 1 start and 3 stop bits)	75	92	108	140	172	188
Frames	197	241	285	329	373	505
Program Data = Bits x Frames + 4 bits (excludes header)	14,779	22,176	30,784	46,064	64,160	94,944
PROM size (bits) = Program Data + 40-bit Header	14,819	22,216	30,824	46,104	64,200	94,984

Figure 21: Internal Configuration Data Structure for an FPGA. This shows the preamble, length count and data frames generated by the Development System.

The Length Count produced by the program = [(40-bit preamble + sum of program data + 1 per daisy chain device) rounded up to multiple of 8] - (2 \leq K \leq 4) where K is a function of DONE and RESET timing selected. An additional 8 is added if roundup increment is less than K. K additional clocks are needed to complete start-up after length count is reached.

RESET Timing

As with DONE timing, the timing of the release of the internal reset can be controlled to occur either a CCLK cycle before, or after, the outputs going active. See [Figure 22](#). This reset keeps all user programmable flip-flops and latches in a zero state during configuration.

Crystal Oscillator Division

A selection allows the user to incorporate a dedicated divide-by-two flip-flop between the crystal oscillator and the alternate clock line. This guarantees a symmetrical clock signal. Although the frequency stability of a crystal oscillator is very good, the symmetry of its waveform can be affected by bias or feedback drive.

Bitstream Error Checking

Bitstream error checking protects against erroneous configuration.

Each Xilinx FPGA bitstream consists of a 40-bit preamble, followed by a device-specific number of data frames. The number of bits per frame is also device-specific; however, each frame ends with three stop bits (111) followed by a start bit for the next frame (0).

All devices in all XC3000 families start reading in a new frame when they find the first 0 after the end of the previous frame. An original XC3000 device does not check for the correct stop bits, but XC3000A, XC3100A, XC3000L, and XC3100L devices check that the last three bits of any frame are actually 111.

Under normal circumstances, all these FPGAs behave the same way; however, if the bitstream is corrupted, an XC3000 device will always start a new frame as soon as it finds the first 0 after the end of the previous frame, even if the data is completely wrong or out-of-sync. Given sufficient zeros in the data stream, the device will also go Done,

but with incorrect configuration and the possibility of internal contention.

An XC3000A/XC3100A/XC3000L/XC3100L device starts any new frame only if the three preceding bits are all ones. If this check fails, it pulls INIT Low and stops the internal configuration, although the Master CCLK keeps running. The user must then start a new configuration by applying a >6 μ s Low level on RESET.

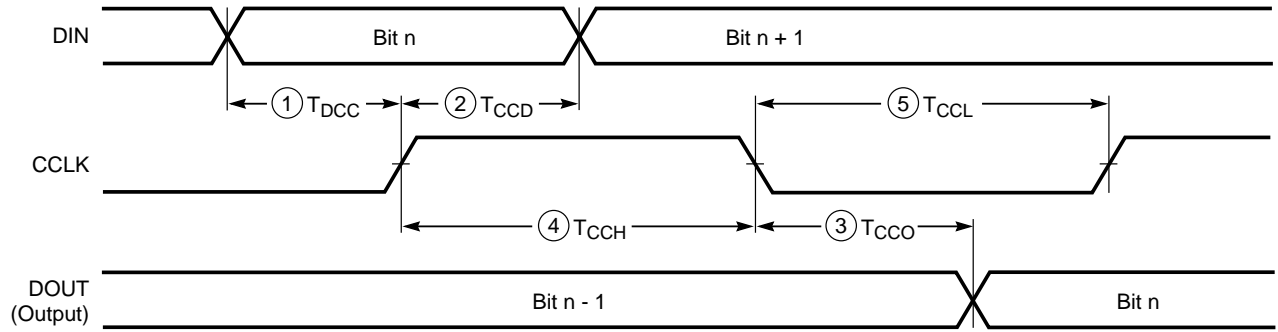
This simple check does not protect against random bit errors, but it offers almost 100 percent protection against erroneous configuration files, defective configuration data sources, synchronization errors between configuration source and FPGA, or PC-board level defects, such as broken lines or solder-bridges.

Reset Spike Protection

A separate modification slows down the RESET input before configuration by using a two-stage shift register driven from the internal clock. It tolerates submicrosecond High spikes on RESET before configuration. The XC3000 master can be connected like an XC4000 master, but with its RESET input used instead of INIT. (On XC3000, INIT is output only).

Soft Start-up

After configuration, the outputs of all FPGAs in a daisy-chain become active simultaneously, as a result of the same CCLK edge. In the original XC3000/3100 devices, each output becomes active in either fast or slew-rate limited mode, depending on the way it is configured. This can lead to large ground-bounce signals. In XC3000A, XC3000L, XC3100A, and XC3100L devices, all outputs become active first in slew-rate limited mode, reducing the ground bounce. After this soft start-up, each individual output slew rate is again controlled by the respective configuration bit.



X5379

	Description		Symbol	Min	Max	Units
	To DOUT	3	T_{CCO}		100	ns
CCLK	DIN setup	1	T_{DCC}	60		ns
	DIN hold	2	T_{CCD}	0		ns
	High time	4	T_{CCH}	0.05		μ s
	Low time (Note 1)	5	T_{CCL}	0.05	5.0	μ s
	Frequency		F_{CC}		10	MHz

- Notes:
1. The max limit of CCLK Low time is caused by dynamic circuitry inside the FPGA.
 2. Configuration must be delayed until the INIT of all FPGAs is High.
 3. At power-up, V_{CC} must rise from 2.0 V to V_{CC} min in less than 25 ms. If this is not possible, configuration can be delayed by holding RESET Low until V_{CC} has reached 4.0 V (2.5 V for the XC3000L). A very long V_{CC} rise time of >100 ms, or a non-monotonically rising V_{CC} may require a >6- μ s High level on RESET, followed by a >6- μ s Low level on RESET and D/P after V_{CC} has reached 4.0 V (2.5 V for the XC3000L).

Figure 30: Slave Serial Mode Programming Switching Characteristics

AND of several slave mode devices, a hold-off signal for a master mode device. After configuration this pin becomes a user-programmable I/O pin.

BCLKIN

This is a direct CMOS level input to the alternate clock buffer (Auxiliary Buffer) in the lower right corner.

XTL1

This user I/O pin can be used to operate as the output of an amplifier driving an external crystal and bias circuitry.

XTL2

This user I/O pin can be used as the input of an amplifier connected to an external crystal and bias circuitry. The I/O Block is left unconfigured. The oscillator configuration is activated by routing a net from the oscillator buffer symbol output and by the MakeBits program.

$\overline{CS0}$, $\overline{CS1}$, $\overline{CS2}$, \overline{WS}

These four inputs represent a set of signals, three active Low and one active High, that are used to control configuration-data entry in the Peripheral mode. Simultaneous assertion of all four inputs generates a Write to the internal data buffer. The removal of any assertion clocks in the D0-D7 data. In Master-Parallel mode, \overline{WS} and $\overline{CS2}$ are the A0 and A1 outputs. After configuration, these pins are user-programmable I/O pins.

$\overline{RDY/BUSY}$

During Peripheral Parallel mode configuration this pin indicates when the chip is ready for another byte of data to be written to it. After configuration is complete, this pin becomes a user-programmed I/O pin.

\overline{RCLK}

During Master Parallel mode configuration, each change on the A0-15 outputs is preceded by a rising edge on \overline{RCLK} , a redundant output signal. After configuration is complete, this pin becomes a user-programmed I/O pin.

D0-D7

This set of eight pins represents the parallel configuration byte for the parallel Master and Peripheral modes. After configuration is complete, they are user-programmed I/O pins.

A0-A15

During Master Parallel mode, these 16 pins present an address output for a configuration EPROM. After configuration, they are user-programmable I/O pins.

DIN

During Slave or Master Serial configuration, this pin is used as a serial-data input. In the Master or Peripheral configuration, this is the Data 0 input. After configuration is complete, this pin becomes a user-programmed I/O pin.

DOUT

During configuration this pin is used to output serial-configuration data to the DIN pin of a daisy-chained slave. After configuration is complete, this pin becomes a user-programmed I/O pin.

TCLKIN

This is a direct CMOS-level input to the global clock buffer. This pin can also be configured as a user programmable I/O pin. However, since TCLKIN is the preferred input to the global clock net, and the global clock net should be used as the primary clock source, this pin is usually the clock input to the chip.

Unrestricted User I/O Pins

I/O

An I/O pin may be programmed by the user to be an Input or an Output pin following configuration. All unrestricted I/O pins, plus the special pins mentioned on the following page, have a weak pull-up resistor that becomes active as soon as the device powers up, and stays active until the end of configuration.

Note: Before and during configuration, all outputs that are not used for the configuration process are 3-stated with a weak pull-up resistor.

XC3000L Switching Characteristics

Xilinx maintains test specifications for each product as controlled documents. To insure the use of the most recently released device performance parameters, please request a copy of the current test-specification revision.

XC3000L Operating Conditions

Symbol	Description	Min	Max	Units
V_{CC}	Supply voltage relative to GND Commercial 0°C to +85°C junction	3.0	3.6	V
V_{IH}	High-level input voltage — TTL configuration	2.0	$V_{CC}+0.3$	V
V_{IL}	Low-level input voltage — TTL configuration	-0.3	0.8	V
T_{IN}	Input signal transition time		250	ns

- Notes:** 1. At junction temperatures above those listed as Operating Conditions, all delay parameters increase by 0.3% per °C.
2. Although the present (1996) devices operate over the full supply voltage range from 3.0 to 5.25 V, Xilinx reserves the right to restrict operation to the 3.0 to 3.6 V range later, when smaller device geometries might preclude operation at 5V. Operating conditions are guaranteed in the 3.0 – 3.6 V V_{CC} range.

XC3000L DC Characteristics Over Operating Conditions

Symbol	Description	Min	Max	Units
V_{OH}	High-level output voltage (@ $I_{OH} = -4.0$ mA, V_{CC} min)	2.40		V
V_{OL}	Low-level output voltage (@ $I_{OL} = 4.0$ mA, V_{CC} min)		0.40	V
V_{OH}	High-level output voltage (@ $I_{OH} = -4.0$ mA, V_{CC} min)	$V_{CC} - 0.2$		V
V_{OL}	Low-level output voltage (@ $I_{OL} = 4.0$ mA, V_{CC} min)		0.2	V
V_{CCPD}	Power-down supply voltage (PWRDWN must be Low)	2.30		V
I_{CCPD}	Power-down supply current ($V_{CC(MAX)}$ @ T_{MAX})		10	μA
I_{CCO}	Quiescent FPGA supply current in addition to I_{CCPD} ¹ Chip thresholds programmed as CMOS levels		20	μA
I_{IL}	Input Leakage Current	-10	+10	μA
C_{IN}	Input capacitance, all packages except PGA175 (sample tested) All Pins except XTL1 and XTL2		10	pF
	XTL1 and XTL2		15	pF
	Input capacitance, PGA 175 (sample tested) All Pins except XTL1 and XTL2		15	pF
	XTL1 and XTL2		20	pF
I_{RIN}	Pad pull-up (when selected) @ $V_{IN} = 0$ V ³	0.01	0.17	mA
I_{RLL}	Horizontal Longline pull-up (when selected) @ logic Low		2.50	mA

- Notes:** 1. With no output current loads, no active input or Longline pull-up resistors, all package pins at V_{CC} or GND, and the FPGA device configured with a tie option. I_{CCO} is in addition to I_{CCPD} .
2. Total continuous output sink current may not exceed 100 mA per ground pin. Total continuous output source may not exceed 100 mA per V_{CC} pin. The number of ground pins varies from the XC3020L to the XC3090L.
3. Not tested. Allows an undriven pin to float High. For any other purpose, use an external pull-up.

XC3000L CLB Switching Characteristics Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Since many internal timing parameters cannot be measured directly, they are derived from benchmark timing patterns. The following guidelines reflect worst-case values over the recommended operating conditions. For more detailed, more precise, and more up-to-date timing information, use the values provided by the timing calculator and used in the simulator.

		Speed Grade		-8		
Description		Symbol		Min	Max	Units
Combinatorial Delay Logic Variables	A, B, C, D, E, to outputs X or Y	1	T_{ILO}		6.7	ns
	FG Mode				7.5	ns
	F and FGM Mode					
Sequential delay Clock k to outputs X or Y		8	T_{CKO}		7.5	ns
	Clock k to outputs X or Y when Q is returned through function generators F or G to drive X or Y					
	FG Mode				14.0	ns
Set-up time before clock K Logic Variables	A, B, C, D, E	2	T_{ICK}	5.0		ns
	FG Mode			5.8		ns
	F and FGM Mode					
Data In	DI	4	T_{DICK}	5.0		ns
	Enable Clock	6	T_{ECCK}	6.0		ns
Hold Time after clock K Logic Variables	A, B, C, D, E	3	T_{CKI}	0		ns
	Data In	5	T_{CKDI}	2.0		ns
	Enable Clock	7	T_{CKEC}	2.0		ns
Clock Clock High time		11	T_{CH}	5.0		ns
	Clock Low time	12	T_{CL}	5.0		ns
	Max. flip-flop toggle rate		F_{CLK}	80.0		MHz
Reset Direct (RD) RD width		13	T_{RPW}	7.0		ns
	delay from RD to outputs X or Y	9	T_{RIO}	7.0		ns
Global Reset (RESET Pad) ¹ RESET width (Low)			T_{MRW}	16.0		ns
	delay from RESET pad to outputs X or Y		T_{MRQ}		23.0	ns

Notes: 1. Timing is based on the XC3042L, for other devices see timing calculator.

2. The CLB K to Q output delay (T_{CKO} , #8) of any CLB, plus the shortest possible interconnect delay, is always longer than the Data In hold time requirement (T_{CKDI} , #5) of any CLB on the same die.

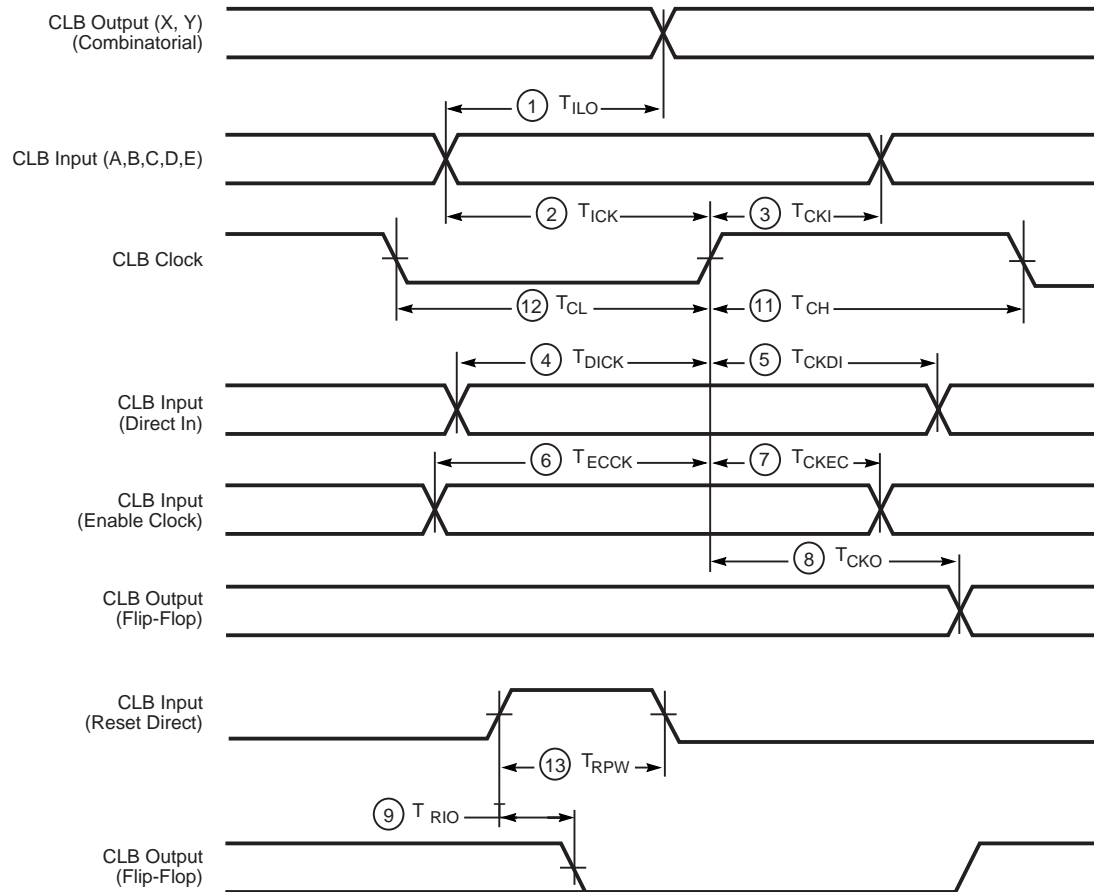
XC3100A CLB Switching Characteristics Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Since many internal timing parameters cannot be measured directly, they are derived from benchmark timing patterns. The following guidelines reflect worst-case values over the recommended operating conditions. For more detailed, more precise, and more up-to-date timing information, use the values provided by the timing calculator and used in the simulator.

Speed Grade			-4		-3		-2		-1		-09		Units
Description	Symbol		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Combinatorial Delay Logic Variables A, B, C, D, E, to outputs X or Y	1	T _{ILO}		3.3		2.7		2.2		1.75		1.5	ns
Sequential delay Clock k to outputs X or Y Clock k to outputs X or Y when Q is returned through function generators F or G to drive X or Y	8	T _{CKO}		2.5		2.1		1.7		1.4		1.25	ns
		T _{QLO}		5.2		4.3		3.5		3.1		2.7	ns
Set-up time before clock K Logic Variables A, B, C, D, E Data In DI Enable Clock EC Reset Direct inactive RD	2	T _{ICK}	2.5		2.1		1.8		1.7		1.5		ns
	4	T _{DICK}	1.6		1.4		1.3		1.2		1.0		ns
	6	T _{ECCCK}	3.2		2.7		2.5		2.3		2.05		ns
			1.0		1.0		1.0		1.0		1.0		ns
Hold Time after clock K Logic Variables A, B, C, D, E Data In DI Enable Clock EC	3	T _{CKI}	0		0		0		0		0		ns
	5	T _{CKDI}	1.0		0.9		0.9		0.8		0.7		ns
	7	T _{CKEC}	0.8		0.7		0.7		0.6		0.55		ns
Clock Clock High time Clock Low time Max. flip-flop toggle rate	11	T _{CH}	2.0		1.6		1.3		1.3		1.3		ns
	12	T _{CL}	2.0		1.6		1.3		1.3		1.3		ns
		F _{CLK}	227		270		323		323		370		MHz
Reset Direct (RD) RD width delay from RD to outputs X or Y	13	T _{RPW}	3.2		2.7		2.3		2.3		2.05		ns
	9	T _{RIO}		3.7		3.1		2.7		2.4		2.15	ns
Global Reset (RESET Pad) ¹ RESET width (Low) (XC3142A) delay from RESET pad to outputs X or Y		T _{MRW}	14.0		12.0		12.0		12.0		12.0		ns
		T _{MRQ}		14.0		12.0		12.0		12.0		12.0	ns
Prelim													

- Notes:** 1. The CLB K to Q output delay (T_{CKO}, #8) of any CLB, plus the shortest possible interconnect delay, is always longer than the Data In hold time requirement (T_{CKDI}, #5) of any CLB on the same die.
2. T_{ILO}, T_{QLO} and T_{ICK} are specified for 4-input functions. For 5-input functions or base FGM functions, each of these specifications for the XC3100A family increases by 0.50 ns (-5), 0.42 ns (-4) and 0.35 ns (-3), 0.35 ns (-2), 0.30 ns (-1), and 0.30 ns (-09).

XC3100A CLB Switching Characteristics Guidelines (continued)



X5424

XC3100L Switching Characteristics

Xilinx maintains test specifications for each product as controlled documents. To insure the use of the most recently released device performance parameters, please request a copy of the current test-specification revision.

XC3100L Operating Conditions

Symbol	Description	Min	Max	Units
V_{CC}	Supply voltage relative to GND Commercial 0°C to +85°C junction	3.0	3.6	V
V_{IH}	High-level input voltage	2.0	$V_{CC} + 0.3$	V
V_{IL}	Low-level input voltage	-0.3	0.8	V
T_{IN}	Input signal transition time		250	ns

- Notes:** 1. At junction temperatures above those listed as Operating Conditions, all delay parameters increase by 0.3% per °C.
2. Although the present (1996) devices operate over the full supply voltage range from 3.0 V to 5.25 V, Xilinx reserves the right to restrict operation to the 3.0 and 3.6 V range later, when smaller device geometries might preclude operation @ 5 V. Operating conditions are guaranteed in the 3.0 – 3.6 V V_{CC} range.

XC3100L DC Characteristics Over Operating Conditions

Symbol	Description	Min	Max	Units
V_{OH}	High-level output voltage (@ $I_{OH} = -4.0$ mA, V_{CC} min)	2.4		V
	High-level output voltage (@ $I_{OH} = -100.0$ μ A, V_{CC} min)	$V_{CC} - 0.2$		V
V_{OL}	Low-level output voltage (@ $I_{OH} = 4.0$ mA, V_{CC} min)		0.40	V
	Low-level output voltage (@ $I_{OH} = +100.0$ μ A, V_{CC} min)		0.2	V
V_{CCPD}	Power-down supply voltage (PWRDWN must be Low)	2.30		V
I_{CCO}	Quiescent FPGA supply current Chip thresholds programmed as CMOS levels ¹		1.5	mA
I_{IL}	Input Leakage Current	-10	+10	μ A
C_{IN}	Input capacitance (sample tested)			
	All pins except XTL1 and XTL2 XTL1 and XTL2		10 15	pF pF
I_{RIN}	Pad pull-up (when selected) @ $V_{IN} = 0$ V ³	0.02	0.17	mA
I_{RLL}	Horizontal long line pull-up (when selected) @ logic Low	0.20	2.80	mA

- Notes:** 1. With no output current loads, no active input or long line pull-up resistors, all package pins at V_{CC} or GND, and the FPGA configured with a tie option.
2. Total continuous output sink current may not exceed 100 mA per ground pin. Total continuous output source current may not exceed 100 mA per V_{CC} pin. The number of ground pins varies from the XC3142L to the XC3190L.
3. Not tested. Allows undriven pins to float High. For any other purpose, use an external pull-up.

XC3100L Absolute Maximum Ratings

Symbol	Description		Units
V_{CC}	Supply voltage relative to GND	-0.5 to +7.0	V
V_{IN}	Input voltage with respect to GND	-0.5 to $V_{CC} + 0.5$	V
V_{TS}	Voltage applied to 3-state output	-0.5 to $V_{CC} + 0.5$	V
T_{STG}	Storage temperature (ambient)	-65 to +150	°C
T_{SOL}	Maximum soldering temperature (10 s @ 1/16 in.)	+260	°C
T_J	Junction temperature plastic	+125	°C
	Junction temperature ceramic	+150	°C

Note: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

XC3100L Global Buffer Switching Characteristics Guidelines

		Speed Grade		
Description	Symbol	-3 Max	-2 Max	Units
Global and Alternate Clock Distribution ¹ Either: Normal IOB input pad through clock buffer to any CLB or IOB clock input Or: Fast (CMOS only) input pad through clock buffer to any CLB or IOB clock input	T_{PID}	5.6	4.7	ns
	T_{PIDC}	4.3	3.7	ns
TBUF driving a Horizontal Longline (L.L.) ¹ I to L.L. while T is Low (buffer active) $T \downarrow$ to L.L. active and valid with single pull-up resistor $T \uparrow$ to L.L. High with single pull-up resistor	T_{IO}	3.1	3.1	ns
	T_{ON}	4.2	4.2	ns
	T_{PUS}	11.4	11.4	ns
BIDI Bidirectional buffer delay	T_{BIDI}	1.0	0.9	ns
		Advance		

Notes: 1. Timing is based on the XC3142L, for other devices see timing calculator.
2. The use of two pull-up resistors per longline, available on other XC3000 devices, is not a valid option for XC3100L devices.

Product Obsolete or Under Obsolescence



XC3000 Series Field Programmable Gate Arrays

XC3000 Series 100-Pin QFP Pinouts

XC3000A, XC3000L, XC3100A, and XC3100L families have identical pinouts

Pin No.		XC3020A XC3030A XC3042A	Pin No.		XC3020A XC3030A XC3042A	Pin No.		XC3020A XC3030A XC3042A
PQFP	TQFP VQFP		PQFP	TQFP VQFP		PQFP	TQFP VQFP	
16	13	GND	50	47	I/O*	84	81	I/O*
17	14	A13-I/O	51	48	I/O*	85	82	I/O*
18	15	A6-I/O	52	49	M1-RD	86	83	I/O
19	16	A12-I/O	53	50	GND*	87	84	D5-I/O
20	17	A7-I/O	54	51	MO-RT	88	85	CS0-I/O
21	18	I/O*	55	52	VCC*	89	86	D4-I/O
22	19	I/O*	56	53	M2-I/O	90	87	I/O
23	20	A11-I/O	57	54	HDC-I/O	91	88	VCC
24	21	A8-I/O	58	55	I/O	92	89	D3-I/O
25	22	A10-I/O	59	56	LDC-I/O	93	90	CS1-I/O
26	23	A9-I/O	60	57	I/O*	94	91	D2-I/O
27	24	VCC*	61	58	I/O*	95	92	I/O
28	25	GND*	62	59	I/O	96	93	I/O*
29	26	PWRDN	63	60	I/O	97	94	I/O*
30	27	TCLKIN-I/O	64	61	I/O	98	95	D1-I/O
31	28	I/O**	65	62	INIT-I/O	99	96	RDY/BUSY-RCLK-I/O
32	29	I/O*	66	63	GND	100	97	DO-DIN-I/O
33	30	I/O*	67	64	I/O	1	98	DOOUT-I/O
34	31	I/O	68	65	I/O	2	99	CCLK
35	32	I/O	69	66	I/O	3	100	VCC*
36	33	I/O	70	67	I/O	4	1	GND*
37	34	I/O	71	68	I/O	5	2	AO-WS-I/O
38	35	I/O	72	69	I/O	6	3	A1-CS2-I/O
39	36	I/O	73	70	I/O	7	4	I/O**
40	37	I/O	74	71	I/O*	8	5	A2-I/O
41	38	VCC	75	72	I/O*	9	6	A3-I/O
42	39	I/O	76	73	XTL2-I/O	10	7	I/O*
43	40	I/O	77	74	GND*	11	8	I/O*
44	41	I/O	78	75	RESET	12	9	A15-I/O
45	42	I/O	79	76	VCC*	13	10	A4-I/O
46	43	I/O	80	77	DONE-PG	14	11	A14-I/O
47	44	I/O	81	78	D7-I/O	15	12	A5-I/O
48	45	I/O	82	79	BCLKIN-XTL1-I/O			
49	46	I/O	83	80	D6-I/O			

Unprogrammed IOBs have a default pull-up. This prevents an undefined pad level for unbonded or unused IOBs. Programmed outputs are default slew-rate limited.

* This table describes the pinouts of three different chips in three different packages. The pin-description column lists 100 of the 118 pads on the XC3042A that are connected to the 100 package pins. Two pads, indicated by double asterisks, do not exist on the XC3030A, which has 98 pads; therefore the corresponding pins have no connections. Twenty-six pads, indicated by single or double asterisks, do not exist on the XC3020A, which has 74 pads; therefore, the corresponding pins have no connections. (See table on [page 65](#).)

Product Obsolete or Under Obsolescence



XC3000 Series Field Programmable Gate Arrays

XC3000 Series 144-Pin Plastic TQFP Pinouts

XC3000A, XC3000L, XC3100A, and XC3100L families have identical pinouts

Pin Number	XC3042A XC3064A XC3090A	Pin Number	XC3042A XC3064A XC3090A	Pin Number	XC3042A XC3064A XC3090A
1	PWRDN	49	I/O	97	I/O
2	I/O-TCLKIN	50	I/O*	98	I/O
3	I/O*	51	I/O	99	I/O*
4	I/O	52	I/O	100	I/O
5	I/O	53	INIT-I/O	101	I/O*
6	I/O*	54	VCC	102	D1-I/O
7	I/O	55	GND	103	RDY/BUSY-RCLK-I/O
8	I/O	56	I/O	104	I/O
9	I/O*	57	I/O	105	I/O
10	I/O	58	I/O	106	D0-DIN-I/O
11	I/O	59	I/O	107	DOOUT-I/O
12	I/O	60	I/O	108	CCLK
13	I/O	61	I/O	109	VCC
14	I/O	62	I/O	110	GND
15	I/O*	63	I/O*	111	A0-WS-I/O
16	I/O	64	I/O*	112	A1-CS2-I/O
17	I/O	65	I/O	113	I/O
18	GND	66	I/O	114	I/O
19	VCC	67	I/O	115	A2-I/O
20	I/O	68	I/O	116	A3-I/O
21	I/O	69	XTL2(IN)-I/O	117	I/O
22	I/O	70	GND	118	I/O
23	I/O	71	RESET	119	A15-I/O
24	I/O	72	VCC	120	A4-I/O
25	I/O	73	DONE-PG	121	I/O*
26	I/O	74	D7-I/O	122	I/O*
27	I/O	75	XTL1(OUT)-BCLKIN-I/O	123	A14-I/O
28	I/O*	76	I/O	124	A5-I/O
29	I/O	77	I/O	125	I/O (XC3090 only)
30	I/O	78	D6-I/O	126	GND
31	I/O*	79	I/O	127	VCC
32	I/O*	80	I/O*	128	A13-I/O
33	I/O	81	I/O	129	A6-I/O
34	I/O*	82	I/O	130	I/O*
35	I/O	83	I/O*	131	I/O (XC3090 only)
36	M1-RD	84	D5-I/O	132	I/O*
37	GND	85	CS0-I/O	133	A12-I/O
38	M0-RT	86	I/O*	134	A7-I/O
39	VCC	87	I/O*	135	I/O
40	M2-I/O	88	D4-I/O	136	I/O
41	HDC-I/O	89	I/O	137	A11-I/O
42	I/O	90	VCC	138	A8-I/O
43	I/O	91	GND	139	I/O
44	I/O	92	D3-I/O	140	I/O
45	LDC-I/O	93	CS1-I/O	141	A10-I/O
46	I/O*	94	I/O*	142	A9-I/O
47	I/O	95	I/O*	143	VCC
48	I/O	96	D2-I/O	144	GND

Unprogrammed IOBs have a default pull-up. This prevents an undefined pad level for unbonded or unused IOBs. Programmed outputs are default slew-rate limited.

* Indicates unconnected package pins (24) for the XC3042A.

Product Obsolete or Under Obsolescence



XC3000 Series Field Programmable Gate Arrays

XC3000 Series 175-Pin Ceramic and Plastic PGA Pinouts

XC3000A, XC3000L, XC3100A, and XC3100L families have identical pinouts

PGA Pin Number	XC3090A, XC3195A	PGA Pin Number	XC3090A, XC3195A	PGA Pin Number	XC3090A, XC3195A	PGA Pin Number	XC3090A, XC3195A
B2	PWRDN	D13	I/O	R14	DONE-PG	N4	DOUT-I/O
D4	TCLKIN-I/O	B14	M1-RDATA	N13	D7-I/O	R2	CCLK
B3	I/O	C14	GND	T14	XTL1(OUT)-BCLKIN-I/O	P3	VCC
C4	I/O	B15	M0-RTRIG	P13	I/O	N3	GND
B4	I/O	D14	VCC	R13	I/O	P2	A0-WS-I/O
A4	I/O	C15	M2-I/O	T13	I/O	M3	A1-CS2-I/O
D5	I/O	E14	HDC-I/O	N12	I/O	R1	I/O
C5	I/O	B16	I/O	P12	D6-I/O	N2	I/O
B5	I/O	D15	I/O	R12	I/O	P1	A2-I/O
A5	I/O	C16	I/O	T12	I/O	N1	A3-I/O
C6	I/O	D16	LDC-I/O	P11	I/O	L3	I/O
D6	I/O	F14	I/O	N11	I/O	M2	I/O
B6	I/O	E15	I/O	R11	I/O	M1	A15-I/O
A6	I/O	E16	I/O	T11	D5-I/O	L2	A4-I/O
B7	I/O	F15	I/O	R10	CS0-I/O	L1	I/O
C7	I/O	F16	I/O	P10	I/O	K3	I/O
D7	I/O	G14	I/O	N10	I/O	K2	A14-I/O
A7	I/O	G15	I/O	T10	I/O	K1	A5-I/O
A8	I/O	G16	I/O	T9	I/O	J1	I/O
B8	I/O	H16	I/O	R9	D4-I/O	J2	I/O
C8	I/O	H15	INIT-I/O	P9	I/O	J3	GND
D8	GND	H14	VCC	N9	VCC	H3	VCC
D9	VCC	J14	GND	N8	GND	H2	A13-I/O
C9	I/O	J15	I/O	P8	D3-I/O	H1	A6-I/O
B9	I/O	J16	I/O	R8	CS1-I/O	G1	I/O
A9	I/O	K16	I/O	T8	I/O	G2	I/O
A10	I/O	K15	I/O	T7	I/O	G3	I/O
D10	I/O	K14	I/O	N7	I/O	F1	I/O
C10	I/O	L16	I/O	P7	I/O	F2	A12-I/O
B10	I/O	L15	I/O	R7	D2-I/O	E1	A7-I/O
A11	I/O	M16	I/O	T6	I/O	E2	I/O
B11	I/O	M15	I/O	R6	I/O	F3	I/O
D11	I/O	L14	I/O	N6	I/O	D1	A11-I/O
C11	I/O	N16	I/O	P6	I/O	C1	A8-I/O
A12	I/O	P16	I/O	T5	I/O	D2	I/O
B12	I/O	N15	I/O	R5	D1-I/O	B1	I/O
C12	I/O	R16	I/O	P5	RDY/BUSY-RCLK-I/O	E3	A10-I/O
D12	I/O	M14	I/O	N5	I/O	C2	A9-I/O
A13	I/O	P15	XTL2(IN)-I/O	T4	I/O	D3	VCC
B13	I/O	N14	GND	R4	I/O	C3	GND
C13	I/O	R15	RESET	P4	I/O		
A14	I/O	P14	VCC	R3	D0-DIN-I/O		

Unprogrammed IOBs have a default pull-up. This prevents an undefined pad level for unbonded or unused IOBs. Programmed outputs are default slew-rate limited.

Pins A2, A3, A15, A16, T1, T2, T3, T15 and T16 are not connected. Pin A1 does not exist.

Product Obsolete or Under Obsolescence

XC3000 Series Field Programmable Gate Arrays



XC3195A PQ208 Pinouts

Pin Description	PQ208	Pin Description	PQ208	Pin Description	PQ208	Pin Description	PQ208
A9-I/O	206	D0-DIN-I/O	154	I/O	102	I/O	48
A10-I/O	205	I/O	153	I/O	101	I/O	47
I/O	204	I/O	152	I/O	100	I/O	46
I/O	203	I/O	151	I/O	99	I/O	45
I/O	202	I/O	150	I/O	98	I/O	44
I/O	201	RDY/BUSY-RCLK-I/O	149	I/O	97	I/O	43
A8-I/O	200	D1-I/O	148	I/O	96	I/O	42
A11-I/O	199	I/O	147	I/O	95	I/O	41
I/O	198	I/O	146	I/O	94	I/O	40
I/O	197	I/O	145	I/O	93	I/O	39
I/O	196	I/O	144	I/O	92	I/O	38
I/O	194	I/O	141	I/O	89	I/O	37
A7-I/O	193	I/O	140	I/O	88	I/O	36
A12-I/O	192	I/O	139	I/O	87	I/O	35
I/O	191	D2-I/O	138	I/O	86	I/O	34
I/O	190	I/O	137	I/O	85	I/O	33
I/O	189	I/O	136	I/O	84	I/O	32
I/O	188	I/O	135	I/O	83	I/O	31
I/O	187	I/O	134	I/O	82	I/O	30
I/O	186	CS1-I/O	133	I/O	81	I/O	29
A6-I/O	185	D3-I/O	132	I/O	80	I/O	28
A13-I/O	184	GND	131	GND	79	VCC	27
VCC	183	VCC	130	VCC	78	GND	26
GND	182	I/O	129	INIT	77	I/O	25
I/O	181	D4-I/O	128	I/O	76	I/O	24
I/O	180	I/O	127	I/O	75	I/O	23
A5-I/O	179	I/O	126	I/O	74	I/O	22
A14-I/O	178	I/O	125	I/O	73	I/O	21
I/O	177	I/O	124	I/O	72	I/O	20
I/O	176	CS0-I/O	123	I/O	71	I/O	19
I/O	175	D5-I/O	122	I/O	70	I/O	18
I/O	174	I/O	121	I/O	69	I/O	17
A4-I/O	173	I/O	120	I/O	68	I/O	14
A15-I/O	172	I/O	119	I/O	67	I/O	13
I/O	171	I/O	118	I/O	66	I/O	12
I/O	169	I/O	117	I/O	63	I/O	11
I/O	168	I/O	116	I/O	62	I/O	10
I/O	167	I/O	115	I/O	61	I/O	9
A3-I/O	166	D6-I/O	114	I/O	60	I/O	8
A2-I/O	165	I/O	113	LDC-I/O	59	I/O	7
I/O	164	I/O	112	I/O	58	I/O	6
I/O	163	I/O	111	I/O	57	I/O	5
I/O	162	I/O	110	I/O	56	I/O	4
I/O	161	XTLX1(OUT)BCLKN-I/O	109	HDC-I/O	55	I/O	3
A1-CS2-I/O	160	D7-I/O	108	M2-I/O	54	TCLKIN-I/O	2
A0-WS-I/O	159	D/P	107	VCC	53	PWRDN	1
GND	158	VCC	106	M0-RTIG	52	GND	208
VCC	157	RESET	105	GND	51	VCC	207
CCLK	156	GND	104	M1/RDATA	50		
DOUT-I/O	155	XTL2(IN)-I/O	103	I/O	49		

Unprogrammed IOBs have a default pull-up. This prevents an undefined pad level for unbonded or unused IOBs. Programmed outputs are default slew-rate limited.

In the PQ208 package, pins 15, 16, 64, 65, 90, 91, 142, 143, 170 and 195 are not connected.

* In PQ208, XC3090A and XC3195A have different pinouts.