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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	144
Number of Logic Elements/Cells	-
Total RAM Bits	30784
Number of I/O	74
Number of Gates	3000
Voltage - Supply	4.75V ~ 5.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	84-LCC (J-Lead)
Supplier Device Package	84-PLCC (29.31x29.31)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc3042a-7pc84c

Detailed Functional Description

The perimeter of configurable Input/Output Blocks (IOBs) provides a programmable interface between the internal logic array and the device package pins. The array of Configurable Logic Blocks (CLBs) performs user-specified logic functions. The interconnect resources are programmed to form networks, carrying logic signals among blocks, analogous to printed circuit board traces connecting MSI/SSI packages.

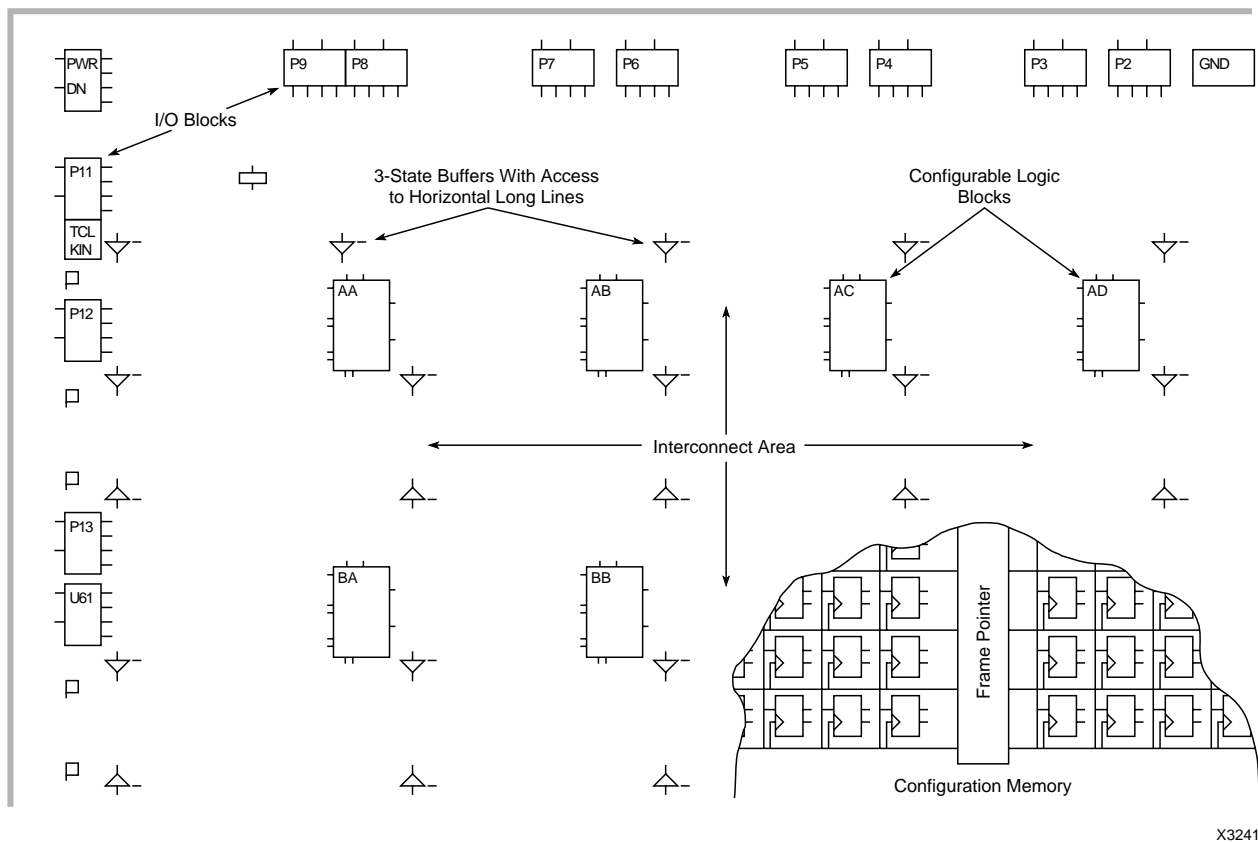
The block logic functions are implemented by programmed look-up tables. Functional options are implemented by program-controlled multiplexers. Interconnecting networks between blocks are implemented with metal segments joined by program-controlled pass transistors.

These FPGA functions are established by a configuration program which is loaded into an internal, distributed array of configuration memory cells. The configuration program is loaded into the device at power-up and may be reloaded on command. The FPGA includes logic and control signals to implement automatic or passive configuration. Program

data may be either bit serial or byte parallel. The development system generates the configuration program bitstream used to configure the device. The memory loading process is independent of the user logic functions.

Configuration Memory

The static memory cell used for the configuration memory in the Field Programmable Gate Array has been designed specifically for high reliability and noise immunity. Integrity of the device configuration memory based on this design is assured even under adverse conditions. As shown in [Figure 3](#), the basic memory cell consists of two CMOS inverters plus a pass transistor used for writing and reading cell data. The cell is only written during configuration and only read during readback. During normal operation, the cell provides continuous control and the pass transistor is off and does not affect cell stability. This is quite different from the operation of conventional memory devices, in which the cells are frequently read and rewritten.



X3241

Figure 2: Field Programmable Gate Array Structure.

It consists of a perimeter of programmable I/O blocks, a core of configurable logic blocks and their interconnect resources. These are all controlled by the distributed array of configuration program memory cells.

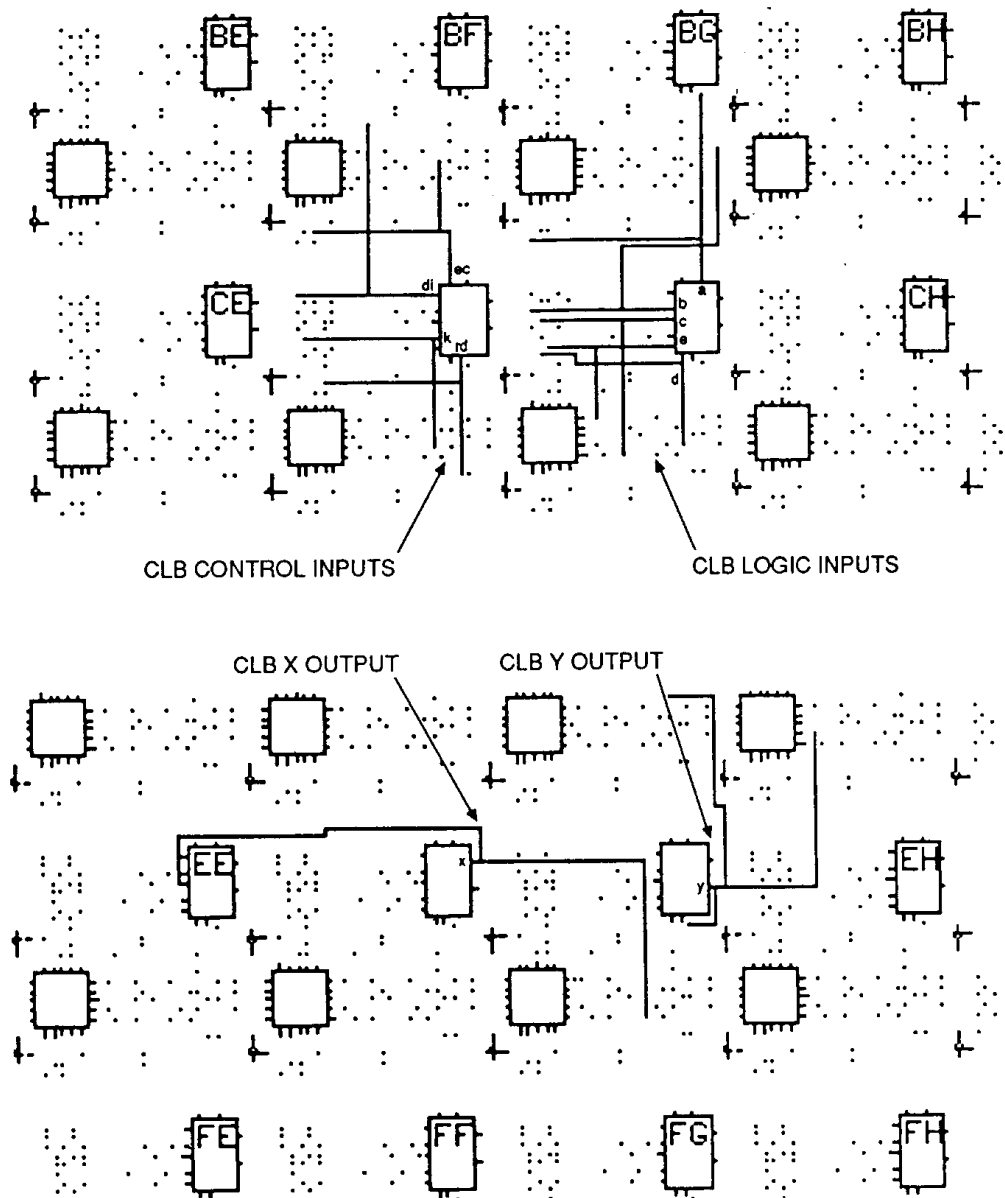


Figure 9: Design Editor Locations of interconnect access, CLB control inputs, logic inputs and outputs. The dot pattern represents the available programmable interconnection points (PIPs).

Some of the interconnect PIPs are directional.

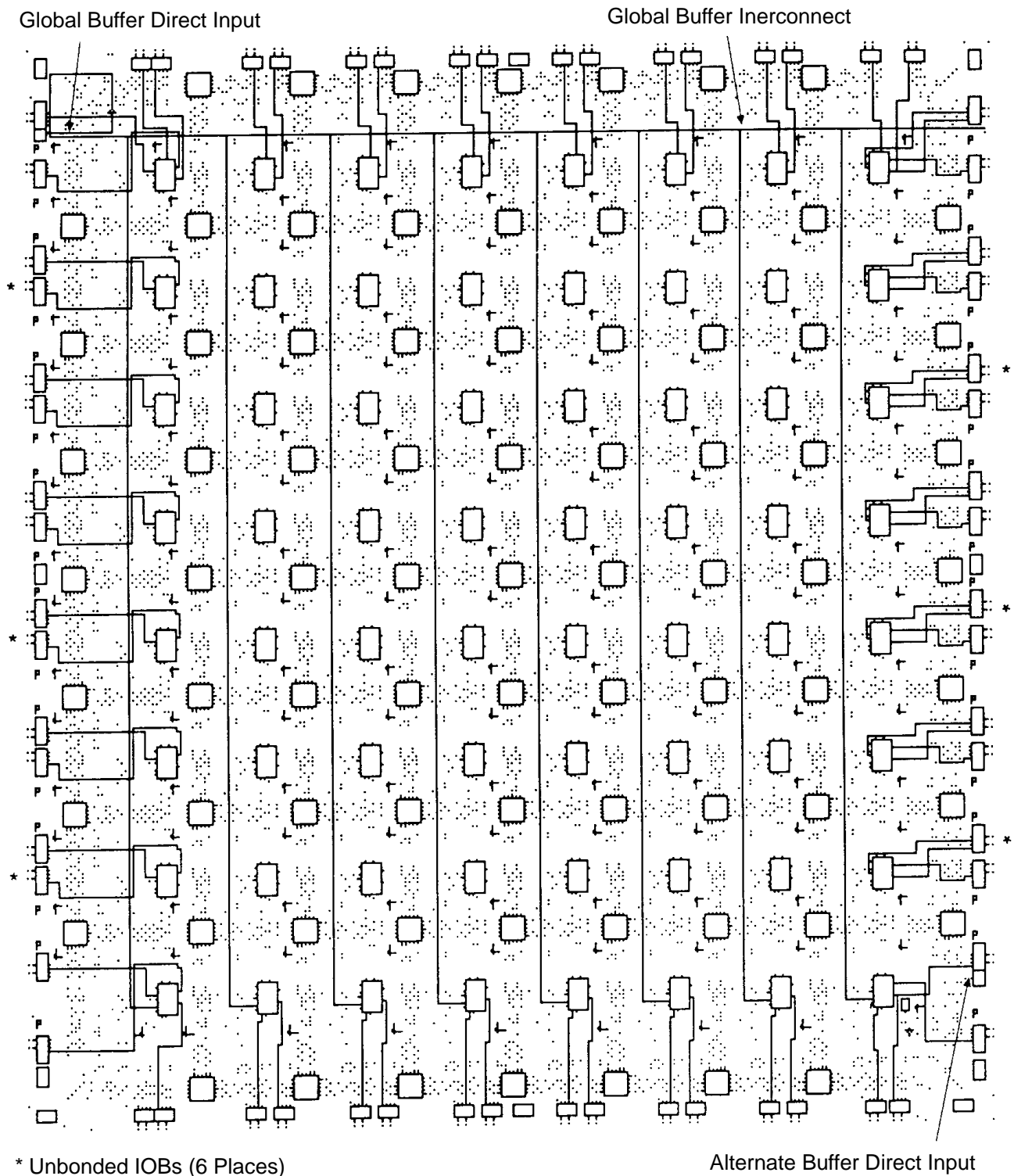


Figure 13: XC3020A Die-Edge IOBs. The XC3020A die-edge IOBs are provided with direct access to adjacent CLBs.

A buffer in the upper left corner of the FPGA chip drives a global net which is available to all K inputs of logic blocks. Using the global buffer for a clock signal provides a skew-free, high fan-out, synchronized clock for use at any or all of the IOBs and CLBs. Configuration bits for the K input to each logic block can select this global line or another routing resource as the clock source for its flip-flops. This net may also be programmed to drive the die edge clock lines for IOB use. An enhanced speed, CMOS threshold, direct access to this buffer is available at the second pad from the top of the left die edge.

A buffer in the lower right corner of the array drives a horizontal Longline that can drive programmed connections to a vertical Longline in each interconnection column. This alternate buffer also has low skew and high fan-out. The network formed by this alternate buffer's Longlines can be selected to drive the K inputs of the CLBs. CMOS threshold, high speed access to this buffer is available from the third pad from the bottom of the right die edge.

Internal Busses

A pair of 3-state buffers, located adjacent to each CLB, permits logic to drive the horizontal Longlines. Logic operation

of the 3-state buffer controls allows them to implement wide multiplexing functions. Any 3-state buffer input can be selected as drive for the horizontal long-line bus by applying a Low logic level on its 3-state control line. See [Figure 16](#). The user is required to avoid contention which can result from multiple drivers with opposing logic levels. Control of the 3-state input by the same signal that drives the buffer input, creates an open-drain wired-AND function. A logic High on both buffer inputs creates a high impedance, which represents no contention. A logic Low enables the buffer to drive the Longline Low. See [Figure 17](#). Pull-up resistors are available at each end of the Longline to provide a High output when all connected buffers are non-conducting. This forms fast, wide gating functions. When data drives the inputs, and separate signals drive the 3-state control lines, these buffers form multiplexers (3-state buses). In this case, care must be used to prevent contention through multiple active buffers of conflicting levels on a common line. Each horizontal Longline is also driven by a weak keeper circuit that prevents undefined floating levels by maintaining the previous logic level when the line is not driven by an active buffer or a pull-up resistor. [Figure 18](#) shows 3-state buffers, Longlines and pull-up resistors.

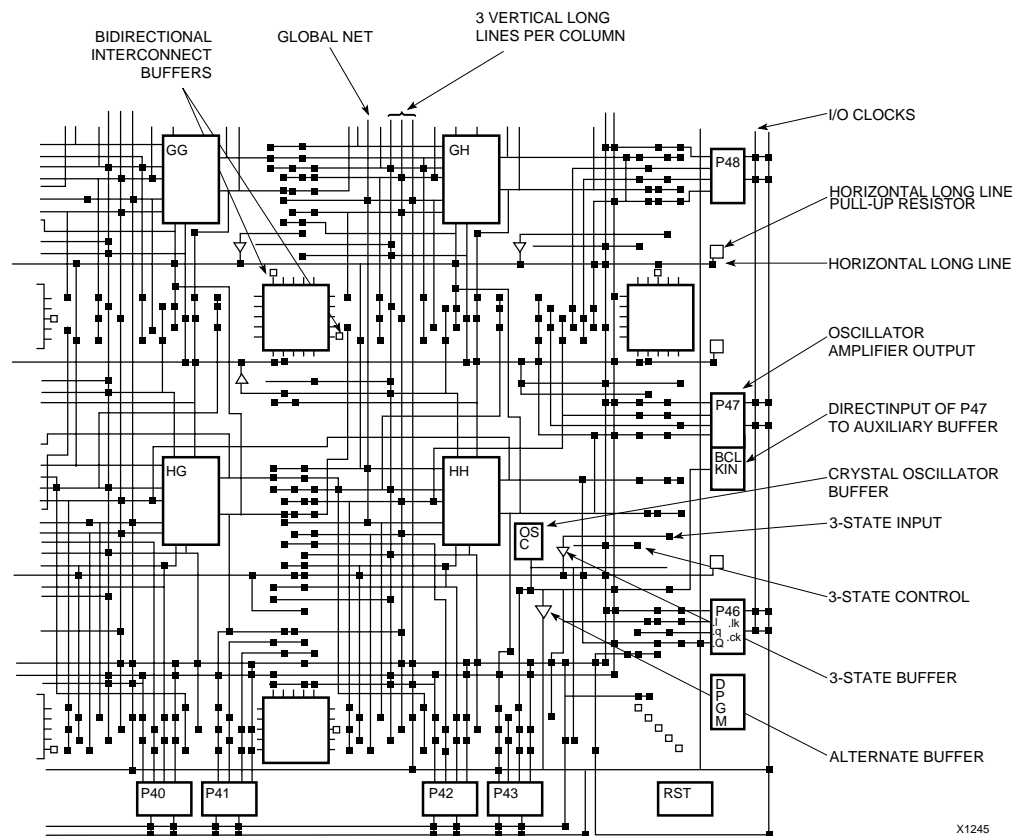


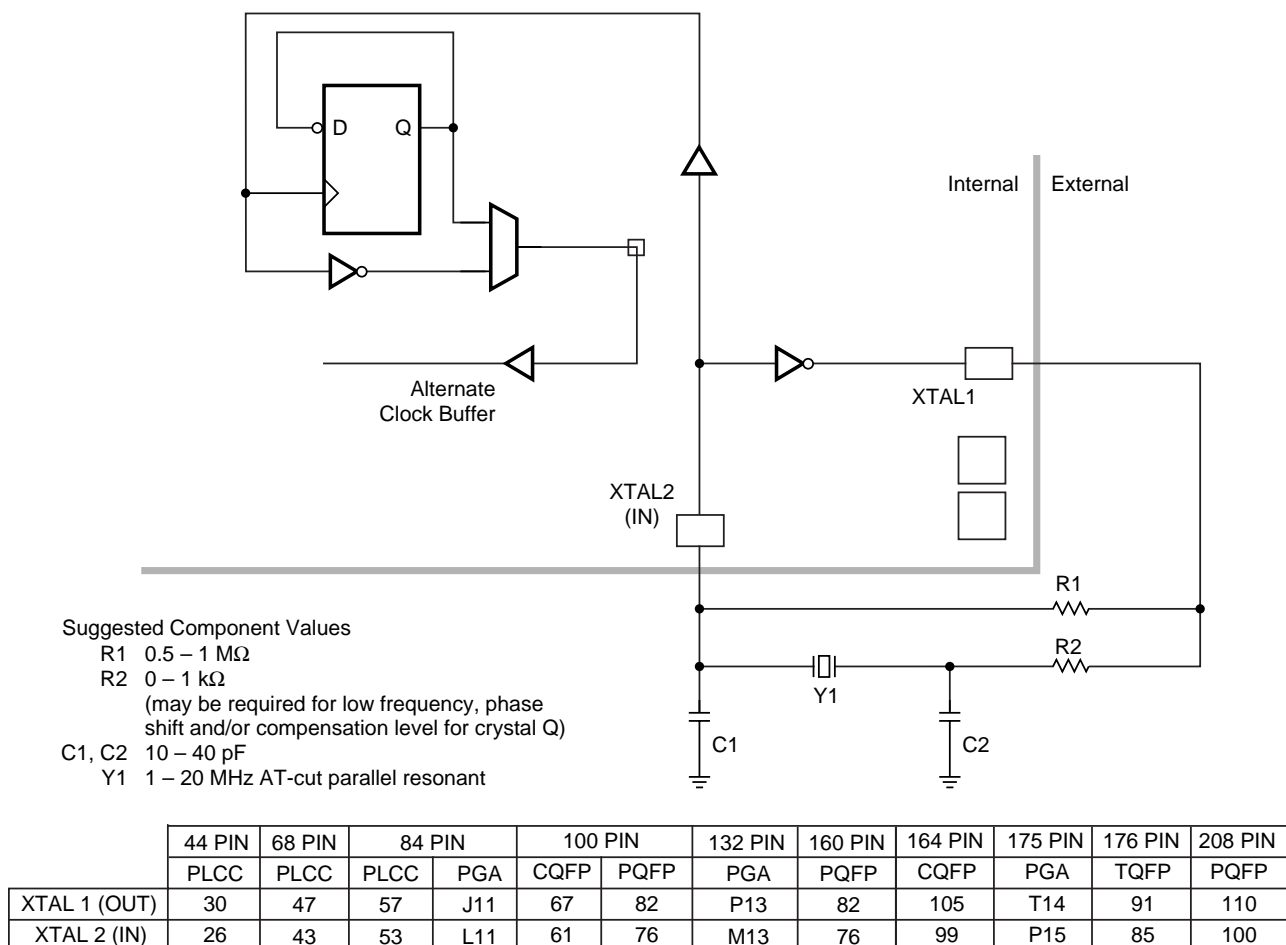
Figure 18: Design Editor.

An extra large view of possible interconnections in the lower right corner of the XC3020A.

Crystal Oscillator

Figure 18 also shows the location of an internal high speed inverting amplifier that may be used to implement an on-chip crystal oscillator. It is associated with the auxiliary buffer in the lower right corner of the die. When the oscillator is configured and connected as a signal source, two special user IOBs are also configured to connect the oscillator amplifier with external crystal oscillator components as shown in Figure 19. A divide by two option is available to assure symmetry. The oscillator circuit becomes active early in the configuration process to allow the oscillator to stabilize. Actual internal connection is delayed until completion of configuration. In Figure 19 the feedback resistor R1, between the output and input, biases the amplifier at threshold. The inversion of the amplifier, together with the R-C networks and an AT-cut series resonant crystal, produce the 360-degree phase shift of the Pierce oscillator. A

series resistor R2 may be included to add to the amplifier output impedance when needed for phase-shift control, crystal resistance matching, or to limit the amplifier input swing to control clipping at large amplitudes. Excess feedback voltage may be corrected by the ratio of C2/C1. The amplifier is designed to be used from 1 MHz to about one-half the specified CLB toggle frequency. Use at frequencies below 1 MHz may require individual characterization with respect to a series resistance. Crystal oscillators above 20 MHz generally require a crystal which operates in a third overtone mode, where the fundamental frequency must be suppressed by an inductor across C2, turning this parallel resonant circuit to double the fundamental crystal frequency, i.e., 2/3 of the desired third harmonic frequency. When the oscillator inverter is not used, these IOBs and their package pins are available for general user I/O.



X7064

Figure 19: Crystal Oscillator Inverter. When activated, and by selecting an output network for its buffer, the crystal oscillator inverter uses two unconfigured package pins and external components to implement an oscillator. An optional divide-by-two mode is available to assure symmetry.

Configuration

Initialization Phase

An internal power-on-reset circuit is triggered when power is applied. When V_{CC} reaches the voltage at which portions of the FPGA device begin to operate (nominally 2.5 to 3 V), the programmable I/O output buffers are 3-stated and a high-impedance pull-up resistor is provided for the user I/O pins. A time-out delay is initiated to allow the power supply voltage to stabilize. During this time the power-down mode is inhibited. The Initialization state time-out (about 11 to 33 ms) is determined by a 14-bit counter driven by a self-generated internal timer. This nominal 1-MHz timer is subject to variations with process, temperature and power supply. As shown in Table 1, five configuration mode choices are available as determined by the input levels of three mode pins; M0, M1 and M2.

Table 1: Configuration Mode Choices

M0	M1	M2	CCLK	Mode	Data
0	0	0	output	Master	Bit Serial
0	0	1	output	Master	Byte Wide Addr. = 0000 up
0	1	0	—	reserved	—
0	1	1	output	Master	Byte Wide Addr. = FFFF down
1	0	0	—	reserved	—
1	0	1	output	Peripheral	Byte Wide
1	1	0	—	reserved	—
1	1	1	input	Slave	Bit Serial

In Master configuration modes, the device becomes the source of the Configuration Clock (CCLK). The beginning of configuration of devices using Peripheral or Slave modes must be delayed long enough for their initialization to be completed. An FPGA with mode lines selecting a Master configuration mode extends its initialization state using four times the delay (43 to 130 ms) to assure that all daisy-chained slave devices, which it may be driving, will be ready even if the master is very fast, and the slave(s) very slow. Figure 20 shows the state sequences. At the end of Initialization, the device enters the Clear state where it clears the configuration memory. The active Low, open-drain initialization signal \overline{INIT} indicates when the Initialization and Clear states are complete. The FPGA tests for the absence of an external active Low \overline{RESET} before it makes a final sample of the mode lines and enters the Configuration state. An external wired-AND of one or more \overline{INIT} pins can be used to control configuration by the assertion of the active-Low \overline{RESET} of a master mode device or to signal a processor that the FPGAs are not yet initialized.

If a configuration has begun, a re-assertion of \overline{RESET} for a minimum of three internal timer cycles will be recognized and the FPGA will initiate an abort, returning to the Clear state to clear the partially loaded configuration memory words. The FPGA will then resample \overline{RESET} and the mode lines before re-entering the Configuration state.

During configuration, the XC3000A, XC3000L, XC3100A, and XC3100L devices check the bit-stream format for stop bits in the appropriate positions. Any error terminates the configuration and pulls \overline{INIT} Low.

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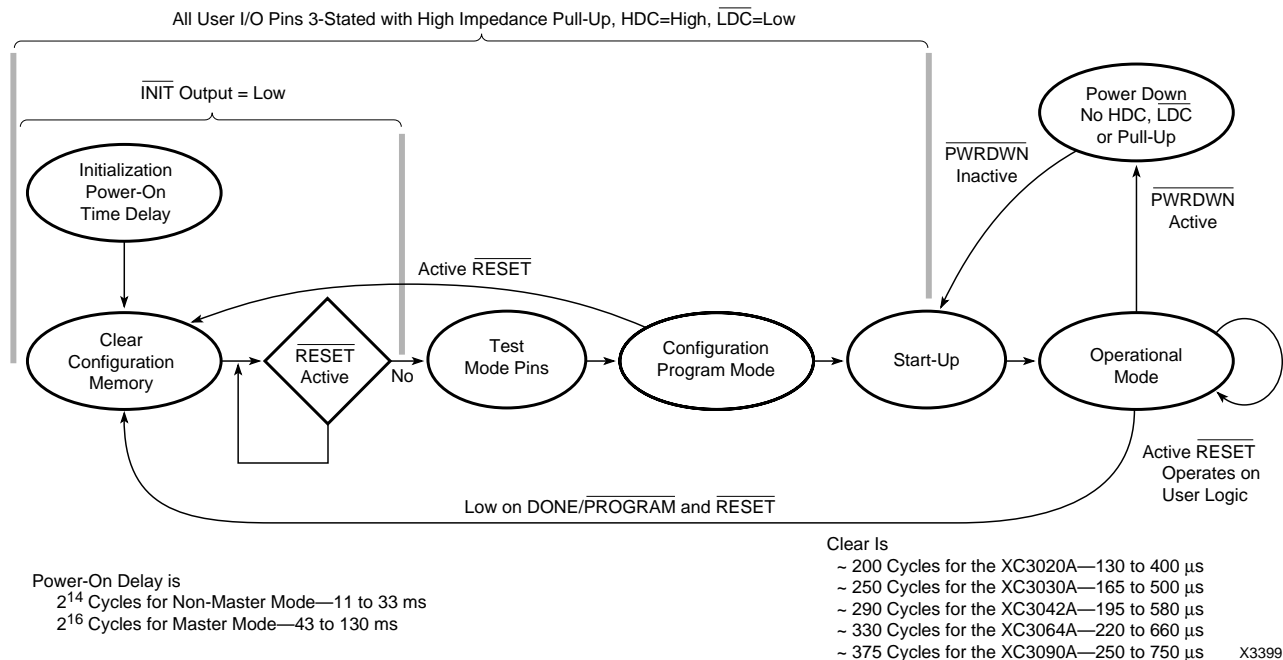


Figure 20: A State Diagram of the Configuration Process for Power-up and Reprogram.

be used to drive the remaining unused routing, as that might affect timing of user nets. Tie can be omitted for quick breadboard iterations where a few additional milliamps of Icc are acceptable.

The configuration bitstream begins with eight High preamble bits, a 4-bit preamble code and a 24-bit length count. When configuration is initiated, a counter in the FPGA is set to zero and begins to count the total number of configuration clock cycles applied to the device. As each configuration data frame is supplied to the device, it is internally assembled into a data word, which is then loaded in parallel into one word of the internal configuration memory array. The configuration loading process is complete when the current length count equals the loaded length count and the required configuration program data frames have been written. Internal user flip-flops are held Reset during configuration.

Two user-programmable pins are defined in the unconfigured Field Programmable Gate Array. High During Configuration (HDC) and Low During Configuration (LDC) as well as DONE/PROG may be used as external control signals during configuration. In Master mode configurations it is convenient to use LDC as an active-Low EPROM Chip Enable. After the last configuration data bit is loaded and the length count compares, the user I/O pins become active. Options allow timing choices of one clock earlier or later for the timing of the end of the internal logic RESET and the assertion of the DONE signal. The open-drain DONE/PROG output can be AND-tied with multiple devices and used as an active-High READY, an active-Low PROM enable or a RESET to other portions of the system. The state diagram of Figure 20 illustrates the configuration process.

Configuration Modes

Master Mode

In Master mode, the FPGA automatically loads configuration data from an external memory device. There are three Master modes that use the internal timing source to supply the configuration clock (CCLK) to time the incoming data. Master Serial mode uses serial configuration data supplied to Data-in (DIN) from a synchronous serial source such as the Xilinx Serial Configuration PROM shown in Figure 23. Master Parallel Low and High modes automatically use parallel data supplied to the D0–D7 pins in response to the 16-bit address generated by the FPGA. Figure 25 shows an example of the parallel Master mode connections required. The HEX starting address is 0000 and increments for Master Low mode and it is FFFF and decrements for Master High mode. These two modes provide address compatibility with microprocessors which begin execution from opposite ends of memory.

Peripheral Mode

Peripheral mode provides a simplified interface through which the device may be loaded byte-wide, as a processor peripheral. Figure 27 shows the peripheral mode connections. Processor write cycles are decoded from the common assertion of the active low Write Strobe (WS), and two active low and one active high Chip Selects (CS0, CS1, CS2). The FPGA generates a configuration clock from the internal timing generator and serializes the parallel input data for internal framing or for succeeding slaves on Data Out (DOUT). A output High on READY/BUSY pin indicates the completion of loading for each byte when the input register is ready for a new byte. As with Master modes, Peripheral mode may also be used as a lead device for a daisy-chain of slave devices.

Slave Serial Mode

Slave Serial mode provides a simple interface for loading the Field Programmable Gate Array configuration as shown in Figure 29. Serial data is supplied in conjunction with a synchronizing input clock. Most Slave mode applications are in daisy-chain configurations in which the data input is driven from the previous FPGA's data out, while the clock is supplied by a lead device in Master or Peripheral mode. Data may also be supplied by a processor or other special circuits.

Daisy Chain

The development system is used to create a composite configuration for selected FPGAs including: a preamble, a length count for the total bitstream, multiple concatenated data programs and a postamble plus an additional fill bit per device in the serial chain. After loading and passing-on the preamble and length count to a possible daisy-chain, a lead device will load its configuration data frames while providing a High DOUT to possible down-stream devices as shown in Figure 25. Loading continues while the lead device has received its configuration program and the current length count has not reached the full value. The additional data is passed through the lead device and appears on the Data Out (DOUT) pin in serial form. The lead device also generates the Configuration Clock (CCLK) to synchronize the serial output data and data in of down-stream FPGAs. Data is read in on DIN of slave devices by the positive edge of CCLK and shifted out the DOUT on the negative edge of CCLK. A parallel Master mode device uses its internal timing generator to produce an internal CCLK of 8 times its EPROM address rate, while a Peripheral mode device produces a burst of 8 CCLKs for each chip select and write-strobe cycle. The internal timing generator continues to operate for general timing and synchronization of inputs in all modes.

Master Serial Mode

The SPROM CE input can be driven from either $\overline{\text{LDC}}$ or DONE. Using $\overline{\text{LDC}}$ avoids potential contention on the DIN pin, if this pin is configured as user-I/O, but $\overline{\text{LDC}}$ is then restricted to be a permanently High user output. Using DONE also avoids contention on DIN, provided the early DONE option is invoked.

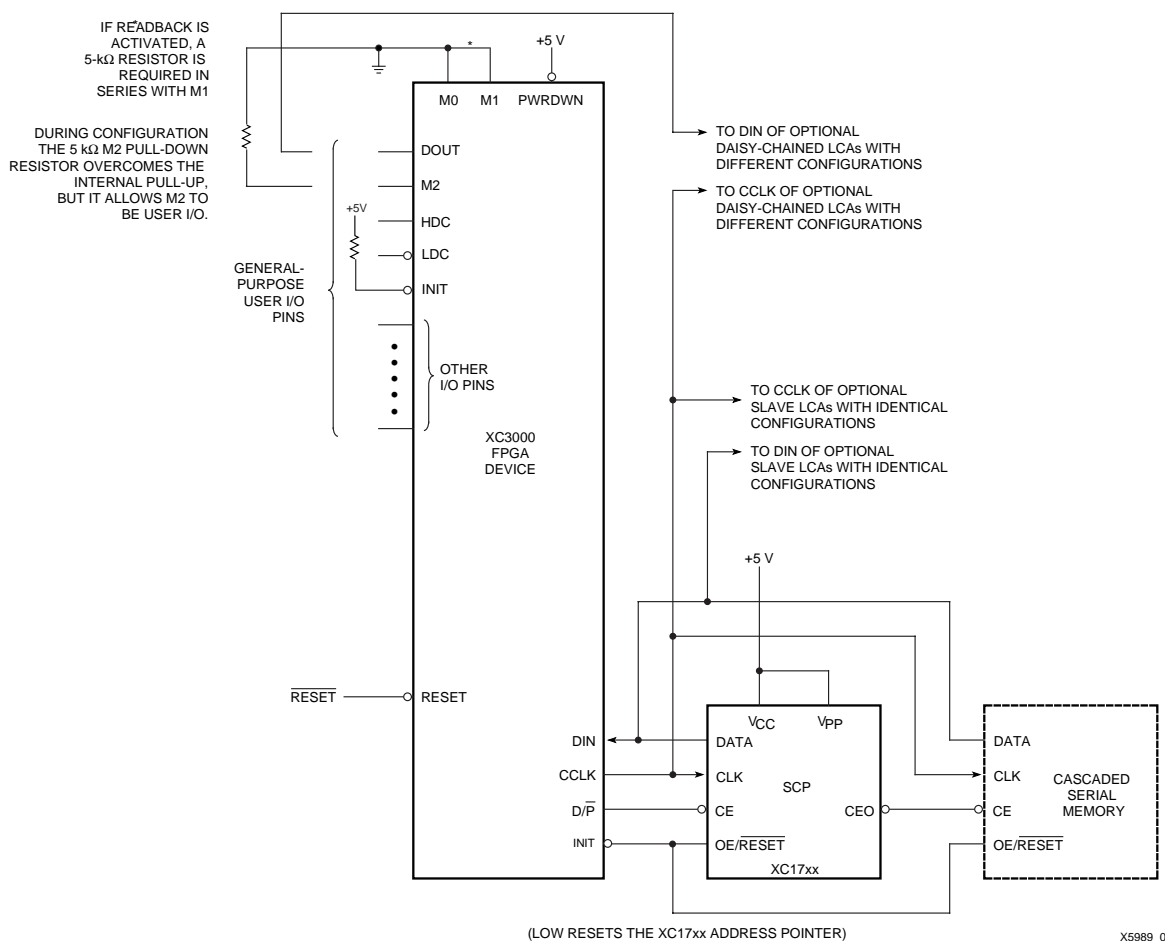
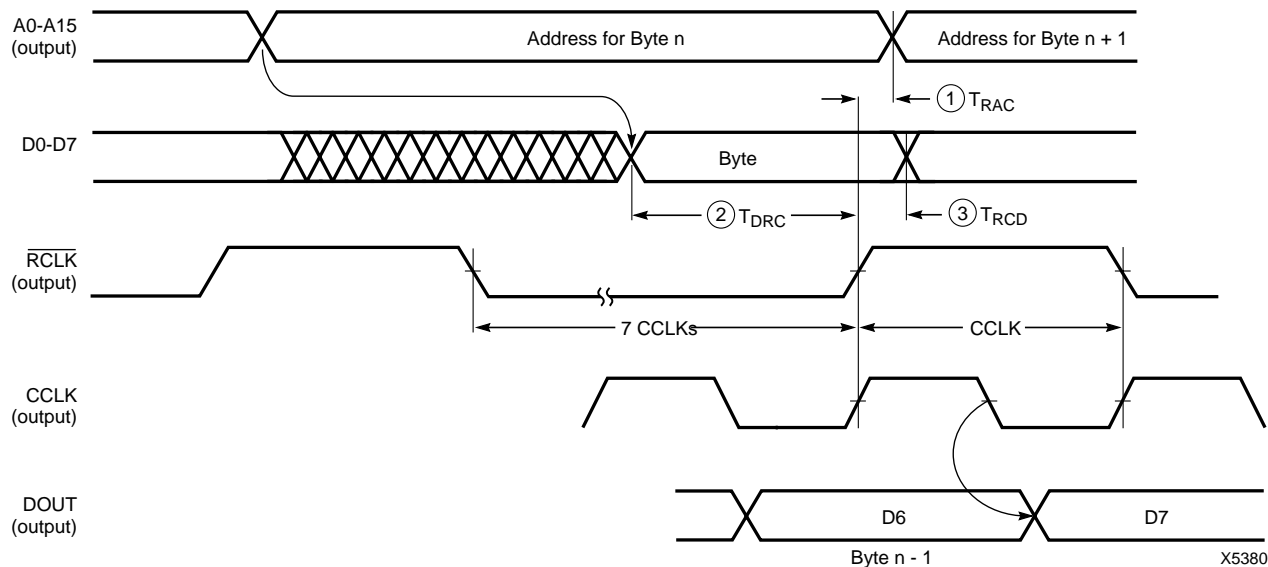


Figure 23: Master Serial Mode Circuit Diagram



	Description	Symbol	Min	Max	Units
RCLK	To address valid	1 T _{RAC}	0	200	ns
	To data setup	2 T _{DRC}	60		ns
	To data hold	3 T _{RCD}	0		ns
	RCLK High	T _{RCH}	600		ns
	RCLK Low	T _{RCL}	4.0		μs

- Notes:
1. At power-up, V_{CC} must rise from 2.0 V to V_{CC} min in less than 25 ms. If this is not possible, configuration can be delayed by holding RESET Low until V_{CC} has reached 4.0 V (2.5 V for the XC3000L). A very long V_{CC} rise time of >100 ms, or a non-monotonically rising V_{CC} may require a >6-μs High level on RESET, followed by a >6-μs Low level on RESET and D/P after V_{CC} has reached 4.0 V (2.5 V for the XC3000L).
 2. Configuration can be controlled by holding RESET Low with or until after the INIT of all daisy-chain slave-mode devices is High.

*This timing diagram shows that the EPROM requirements are extremely relaxed:
EPROM access time can be longer than 4000 ns. EPROM data output has no hold time requirements.*

Figure 26: Master Parallel Mode Programming Switching Characteristics

Peripheral Mode

Peripheral mode uses the trailing edge of the logic AND condition of the $\overline{CS0}$, $\overline{CS1}$, $\overline{CS2}$, and \overline{WS} inputs to accept byte-wide data from a microprocessor bus. In the lead FPGA, this data is loaded into a double-buffered UART-like parallel-to-serial converter and is serially shifted into the internal logic. The lead FPGA presents the preamble data (and all data that overflows the lead device) on the DOUT pin.

The Ready/Busy output from the lead device acts as a handshake signal to the microprocessor. $\overline{RDY/BUSY}$ goes Low when a byte has been received, and goes High again

when the byte-wide input buffer has transferred its information into the shift register, and the buffer is ready to receive new data. The length of the \overline{BUSY} signal depends on the activity in the UART. If the shift register had been empty when the new byte was received, the \overline{BUSY} signal lasts for only two CCLK periods. If the shift register was still full when the new byte was received, the \overline{BUSY} signal can be as long as nine CCLK periods.

Note that after the last byte has been entered, only seven of its bits are shifted out. CCLK remains High with DOUT equal to bit 6 (the next-to-last bit) of the last byte entered.

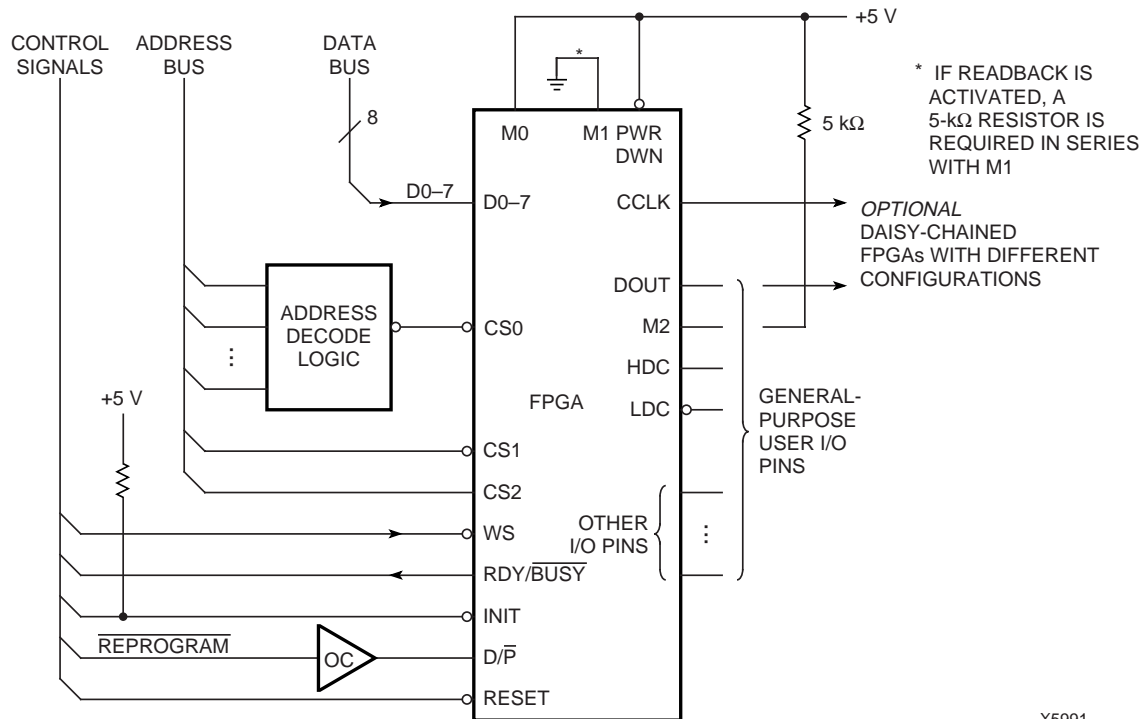
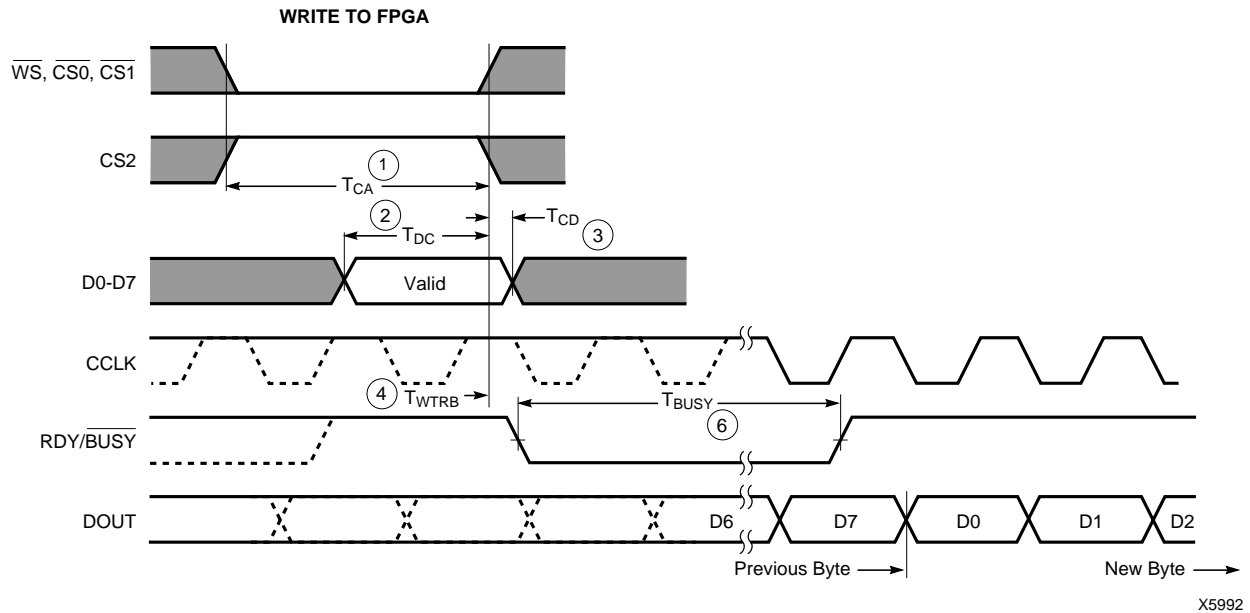


Figure 27: Peripheral Mode Circuit Diagram



	Description	Symbol	Min	Max	Units
WRITE	Effective Write time required (Assertion of $\overline{CS0}$, $\overline{CS1}$, $\overline{CS2}$, \overline{WS})	1 T_{CA}	100		ns
	DIN Setup time required	2 T_{DC}	60		ns
	DIN Hold time required	3 T_{CD}	0		ns
	RDY/BUSY delay after end of WS	4 T_{WTRB}		60	ns
RDY	Earliest next WS after end of BUSY	5 T_{RBWT}	0		ns
	BUSY Low time generated	6 T_{BUSY}	2.5	9	CCLK periods

- Notes:
1. At power-up, V_{CC} must rise from 2.0 V to V_{CC} min in less than 25 ms. If this is not possible, configuration can be delayed by holding \overline{RESET} Low until V_{CC} has reached 4.0 V (2.5 V for the XC3000L). A very long V_{CC} rise time of >100 ms, or a non-monotonically rising V_{CC} may require a >6- μ s High level on \overline{RESET} , followed by a >6- μ s Low level on \overline{RESET} and $\overline{D/P}$ after V_{CC} has reached 4.0 V (2.5 V for the XC3000L).
 2. Configuration must be delayed until the INIT of all FPGAs is High.
 3. Time from end of WS to CCLK cycle for the new byte of data depends on completion of previous byte processing and the phase of the internal timing generator for CCLK.
 4. CCLK and DOUT timing is tested in slave mode.
 5. T_{BUSY} indicates that the double-buffered parallel-to-serial converter is not yet ready to receive new data. The shortest T_{BUSY} occurs when a byte is loaded into an empty parallel-to-serial converter. The longest T_{BUSY} occurs when a new word is loaded into the input register before the second-level buffer has started shifting out data.

Note: This timing diagram shows very relaxed requirements: Data need not be held beyond the rising edge of \overline{WS} . \overline{BUSY} will go active within 60 ns after the end of WS. \overline{BUSY} will stay active for several microseconds. \overline{WS} may be asserted immediately after the end of \overline{BUSY} .

Figure 28: Peripheral Mode Programming Switching Characteristics

Pin Functions During Configuration

Configuration Mode <M2:M1:M0>					***		**										****		
SLAVE SERIAL <1:1:1>	MASTER- SERIAL <0:0:0>	PERIPH <1:0:1>	MASTER- HIGH <1:1:0>	MASTER- LOW <1:0:0>	44 PLCC	64 VQFP	68 PLCC	84 PLCC	84 PGA	100 PQFP	100 VQFP TQFP	132 PGA	144 TQFP	160 PQFP	175 PGA	176 TQFP	208 PQFP	User Function	
POWER DWN (I)	POWER DWN (I)	POWER DWN (I)	POWER DWN (I)	POWER DWN (I)	7	17	10	12	B2	29	26	A1	1	159	B2	1	3	POWER DWN (1)	
M1 (HIGH) (I)	M1 (LOW) (I)	M1 (LOW) (I)	M1 (HIGH) (I)	M1 (LOW) (I)	16	31	25	31	J2	52	49	B13	36	40	B14	45	48	RDATA	
M0 (HIGH) (I)	M0 (LOW) (I)	M0 (HIGH) (I)	M0 (LOW) (I)	M0 (LOW) (I)	17	32	26	32	L1	54	51	A14	38	42	B15	47	50	RTRIG (I)	
M2 (HIGH) (I)	M2 (LOW) (I)	M2 (HIGH) (I)	M2 (HIGH) (I)	M2 (HIGH) (I)	18	33	27	33	K2	56	53	C13	40	44	C15	49	56	I/O	
HDC (HIGH)	HDC (HIGH)	HDC (HIGH)	HDC (HIGH)	HDC (HIGH)	19	34	28	34	K3	57	54	B14	41	45	E14	50	57	I/O	
LDC (LOW)	LDC (LOW)	LDC (LOW)	LDC (LOW)	LDC (LOW)	20	36	30	36	L3	59	56	D14	45	49	D16	54	61	I/O	
INIT*	INIT*	INIT*	INIT*	INIT*	22	40	34	42	K6	65	62	G14	53	59	H15	65	77	I/O	
GND	GND	GND	GND	GND	23	41	35	43	J6	66	63	H12	55	61	J14	67	79	GND	
					26	47	43	53	L11	76	73	M13	69	76	P15	85	100	XTL2 OR I/O	
RESET (I)	RESET (I)	RESET (I)	RESET (I)	RESET (I)	27	48	44	54	K10	78	75	P14	71	78	R15	87	102	RESET (I)	
DONE	DONE	DONE	DONE	DONE	28	49	45	55	J10	80	77	N13	73	80	R14	89	107	PROGRAM (I)	
		DATA 7 (I)	DATA 7 (I)	DATA 7 (I)		50	46	56	K11	81	78	M12	74	81	N13	90	109	I/O	
						30	51	47	57	J11	82	79	P13	75	82	T14	91	110	XTL1 OR I/O
		DATA 6 (I)	DATA 6 (I)	DATA 6 (I)		52	48	58	H10	83	80	N11	78	86	P12	96	115	I/O	
		DATA 5 (I)	DATA 5 (I)	DATA 5 (I)		53	49	60	F10	87	84	M9	84	92	T11	102	122	I/O	
		CS0 (I)				54	50	61	G10	88	85	N9	85	93	R10	103	123	I/O	
		DATA 4 (I)	DATA 4 (I)	DATA 4 (I)		55	51	62	G11	89	86	N8	88	96	R9	108	128	I/O	
		DATA 3 (I)	DATA 3 (I)	DATA 3 (I)		57	53	65	F11	92	89	N7	92	102	P8	112	132	I/O	
		CS1 (I)				58	54	66	E11	93	90	P6	93	103	R8	113	133	I/O	
		DATA 2 (I)	DATA 2 (I)	DATA 2 (I)		59	55	67	E10	94	91	M6	96	106	R7	118	138	I/O	
		DATA 1 (I)	DATA 1 (I)	DATA 1 (I)		60	56	70	D10	98	95	M5	102	114	R5	124	145	I/O	
		RDY/BUSY	RCLK	RCLK		61	57	71	C11	99	96	N4	103	115	P5	125	146	I/O	
		DATA 0 (I)	DATA 0 (I)	DATA 0 (I)	38	62	58	72	B11	100	97	N2	106	119	R3	130	151	I/O	
		DOUT	DOUT	DOUT	39	63	59	73	C10	1	98	M3	107	120	N4	131	152	I/O	
		CCLK (I)	CCLK (O)	CCLK (O)	CCLK (O)	40	64	60	74	A11	2	99	P1	108	121	R2	132	153	CCLK (I)
				WS (I)	A0	A0		1	61	75	B10	5	2	M2	111	124	P2	135	161
CS2 (I)	A1			A1		2	62	76	B9	6	3	N1	112	125	M3	136	162	I/O	
				A2	A2		3	63	77	A10	8	5	L2	115	128	P1	140	165	I/O
				A3	A3		4	64	78	A9	9	6	L1	116	129	N1	141	166	I/O
				A15	A15			65	81	B6	12	9	K1	119	132	M1	146	172	5
				A4	A4		5	66	82	B7	13	10	J2	120	133	L2	147	173	I/O
				A14	A14		6	67	83	A7	14	11	H1	123	136	K2	150	178	I/O
				A5	A5		7	68	84	C7	15	12	H2	124	137	K1	151	179	I/O
				A13	A13		9	2	2	A6	17	14	G2	128	141	H2	156	184	I/O
				A6	A6		10	3	3	A5	18	15	G1	129	142	H1	157	185	I/O
				A12	A12		11	4	4	B5	19	16	F2	133	147	F2	164	192	I/O
				A7	A7		12	5	5	C5	20	17	E1	134	148	E1	165	193	I/O
		A11	A11		13	6	8	A3	23	20	D1	137	151	D1	169	199	I/O		
		A8	A8		14	7	9	A2	24	21	D2	138	152	C1	170	200	I/O		
		A10	A10		15	8	10	B3	25	22	B1	141	155	E3	173	203	I/O		
		A9	A9		16	9	11	A1	26	26	C2	142	156	C2	174	204	I/O		
																		All Others	
					X	X	X	X	X	X									XC3x20A etc. XC3x30A etc.
								X	X	X	X	X	X						XC3x42A etc. XC3x64A etc.
								X**					X	X					XC3x90A etc. XC3195A
								X**					X	X	X	X	X	X	
								X**						X	X		X	X	
Notes:																			

Notes:

Generic I/O pins are not shown.

For a detailed description of the configuration modes, see [page 25](#) through [page 34](#).

For pinout details, see [page 65](#) through [page 76](#).

Represents a weak pull-up before and during configuration.

* INIT is an open drain output during configuration.

(I) Represents an input.

** Pin assignment for the XC3064A/XC3090A and XC3195A differ from those shown.

*** Peripheral mode and master parallel mode are not supported in the PC44 package.

**** Pin assignments for the XC3195A PQ208 differ from those shown.

Pin assignments of PGA Footprint PLCC sockets and PGA packages are not identical.

The information on this page is provided as a convenient summary. For detailed pin descriptions, see the preceding two pages.

Note: Before and during configuration, all outputs that are not used for the configuration process are 3-stated with a weak pull-up resistor.

XC3000A Switching Characteristics

Xilinx maintains test specifications for each product as controlled documents. To insure the use of the most recently released device performance parameters, please request a copy of the current test-specification revision.

XC3000A Operating Conditions

Symbol	Description	Min	Max	Units
V_{CC}	Supply voltage relative to GND Commercial 0°C to +85°C junction	4.75	5.25	V
	Supply voltage relative to GND Industrial -40°C to +100°C junction	4.5	5.5	V
V_{IHT}	High-level input voltage — TTL configuration	2.0	V_{CC}	V
V_{ILT}	Low-level input voltage — TTL configuration	0	0.8	V
V_{IHC}	High-level input voltage — CMOS configuration	70%	100%	V_{CC}
V_{ILC}	Low-level input voltage — CMOS configuration	0	20%	V_{CC}
T_{IN}	Input signal transition time		250	ns

Note: At junction temperatures above those listed as Operating Conditions, all delay parameters increase by 0.3% per °C.

XC3000A DC Characteristics Over Operating Conditions

Symbol	Description	Min	Max	Units
V_{OH}	High-level output voltage (@ $I_{OH} = -4.0$ mA, V_{CC} min)	3.86		V
V_{OL}	Low-level output voltage (@ $I_{OL} = 4.0$ mA, V_{CC} min)		0.40	V
V_{OH}	High-level output voltage (@ $I_{OH} = -4.0$ mA, V_{CC} min)	3.76		V
V_{OL}	Low-level output voltage (@ $I_{OL} = 4.0$ mA, V_{CC} min)		0.40	V
V_{CCPD}	Power-down supply voltage (PWRDWN must be Low)	2.30		V
I_{CCPD}	Power-down supply current ($V_{CC(MAX)}$ @ T_{MAX})		100	μA
		3020A	160	μA
		3030A	240	μA
		3064A	340	μA
		3090A	500	μA
I_{CCO}	Quiescent FPGA supply current in addition to I_{CCPD}		500	μA
	Chip thresholds programmed as CMOS levels		10	μA
	Chip thresholds programmed as TTL levels			
I_{IL}	Input Leakage Current	-10	+10	μA
C_{IN}	Input capacitance, all packages except PGA175 (sample tested)			
	All Pins except XTL1 and XTL2		10	pF
	XTL1 and XTL2		15	pF
	Input capacitance, PGA 175 (sample tested)			
	All Pins except XTL1 and XTL2		16	pF
	XTL1 and XTL2		20	pF
I_{RIN}	Pad pull-up (when selected) @ $V_{IN} = 0$ V ³	0.02	0.17	mA
I_{RLL}	Horizontal Longline pull-up (when selected) @ logic Low		3.4	mA

- Notes:**
1. With no output current loads, no active input or Longline pull-up resistors, all package pins at V_{CC} or GND, and the FPGA device configured with a tie option.
 2. Total continuous output sink current may not exceed 100 mA per ground pin. Total continuous output source may not exceed 100 mA per V_{CC} pin. The number of ground pins varies from the XC3020A to the XC3090A.
 3. Not tested. Allow an undriven pin to float High. For any other purposes use an external pull-up.

XC3000A CLB Switching Characteristics Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Since many internal timing parameters cannot be measured directly, they are derived from benchmark timing patterns. The following guidelines reflect worst-case values over the recommended operating conditions. For more detailed, more precise, and more up-to-date timing information, use the values provided by the timing calculator and used in the simulator.

		Speed Grade		-7		-6		
Description		Symbol		Min	Max	Min	Max	Units
Combinatorial Delay Logic Variables A, B, C, D, E, to outputs X or Y FG Mode F and FGM Mode		1	T_{ILO}		5.1		4.1	ns
					5.6		4.6	ns
Sequential delay Clock k to outputs X or Y Clock k to outputs X or Y when Q is returned through function generators F or G to drive X or Y FG Mode F and FGM Mode		8	T_{CKO}		4.5		4.0	ns
			T_{QLO}		9.5		8.0	ns
					10.0		8.5	ns
Set-up time before clock K Logic Variables A, B, C, D, E FG Mode F and FGM Mode Data In DI Enable Clock EC		2	T_{ICK}	4.5		3.5		ns
				5.0		4.0		ns
		4	T_{DICK}	4.0		3.0		ns
		6	T_{ECKK}	4.5		4.0		ns
Hold Time after clock K Logic Variables A, B, C, D, E Data In DI ² Enable Clock EC		3	T_{CKI}	0		0		ns
		5	T_{CKDI}	1.0		1.0		ns
		7	T_{CKEC}	2.0		2.0		ns
Clock Clock High time Clock Low time Max. flip-flop toggle rate		11	T_{CH}	4.0		3.5		ns
		12	T_{CL}	4.0		3.5		ns
			F_{CLK}	113.0		135.0		MHz
Reset Direct (RD) RD width delay from RD to outputs X or Y		13	T_{RPW}	6.0		5.0		ns
		9	T_{RIO}		6.0		5.0	ns
Global Reset (RESET Pad) ¹ RESET width (Low) delay from RESET pad to outputs X or Y			T_{MRW}	16.0		14.0		ns
			T_{MRQ}		19.0		17.0	ns

- Notes:** 1. Timing is based on the XC3042A, for other devices see timing calculator.
2. The CLB K to Q output delay (T_{CKO} , #8) of any CLB, plus the shortest possible interconnect delay, is always longer than the Data In hold time requirement (T_{CKDI} , #5) of any CLB on the same die.

XC3000A IOB Switching Characteristics Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Since many internal timing parameters cannot be measured directly, they are derived from benchmark timing patterns. The following guidelines reflect worst-case values over the recommended operating conditions. For more detailed, more precise, and more up-to-date timing information, use the values provided by the timing calculator and used in the simulator.

Description	Speed Grade		-7		-6		Units
	Symbol		Min	Max	Min	Max	
Propagation Delays (Input)							
Pad to Direct In (I)	3	T _{PID}		4.0		3.0	ns
Pad to Registered In (Q) with latch transparent		T _{PTG}		15.0		14.0	ns
Clock (IK) to Registered In (Q)	4	T _{IKRI}		3.0		2.5	ns
Set-up Time (Input)							
Pad to Clock (IK) set-up time	1	T _{PICK}	14.0		12.0		ns
Propagation Delays (Output)							
Clock (OK) to Pad (fast)	7	T _{OKPO}		8.0		7.0	ns
same (slew rate limited)	7	T _{OKPO}		18.0		15.0	ns
Output (O) to Pad (fast)	10	T _{OPF}		6.0		5.0	ns
same (slew-rate limited)	10	T _{OPS}		16.0		13.0	ns
3-state to Pad begin hi-Z (fast)	9	T _{TSHZ}		10.0		9.0	ns
same (slew-rate limited)	9	T _{TSHZ}		20.0		12.0	ns
3-state to Pad active and valid (fast)	8	T _{TSO}		11.0		10.0	ns
same (slew -rate limited)	8	T _{TSO}		21.0		18.0	ns
Set-up and Hold Times (Output)							
Output (O) to clock (OK) set-up time	5	T _{OOK}	8.0		7.0		ns
Output (O) to clock (OK) hold time	6	T _{OKO}	0		0		ns
Clock							
Clock High time	11	T _{IOH}	4.0		3.5		ns
Clock Low time	12	T _{IOL}	4.0		3.5		ns
Max. flip-flop toggle rate		F _{CLK}	113.0		135.0		MHz
Global Reset Delays (based on XC3042A)							
RESET Pad to Registered In (Q)	13	T _{RR}		24.0		23.0	ns
RESET Pad to output pad (fast)	15	T _{RPO}		33.0		29.0	ns
(slew-rate limited)	15	T _{RPO}		43.0		37.0	ns

- Notes:
1. Timing is measured at pin threshold, with 50 pF external capacitive loads (incl. test fixture). Typical slew rate limited output rise/fall times are approximately four times longer.
 2. Voltage levels of unused (bonded and unbonded) pads must be valid logic levels. Each can be configured with the internal pull-up resistor or alternatively configured as a driven output or driven from an external source.
 3. Input pad set-up time is specified with respect to the internal clock (ik). In order to calculate system set-up time, subtract clock delay (pad to ik) from the input pad set-up time value. Input pad holdtime with respect to the internal clock (ik) is negative. This means that pad level changes immediately before the internal clock edge (ik) will not be recognized.
 4. T_{PID}, T_{PTG}, and T_{PICK} are 3 ns higher for XTL2 when the pin is configured as a user input.

XC3000L Switching Characteristics

Xilinx maintains test specifications for each product as controlled documents. To insure the use of the most recently released device performance parameters, please request a copy of the current test-specification revision.

XC3000L Operating Conditions

Symbol	Description	Min	Max	Units
V_{CC}	Supply voltage relative to GND Commercial 0°C to +85°C junction	3.0	3.6	V
V_{IH}	High-level input voltage — TTL configuration	2.0	$V_{CC}+0.3$	V
V_{IL}	Low-level input voltage — TTL configuration	-0.3	0.8	V
T_{IN}	Input signal transition time		250	ns

- Notes:** 1. At junction temperatures above those listed as Operating Conditions, all delay parameters increase by 0.3% per °C.
2. Although the present (1996) devices operate over the full supply voltage range from 3.0 to 5.25 V, Xilinx reserves the right to restrict operation to the 3.0 to 3.6 V range later, when smaller device geometries might preclude operation at 5V. Operating conditions are guaranteed in the 3.0 – 3.6 V V_{CC} range.

XC3000L DC Characteristics Over Operating Conditions

Symbol	Description	Min	Max	Units
V_{OH}	High-level output voltage (@ $I_{OH} = -4.0$ mA, V_{CC} min)	2.40		V
V_{OL}	Low-level output voltage (@ $I_{OL} = 4.0$ mA, V_{CC} min)		0.40	V
V_{OH}	High-level output voltage (@ $I_{OH} = -4.0$ mA, V_{CC} min)	$V_{CC} - 0.2$		V
V_{OL}	Low-level output voltage (@ $I_{OL} = 4.0$ mA, V_{CC} min)		0.2	V
V_{CCPD}	Power-down supply voltage (PWRDWN must be Low)	2.30		V
I_{CCPD}	Power-down supply current ($V_{CC(MAX)}$ @ T_{MAX})		10	μA
I_{CCO}	Quiescent FPGA supply current in addition to I_{CCPD} ¹ Chip thresholds programmed as CMOS levels		20	μA
I_{IL}	Input Leakage Current	-10	+10	μA
C_{IN}	Input capacitance, all packages except PGA175 (sample tested) All Pins except XTL1 and XTL2 XTL1 and XTL2		10 15	pF pF
	Input capacitance, PGA 175 (sample tested) All Pins except XTL1 and XTL2 XTL1 and XTL2		15 20	pF pF
I_{RIN}	Pad pull-up (when selected) @ $V_{IN} = 0$ V ³	0.01	0.17	mA
I_{RLL}	Horizontal Longline pull-up (when selected) @ logic Low		2.50	mA

- Notes:** 1. With no output current loads, no active input or Longline pull-up resistors, all package pins at V_{CC} or GND, and the FPGA device configured with a tie option. I_{CCO} is in addition to I_{CCPD} .
2. Total continuous output sink current may not exceed 100 mA per ground pin. Total continuous output source may not exceed 100 mA per V_{CC} pin. The number of ground pins varies from the XC3020L to the XC3090L.
3. Not tested. Allows an undriven pin to float High. For any other purpose, use an external pull-up.

XC3000L Absolute Maximum Ratings

Symbol	Description		Units
V_{CC}	Supply voltage relative to GND	-0.5 to +7.0	V
V_{IN}	Input voltage with respect to GND	-0.5 to $V_{CC} + 0.5$	V
V_{TS}	Voltage applied to 3-state output	-0.5 to $V_{CC} + 0.5$	V
T_{STG}	Storage temperature (ambient)	-65 to +150	°C
T_{SOL}	Maximum soldering temperature (10 s @ 1/16 in.)	+260	°C
T_J	Junction temperature plastic	+125	°C
	Junction temperature ceramic	+150	°C

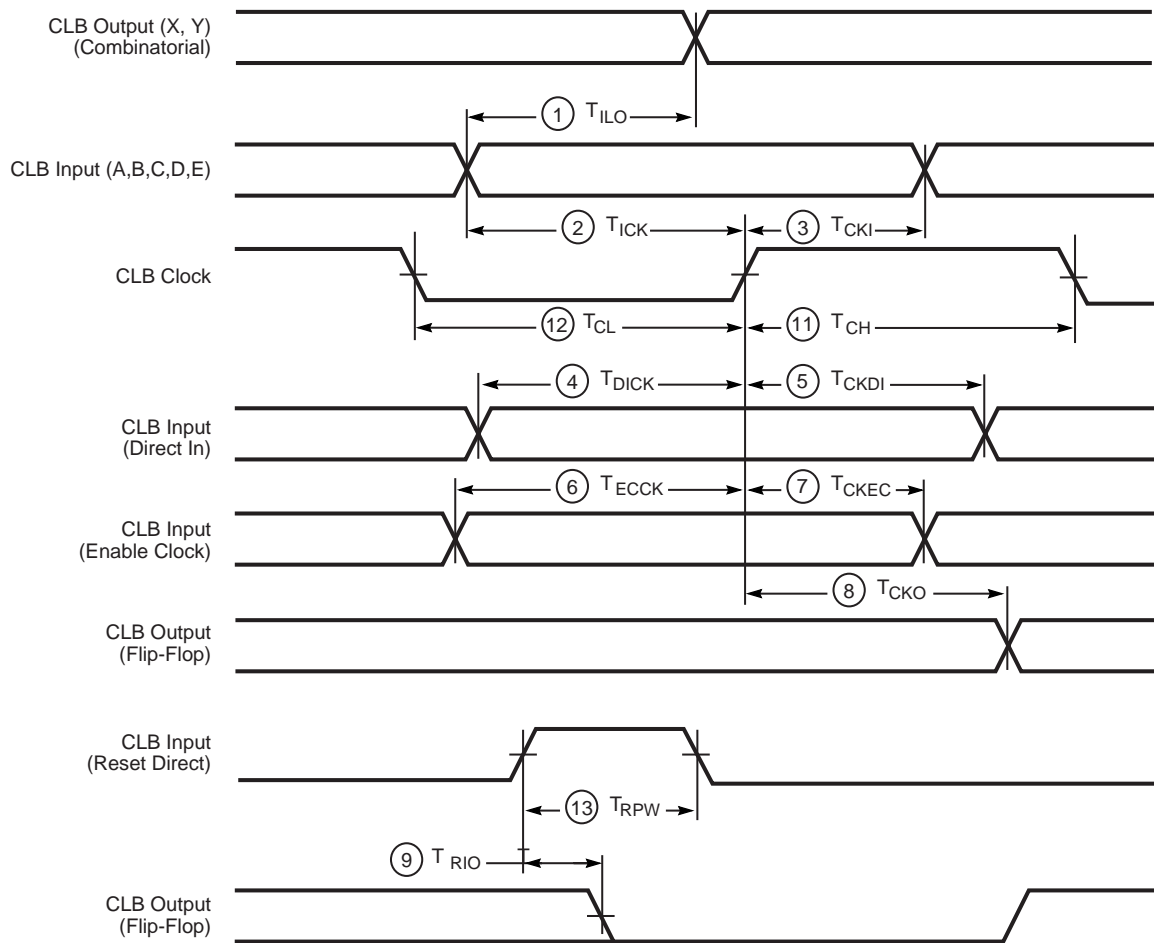
Note: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

XC3000L Global Buffer Switching Characteristics Guidelines

		Speed Grade	-8	
Description	Symbol	Max	Units	
Global and Alternate Clock Distribution ¹ Either: Normal IOB input pad through clock buffer to any CLB or IOB clock input Or: Fast (CMOS only) input pad through clock buffer to any CLB or IOB clock input	T_{PID}	9.0	ns	
	T_{PIDC}	7.0	ns	
TBUF driving a Horizontal Longline (L.L.) ¹ I to L.L. while T is Low (buffer active) $T \downarrow$ to L.L. active and valid with single pull-up resistor $T \uparrow$ to L.L. High with single pull-up resistor	T_{IO}	5.0	ns	
	T_{ON}	12.0	ns	
	T_{PUS}	24.0	ns	
BIDI Bidirectional buffer delay	T_{BIDI}	2.0	ns	

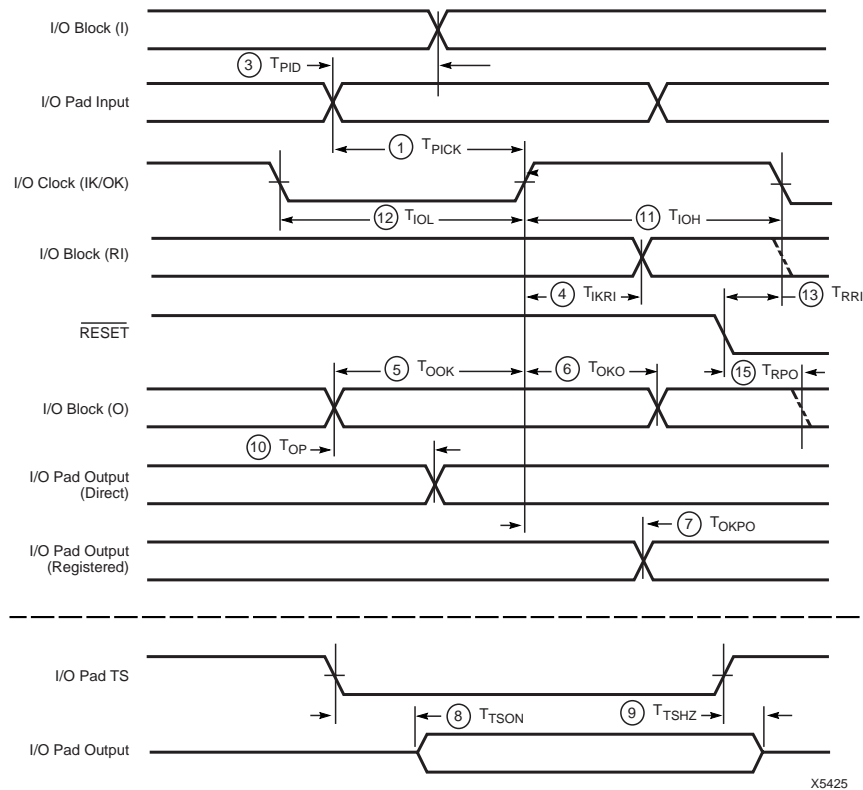
Notes: 1. Timing is based on the XC3042A, for other devices see timing calculator.
2. The use of two pull-up resistors per Longline, available on other XC3000 devices, is not a valid option for XC3000L devices.

XC3000L CLB Switching Characteristics Guidelines (continued)

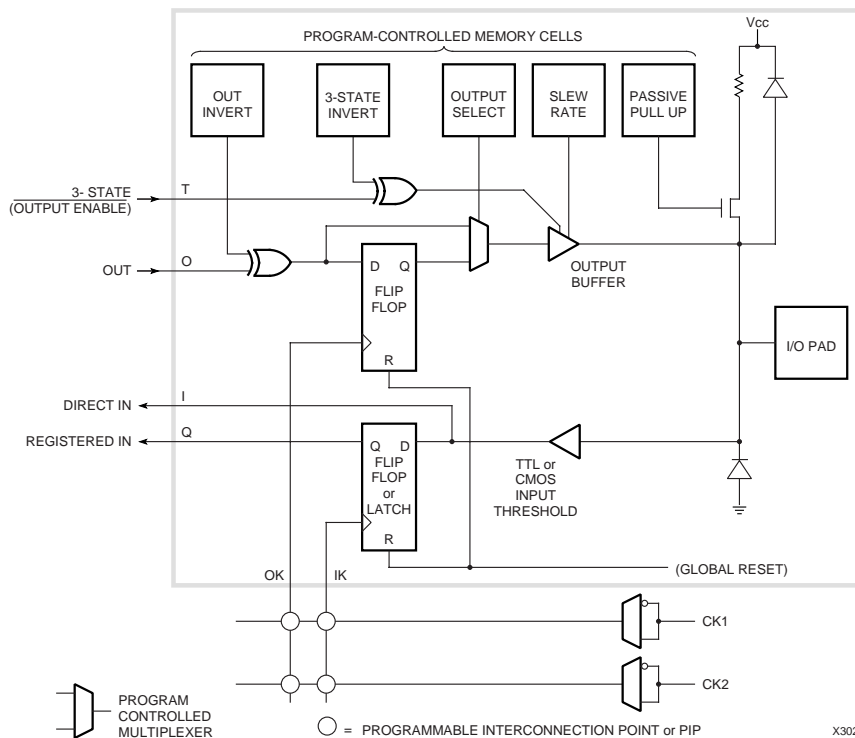


X5424

XC3000L IOB Switching Characteristics Guidelines (continued)

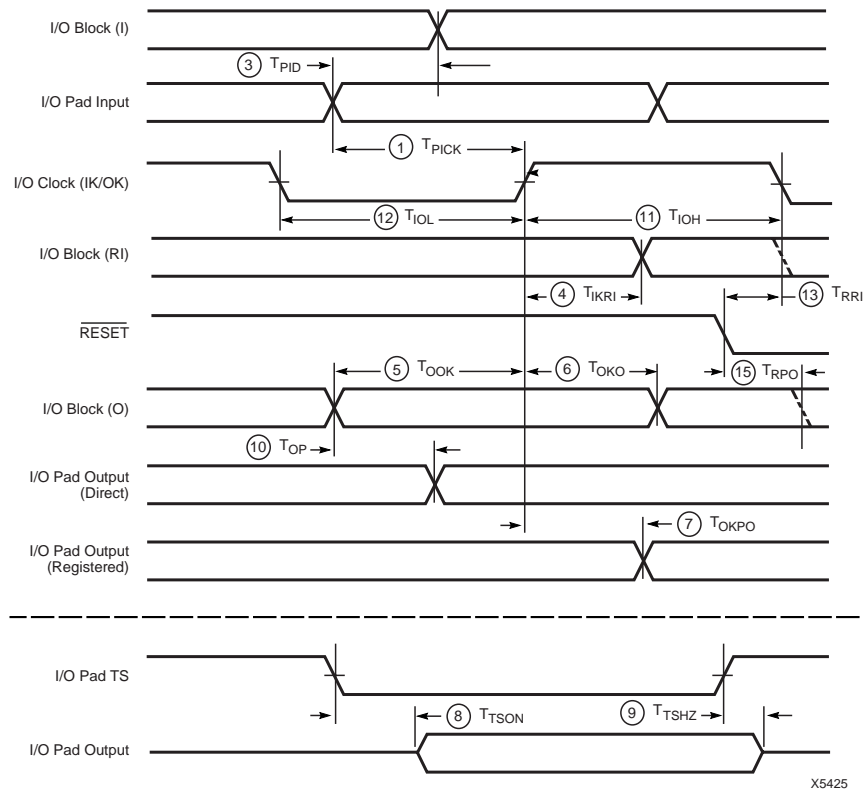


X5425

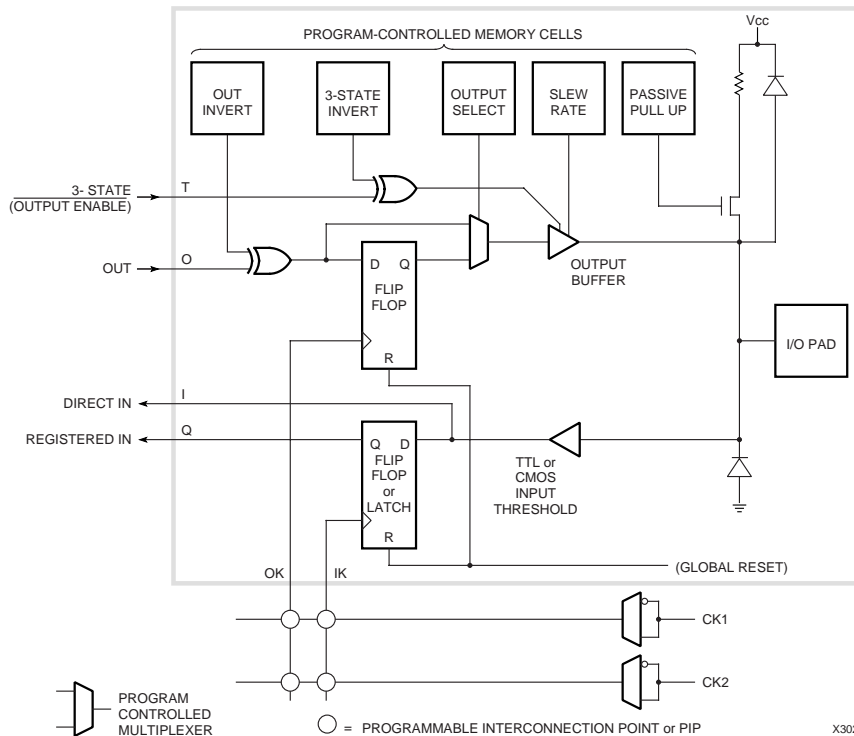


X3029

XC3100A IOB Switching Characteristics Guidelines (continued)



X5425



X3029