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AMD Xilinx - XC3042A-7PQ100C Datasheet



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Understanding <u>Embedded - FPGAs (Field</u> <u>Programmable Gate Array)</u>

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	144
Number of Logic Elements/Cells	-
Total RAM Bits	30784
Number of I/O	82
Number of Gates	3000
Voltage - Supply	4.75V ~ 5.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	100-BQFP
Supplier Device Package	100-PQFP (20x14)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc3042a-7pq100c

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Detailed Functional Description

The perimeter of configurable Input/Output Blocks (IOBs) provides a programmable interface between the internal logic array and the device package pins. The array of Configurable Logic Blocks (CLBs) performs user-specified logic functions. The interconnect resources are programmed to form networks, carrying logic signals among blocks, analogous to printed circuit board traces connecting MSI/SSI packages.

The block logic functions are implemented by programmed look-up tables. Functional options are implemented by program-controlled multiplexers. Interconnecting networks between blocks are implemented with metal segments joined by program-controlled pass transistors.

These FPGA functions are established by a configuration program which is loaded into an internal, distributed array of configuration memory cells. The configuration program is loaded into the device at power-up and may be reloaded on command. The FPGA includes logic and control signals to implement automatic or passive configuration. Program data may be either bit serial or byte parallel. The development system generates the configuration program bitstream used to configure the device. The memory loading process is independent of the user logic functions.

Configuration Memory

The static memory cell used for the configuration memory in the Field Programmable Gate Array has been designed specifically for high reliability and noise immunity. Integrity of the device configuration memory based on this design is assured even under adverse conditions. As shown in Figure 3, the basic memory cell consists of two CMOS inverters plus a pass transistor used for writing and reading cell data. The cell is only written during configuration and only read during readback. During normal operation, the cell provides continuous control and the pass transistor is off and does not affect cell stability. This is quite different from the operation of conventional memory devices, in which the cells are frequently read and rewritten.



X3241

Figure 2: Field Programmable Gate Array Structure.

It consists of a perimeter of programmable I/O blocks, a core of configurable logic blocks and their interconnect resources. These are all controlled by the distributed array of configuration program memory cells.





Longlines

The Longlines bypass the switch matrices and are intended primarily for signals that must travel a long distance, or must have minimum skew among multiple destinations. Longlines, shown in Figure 14, run vertically and horizontally the height or width of the interconnect area. Each interconnection column has three vertical Longlines, and each interconnection row has two horizontal Longlines. Two additional Longlines are located adjacent to the outer sets of switching matrices. In devices larger than the XC3020A and XC3120A FPGAs, two vertical Longlines in each column are connectable half-length lines. On the XC3020A and XC3120A FPGAs, only the outer Longlines are connectable half-length lines.

Longlines can be driven by a logic block or IOB output on a column-by-column basis. This capability provides a common low skew control or clock line within each column of logic blocks. Interconnections of these Longlines are shown in Figure 15. Isolation buffers are provided at each input to a Longline and are enabled automatically by the development system when a connection is made.



Figure 14: Horizontal and Vertical Longlines. These Longlines provide high fan-out, low-skew signal distribution in each row and column. The global buffer in the upper left die corner drives a common line throughout the FPGA.

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Figure 15: Programmable Interconnection of Longlines. This is provided at the edges of the routing area. Three-state buffers allow the use of horizontal Longlines to form on-chip wired AND and multiplexed buses. The left two non-clock vertical Longlines per column (except XC3020A) and the outer perimeter Longlines may be programmed as connectable half-length lines.



Figure 16: 3-State Buffers Implement a Wired-AND Function. When all the buffer 3-state lines are High, (high impedance), the pull-up resistor(s) provide the High output. The buffer inputs are driven by the control signals or a Low.



Figure 17: 3-State Buffers Implement a Multiplexer. The selection is accomplished by the buffer 3-state signal.

A re-program is initiated.when a configured XC3000 series device senses a High-to-Low transition and subsequent >6 μ s Low level on the DONE/PROG package pin, or, if this pin is externally held permanently Low, a High-to-Low transition and subsequent >6 μ s Low time on the RESET package pin.

The device returns to the Clear state where the configuration memory is cleared and mode lines re-sampled, as for an aborted configuration. The complete configuration program is cleared and loaded during each configuration program cycle.

Length count control allows a system of multiple Field Programmable Gate Arrays, of assorted sizes, to begin operation in a synchronized fashion. The configuration program generated by the development system begins with a preamble of 11111110010 followed by a 24-bit length count representing the total number of configuration clocks needed to complete loading of the configuration program(s). The data framing is shown in Figure 21. All FPGAs connected in series read and shift preamble and length count in on positive and out on negative configuration clock edges. A device which has received the preamble and length count then presents a High Data Out until it has intercepted the appropriate number of data frames. When the configuration program memory of an FPGA is full and the length count does not yet compare, the device shifts any additional data through, as it did for preamble and length count. When the FPGA configuration memory is full and the length count compares, the device will execute



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Device	XC3020A XC3020L XC3120A	XC3030A XC3030L XC3130A	XC3042A XC3042L XC3142A XC3142L	XC3064A XC3064L XC3164A	XC3090A XC3090L XC3190A XC3190L	XC3195A
Gates	1,000 to 1,500	1,500 to 2,000	2,000 to 3,000	3,500 to 4,500	5,000 to 6,000	6,500 to 7,500
CLBs	64	100	144	224	320	484
Row x Col	(8 x 8)	(10 x 10)	(12 x 12)	(16 x 14)	(20 x 16)	(22 x 22)
IOBs	64	80	96	120	144	176
Flip-flops	256	360	480	688	928	1,320
Horizontal Longlines	16	20	24	32	40	44
TBUFs/Horizontal LL	9	11	13	15	17	23
Bits per Frame (including1 start and 3 stop bits)	75	92	108	140	172	188
Frames	197	241	285	329	373	505
Program Data = Bits x Frames + 4 bits (excludes header)	14,779	22,176	30,784	46,064	64,160	94,944
PROM size (bits) = Program Data + 40-bit Header	14,819	22,216	30,824	46,104	64,200	94,984

Figure 21: Internal Configuration Data Structure for an FPGA. This shows the preamble, length count and data frames generated by the Development System.

The Length Count produced by the program = [(40-bit preamble + sum of program data + 1 per daisy chain device) rounded up to multiple of 8] – ($2 \le K \le 4$) where K is a function of DONE and RESET timing selected. An additional 8 is added if roundup increment is less than K. K additional clocks are needed to complete start-up after length count is reached.



Special Configuration Functions

The configuration data includes control over several special functions in addition to the normal user logic functions and interconnect.

- Input thresholds
- Readback disable
- DONE pull-up resistor
- DONE timing
- RESET timing
- Oscillator frequency divided by two

Each of these functions is controlled by configuration data bits which are selected as part of the normal development system bitstream generation process.

Input Thresholds

Prior to the completion of configuration all FPGA input thresholds are TTL compatible. Upon completion of configuration, the input thresholds become either TTL or CMOS compatible as programmed. The use of the TTL threshold option requires some additional supply current for threshold shifting. The exception is the threshold of the PWRDWN input and direct clocks which always have a CMOS input. Prior to the completion of configuration the user I/O pins each have a high impedance pull-up. The configuration program can be used to enable the IOB pull-up resistors in the Operational mode to act either as an input load or to avoid a floating input on an otherwise unused pin.

Readback

The contents of a Field Programmable Gate Array may be read back if it has been programmed with a bitstream in which the Readback option has been enabled. Readback may be used for verification of configuration and as a method of determining the state of internal logic nodes during debugging. There are three options in generating the configuration bitstream.

- "Never" inhibits the Readback capability.
- "One-time," inhibits Readback after one Readback has been executed to verify the configuration.
- "On-command" allows unrestricted use of Readback.

Readback is accomplished without the use of any of the user I/O pins; only M0, M1 and CCLK are used. The initiation of Readback is produced by a Low to High transition of the M0/RTRIG (Read Trigger) pin. The CCLK input must then be driven by external logic to read back the configuration data. The first three Low-to-High CCLK transitions clock out dummy data. The subsequent Low-to-High CCLK transitions shift the data frame information out on the M1/RDATA (Read Data) pin. Note that the logic polarity is always inverted, a zero in configuration becomes a one in Readback, and vice versa. Note also that each Readback frame has one Start bit (read back as a one) but, unlike in

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configuration, each Readback frame has only one Stop bit (read back as a zero). The third leading dummy bit mentioned above can be considered the Start bit of the first frame. All data frames must be read back to complete the process and return the Mode Select and CCLK pins to their normal functions.

Readback data includes the current state of each CLB flip-flop, each input flip-flop or latch, and each device pad. These data are imbedded into unused configuration bit positions during Readback. This state information is used by the development system In-Circuit Verifier to provide visibility into the internal operation of the logic while the system is operating. To readback a uniform time-sample of all storage elements, it may be necessary to inhibit the system clock.

Reprogram

To initiate a re-programming cycle, the dual-function pin DONE/PROG must be given a High-to-Low transition. To reduce sensitivity to noise, the input signal is filtered for two cycles of the FPGA internal timing generator. When reprogram begins, the user-programmable I/O output buffers are disabled and high-impedance pull-ups are provided for the package pins. The device returns to the Clear state and clears the configuration memory before it indicates 'initialized'. Since this Clear operation uses chip-individual internal timing, the master might complete the Clear operation and then start configuration before the slave has completed the Clear operation. To avoid this problem, the slave INIT pins must be AND-wired and used to force a RESET on the master (see Figure 25). Reprogram control is often implemented using an external open-collector driver which pulls DONE/PROG Low. Once a stable request is recognized, the DONE/PROG pin is held Low until the new configuration has been completed. Even if the re-program request is externally held Low beyond the configuration period, the FPGA will begin operation upon completion of configuration.

DONE Pull-up

DONE/PROG is an open-drain I/O pin that indicates the FPGA is in the operational state. An optional internal pull-up resistor can be enabled by the user of the development system. The DONE/PROG pins of multiple FPGAs in a daisy-chain may be connected together to indicate all are DONE or to direct them all to reprogram.

DONE Timing

The timing of the DONE status signal can be controlled by a selection to occur either a CCLK cycle before, or after, the outputs going active. See Figure 22. This facilitates control of external functions such as a PROM enable or holding a system in a wait state.

RESET Timing

As with DONE timing, the timing of the release of the internal reset can be controlled to occur either a CCLK cycle before, or after, the outputs going active. See Figure 22. This reset keeps all user programmable flip-flops and latches in a zero state during configuration.

Crystal Oscillator Division

A selection allows the user to incorporate a dedicated divide-by-two flip-flop between the crystal oscillator and the alternate clock line. This guarantees a symmetrical clock signal. Although the frequency stability of a crystal oscillator is very good, the symmetry of its waveform can be affected by bias or feedback drive.

Bitstream Error Checking

Bitstream error checking protects against erroneous configuration.

Each Xilinx FPGA bitstream consists of a 40-bit preamble, followed by a device-specific number of data frames. The number of bits per frame is also device-specific; however, each frame ends with three stop bits (111) followed by a start bit for the next frame (0).

All devices in all XC3000 families start reading in a new frame when they find the first 0 after the end of the previous frame. An original XC3000 device does not check for the correct stop bits, but XC3000A, XC3100A, XC3000L, and XC3100L devices check that the last three bits of any frame are actually 111.

Under normal circumstances, all these FPGAs behave the same way; however, if the bitstream is corrupted, an XC3000 device will always start a new frame as soon as it finds the first 0 after the end of the previous frame, even if the data is completely wrong or out-of-sync. Given sufficient zeros in the data stream, the device will also go Done, but with incorrect configuration and the possibility of internal contention.

An XC3000A/XC3100A/XC3000L/XC3100L device starts any new frame only if the three preceding bits are all ones. If this check fails, it pulls $\overline{\text{INIT}}$ Low and stops the internal configuration, although the Master CCLK keeps running. The user must then <u>start a</u> new configuration by applying a >6 µs Low level on RESET.

This simple check does not protect against random bit errors, but it offers almost 100 percent protection against erroneous configuration files, defective configuration data sources, synchronization errors between configuration source and FPGA, or PC-board level defects, such as broken lines or solder-bridges.

Reset Spike Protection

A separate modification slows down the RESET input before configuration by using a two-stage shift register driven from the internal clock. It tolerates submicrosecond High spikes on RESET before configuration. The XC3000 master can be connected like an XC4000 master, but with its RESET input used instead of INIT. (On XC3000, INIT is output only).

Soft Start-up

After configuration, the outputs of all FPGAs in a daisy-chain become active simultaneously, as a result of the same CCLK edge. In the original XC3000/3100 devices, each output becomes active in either fast or slew-rate limited mode, depending on the way it is configured. This can lead to large ground-bounce signals. In XC3000A, XC3000L, XC3100A, and XC3100L devices, all outputs become active first in slew-rate limited mode, reducing the ground bounce. After this soft start-up, each individual output slew rate is again controlled by the respective configuration bit.



Configuration Timing

This section describes the configuration modes in detail.

Master Serial Mode

In Master Serial mode, the CCLK output of the lead FPGA drives a Xilinx Serial PROM that feeds the DIN input. Each rising edge of the CCLK output increments the Serial PROM internal address counter. This puts the next data bit on the SPROM data output, connected to the DIN pin. The lead FPGA accepts this data on the subsequent rising CCLK edge.

The lead FPGA then presents the preamble data (and all data that overflows the lead device) on its DOUT pin. There is an internal delay of 1.5 CCLK periods, which means that

DOUT changes on the falling CCLK edge, and the next device in the daisy-chain accepts data on the subsequent rising CCLK edge.

The SPROM <u>CE</u> input can be driven from either <u>LDC</u> or DONE. Using <u>LDC</u> avoids potential contention on the DIN pin, if this pin is configured as user-I/O, but <u>LDC</u> is then restricted to be a permanently High user output. Using DONE also avoids contention on DIN, provided the early DONE option is invoked.



Figure 23: Master Serial Mode Circuit Diagram

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CCLK (Output) (2) T_{CKDS} **T**DSCK (1)Serial Data In n n + 1 n + 2 Serial DOUT n – 3 n – 2 n – 1 n (Output) X3223

	Description		Symbol	Min	Max	Units
CCLK	Data In setup	1	T _{DSCK}	60		ns
COLK	Data In hold	2	C _{KDS}	0		ns

Notes: 1. At power-up, V_{CC} must rise from 2.0 V to V_{CC} min in less than 25 ms. If this is not possible, configuration can be delayed by holding RESET Low until V_{CC} has reached 4.0 V (2.5 V for the XC3000L). A very long V_{CC} rise time of >100 ms, or a non-monotonically rising V_{CC} may require >6- μ s High level on RESET, followed by a >6- μ s Low level on RESET and D/P after VCC has reached 4.0 V (2.5 V for the XC3000L).

2. Configuration can be controlled by holding RESET Low with or until after the INIT of all daisy-chain slave-mode devices is High.

3. Master-serial-mode timing is based on slave-mode testing.

Figure 24: Master Serial Mode Programming Switching Characteristics

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	Description		Symbol	Min	Max	Units
	To address valid	1	T _{RAC}	0	200	ns
	To data setup	2	T _{DRC}	60		ns
RCLK	To data hold	3	T _{RCD}	0		ns
	RCLK High		T _{RCH}	600		ns
	RCLK Low		T _{RCL}	4.0		μs

Notes: 1. At power-up, V_{CC} must rise from 2.0 V to V_{CC} min in less than 25 ms. If this is not possible, configuration can be delayed by holding RESET Low until VCC has reached 4.0 V (2.5 V for the XC3000L). A very long V_{CC} rise time of >100 ms, or a non-monotonically rising V_{CC} may require a >6-μs High level on RESET, followed by a >6-μs Low level on RESET and D/P after V_{CC} has reached 4.0 V (2.5 V for the XC3000L).
2. Configuration can be controlled by holding RESET Low with or until after the INIT of all daisy-chain slave-mode devices is

High.

This timing diagram shows that the EPROM requirements are extremely relaxed: EPROM access time can be longer than 4000 ns. EPROM data output has no hold time requirements.

Figure 26: Master Parallel Mode Programming Switching Characteristics



Peripheral Mode

Peripheral mode uses the trailing edge of the logic AND condition of the CS0, CS1, CS2, and WS inputs to accept byte-wide data from a microprocessor bus. In the lead FPGA, this data is loaded into a double-buffered UART-like parallel-to-serial converter and is serially shifted into the internal logic. The lead FPGA presents the preamble data (and all data that overflows the lead device) on the DOUT pin.

The Ready/Busy output from the lead device acts as a handshake signal to the microprocessor. RDY/BUSY goes Low when a byte has been received, and goes High again

when the byte-wide input buffer has transferred its information into the shift register, and the buffer is ready to receive new data. The length of the BUSY signal depends on the activity in the UART. If the shift register had been empty when the new byte was received, the BUSY signal lasts for only two CCLK periods. If the shift register was still full when the new byte was received, the BUSY signal can be as long as nine CCLK periods.

Note that after the last byte has been entered, only seven of its bits are shifted out. CCLK remains High with DOUT equal to bit 6 (the next-to-last bit) of the last byte entered.



Figure 27: Peripheral Mode Circuit Diagram

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	Description		Symbol	Min	Max	Units
	To DOUT	3	T _{CCO}		100	ns
CCLK	DIN setup DIN hold High time Low time (Note 1) Frequency	1 2 4 5	T _{DCC} T _{CCD} T _{CCH} T _{CCL} F _{CC}	60 0 0.05 0.05	5.0 10	ns ns μs MHz

Notes: 1. The max limit of CCLK Low time is caused by dynamic circuitry inside the FPGA.

2. Configuration must be delayed until the INIT of all FPGAs is High.

3. At power-up, V_{CC} must rise from 2.0 V to V_{CC} min in less than 25 ms. If this is not possible, configuration can be delayed by holding RESET Low until VCC has reached 4.0 V (2.5 V for the XC3000L). A very long V_{CC} rise time of >100 ms, or a non-monotonically rising V_{CC} may require a >6- μ s High level on RESET, followed by a >6- μ s Low level on RESET and D/P after V_{CC} has reached 4.0 V (2.5 V for the XC3000L).

Figure 30: Slave Serial Mode Programming Switching Characteristics

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SPECIFIED WORST-CASE VALUES 1.00 MAX MILITARY (4.5-V) 0.80 NORMALIZED DELAY 0.60 TYPICAL COMMERCIAL (+5.0)V, 25°C) TYPICAL MILITARY MIN MILITARY (4.5 V) 0.40 OMMERCIA MIN MILITARY (5.5 0.20 - 55 - 40 - 20 0 25 40 70 80 100 125

Figure 32: Relative Delay as a Function of Temperature, Supply Voltage and Processing Variations



Figure 33: Clock Rate as a Function of Logic Complexity (Number of Combinational Levels between Flip-Flops)

Power

Power Distribution

Power for the FPGA is distributed through a grid to achieve high noise immunity and isolation between logic and I/O. Inside the FPGA, a dedicated V_{CC} and ground ring surrounding the logic array provides power to the I/O drivers. An independent matrix of V_{CC} and groundlines supplies the interior logic of the device. This power distribution grid provides a stable supply and ground for all internal logic, providing the external package power pins are all connected and appropriately decoupled. Typically a 0.1- μ F capacitor connected near the V_{CC} and ground pins will provide adequate decoupling.

Output buffers capable of driving the specified 4- or 8-mA loads under worst-case conditions may be capable of driving as much as 25 to 30 times that current in a best case. Noise can be reduced by minimizing external load capacitance and reducing simultaneous output transitions in the same direction. It may also be beneficial to locate heavily loaded output buffers near the ground pads. The I/O Block output buffers have a slew-limited mode which should be used where output rise and fall times are not speed critical. Slew-limited outputs maintain their dc drive capability, but generate less external reflections and internal noise.



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AND of several slave mode devices, a hold-off signal for a master mode device. After configuration this pin becomes a user-programmable I/O pin.

BCLKIN

This is a direct CMOS level input to the alternate clock buffer (Auxiliary Buffer) in the lower right corner.

XTL1

This user I/O pin can be used to operate as the output of an amplifier driving an external crystal and bias circuitry.

XTL2

This user I/O pin can be used as the input of an amplifier connected to an external crystal and bias circuitry. The I/O Block is left unconfigured. The oscillator configuration is activated by routing a net from the oscillator buffer symbol output and by the MakeBits program.

CS0, CS1, CS2, WS

These four inputs represent a set of signals, three active Low and one active High, that are used to control configuration-data entry in the Peripheral mode. Simultaneous assertion of all four inputs generates a Write to the internal data buffer. The removal of any assertion clocks in the D0-D7 data. In Master-Parallel mode, WS and CS2 are the A0 and A1 outputs. After configuration, these pins are user-programmable I/O pins.

RDY/BUSY

During Peripheral Parallel mode configuration this pin indicates when the chip is ready for another byte of data to be written to it. After configuration is complete, this pin becomes a user-programmed I/O pin.

RCLK

During Master Parallel mode configuration, each change on the A0-15 outputs is preceded by a rising edge on RCLK, a redundant output signal. After configuration is complete, this pin becomes a user-programmed I/O pin. This set of eight pins represents the parallel configuration byte for the parallel Master and Peripheral modes. After configuration is complete, they are user-programmed I/O pins.

A0-A15

D0-D7

During Master Parallel mode, these 16 pins present an address output for a configuration EPROM. After configuration, they are user-programmable I/O pins.

DIN

During Slave or Master Serial configuration, this pin is used as a serial-data input. In the Master or Peripheral configuration, this is the Data 0 input. After configuration is complete, this pin becomes a user-programmed I/O pin.

DOUT

During configuration this pin is used to output serial-configuration data to the DIN pin of a daisy-chained slave. After configuration is complete, this pin becomes a user-programmed I/O pin.

TCLKIN

This is a direct CMOS-level input to the global clock buffer. This pin can also be configured as a user programmable I/O pin. However, since TCLKIN is the preferred input to the global clock net, and the global clock net should be used as the primary clock source, this pin is usually the clock input to the chip.

Unrestricted User I/O Pins

I/O

An I/O pin may be programmed by the user to be an Input or an Output pin following configuration. All unrestricted I/O pins, plus the special pins mentioned on the following page, have a weak pull-up resistor that becomes active as soon as the device powers up, and stays active until the end of configuration.

Note: Before and during configuration, all outputs that are not used for the configuration process are 3-stated with a weak pull-up resistor.



XC3000A Switching Characteristics

Xilinx maintains test specifications for each product as controlled documents. To insure the use of the most recently released device performance parameters, please request a copy of the current test-specification revision.

XC3000A Operating Conditions

Symbol	Description	Min	Max	Units
V _{CC}	Supply voltage relative to GND Commercial 0°C to +85°C junction	4.75	5.25	V
	Supply voltage relative to GND Industrial -40°C to +100°C junction	4.5	5.5	V
V _{IHT}	High-level input voltage — TTL configuration	2.0	V _{CC}	V
V _{ILT}	Low-level input voltage — TTL configuration	0	0.8	V
V _{IHC}	High-level input voltage — CMOS configuration	70%	100%	V _{CC}
V _{ILC}	Low-level input voltage — CMOS configuration	0	20%	V _{CC}
T _{IN}	Input signal transition time		250	ns

Note: At junction temperatures above those listed as Operating Conditions, all delay parameters increase by 0.3% per °C.

XC3000A DC Characteristics Over Operating Conditions

Symbol	Description		Min	Max	Units
V _{OH}	High-level output voltage (@ $I_{OH} = -4.0 \text{ mA}, V_{CC} \text{ min}$)	Commercial	3.86		V
V _{OL}	Low-level output voltage (@ I _{OL} = 4.0 mA, V _{CC} min)	Commercial		0.40	V
V _{OH}	High-level output voltage (@ $I_{OH} = -4.0 \text{ mA}, V_{CC} \text{ min}$)	Industrial	3.76		V
V _{OL}	Low-level output voltage (@ I _{OL} = 4.0 mA, V _{CC} min)	Industrial		0.40	V
V _{CCPD}	Power-down supply voltage (PWRDWN must be Low)		2.30		V
I _{CCPD}	Power-down supply current				
	(V _{CC(MAX)} @ T _{MAX})	3020A		100	μA
		3030A		160	μA
		3042A		240	μA
		3064A		340	μA
		3090A		500	μA
	Quiescent FPGA supply current in addition to I _{CCPD}				
Icco	Chip thresholds programmed as CMOS levels			500	μA
	Chip thresholds programmed as TTL levels			10	μA
IIL	Input Leakage Current		-10	+10	μA
	Input capacitance, all packages except PGA175				
	(sample tested)				
	All Pins except XTL1 and XTL2			10	pF
C	XTL1 and XTL2			15	pF
CIN	Input capacitance, PGA 175				
	(sample tested)				
	All Pins except XTL1 and XTL2			16	pF
	XTL1 and XTL2			20	pF
I _{RIN}	Pad pull-up (when selected) @ $V_{IN} = 0 V^3$		0.02	0.17	mA
I _{RLL}	Horizontal Longline pull-up (when selected) @ logic Low			3.4	mA

Notes: 1. With no output current loads, no active input or Longline pull-up resistors, all package pins at V_{CC} or GND, and the FPGA device configured with a tie option.

 Total continuous output sink current may not exceed 100 mA per ground pin. Total continuous output source may not exceed 100 mA per V_{CC} pin. The number of ground pins varies from the XC3020A to the XC3090A.

3. Not tested. Allow an undriven pin to float High. For any other purposes use an external pull-up.

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XC3000A IOB Switching Characteristics Guidelines (continued)







XC3000L Switching Characteristics

Xilinx maintains test specifications for each product as controlled documents. To insure the use of the most recently released device performance parameters, please request a copy of the current test-specification revision.

XC3000L Operating Conditions

Symbol	Description	Min	Max	Units
V _{CC}	Supply voltage relative to GND Commercial 0°C to +85°C junction	3.0	3.6	V
V _{IH}	High-level input voltage — TTL configuration	2.0	V _{CC} +0.3	V
V _{IL}	Low-level input voltage — TTL configuration	-0.3	0.8	V
T _{IN}	Input signal transition time		250	ns

Notes: 1. At junction temperatures above those listed as Operating Conditions, all delay parameters increase by 0.3% per °C. 2. Although the present (1996) devices operate over the full supply voltage range from 3.0 to 5.25 V, Xilinx reserves the right to restrict operation to the 3.0 to 3.6 V range later, when smaller device geometries might preclude operation at 5V. Operating conditions are guaranteed in the $3.0 - 3.6 \text{ V V}_{CC}$ range.

XC3000L DC Characteristics Over Operating Conditions

Symbol	Description	Min	Max	Units
V _{OH}	High-level output voltage (@ I _{OH} = -4.0 mA, V _{CC} min)	2.40		V
V _{OL}	Low-level output voltage (@ I _{OL} = 4.0 mA, V _{CC} min)		0.40	V
V _{OH}	High-level output voltage (@ $I_{OH} = -4.0 \text{ mA}, V_{CC} \text{ min}$)	V _{CC} -0.2		V
V _{OL}	Low-level output voltage (@ I _{OL} = 4.0 mA, V _{CC} min)		0.2	V
V _{CCPD}	Power-down supply voltage (PWRDWN must be Low)	2.30		V
I _{CCPD}	Power-down supply current (V _{CC(MAX)} @ T _{MAX})		10	μA
Icco	Quiescent FPGA supply current in addition to I _{CCPD} ¹ Chip thresholds programmed as CMOS levels		20	μA
IIL	Input Leakage Current	-10	+10	μA
6	Input capacitance, all packages except PGA175 (sample tested) All Pins except XTL1 and XTL2 XTL1 and XTL2		10 15	pF pF
CIN	Input capacitance, PGA 175 (sample tested) All Pins except XTL1 and XTL2 XTL1 and XTL2		15 20	pF pF
I _{RIN}	Pad pull-up (when selected) @ $V_{IN} = 0 V^3$	0.01	0.17	mA
I _{RLL}	Horizontal Longline pull-up (when selected) @ logic Low		2.50	mA

Notes: 1. With no output current loads, no active input or Longline pull-up resistors, all package pins at V_{CC} or GND, and the FPGA

device configured with a tie option. I_{CCO} is in addition to I_{CCPD}.
2. Total continuous output sink current may not exceed 100 mA per ground pin. Total continuous output source may not exceed 100 mA per V_{CC} pin. The number of ground pins varies from the XC3020L to the XC3090L.

3. Not tested. Allows an undriven pin to float High. For any other purpose, use an external pull-up.

XC3000L CLB Switching Characteristics Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Since many internal timing parameters cannot be measured directly, they are derived from benchmark timing patterns. The following guidelines reflect worst-case values over the recommended operating conditions. For more detailed, more precise, and more up-to-date timing information, use the values provided by the timing calculator and used in the simulator.

		Sp	beed Grade	-	·8	
	Description	S	Symbol	Min	Max	Units
Combinatorial Delay						
Logic Variables	A, B, C, D, E, to outputs X or Y					
	FG Mode	1	T _{ILO}		6.7	ns
	F and FGM Mode				7.5	ns
Sequential delay						
Clock k to outputs	s X or Y	8	Тско		7.5	ns
Clock k to outputs	s X or Y when Q is returned		0.10			
through function g	generators F or G to drive X or Y					
	FG Mode		T _{QLO}		14.0	ns
	F and FGM Mode				14.8	ns
Set-up time before clo	ck K					
Logic Variables	A, B, C, D, E					
	FG Mode	2	TICK	5.0		ns
	F and FGM Mode			5.8		ns
Data In	DI	4	TDICK	5.0		ns
Enable Clock	EC	6	T _{ECCK}	6.0		ns
Hold Time after clock	K					
Logic Variables	A, B, C, D, E	3	Тскі	0		ns
Data In	DI ²	5	T _{CKDI}	2.0		ns
Enable Clock	EC	7	T _{CKEC}	2.0		ns
Clock						
Clock High time		11	T _{CH}	5.0		ns
Clock Low time		12	T _{CL}	5.0		ns
Max. flip-flop togg	gle rate		F _{CLK}	80.0		MHz
Reset Direct (RD)						
RD width		13	T _{RPW}	7.0		ns
delay from RD to	outputs X or Y	9	T _{RIO}	7.0		ns
Global Reset (RESET	Pad) ¹					
RESET width (Lo	<u>w</u>)		T _{MRW}	16.0		ns
delay from RESE	T pad to outputs X or Y		T _{MRQ}		23.0	ns

Notes: 1. Timing is based on the XC3042L, for other devices see timing calculator.

The CLB K to Q output delay (T_{CKO}, #8) of any CLB, plus the shortest possible interconnect delay, is always longer than the Data In hold time requirement (T_{CKDI}, #5) of any CLB on the same die.



XC3100A CLB Switching Characteristics Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Since many internal timing parameters cannot be measured directly, they are derived from benchmark timing patterns. The following guidelines reflect worst-case values over the recommended operating conditions. For more detailed, more precise, and more up-to-date timing information, use the values provided by the timing calculator and used in the simulator.

Sp		peed Grade		4	-	3	-	2	-	1	-0)9	
Description	S	ymbol	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Units
Combinatorial Delay Logic Variables A, B, C, D, E, to outputs X or Y	1	T _{ILO}		3.3		2.7		2.2		1.75		1.5	ns
Sequential delay Clock k to outputs X or Y Clock k to outputs X or Y when Q is returned through function generators F or G to drive		Тско		2.5		2.1		1.7		1.4		1.25	ns
Set-up time before clock K Logic Variables A, B, C, D, E Data In DI Enable Clock EC Reset Direct inactive RD	2 4 6	T _{ICK} T _{DICK} T _{ECCK}	2.5 1.6 3.2 1.0	0.2	2.1 1.4 2.7 1.0		1.8 1.3 2.5 1.0		1.7 1.2 2.3 1.0		1.5 1.0 2.05 1.0		ns ns ns ns
Hold Time after clock K Logic Variables A, B, C, D, E Data In DI Enable Clock EC	3 5 7	Т _{СКІ} Т _{СКDI} Т _{СКЕС}	0 1.0 0.8		0 0.9 0.7		0 0.9 0.7		0 0.8 0.6		0 0.7 0.55		ns ns ns
Clock Clock High time Clock Low time Max. flip-flop toggle rate		T _{CH} T _{CL} F _{CLK}	2.0 2.0 227		1.6 1.6 270		1.3 1.3 323		1.3 1.3 323		1.3 1.3 370		ns ns MHz
Reset Direct (RD) RD width delay from RD to outputs X or Y		T _{RPW} T _{RIO}	3.2	3.7	2.7	3.1	2.3	2.7	2.3	2.4	2.05	2.15	ns ns
Global Reset (RESET Pad) ¹ RESET wid <u>th (Low)</u> (XC3142A) delay from RESET pad to outputs X or Y		T _{MRW} T _{MRQ}	14.0	14.0	12.0	12.0	12.0	12.0	12.0	12.0	12.0	12.0	ns ns
											Pre	lim	

Notes: 1. The CLB K to Q output delay (T_{CKO}, #8) of any CLB, plus the shortest possible interconnect delay, is always longer than the Data In hold time requirement (T_{CKDI}, #5) of any CLB on the same die.
 2. T_{ILO}, T_{QLO} and T_{ICK} are specified for 4-input functions. For 5-input functions or base FGM functions, each of these

T_{ILO}, T_{QLO} and T_{ICK} are specified for 4-input functions. For 5-input functions or base FGM functions, each of these specifications for the XC3100A family increases by 0.50 ns (-5), 0.42 ns (-4) and 0.35 ns (-3), 0.35 ns (-2), 0.30 ns (-1), and 0.30 ns (-09).

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XC3100L CLB Switching Characteristics Guidelines (continued)





XC3000 Series 208-Pin PQFP Pinouts

XC3000A, and XC3000L families have identical pinouts

Pin Number	XC3090A	Pin Number	XC3090A	Pin Number	XC3090A	Pin Number	XC3090A
1	-	53	-	105	-	157	-
2	GND	54	-	106	VCC	158	-
3	PWRDWN	55	VCC	107	D/P	159	-
4	TCLKIN-I/O	56	M2-I/O	108	-	160	GND
5	I/O	57	HDC-I/O	109	D7-I/O	161	WS-A0-I/O
6	I/O	58	I/O	110	XTL1-BCLKIN-I/O	162	CS2-A1-I/O
7	I/O	59	I/O	111	I/O	163	I/O
8	I/O	60	I/O	112	I/O	164	I/O
9	I/O	61	LDC-I/O	113	I/O	165	A2-I/O
10	I/O	62	I/O	114	I/O	166	A3-I/O
11	I/O	63	I/O	115	D6-I/O	167	I/O
12	I/O	64	-	116	I/O	168	I/O
13	I/O	65	-	117	I/O	169	-
14	I/O	66	-	118	I/O	170	-
15	-	67	-	119	-	171	_
16	I/O	68	I/O	120	I/O	172	A15-I/O
17	I/O	69	I/O	121	I/O	173	A4-I/O
18	I/O	70	I/O	122	D5-I/O	174	I/O
19	I/O	71	I/O	123	CS0-I/O	175	I/O
20	I/O	72	-	124	I/O	176	_
21	I/O	73	-	125	I/O	177	-
22	I/O	74	I/O	126	I/O	178	A14-I/O
23	I/O	75	I/O	127	I/O	179	A5-I/O
24	I/O	76	I/O	128	D4-I/O	180	I/O
25	GND	77	INIT-I/O	129	I/O	181	I/O
26	VCC	78	VCC	130	VCC	182	GND
27	I/O	79	GND	131	GND	183	VCC
28	I/O	80	I/O	132	D3-I/O	184	A13-I/O
29	I/O	81	I/O	133	CS1-I/O	185	A6-I/O
30	I/O	82	I/O	134	I/O	186	I/O
31	I/O	83	-	135	I/O	187	I/O
32	I/O	84	-	136	I/O	188	_
33	I/O	85	I/O	137	I/O	189	-
34	I/O	86	I/O	138	D2-I/O	190	I/O
35	I/O	87	I/O	139	I/O	191	I/O
36	I/O	88	I/O	140	I/O	192	A12-I/O
37	-	89	I/O	141	I/O	193	A7-I/O
38	I/O	90	-	142	-	194	-
39	I/O	91	-	143	I/O	195	-
40	I/O	92	-	144	I/O	196	-
41	I/O	93	I/O	145	D1-I/O	197	I/O
42	I/O	94	I/O	146	RDY/BUSY-RCLK-I/O	198	I/O
43	I/O	95	I/O	147	I/O	199	A11-I/O
44	I/O	96	I/O	148	I/O	200	A8-I/O
45	I/O	97	I/O	149	I/O	201	I/O
46	I/O	98	I/O	150	I/O	202	I/O
47	I/O	99	I/O	151	DIN-D0-I/O	203	A10-I/O
48	M1-RDATA	100	XTL2-I/O	152	DOUT-I/O	204	A9-I/O
49	GND	101	GND	153	CCLK	205	VCC
50	M0-RTRIG	102	RESET	154	VCC	206	-
51	-	103	-	155	-	207	-
52	-	104	-	156	-	208	-
1		L			1		

Unprogrammed IOBs have a default pull-up. This prevents an undefined pad level for unbonded or unused IOBs. Programmed outputs are default slew-rate limited.

* In PQ208, XC3090A and XC3195A have different pinouts.