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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	144
Number of Logic Elements/Cells	-
Total RAM Bits	30784
Number of I/O	82
Number of Gates	3000
Voltage - Supply	3V ~ 3.6V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	100-TQFP
Supplier Device Package	100-VQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc3042l-8vq100c

Configurable Logic Block

The array of CLBs provides the functional elements from which the user's logic is constructed. The logic blocks are arranged in a matrix within the perimeter of IOBs. For example, the XC3020A has 64 such blocks arranged in 8 rows and 8 columns. The development system is used to compile the configuration data which is to be loaded into the internal configuration memory to define the operation and interconnection of each block. User definition of CLBs and their interconnecting networks may be done by automatic translation from a schematic-capture logic diagram or optionally by installing library or user macros.

Each CLB has a combinatorial logic section, two flip-flops, and an internal control section. See Figure 5. There are: five logic inputs (A, B, C, D and E); a common clock input (K); an asynchronous direct RESET input (RD); and an enable clock (EC). All may be driven from the interconnect resources adjacent to the blocks. Each CLB also has two outputs (X and Y) which may drive interconnect networks.

Data input for either flip-flop within a CLB is supplied from the function F or G outputs of the combinatorial logic, or the block input, DI. Both flip-flops in each CLB share the asynchronous RD which, when enabled and High, is dominant over clocked inputs. All flip-flops are reset by the active-Low chip input, RESET, or during the configuration process. The flip-flops share the enable clock (EC) which, when Low, recirculates the flip-flops' present states and inhibits response to the data-in or combinatorial function inputs on a CLB. The user may enable these control inputs and select their sources. The user may also select the clock net input (K), as well as its active sense within each CLB. This programmable inversion eliminates the need to route both phases of a clock signal throughout the device.

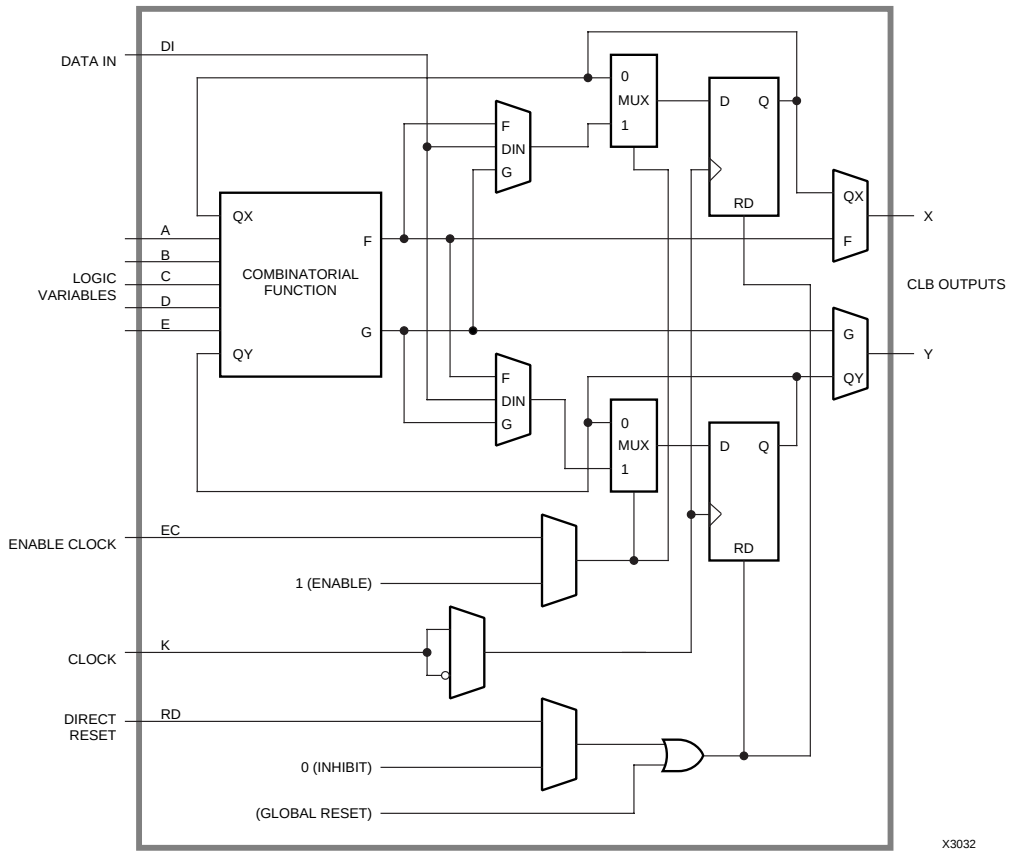


Figure 5: Configurable Logic Block.

Each CLB includes a combinatorial logic section, two flip-flops and a program memory controlled multiplexer selection of function. It has the following:

- five logic variable inputs A, B, C, D, and E
- a direct data in DI
- an enable clock EC
- a clock (invertible) K
- an asynchronous direct RESET RD
- two outputs X and Y

Configuration

Initialization Phase

An internal power-on-reset circuit is triggered when power is applied. When V_{CC} reaches the voltage at which portions of the FPGA device begin to operate (nominally 2.5 to 3 V), the programmable I/O output buffers are 3-stated and a high-impedance pull-up resistor is provided for the user I/O pins. A time-out delay is initiated to allow the power supply voltage to stabilize. During this time the power-down mode is inhibited. The Initialization state time-out (about 11 to 33 ms) is determined by a 14-bit counter driven by a self-generated internal timer. This nominal 1-MHz timer is subject to variations with process, temperature and power supply. As shown in Table 1, five configuration mode choices are available as determined by the input levels of three mode pins; M0, M1 and M2.

Table 1: Configuration Mode Choices

M0	M1	M2	CCLK	Mode	Data
0	0	0	output	Master	Bit Serial
0	0	1	output	Master	Byte Wide Addr. = 0000 up
0	1	0	—	reserved	—
0	1	1	output	Master	Byte Wide Addr. = FFFF down
1	0	0	—	reserved	—
1	0	1	output	Peripheral	Byte Wide
1	1	0	—	reserved	—
1	1	1	input	Slave	Bit Serial

In Master configuration modes, the device becomes the source of the Configuration Clock (CCLK). The beginning of configuration of devices using Peripheral or Slave modes must be delayed long enough for their initialization to be completed. An FPGA with mode lines selecting a Master configuration mode extends its initialization state using four times the delay (43 to 130 ms) to assure that all daisy-chained slave devices, which it may be driving, will be ready even if the master is very fast, and the slave(s) very slow. Figure 20 shows the state sequences. At the end of Initialization, the device enters the Clear state where it clears the configuration memory. The active Low, open-drain initialization signal $\overline{\text{INIT}}$ indicates when the Initialization and Clear states are complete. The FPGA tests for the absence of an external active Low $\overline{\text{RESET}}$ before it makes a final sample of the mode lines and enters the Configuration state. An external wired-AND of one or more $\overline{\text{INIT}}$ pins can be used to control configuration by the assertion of the active-Low $\overline{\text{RESET}}$ of a master mode device or to signal a processor that the FPGAs are not yet initialized.

If a configuration has begun, a re-assertion of $\overline{\text{RESET}}$ for a minimum of three internal timer cycles will be recognized and the FPGA will initiate an abort, returning to the Clear state to clear the partially loaded configuration memory words. The FPGA will then resample $\overline{\text{RESET}}$ and the mode lines before re-entering the Configuration state.

During configuration, the XC3000A, XC3000L, XC3100A, and XC3100L devices check the bit-stream format for stop bits in the appropriate positions. Any error terminates the configuration and pulls INIT Low.

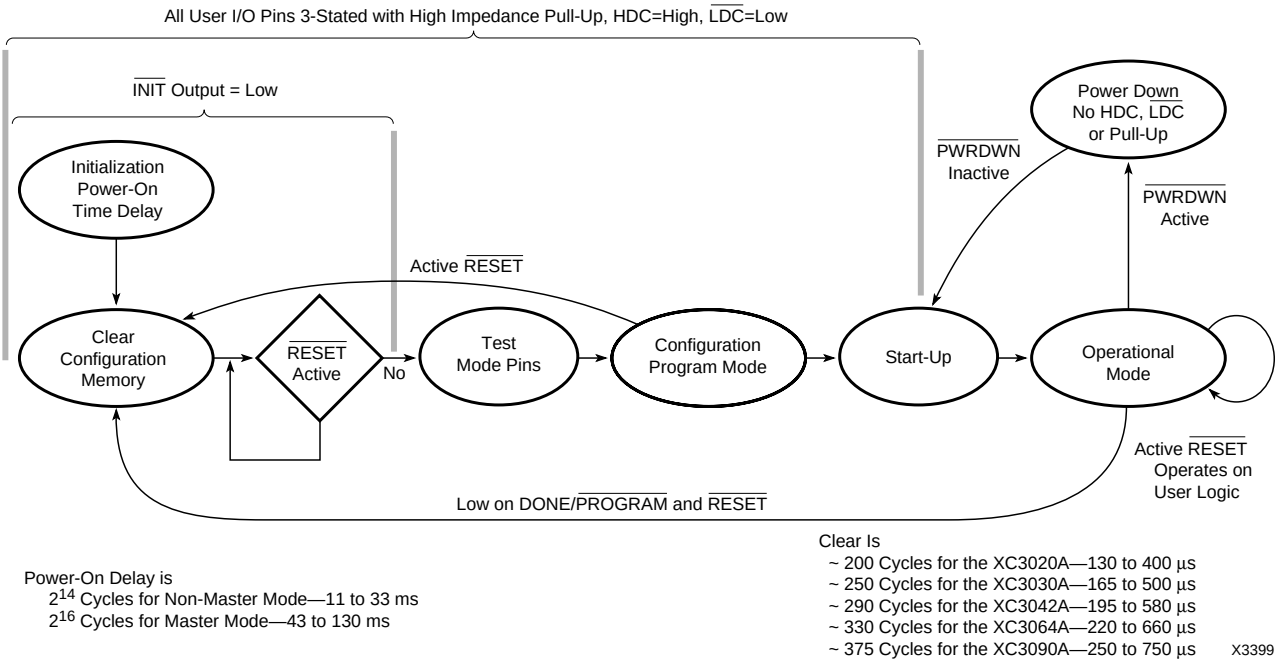


Figure 20: A State Diagram of the Configuration Process for Power-up and Reprogram.

a synchronous start-up sequence and become operational. See Figure 22. Two CCLK cycles after the completion of loading configuration data, the user I/O pins are enabled as configured. As selected, the internal user-logic RESET is released either one clock cycle before or after the I/O pins become active. A similar timing selection is programmable for the DONE/PROG output signal. DONE/PROG may also be programmed to be an open drain or include a pull-up resistor to accommodate wired ANDing. The High During Configuration (HDC) and Low During Configuration (LDC) are two user I/O pins which are driven active while an FPGA is in its Initialization, Clear or Configure states. They and DONE/PROG provide signals for control of external logic signals such as RESET, bus enable or PROM enable during configuration. For parallel Master configuration modes, these signals provide PROM enable control and allow the data pins to be shared with user logic signals.

User I/O inputs can be programmed to be either TTL or CMOS compatible thresholds. At power-up, all inputs have TTL thresholds and can change to CMOS thresholds at the completion of configuration if the user has selected CMOS thresholds. The threshold of PWRDWN and the direct clock inputs are fixed at a CMOS level.

If the crystal oscillator is used, it will begin operation before configuration is complete to allow time for stabilization before it is connected to the internal circuitry.

Configuration Data

Configuration data to define the function and interconnection within a Field Programmable Gate Array is loaded from an external storage at power-up and after a re-program signal. Several methods of automatic and controlled loading of the required data are available. Logic levels applied to mode selection pins at the start of configuration time determine the method to be used. See Table 1. The data may be either bit-serial or byte-parallel, depending on the configuration mode. The different FPGAs have different sizes and numbers of data frames. To maintain compatibility between various device types, the Xilinx product families use compatible configuration formats. For the XC3020A, configuration requires 14779 bits for each device, arranged in 197 data frames. An additional 40 bits are used in the header. See Figure 22. The specific data format for each device is produced by the development system and one or more of these files can then be combined and appended to a length count preamble and be transformed into a PROM format file by the development system. A compatibility exception precludes the use of an XC2000-series device as the master for XC3000-series devices if their DONE or RESET are programmed to occur after their outputs become active. The Tie Option defines output levels of unused blocks of a design and connects these to unused routing resources. This prevents indeterminate levels that might produce parasitic supply currents. If unused blocks are not sufficient to complete the tie, the user can indicate nets which must not

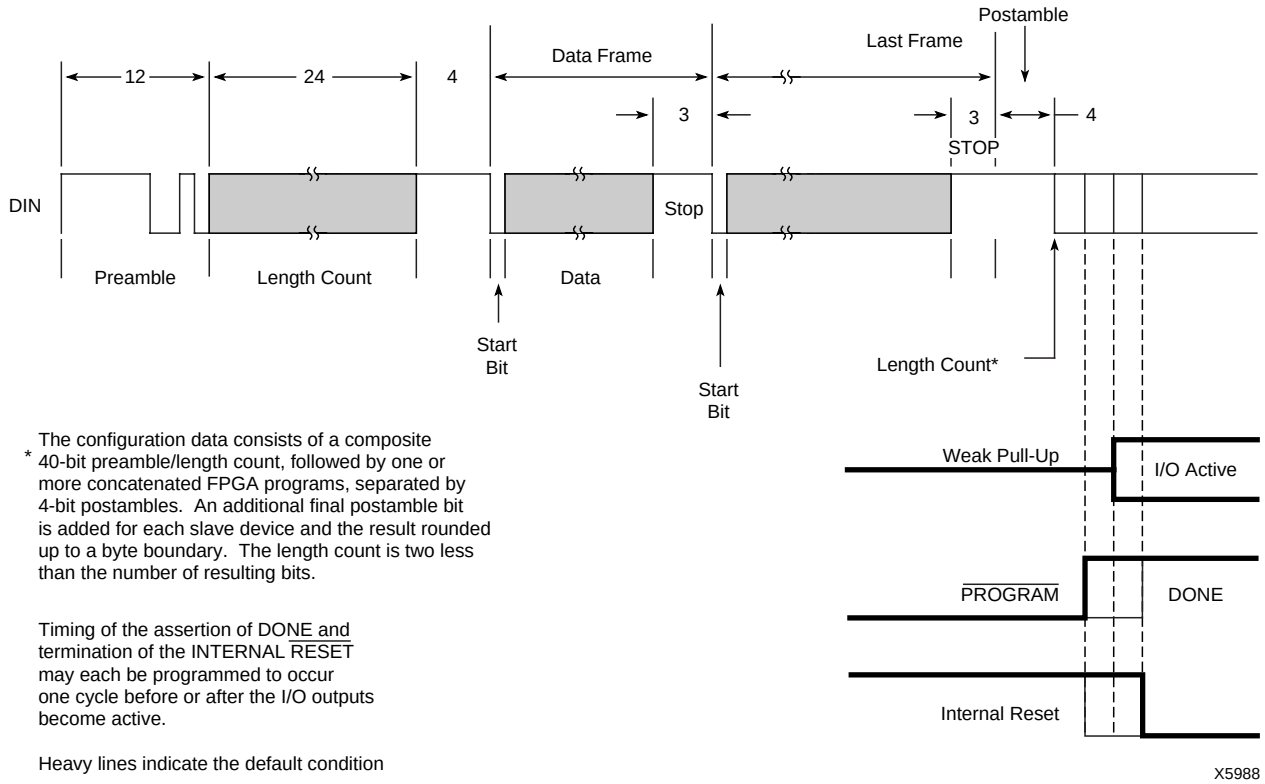


Figure 22: Configuration and Start-up of One or More FPGAs.

Master Parallel Mode

In Master Parallel mode, the lead FPGA directly addresses an industry-standard byte-wide EPROM and accepts eight data bits right before incrementing (or decrementing) the address outputs.

The eight data bits are serialized in the lead FPGA, which then presents the preamble data (and all data that overflows the lead device) on the DOUT pin. There is an internal delay of 1.5 CCLK periods, after the rising CCLK edge that accepts a byte of data, and also changes the EPROM address, until the falling CCLK edge that makes the LSB (D0) of this byte appear at DOUT. This means that DOUT changes on the falling CCLK edge, and the next device in the daisy chain accepts data on the subsequent rising CCLK edge.

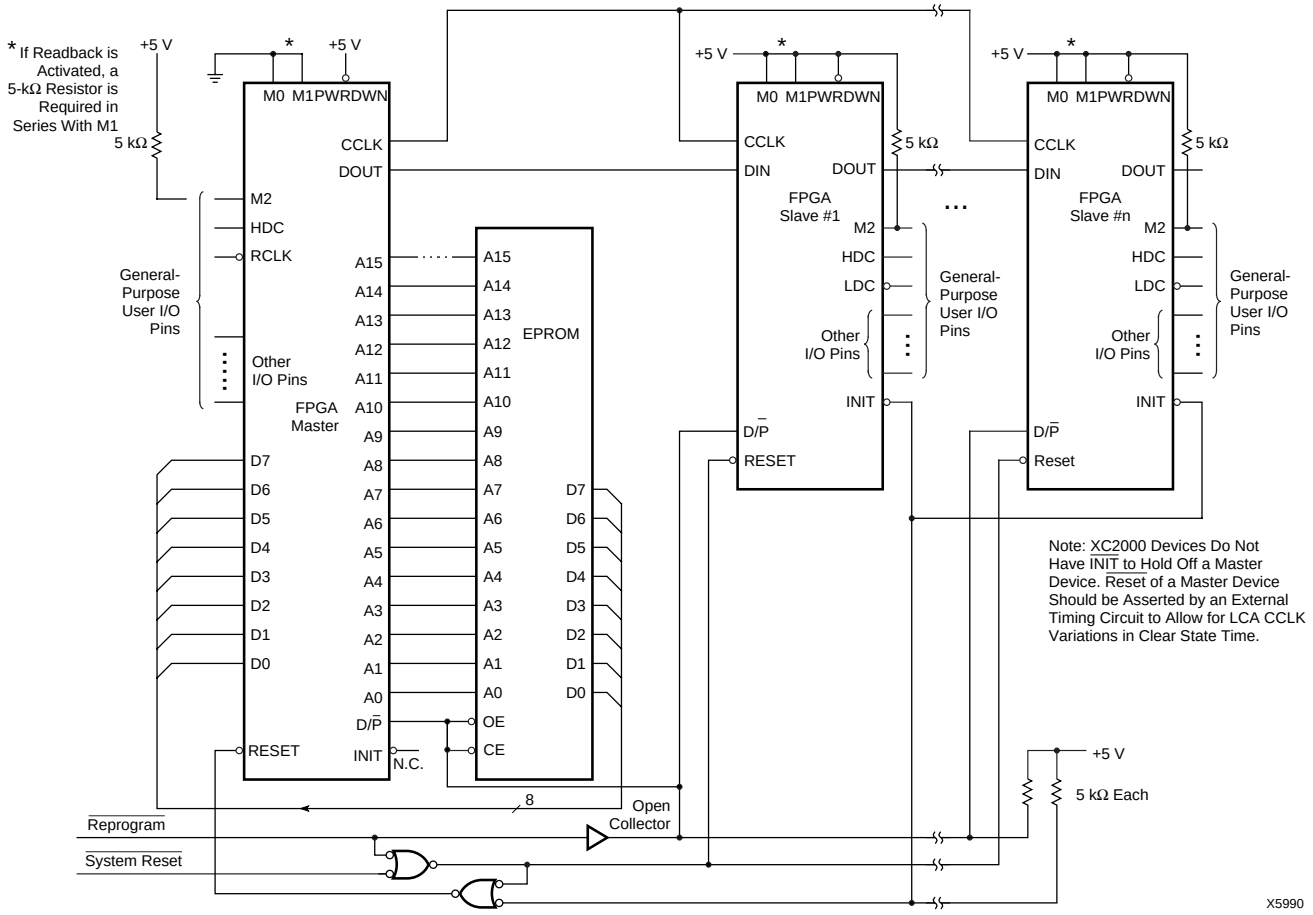


Figure 25: Master Parallel Mode Circuit Diagram

Slave Serial Mode

In Slave Serial mode, an external signal drives the CCLK input(s) of the FPGA(s). The serial configuration bitstream must be available at the DIN input of the lead FPGA a short set-up time before each rising CCLK edge. The lead device then presents the preamble data (and all data that overflows the lead device) on its DOUT pin. There is an internal delay of 0.5 CCLK periods, which means that DOUT changes on the falling CCLK edge, and the next device in the daisy-chain accepts data on the subsequent rising CCLK edge.

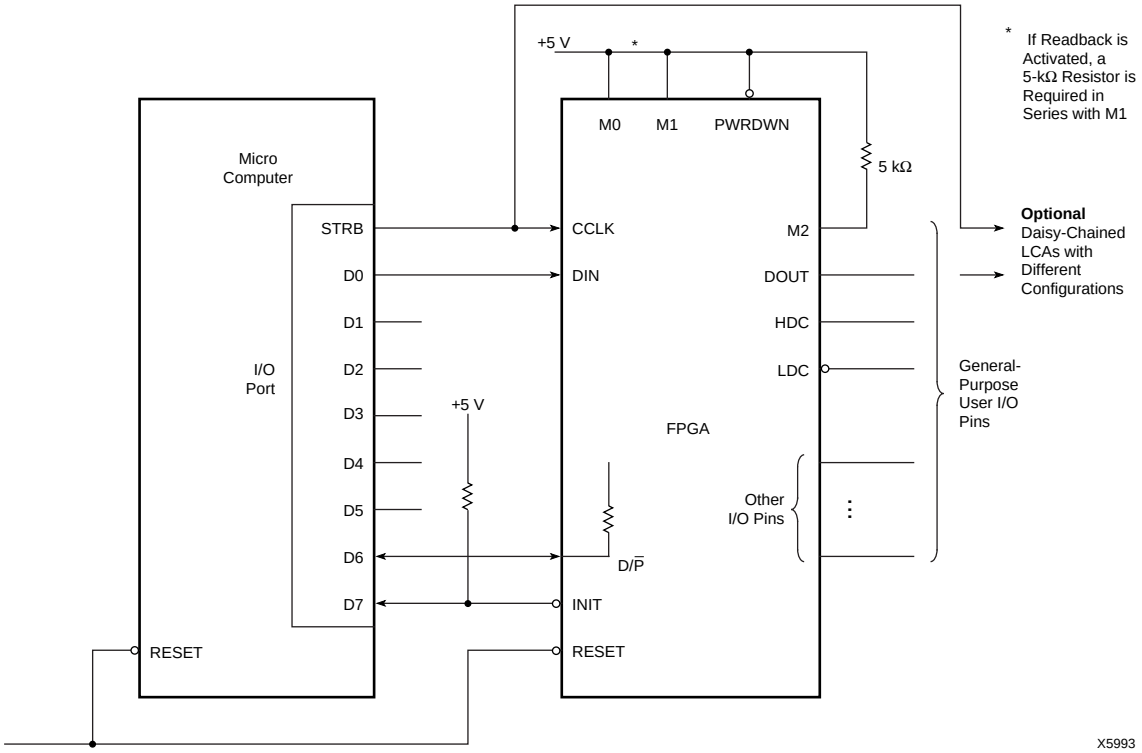
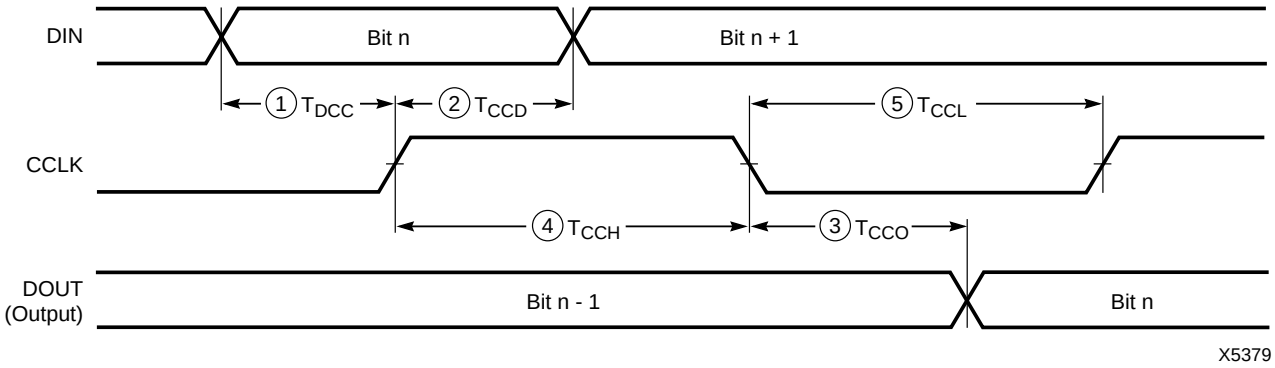


Figure 29: Slave Serial Mode Circuit Diagram



	Description	Symbol		Min	Max	Units
CCLK	To DOUT	3	T_{CCO}		100	ns
	DIN setup	1	T_{DCC}	60		ns
	DIN hold	2	T_{CCD}	0		ns
	High time	4	T_{CCH}	0.05		µs
	Low time (Note 1)	5	T_{CCL}	0.05	5.0	µs
	Frequency		F_{CC}		10	MHz

Notes: 1. The max limit of CCLK Low time is caused by dynamic circuitry inside the FPGA.
2. Configuration must be delayed until the INIT of all FPGAs is High.
3. At power-up, V_{CC} must rise from 2.0 V to V_{CC} min in less than 25 ms. If this is not possible, configuration can be delayed by holding RESET Low until VCC has reached 4.0 V (2.5 V for the XC3000L). A very long V_{CC} rise time of >100 ms, or a non-monotonically rising V_{CC} may require a >6-µs High level on RESET, followed by a >6-µs Low level on RESET and D/P after V_{CC} has reached 4.0 V (2.5 V for the XC3000L).

Figure 30: Slave Serial Mode Programming Switching Characteristics

Pin Functions During Configuration

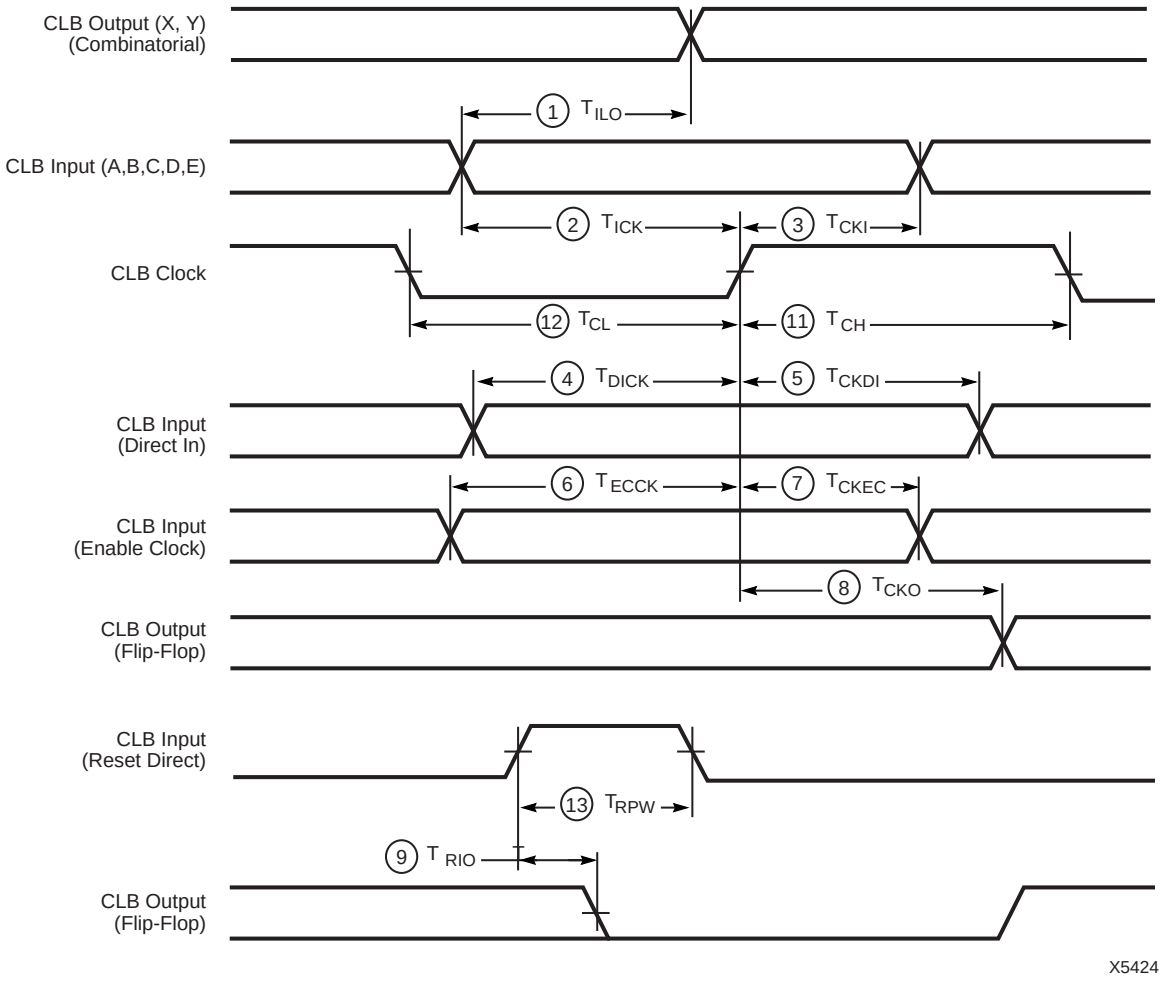
Configuration Mode <M2:M1:M0>					***		**										****	
SLAVE SERIAL <1:1:1>	MASTER-SERIAL <0:0:0>	PERIPH <1:0:1>	MASTER-HIGH <1:1:0>	MASTER-LOW <1:0:0>	44 PLCC	64 VQFP	68 PLCC	84 PLCC	84 PGA	100 PQFP	100 VQFP TQFP	132 PGA	144 TQFP	160 PQFP	175 PGA	176 TQFP	208 PQFP	User Function
POWR DWN (I)	POWER DWN (I)	POWER DWN (I)	POWER DWN (I)	POWER DWN (I)	7	17	10	12	B2	29	26	A1	1	159	B2	1	3	POWER DWN (1)
M1 (HIGH) (I)	M1 (LOW) (I)	M1 (LOW) (I)	M1 (HIGH) (I)	M1 (LOW) (I)	16	31	25	31	J2	52	49	B13	36	40	B14	45	48	RDATA
M0 (HIGH) (I)	M0 (LOW) (I)	M0 (HIGH) (I)	M0 (LOW) (I)	M0 (LOW) (I)	17	32	26	32	L1	54	51	A14	38	42	B15	47	50	RTRIG (I)
M2 (HIGH) (I)	M2 (LOW) (I)	M2 (HIGH) (I)	M2 (HIGH) (I)	M2 (HIGH) (I)	18	33	27	33	K2	56	53	C13	40	44	C15	49	56	I/O
HDC (HIGH)	HDC (HIGH)	HDC (HIGH)	HDC (HIGH)	HDC (HIGH)	19	34	28	34	K3	57	54	B14	41	45	E14	50	57	I/O
LDC (LOW)	LDC (LOW)	LDC (LOW)	LDC (LOW)	LDC (LOW)	20	36	30	36	L3	59	56	D14	45	49	D16	54	61	I/O
INIT*	INIT*	INIT*	INIT*	INIT*	22	40	34	42	K6	65	62	G14	53	59	H15	65	77	I/O
GND	GND	GND	GND	GND	23	41	35	43	J6	66	63	H12	55	61	J14	67	79	GND
					26	47	43	53	L11	76	73	M13	69	76	P15	85	100	XTL2 OR I/O
RESET (I)	RESET (I)	RESET (I)	RESET (I)	RESET (I)	27	48	44	54	K10	78	75	P14	71	78	R15	87	102	RESET (I)
DONE	DONE	DONE	DONE	DONE	28	49	45	55	J10	80	77	N13	73	80	R14	89	107	PROGRAM (I)
		DATA 7 (I)	DATA 7 (I)	DATA 7 (I)		50	46	56	K11	81	78	M12	74	81	N13	90	109	I/O
					30	51	47	57	J11	82	79	P13	75	82	T14	91	110	XTL1 OR I/O
		DATA 6 (I)	DATA 6 (I)	DATA 6 (I)		52	48	58	H10	83	80	N11	78	86	P12	96	115	I/O
		DATA 5 (I)	DATA 5 (I)	DATA 5 (I)		53	49	60	F10	87	84	M9	84	92	T11	102	122	I/O
		CS0 (I)				54	50	61	G10	88	85	N9	85	93	R10	103	123	I/O
		DATA 4 (I)	DATA 4 (I)	DATA 4 (I)		55	51	62	G11	89	86	N8	88	96	R9	108	128	I/O
		DATA 3 (I)	DATA 3 (I)	DATA 3 (I)		57	53	65	F11	92	89	N7	92	102	P8	112	132	I/O
		CS1 (I)				58	54	66	E11	93	90	P6	93	103	R8	113	133	I/O
		DATA 2 (I)	DATA 2 (I)	DATA 2 (I)		59	55	67	E10	94	91	M6	96	106	R7	118	138	I/O
		DATA 1 (I)	DATA 1 (I)	DATA 1 (I)		60	56	70	D10	98	95	M5	102	114	R5	124	145	I/O
		RDY/BUSY	$\overline{\text{RCLK}}$	$\overline{\text{RCLK}}$		61	57	71	C11	99	96	N4	103	115	P5	125	146	I/O
DIN (I)	DIN (I)	DATA 0 (I)	DATA 0 (I)	DATA 0 (I)	38	62	58	72	B11	100	97	N2	106	119	R3	130	151	I/O
DOUT	DOUT	DOUT	DOUT	DOUT	39	63	59	73	C10	1	98	M3	107	120	N4	131	152	I/O
CCLK (I)	CCLK (O)	CCLK (O)	CCLK (O)	CCLK (O)	40	64	60	74	A11	2	99	P1	108	121	R2	132	153	CCLK (I)
		WS (I)	A0	A0		1	61	75	B10	5	2	M2	111	124	P2	135	161	I/O
		CS2 (I)	A1	A1		2	62	76	B9	6	3	N1	112	125	M3	136	162	I/O
			A2	A2		3	63	77	A10	8	5	L2	115	128	P1	140	165	I/O
			A3	A3		4	64	78	A9	9	6	L1	116	129	N1	141	166	I/O
			A15	A15			65	81	B6	12	9	K1	119	132	M1	146	172	5
			A4	A4		5	66	82	B7	13	10	J2	120	133	L2	147	173	I/O
			A14	A14		6	67	83	A7	14	11	H1	123	136	K2	150	178	I/O
			A5	A5		7	68	84	C7	15	12	H2	124	137	K1	151	179	I/O
			A13	A13		9	2	2	A6	17	14	G2	128	141	H2	156	184	I/O
			A6	A6		10	3	3	A5	18	15	G1	129	142	H1	157	185	I/O
			A12	A12		11	4	4	B5	19	16	F2	133	147	F2	164	192	I/O
			A7	A7		12	5	5	C5	20	17	E1	134	148	E1	165	193	I/O
			A11	A11		13	6	8	A3	23	20	D1	137	151	D1	169	199	I/O
			A8	A8		14	7	9	A2	24	21	D2	138	152	C1	170	200	I/O
			A10	A10		15	8	10	B3	25	22	B1	141	155	E3	173	203	I/O
			A9	A9		16	9	11	A1	26	26	C2	142	156	C2	174	204	I/O
																		All Others
							X	X	X	X								XC3x20A etc.
					X	X	X	X	X	X	X							XC3x30A etc.
								X	X	X	X	X	X					XC3x42A etc.
								X**				X	X					XC3x64A etc.
								X**					X	X	X	X	X	XC3x90A etc.
								X**						X	X		X	XC3195A

Notes:

Generic I/O pins are not shown.
For a detailed description of the configuration modes, see page 25 through page 34.
For pinout details, see page 65 through page 76.
Represents a weak pull-up before and during configuration.
* INIT is an open drain output during configuration.
(I) Represents an input.
** Pin assignment for the XC3064A/XC3090A and XC3195A differ from those shown.
*** Peripheral mode and master parallel mode are not supported in the PC44 package.
**** Pin assignments for the XC3195A PQ208 differ from those shown.
Pin assignments of PGA Footprint PLCC sockets and PGA packages are not identical.
The information on this page is provided as a convenient summary. For detailed pin descriptions, see the preceding two pages.

Note: Before and during configuration, all outputs that are not used for the configuration process are 3-stated with a weak pull-up resistor.

XC3000A CLB Switching Characteristics Guidelines (continued)



XC3000L Absolute Maximum Ratings

Symbol	Description		Units
V_{CC}	Supply voltage relative to GND	–0.5 to +7.0	V
V_{IN}	Input voltage with respect to GND	–0.5 to V_{CC} +0.5	V
V_{TS}	Voltage applied to 3-state output	–0.5 to V_{CC} +0.5	V
T_{STG}	Storage temperature (ambient)	–65 to +150	°C
T_{SOL}	Maximum soldering temperature (10 s @ 1/16 in.)	+260	°C
T_J	Junction temperature plastic	+125	°C
	Junction temperature ceramic	+150	°C

Note: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

XC3000L Global Buffer Switching Characteristics Guidelines

	Speed Grade	-8	
Description	**Symbol**	**Max**	**Units**
Global and Alternate Clock Distribution[1]			
Either: **Normal** IOB input pad through clock buffer to any CLB or IOB clock input	T_{PID}	9.0	ns
Or: **Fast** (CMOS only) input pad through clock buffer to any CLB or IOB clock input	T_{PIDC}	7.0	ns
TBUF driving a Horizontal Longline (L.L.)[1]			
I to L.L. while T is Low (buffer active)	T_{IO}	5.0	ns
T↓ to L.L. active and valid with single pull-up resistor	T_{ON}	12.0	ns
T↑ to L.L. High with single pull-up resistor	T_{PUS}	24.0	ns
BIDI			
Bidirectional buffer delay	T_{BIDI}	2.0	ns

Notes: 1. Timing is based on the XC3042A, for other devices see timing calculator.
2. The use of two pull-up resistors per Longline, available on other XC3000 devices, is not a valid option for XC3000L devices.

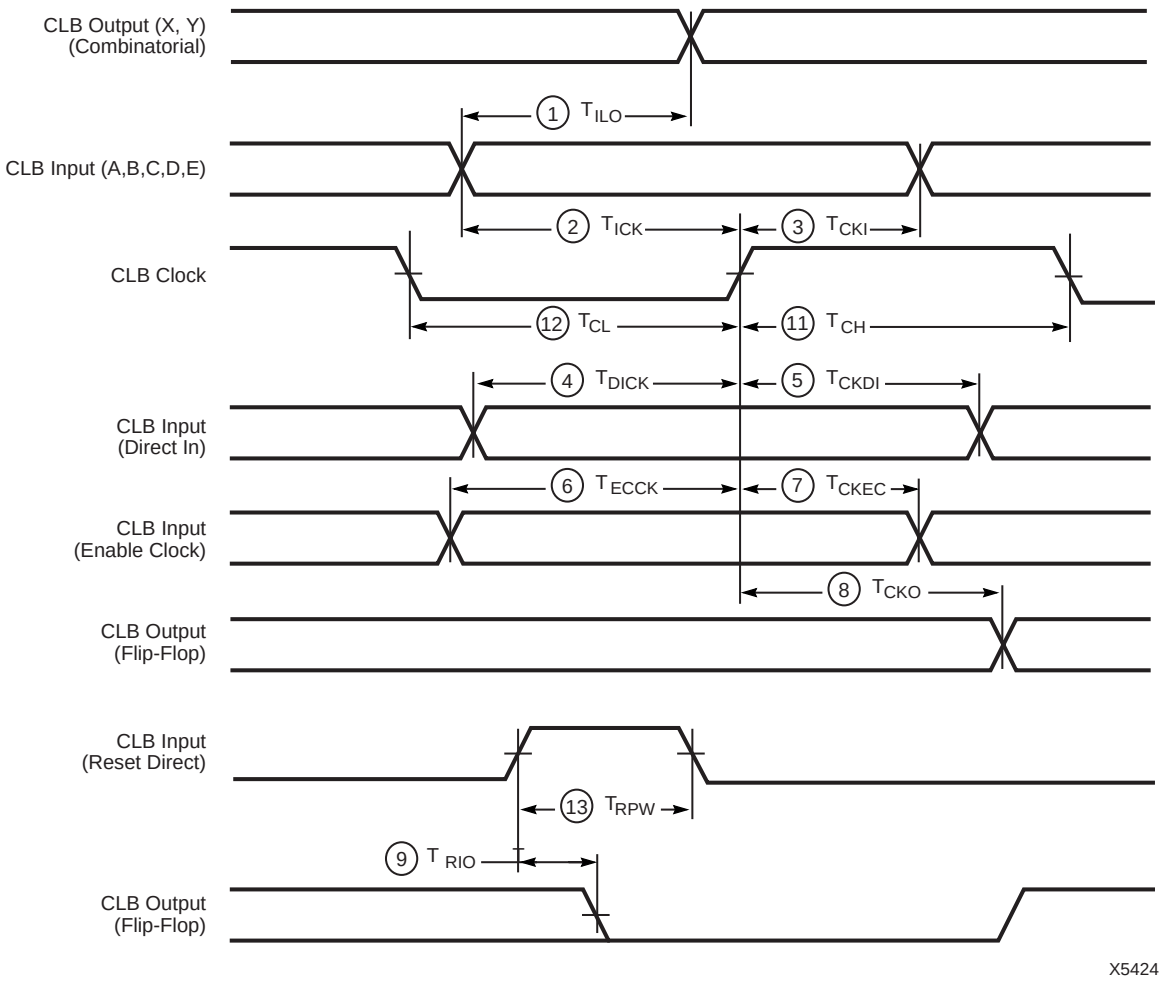
XC3000L CLB Switching Characteristics Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Since many internal timing parameters cannot be measured directly, they are derived from benchmark timing patterns. The following guidelines reflect worst-case values over the recommended operating conditions. For more detailed, more precise, and more up-to-date timing information, use the values provided by the timing calculator and used in the simulator.

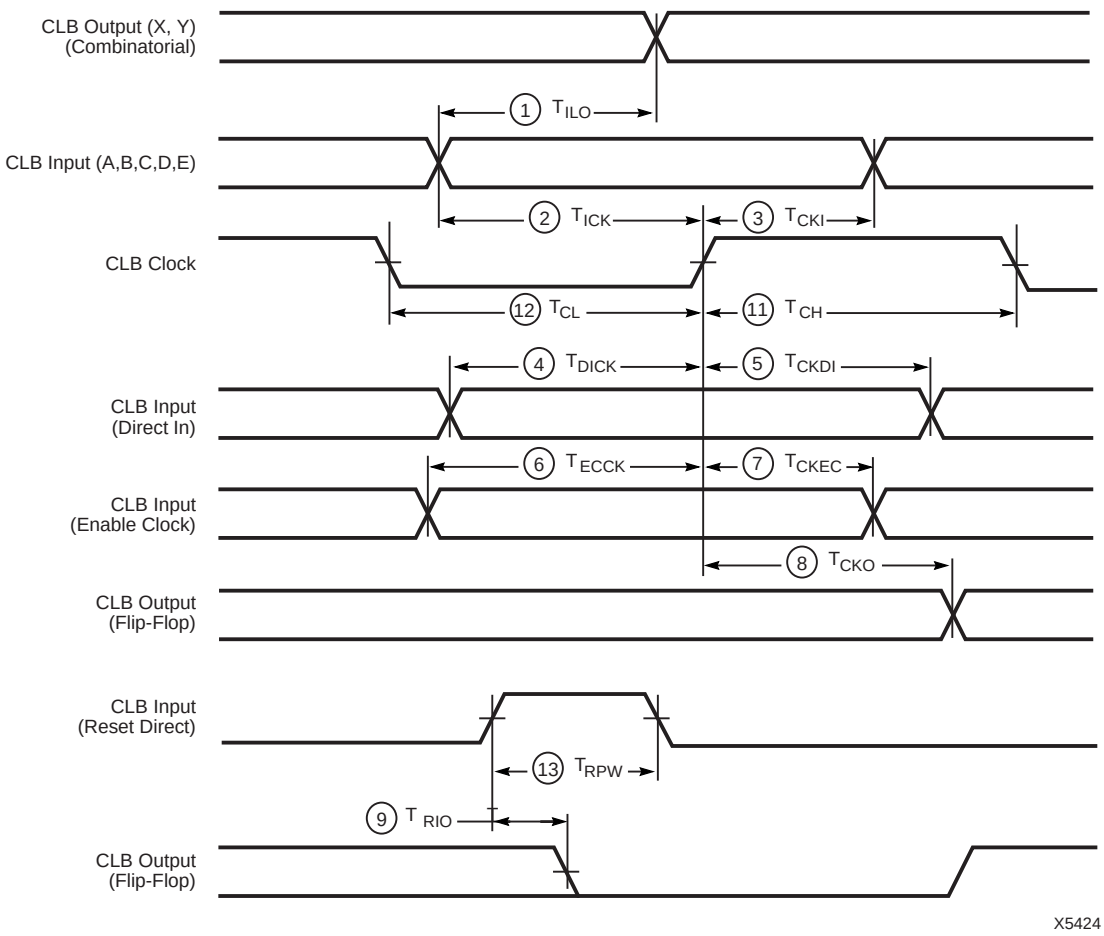
		Speed Grade		-8		
Description		**Symbol**		**Min**	**Max**	**Units**
Combinatorial Delay						
Logic Variables	A, B, C, D, E, to outputs X or Y					
	FG Mode	1	T_{ILO}		6.7	ns
	F and FGM Mode				7.5	ns
Sequential delay						
Clock k to outputs X or Y		8	T_{CKO}		7.5	ns
Clock k to outputs X or Y when Q is returned through function generators F or G to drive X or Y			T_{QLO}			
	FG Mode				14.0	ns
	F and FGM Mode				14.8	ns
Set-up time before clock K						
Logic Variables	A, B, C, D, E					
	FG Mode	2	T_{ICK}	5.0		ns
	F and FGM Mode			5.8		ns
Data In	DI	4	T_{DICK}	5.0		ns
Enable Clock	EC	6	T_{ECCK}	6.0		ns
Hold Time after clock K						
Logic Variables	A, B, C, D, E	3	T_{CKI}	0		ns
Data In	DI[2]	5	T_{CKDI}	2.0		ns
Enable Clock	EC	7	T_{CKEC}	2.0		ns
Clock						
Clock High time		11	T_{CH}	5.0		ns
Clock Low time		12	T_{CL}	5.0		ns
Max. flip-flop toggle rate			F_{CLK}	80.0		MHz
Reset Direct (RD)						
RD width		13	T_{RPW}	7.0		ns
delay from RD to outputs X or Y		9	T_{RIO}	7.0		ns
Global Reset ($\overline{\text{RESET}}$ Pad)[1]						
$\overline{\text{RESET}}$ width (Low)			T_{MRW}	16.0		ns
delay from $\overline{\text{RESET}}$ pad to outputs X or Y			T_{MRQ}		23.0	ns

Notes: 1. Timing is based on the XC3042L, for other devices see timing calculator.
2. The CLB K to Q output delay (T_{CKO}, #8) of any CLB, plus the shortest possible interconnect delay, is always longer than the Data In hold time requirement (T_{CKDI}, #5) of any CLB on the same die.

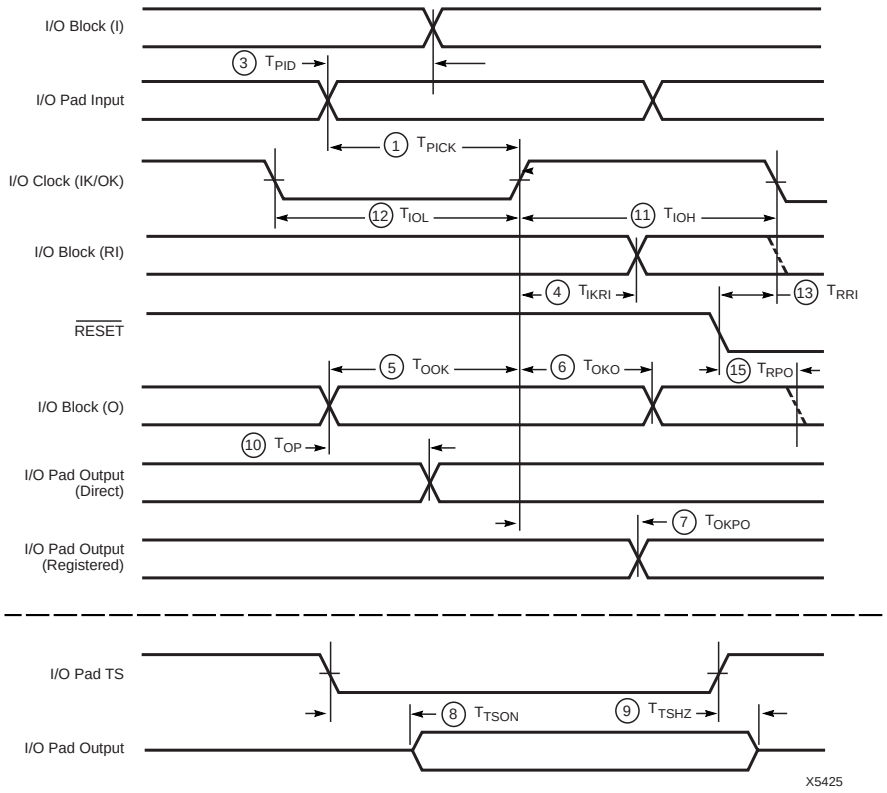
XC3000L CLB Switching Characteristics Guidelines (continued)

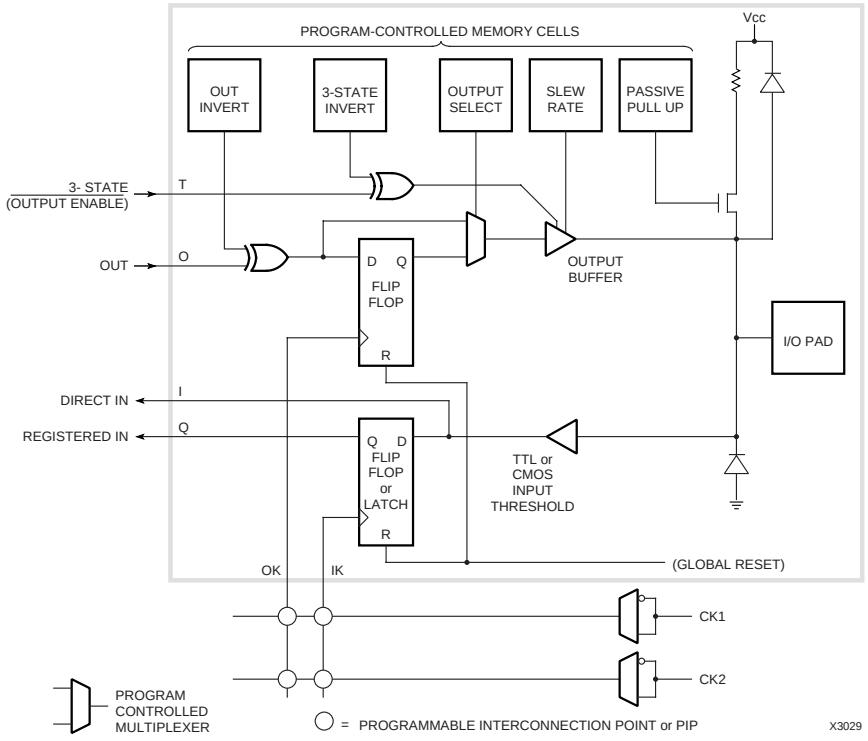


XC3100A CLB Switching Characteristics Guidelines (continued)



XC3100A IOB Switching Characteristics Guidelines (continued)





XC3100L Switching Characteristics

Xilinx maintains test specifications for each product as controlled documents. To insure the use of the most recently released device performance parameters, please request a copy of the current test-specification revision.

XC3100L Operating Conditions

Symbol	Description	Min	Max	Units
V_{CC}	Supply voltage relative to GND Commercial 0°C to +85°C junction	3.0	3.6	V
V_{IH}	High-level input voltage	2.0	V_{CC} + 0.3	V
V_{IL}	Low-level input voltage	-0.3	0.8	V
T_{IN}	Input signal transition time		250	ns

Notes: 1. At junction temperatures above those listed as Operating Conditions, all delay parameters increase by 0.3% per °C.
2. Although the present (1996) devices operate over the full supply voltage range from 3.0 V to 5.25 V, Xilinx reserves the right to restrict operation to the 3.0 and 3.6 V range later, when smaller device geometries might preclude operation @ 5 V. Operating conditions are guaranteed in the 3.0 – 3.6 V V_{CC} range.

XC3100L DC Characteristics Over Operating Conditions

Symbol	Description	Min	Max	Units
V_{OH}	High-level output voltage (@ I_{OH} = -4.0 mA, V_{CC} min)	2.4		V
	High-level output voltage (@ I_{OH} = -100.0 µA, V_{CC} min)	V_{CC} -0.2		V
V_{OL}	Low-level output voltage (@ I_{OH} = 4.0 mA, V_{CC} min)		0.40	V
	Low-level output voltage (@ I_{OH} = +100.0 µA, V_{CC} min)		0.2	V
V_{CCPD}	Power-down supply voltage (PWRDWN must be Low)	2.30		V
I_{CCO}	Quiescent FPGA supply current Chip thresholds programmed as CMOS levels[1]		1.5	mA
I_{IL}	Input Leakage Current	-10	+10	µA
C_{IN}	Input capacitance (sample tested) All pins except XTL1 and XTL2 XTL1 and XTL2		 10 15	 pF pF
I_{RIN}	Pad pull-up (when selected) @ V_{IN} = 0 V [3]	0.02	0.17	mA
I_{RLL}	Horizontal long line pull-up (when selected) @ logic Low	0.20	2.80	mA

Notes: 1. With no output current loads, no active input or long line pull-up resistors, all package pins at V_{CC} or GND, and the FPGA configured with a tie option.
2. Total continuous output sink current may not exceed 100 mA per ground pin. Total continuous output source current may not exceed 100 mA per V_{CC} pin. The number of ground pins varies from the XC3142L to the XC3190L.
3. Not tested. Allows undriven pins to float High. For any other purpose, use an external pull-up.

XC3000 Series 64-Pin Plastic VQFP Pinouts

XC3000A, XC3000L, and XC3100A families have identical pinouts

Pin No.	XC3030A
1	A0-WS-I/O
2	A1-CS2-I/O
3	A2-I/O
4	A3-I/O
5	A4-I/O
6	A14-I/O
7	A5-I/O
8	**GND**
9	A13-I/O
10	A6-I/O
11	A12-I/O
12	A7-I/O
13	A11-I/O
14	A8-I/O
15	A10-I/O
16	A9-I/O
17	PWRDN
18	TCLKIN-I/O
19	I/O
20	I/O
21	I/O
22	I/O
23	I/O
24	**VCC**
25	I/O
26	I/O
27	I/O
28	I/O
29	I/O
30	I/O
31	M1-$\overline{\text{RDATA}}$
32	M0-RTRIG

Pin No.	XC3030A
33	M2-I/O
34	HDC-I/O
35	I/O
36	$\overline{\text{LDC}}$-I/O
37	I/O
38	I/O
39	I/O
40	$\overline{\text{INIT}}$-I/O
41	**GND**
42	I/O
43	I/O
44	I/O
45	I/O
46	I/O
47	XTAL2(IN)-I/O
48	$\overline{\text{RESET}}$
49	DONE-PG
50	D7-I/O
51	XTAL1(OUT)-BCLKIN-I/O
52	D6-I/O
53	D5-I/O
54	$\overline{\text{CS0}}$-I/O
55	D4-I/O
56	VCC
57	D3-I/O
58	$\overline{\text{CS1}}$-I/O
59	D2-I/O
60	D1-I/O
61	RDY/$\overline{\text{BUSY}}$-RCLK-I/O
62	D0-DIN-I/O
63	DOUT-I/O
64	CCLK

XC3000 Series 144-Pin Plastic TQFP Pinouts

XC3000A, XC3000L, XC3100A, and XC3100L families have identical pinouts

Pin Number	XC3042A XC3064A XC3090A
1	$\overline{\text{PWRDN}}$
2	I/O-TCLKIN
3	I/O*
4	I/O
5	I/O
6	I/O*
7	I/O
8	I/O
9	I/O*
10	I/O
11	I/O
12	I/O
13	I/O
14	I/O
15	I/O*
16	I/O
17	I/O
18	GND
19	VCC
20	I/O
21	I/O
22	I/O
23	I/O
24	I/O
25	I/O
26	I/O
27	I/O
28	I/O*
29	I/O
30	I/O
31	I/O*
32	I/O*
33	I/O
34	I/O*
35	I/O
36	M1-$\overline{\text{RD}}$
37	GND
38	M0-RT
39	VCC
40	M2-I/O
41	HDC-I/O
42	I/O
43	I/O
44	I/O
45	$\overline{\text{LDC}}$-I/O
46	I/O*
47	I/O
48	I/O

Pin Number	XC3042A XC3064A XC3090A
49	I/O
50	I/O*
51	I/O
52	I/O
53	$\overline{\text{INIT}}$-I/O
54	VCC
55	GND
56	I/O
57	I/O
58	I/O
59	I/O
60	I/O
61	I/O
62	I/O
63	I/O*
64	I/O*
65	I/O
66	I/O
67	I/O
68	I/O
69	XTL2(IN)-I/O
70	GND
71	$\overline{\text{RESET}}$
72	VCC
73	DONE-$\overline{\text{PG}}$
74	D7-I/O
75	XTL1(OUT)-BCLKIN-I/O
76	I/O
77	I/O
78	D6-I/O
79	I/O
80	I/O*
81	I/O
82	I/O
83	I/O*
84	D5-I/O
85	$\overline{\text{CS0}}$-I/O
86	I/O*
87	I/O*
88	D4-I/O
89	I/O
90	VCC
91	GND
92	D3-I/O
93	$\overline{\text{CS1}}$-I/O
94	I/O*
95	I/O*
96	D2-I/O

Pin Number	XC3042A XC3064A XC3090A
97	I/O
98	I/O
99	I/O*
100	I/O
101	I/O*
102	D1-I/O
103	RDY/$\overline{\text{BUSY}}$-$\overline{\text{RCLK}}$-I/O
104	I/O
105	I/O
106	D0-DIN-I/O
107	DOUT-I/O
108	CCLK
109	VCC
110	GND
111	A0-$\overline{\text{WS}}$-I/O
112	A1-CS2-I/O
113	I/O
114	I/O
115	A2-I/O
116	A3-I/O
117	I/O
118	I/O
119	A15-I/O
120	A4-I/O
121	I/O*
122	I/O*
123	A14-I/O
124	A5-I/O
125	I/O (XC3090 only)
126	GND
127	VCC
128	A13-I/O
129	A6-I/O
130	I/O*
131	I/O (XC3090 only)
132	I/O*
133	A12-I/O
134	A7-I/O
135	I/O
136	I/O
137	A11-I/O
138	A8-I/O
139	I/O
140	I/O
141	A10-I/O
142	A9-I/O
143	VCC
144	GND

Unprogrammed IOBs have a default pull-up. This prevents an undefined pad level for unbonded or unused IOBs. Programmed outputs are default slew-rate limited.

* Indicates unconnected package pins (24) for the XC3042A.

XC3000 Series 160-Pin PQFP Pinouts

XC3000A, XC3000L, XC3100A, and XC3100L families have identical pinouts

PQFP Pin Number	XC3064A, XC3090A, XC3195A
1	I/O*
2	I/O*
3	I/O*
4	I/O
5	I/O
6	I/O
7	I/O
8	I/O
9	I/O
10	I/O
11	I/O
12	I/O
13	I/O
14	I/O
15	I/O
16	I/O
17	I/O
18	I/O
19	GND
20	VCC
21	I/O*
22	I/O
23	I/O
24	I/O
25	I/O
26	I/O
27	I/O
28	I/O
29	I/O
30	I/O
31	I/O
32	I/O
33	I/O
34	I/O
35	I/O
36	I/O
37	I/O
38	I/O*
39	I/O*
40	M1-$\overline{\text{RDATA}}$

PQFP Pin Number	XC3064A, XC3090A, XC3195A
41	GND
42	M0–RTRIG
43	VCC
44	M2-I/O
45	HDC-I/O
46	I/O
47	I/O
48	I/O
49	$\overline{\text{LDC}}$-I/O
50	I/O*
51	I/O*
52	I/O
53	I/O
54	I/O
55	I/O
56	I/O
57	I/O
58	I/O
59	$\overline{\text{INIT}}$-I/O
60	VCC
61	GND
62	I/O
63	I/O
64	I/O
65	I/O
66	I/O
67	I/O
68	I/O
69	I/O
70	I/O
71	I/O
72	I/O
73	I/O
74	I/O
75	I/O*
76	XTL2-I/O
77	GND
78	$\overline{\text{RESET}}$
79	VCC
80	DONE/$\overline{\text{PG}}$

PQFP Pin Number	XC3064A, XC3090A, XC3195A
81	D7-I/O
82	XTL1-I/O-BCLKIN
83	I/O*
84	I/O
85	I/O
86	D6-I/O
87	I/O
88	I/O
89	I/O
90	I/O
91	I/O
92	D5-I/O
93	$\overline{\text{CS0}}$-I/O
94	I/O*
95	I/O*
96	I/O
97	I/O
98	D4-I/O
99	I/O
100	VCC
101	GND
102	D3-I/O
103	$\overline{\text{CS1}}$-I/O
104	I/O
105	I/O
106	I/O*
107	I/O*
108	D2-I/O
109	I/O
110	I/O
111	I/O
112	I/O
113	I/O
114	D1-I/O
115	RDY/$\overline{\text{BUSY}}$-$\overline{\text{RCLK}}$-I/O
116	I/O
117	I/O
118	I/O*
119	D0-DIN-I/O
120	DOUT-I/O

PQFP Pin Number	XC3064A, XC3090A, XC3195A
121	CCLK
122	VCC
123	GND
124	A0-$\overline{\text{WS}}$-I/O
125	A1-CS2-I/O
126	I/O
127	I/O
128	A2-I/O
129	A3-I/O
130	I/O
131	I/O
132	A15-I/O
133	A4-I/O
134	I/O
135	I/O
136	A14-I/O
137	A5-I/O
138	I/O*
139	GND
140	VCC
141	A13-I/O
142	A6-I/O
143	I/O*
144	I/O*
145	I/O
146	I/O
147	A12-I/O
148	A7-I/O
149	I/O
150	I/O
151	A11-I/O
152	A8-I/O
153	I/O
154	I/O
155	A10-I/O
156	A9-I/O
157	VCC
158	GND
159	$\overline{\text{PWRDWN}}$
160	TCLKIN-I/O

Unprogrammed IOBs have a default pull-up. This prevents an undefined pad level for unbonded or unused IOBs. Programmed IOBs are default slew-rate limited.

* Indicates unconnected package pins (18) for the XC3064A.

XC3000 Series 176-Pin TQFP Pinouts

XC3000A, XC3000L, XC3100A, and XC3100L families have identical pinouts

Pin Number	XC3090A
1	$\overline{\text{PWRDWN}}$
2	TCLKIN-I/O
3	I/O
4	I/O
5	I/O
6	I/O
7	I/O
8	I/O
9	I/O
10	I/O
11	I/O
12	I/O
13	I/O
14	I/O
15	I/O
16	I/O
17	I/O
18	I/O
19	I/O
20	I/O
21	I/O
22	GND
23	VCC
24	I/O
25	I/O
26	I/O
27	I/O
28	I/O
29	I/O
30	I/O
31	I/O
32	I/O
33	I/O
34	I/O
35	I/O
36	I/O
37	I/O
38	I/O
39	I/O
40	I/O
41	I/O
42	I/O
43	I/O
44	–

Pin Number	XC3090A
45	M1-$\overline{\text{RDATA}}$
46	GND
47	M0-RTRIG
48	VCC
49	M2-I/O
50	HDC-I/O
51	I/O
52	I/O
53	I/O
54	$\overline{\text{LDC}}$-I/O
55	–
56	I/O
57	I/O
58	I/O
59	I/O
60	I/O
61	I/O
62	I/O
63	I/O
64	I/O
65	$\overline{\text{INIT}}$-I/O
66	VCC
67	GND
68	I/O
69	I/O
70	I/O
71	I/O
72	I/O
73	I/O
74	I/O
75	I/O
76	I/O
77	I/O
78	I/O
79	I/O
80	I/O
81	I/O
82	–
83	–
84	I/O
85	XTAL2(IN)-I/O
86	GND
87	$\overline{\text{RESET}}$
88	VCC

Pin Number	XC3090A
89	DONE-$\overline{\text{PG}}$
90	D7-I/O
91	XTAL1(OUT)-BCLKIN-I/O
92	I/O
93	I/O
94	I/O
95	I/O
96	D6-I/O
97	I/O
98	I/O
99	I/O
100	I/O
101	I/O
102	D5-I/O
103	$\overline{\text{CS0}}$-I/O
104	I/O
105	I/O
106	I/O
107	I/O
108	D4-I/O
109	I/O
110	VCC
111	GND
112	D3-I/O
113	$\overline{\text{CS1}}$-I/O
114	I/O
115	I/O
116	I/O
117	I/O
118	D2-I/O
119	I/O
120	I/O
121	I/O
122	I/O
123	I/O
124	D1-I/O
125	RDY/$\overline{\text{BUSY}}$-$\overline{\text{RCLK}}$-I/O
126	I/O
127	I/O
128	I/O
129	I/O
130	D0-DIN-I/O
131	DOUT-I/O
132	CCLK

Pin Number	XC3090A
133	VCC
134	GND
135	A0-$\overline{\text{WS}}$-I/O
136	A1-CS2-I/O
137	–
138	I/O
139	I/O
140	A2-I/O
141	A3-I/O
142	–
143	–
144	I/O
145	I/O
146	A15-I/O
147	A4-I/O
148	I/O
149	I/O
150	A14-I/O
151	A5-I/O
152	I/O
153	I/O
154	GND
155	VCC
156	A13-I/O
157	A6-I/O
158	I/O
159	I/O
160	–
161	–
162	I/O
163	I/O
164	A12-I/O
165	A7-I/O
166	I/O
167	I/O
168	–
169	A11-I/O
170	A8-I/O
171	I/O
172	I/O
173	A10-I/O
174	A9-I/O
175	VCC
176	GND

Unprogrammed IOBs have a default pull-up. This prevents an undefined pad level for unbonded or unused IOBs. Programmed outputs are default slew-rate limited.

XC3195A PQ208 Pinouts

Pin Description	PQ208
A9-I/O	206
A10-I/O	205
I/O	204
I/O	203
I/O	202
I/O	201
A8-I/O	200
A11-I/O	199
I/O	198
I/O	197
I/O	196
I/O	194
A7-I/O	193
A12-I/O	192
I/O	191
I/O	190
I/O	189
I/O	188
I/O	187
I/O	186
A6-I/O	185
A13-I/O	184
VCC	183
GND	182
I/O	181
I/O	180
A5-I/O	179
A14-I/O	178
I/O	177
I/O	176
I/O	175
I/O	174
A4-I/O	173
A15-I/O	172
I/O	171
I/O	169
I/O	168
I/O	167
A3-I/O	166
A2-I/O	165
I/O	164
I/O	163
I/O	162
I/O	161
A1-CS2-I/O	160
A0-$\overline{WS}$-I/O	159
GND	158
VCC	157
CCLK	156
DOUT-I/O	155

Pin Description	PQ208
D0-DIN-I/O	154
I/O	153
I/O	152
I/O	151
I/O	150
RDY/BUSY-RCLK-I/O	149
D1-I/O	148
I/O	147
I/O	146
I/O	145
I/O	144
I/O	141
I/O	140
I/O	139
D2-I/O	138
I/O	137
I/O	136
I/O	135
I/O	134
$\overline{CS1}$-I/O	133
D3-I/O	132
GND	131
VCC	130
I/O	129
D4-I/O	128
I/O	127
I/O	126
I/O	125
I/O	124
$\overline{CS0}$-I/O	123
D5-I/O	122
I/O	121
I/O	120
I/O	119
I/O	118
I/O	117
I/O	116
I/O	115
D6-I/O	114
I/O	113
I/O	112
I/O	111
I/O	110
XTLX1(OUT)BCLKN-I/O	109
D7-I/O	108
D/$\overline{P}$	107
VCC	106
$\overline{RESET}$	105
GND	104
XTL2(IN)-I/O	103

Pin Description	PQ208
I/O	102
I/O	101
I/O	100
I/O	99
I/O	98
I/O	97
I/O	96
I/O	95
I/O	94
I/O	93
I/O	92
I/O	89
I/O	88
I/O	87
I/O	86
I/O	85
I/O	84
I/O	83
I/O	82
I/O	81
I/O	80
GND	79
VCC	78
$\overline{INIT}$	77
I/O	76
I/O	75
I/O	74
I/O	73
I/O	72
I/O	71
I/O	70
I/O	69
I/O	68
I/O	67
I/O	66
I/O	63
I/O	62
I/O	61
I/O	60
$\overline{LDC}$-I/O	59
I/O	58
I/O	57
I/O	56
HDC-I/O	55
M2-I/O	54
VCC	53
M0-RTIG	52
GND	51
M1/$\overline{RDATA}$	50
I/O	49

Pin Description	PQ208
I/O	48
I/O	47
I/O	46
I/O	45
I/O	44
I/O	43
I/O	42
I/O	41
I/O	40
I/O	39
I/O	38
I/O	37
I/O	36
I/O	35
I/O	34
I/O	33
I/O	32
I/O	31
I/O	30
I/O	29
I/O	28
VCC	27
GND	26
I/O	25
I/O	24
I/O	23
I/O	22
I/O	21
I/O	20
I/O	19
I/O	18
I/O	17
I/O	14
I/O	13
I/O	12
I/O	11
I/O	10
I/O	9
I/O	8
I/O	7
I/O	6
I/O	5
I/O	4
I/O	3
TCLKIN-I/O	2
$\overline{PWRDN}$	1
GND	208
VCC	207

Unprogrammed IOBs have a default pull-up. This prevents an undefined pad level for unbonded or unused IOBs. Programmed outputs are default slew-rate limited.
In the PQ208 package, pins 15, 16, 64, 65, 90, 91, 142, 143, 170 and 195 are not connected.
* In PQ208, XC3090A and XC3195A have different pinouts.

Product Availability

Pins		44	64	68	84		100			132		144	160	175		176	208
Type		Plast. PLCC	Plast. VQFP	Plast. PLCC	Plast. PLCC	Cer. PGA	Plast. PQFP	Plast. TQFP	Plast. VQFP	Plast. PGA	Cer. PGA	Plast. TQFP	Plast. PQFP	Plast. PGA	Cer. PGA	Plast. TQFP	Plast. PQFP
Code		PC44	VQ64	PC68	PC84	PG84	PQ100	TQ100	VQ100	PP132	PG132	TQ144	PQ160	PP175	PG175	TQ176	PQ208
XC3020A	-7			CI	CI		CI										
	-6			C	C		C										
XC3030A	-7	CI	CI	CI	CI		CI		CI								
	-6	C	C	C	C		C		C								
XC3042A	-7				CI	CI	CI		CI		CI	CI					
	-6				C	C	C		C		C	C					
XC3064A	-7				CI					CI	CI	CI	CI				
	-6				C					C	C	C	C				
XC3090A	-7				CI							CI	CI	CI	CI	CI	CI
	-6				C							C	C	C	C	C	C
XC3020L	-8				CI												
XC3030L	-8		CI		CI				CI								
XC3042L	-8				CI				CI			CI					
XC3064L	-8				CI							CI					
XC3090L	-8				CI							CI				CI	
XC3120A	-4			CI	CI		CI										
	-3			CI	CI		CI										
	-2			CI	CI		CI										
	-1			C	C		C										
	-09			C	C		C										
XC3130A	-4	CI	CI	CI	CI		CI		CI								
	-3	CI	CI	CI	CI		CI		CI								
	-2	CI	CI	CI	CI		CI		CI								
	-1	C	C	C	C		C		C								
	-09	C	C	C	C		C		C								
XC3142A	-4				CI		CI		C			CI					
	-3				CI		CI		CI			CI					
	-2				CI		CI		CI			CI					
	-1				C		C		C			C					
	-09				C		C		C			C					
XC3164A	-4				CI							CI	CI				
	-3				CI							CI	CI				
	-2				CI							CI	CI				
	-1				C							C	C				
	-09				C							C	C				
XC3190A	-4				CI							CI	CI	CI	CI	CI	CI
	-3				CI							CI	CI	CI	CI	CI	CI
	-2				CI							CI	CI	CI	CI	CI	CI
	-1				C							C	C	C	C	C	C
	-09				C							C	C	C	C	C	C
XC3195A	-4				CI								CI	CI	CI		CI
	-3				CI								CI	CI	CI		CI
	-2				CI								CI	CI	CI		CI
	-1				C								C	C	C		C
	-09				C								C	C	C		C

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