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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	320
Number of Logic Elements/Cells	-
Total RAM Bits	64160
Number of I/O	70
Number of Gates	6000
Voltage - Supply	4.75V ~ 5.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	84-LCC (J-Lead)
Supplier Device Package	84-PLCC (29.31x29.31)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc3090a-7pc84c

Longlines

The Longlines bypass the switch matrices and are intended primarily for signals that must travel a long distance, or must have minimum skew among multiple destinations. Longlines, shown in Figure 14, run vertically and horizontally the height or width of the interconnect area. Each interconnection column has three vertical Longlines, and each interconnection row has two horizontal Longlines. Two additional Longlines are located adjacent to the outer sets of switching matrices. In devices larger than the XC3020A and XC3120A FPGAs, two vertical Longlines in each column are connectable half-length lines. On the XC3020A and XC3120A FPGAs, only the outer Longlines are connectable half-length lines.

Longlines can be driven by a logic block or IOB output on a column-by-column basis. This capability provides a common low skew control or clock line within each column of logic blocks. Interconnections of these Longlines are shown in Figure 15. Isolation buffers are provided at each input to a Longline and are enabled automatically by the development system when a connection is made.

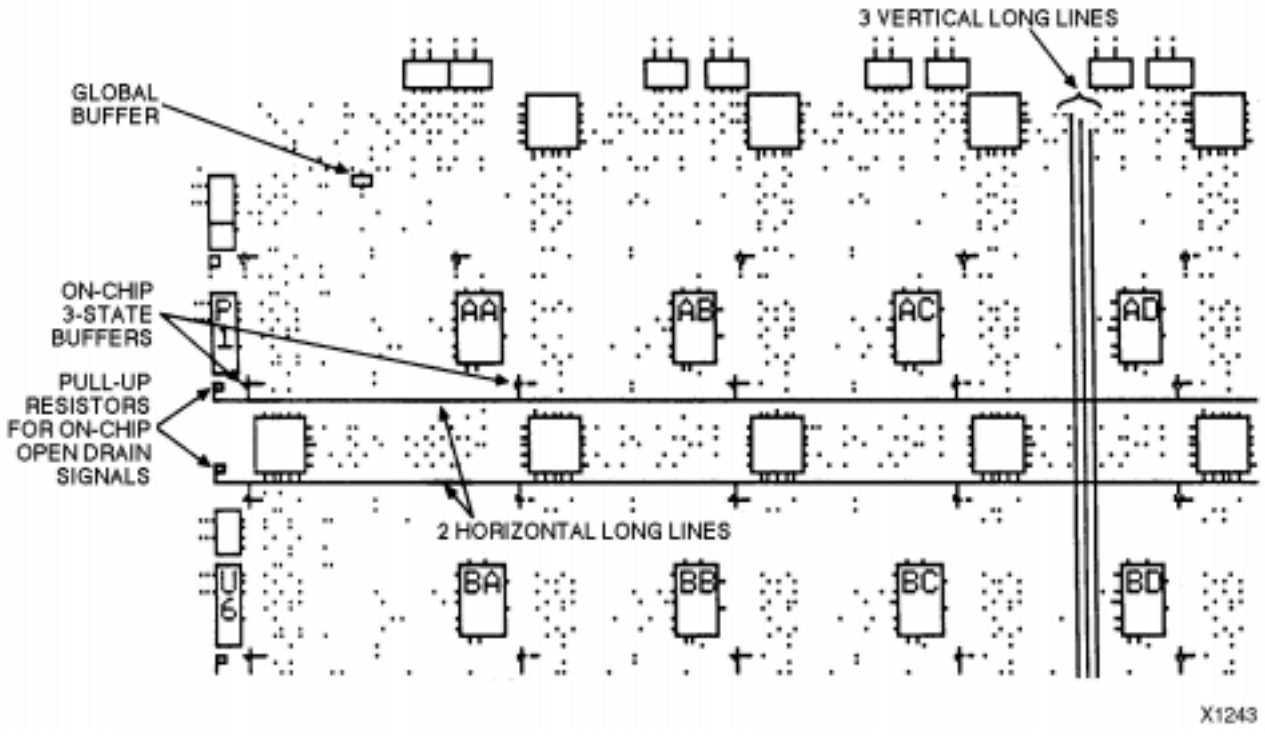


Figure 14: Horizontal and Vertical Longlines. These Longlines provide high fan-out, low-skew signal distribution in each row and column. The global buffer in the upper left die corner drives a common line throughout the FPGA.

A buffer in the upper left corner of the FPGA chip drives a global net which is available to all K inputs of logic blocks. Using the global buffer for a clock signal provides a skew-free, high fan-out, synchronized clock for use at any or all of the IOBs and CLBs. Configuration bits for the K input to each logic block can select this global line or another routing resource as the clock source for its flip-flops. This net may also be programmed to drive the die edge clock lines for IOB use. An enhanced speed, CMOS threshold, direct access to this buffer is available at the second pad from the top of the left die edge.

A buffer in the lower right corner of the array drives a horizontal Longline that can drive programmed connections to a vertical Longline in each interconnection column. This alternate buffer also has low skew and high fan-out. The network formed by this alternate buffer's Longlines can be selected to drive the K inputs of the CLBs. CMOS threshold, high speed access to this buffer is available from the third pad from the bottom of the right die edge.

Internal Busses

A pair of 3-state buffers, located adjacent to each CLB, permits logic to drive the horizontal Longlines. Logic operation of the 3-state buffer controls allows them to implement wide multiplexing functions. Any 3-state buffer input can be selected as drive for the horizontal long-line bus by applying a Low logic level on its 3-state control line. See Figure 16. The user is required to avoid contention which can result from multiple drivers with opposing logic levels. Control of the 3-state input by the same signal that drives the buffer input, creates an open-drain wired-AND function. A logic High on both buffer inputs creates a high impedance, which represents no contention. A logic Low enables the buffer to drive the Longline Low. See Figure 17. Pull-up resistors are available at each end of the Longline to provide a High output when all connected buffers are non-conducting. This forms fast, wide gating functions. When data drives the inputs, and separate signals drive the 3-state control lines, these buffers form multiplexers (3-state busses). In this case, care must be used to prevent contention through multiple active buffers of conflicting levels on a common line. Each horizontal Longline is also driven by a weak keeper circuit that prevents undefined floating levels by maintaining the previous logic level when the line is not driven by an active buffer or a pull-up resistor. Figure 18 shows 3-state buffers, Longlines and pull-up resistors.

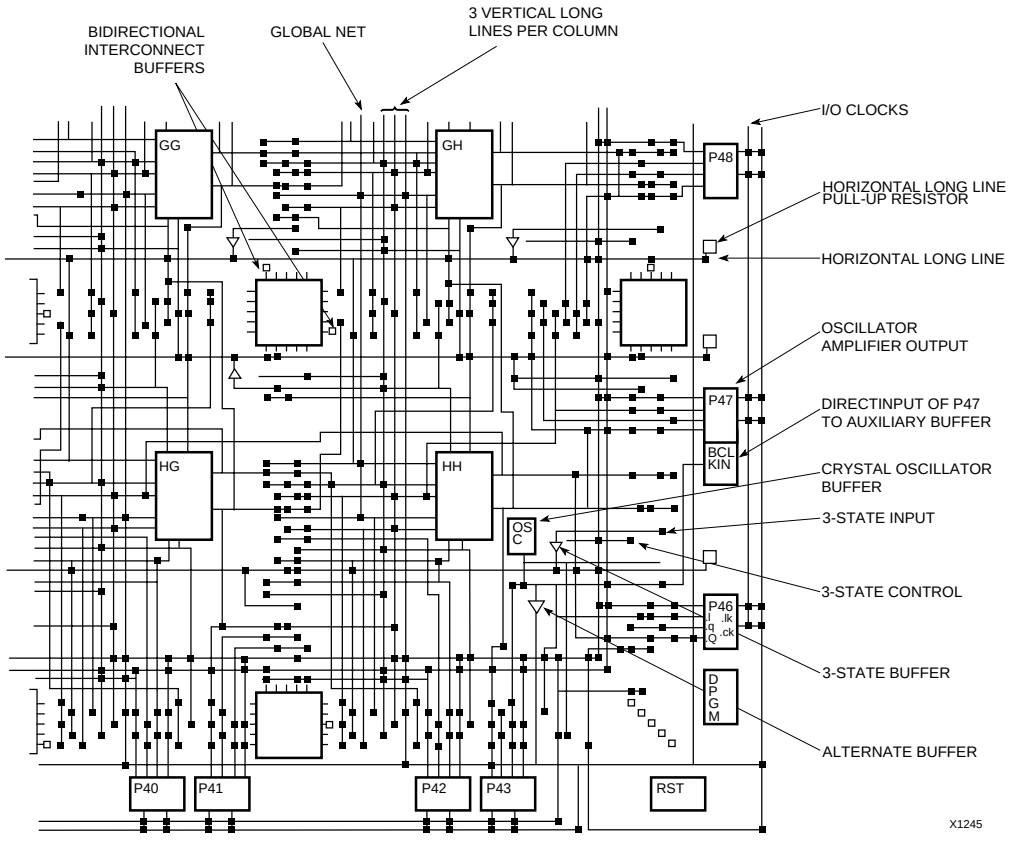
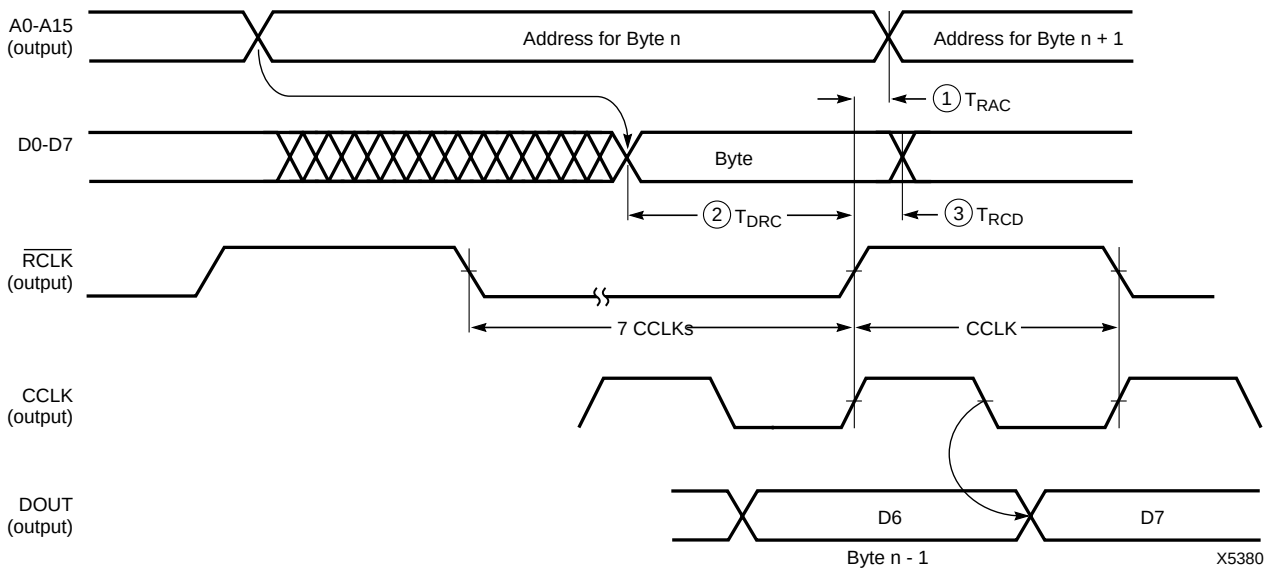


Figure 18: Design Editor.
An extra large view of possible interconnections in the lower right corner of the XC3020A.



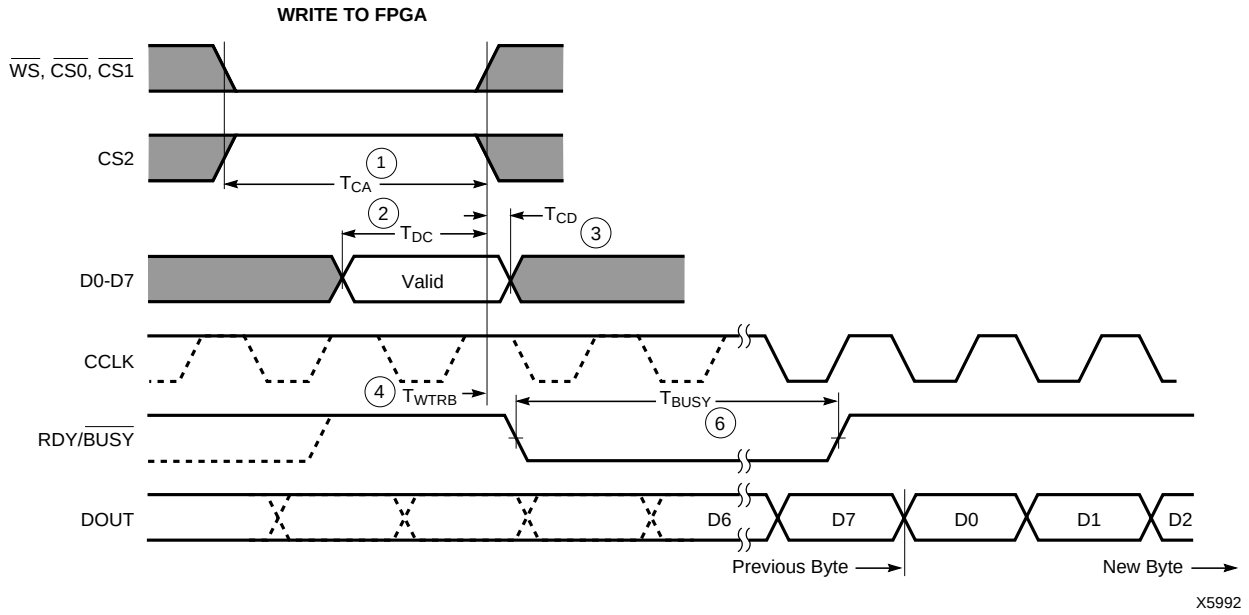
	Description	Symbol		Min	Max	Units
RCLK	To address valid	1	T_{RAC}	0	200	ns
	To data setup	2	T_{DRC}	60		ns
	To data hold	3	T_{RCD}	0		ns
	RCLK High		T_{RCH}	600		ns
	RCLK Low		T_{RCL}	4.0		µs

Notes: 1. At power-up, V_{CC} must rise from 2.0 V to V_{CC} min in less than 25 ms. If this is not possible, configuration can be delayed by holding $\overline{\text{RESET}}$ Low until VCC has reached 4.0 V (2.5 V for the XC3000L). A very long V_{CC} rise time of >100 ms, or a non-monotonically rising V_{CC} may require a >6-µs High level on $\overline{\text{RESET}}$, followed by a >6-µs Low level on $\overline{\text{RESET}}$ and D/P after V_{CC} has reached 4.0 V (2.5 V for the XC3000L).

2. Configuration can be controlled by holding $\overline{\text{RESET}}$ Low with or until after the $\overline{\text{INIT}}$ of all daisy-chain slave-mode devices is High.

This timing diagram shows that the EPROM requirements are extremely relaxed:
EPROM access time can be longer than 4000 ns. EPROM data output has no hold time requirements.

Figure 26: Master Parallel Mode Programming Switching Characteristics



	Description	Symbol		Min	Max	Units
WRITE	Effective Write time required (Assertion of CS0, CS1, CS2, WS)	1	T_{CA}	100		ns
	DIN Setup time required	2	T_{DC}	60		ns
	DIN Hold time required	3	T_{CD}	0		ns
	RDY/BUSY delay after end of WS	4	T_{WTRB}		60	ns
RDY	Earliest next WS after end of BUSY	5	T_{RBWT}	0		ns
	BUSY Low time generated	6	T_{BUSY}	2.5	9	CCLK periods

Notes:
1. At power-up, V_{CC} must rise from 2.0 V to V_{CC} min in less than 25 ms. If this is not possible, configuration can be delayed by holding RESET Low until V_{CC} has reached 4.0 V (2.5 V for the XC3000L). A very long V_{CC} rise time of >100 ms, or a non-monotonically rising V_{CC} may require a >6-µs High level on RESET, followed by a >6-µs Low level on RESET and D/P after V_{CC} has reached 4.0 V (2.5 V for the XC3000L).
2. Configuration must be delayed until the INIT of all FPGAs is High.
3. Time from end of WS to CCLK cycle for the new byte of data depends on completion of previous byte processing and the phase of the internal timing generator for CCLK.
4. CCLK and DOUT timing is tested in slave mode.
5. T_{BUSY} indicates that the double-buffered parallel-to-serial converter is not yet ready to receive new data. The shortest T_{BUSY} occurs when a byte is loaded into an empty parallel-to-serial converter. The longest TBUSY occurs when a new word is loaded into the input register before the second-level buffer has started shifting out data.

Note: *This timing diagram shows very relaxed requirements: Data need not be held beyond the rising edge of WS. BUSY will go active within 60 ns after the end of WS. BUSY will stay active for several microseconds. WS may be asserted immediately after the end of BUSY.*

Figure 28: Peripheral Mode Programming Switching Characteristics

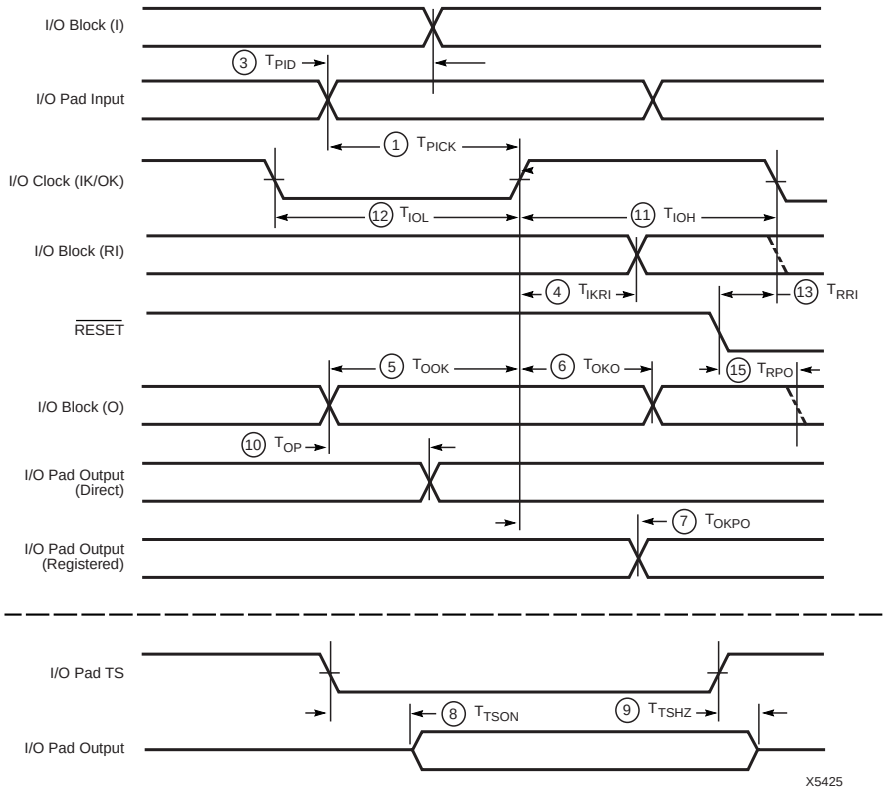
XC3000A IOB Switching Characteristics Guidelines

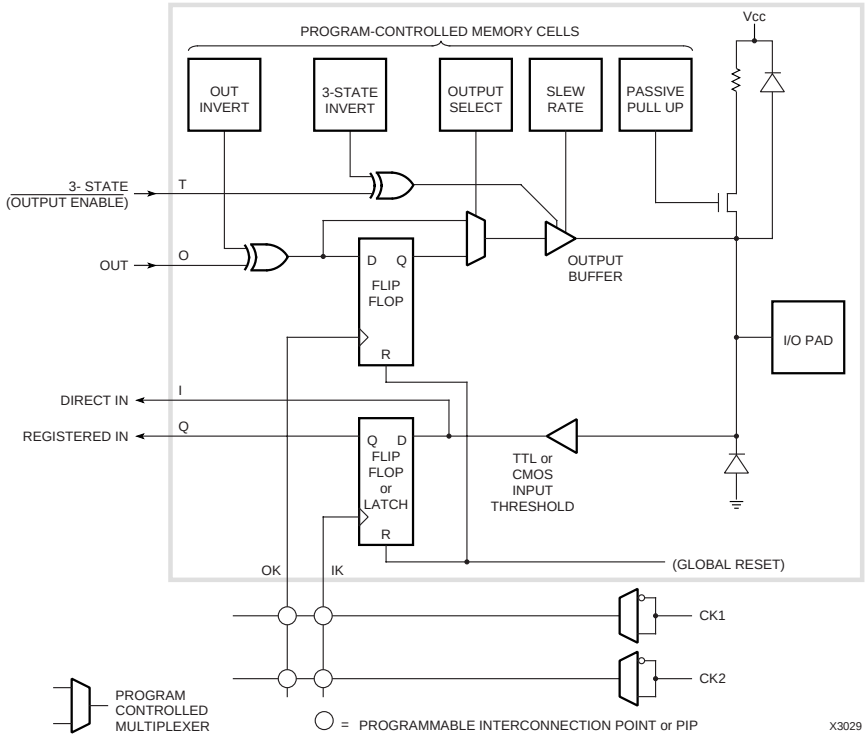
Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Since many internal timing parameters cannot be measured directly, they are derived from benchmark timing patterns. The following guidelines reflect worst-case values over the recommended operating conditions. For more detailed, more precise, and more up-to-date timing information, use the values provided by the timing calculator and used in the simulator.

		Speed Grade		-7		-6		
Description		**Symbol**		**Min**	**Max**	**Min**	**Max**	**Units**
Propagation Delays (Input)								
Pad to Direct In (I)		3	T_{PID}		4.0		3.0	ns
Pad to Registered In (Q) with latch transparent			T_{PTG}		15.0		14.0	ns
Clock (IK) to Registered In (Q)		4	T_{IKRI}		3.0		2.5	ns
Set-up Time (Input)								
Pad to Clock (IK) set-up time		1	T_{PICK}	14.0		12.0		ns
Propagation Delays (Output)								
Clock (OK) to Pad	(fast)	7	T_{OKPO}		8.0		7.0	ns
same	(slew rate limited)	7	T_{OKPO}		18.0		15.0	ns
Output (O) to Pad	(fast)	10	T_{OPF}		6.0		5.0	ns
same	(slew-rate limited)	10	T_{OPS}		16.0		13.0	ns
3-state to Pad begin hi-Z	(fast)	9	T_{TSHZ}		10.0		9.0	ns
same	(slew-rate limited)	9	T_{TSHZ}		20.0		12.0	ns
3-state to Pad active and valid	(fast)	8	T_{TSON}		11.0		10.0	ns
same	(slew -rate limited)	8	T_{TSON}		21.0		18.0	ns
Set-up and Hold Times (Output)								
Output (O) to clock (OK) set-up time		5	T_{OOK}	8.0		7.0		ns
Output (O) to clock (OK) hold time		6	T_{OKO}	0		0		ns
Clock								
Clock High time		11	T_{IOH}	4.0		3.5		ns
Clock Low time		12	T_{IOL}	4.0		3.5		ns
Max. flip-flop toggle rate			F_{CLK}	113.0		135.0		MHz
Global Reset Delays (based on XC3042A)								
$\overline{\text{RESET}}$ Pad to Registered In	(Q)	13	T_{RRI}		24.0		23.0	ns
$\overline{\text{RESET}}$ Pad to output pad	(fast)	15	T_{RPO}		33.0		29.0	ns
	(slew-rate limited)	15	T_{RPO}		43.0		37.0	ns

Notes:
1. Timing is measured at pin threshold, with 50 pF external capacitive loads (incl. test fixture). Typical slew rate limited output rise/fall times are approximately four times longer.
2. Voltage levels of unused (bonded and unbonded) pads must be valid logic levels. Each can be configured with the internal pull-up resistor or alternatively configured as a driven output or driven from an external source.
3. Input pad set-up time is specified with respect to the internal clock (ik). In order to calculate system set-up time, subtract clock delay (pad to ik) from the input pad set-up time value. Input pad holdtime with respect to the internal clock (ik) is negative. This means that pad level changes immediately before the internal clock edge (ik) will not be recognized.
4. T_{PID}, T_{PTG}, and T_{PICK} are 3 ns higher for XTL2 when the pin is configured as a user input.

XC3000A IOB Switching Characteristics Guidelines (continued)





XC3000L Switching Characteristics

Xilinx maintains test specifications for each product as controlled documents. To insure the use of the most recently released device performance parameters, please request a copy of the current test-specification revision.

XC3000L Operating Conditions

Symbol	Description	Min	Max	Units
V_{CC}	Supply voltage relative to GND Commercial 0°C to +85°C junction	3.0	3.6	V
V_{IH}	High-level input voltage — TTL configuration	2.0	V_{CC}+0.3	V
V_{IL}	Low-level input voltage — TTL configuration	-0.3	0.8	V
T_{IN}	Input signal transition time		250	ns

Notes: 1. At junction temperatures above those listed as Operating Conditions, all delay parameters increase by 0.3% per °C.
2. Although the present (1996) devices operate over the full supply voltage range from 3.0 to 5.25 V, Xilinx reserves the right to restrict operation to the 3.0 to 3.6 V range later, when smaller device geometries might preclude operation at 5V. Operating conditions are guaranteed in the 3.0 – 3.6 V V_{CC} range.

XC3000L DC Characteristics Over Operating Conditions

Symbol	Description	Min	Max	Units
V_{OH}	High-level output voltage (@ I_{OH} = –4.0 mA, V_{CC} min)	2.40		V
V_{OL}	Low-level output voltage (@ I_{OL} = 4.0 mA, V_{CC} min)		0.40	V
V_{OH}	High-level output voltage (@ I_{OH} = –4.0 mA, V_{CC} min)	V_{CC} -0.2		V
V_{OL}	Low-level output voltage (@ I_{OL} = 4.0 mA, V_{CC} min)		0.2	V
V_{CCPD}	Power-down supply voltage (PWRDWN must be Low)	2.30		V
I_{CCPD}	Power-down supply current ($V_{CC(MAX)}$ @ T_{MAX})		10	µA
I_{CCO}	Quiescent FPGA supply current in addition to I_{CCPD}[1] Chip thresholds programmed as CMOS levels		 20	 µA
I_{IL}	Input Leakage Current	–10	+10	µA
C_{IN}	Input capacitance, all packages except PGA175 (sample tested) All Pins except XTL1 and XTL2 XTL1 and XTL2		 10 15	 pF pF
	Input capacitance, PGA 175 (sample tested) All Pins except XTL1 and XTL2 XTL1 and XTL2		 15 20	 pF pF
I_{RIN}	Pad pull-up (when selected) @ V_{IN} = 0 V[3]	0.01	0.17	mA
I_{RLL}	Horizontal Longline pull-up (when selected) @ logic Low		2.50	mA

Notes: 1. With no output current loads, no active input or Longline pull-up resistors, all package pins at V_{CC} or GND, and the FPGA device configured with a tie option. I_{CCO} is in addition to I_{CCPD}.
2. Total continuous output sink current may not exceed 100 mA per ground pin. Total continuous output source may not exceed 100 mA per V_{CC} pin. The number of ground pins varies from the XC3020L to the XC3090L.
3. Not tested. Allows an undriven pin to float High. For any other purpose, use an external pull-up.

XC3000L Absolute Maximum Ratings

Symbol	Description		Units
V_{CC}	Supply voltage relative to GND	–0.5 to +7.0	V
V_{IN}	Input voltage with respect to GND	–0.5 to V_{CC} +0.5	V
V_{TS}	Voltage applied to 3-state output	–0.5 to V_{CC} +0.5	V
T_{STG}	Storage temperature (ambient)	–65 to +150	°C
T_{SOL}	Maximum soldering temperature (10 s @ 1/16 in.)	+260	°C
T_J	Junction temperature plastic	+125	°C
	Junction temperature ceramic	+150	°C

Note: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

XC3000L Global Buffer Switching Characteristics Guidelines

	Speed Grade	-8	
Description	**Symbol**	**Max**	**Units**
Global and Alternate Clock Distribution[1]			
Either: **Normal** IOB input pad through clock buffer to any CLB or IOB clock input	T_{PID}	9.0	ns
Or: **Fast** (CMOS only) input pad through clock buffer to any CLB or IOB clock input	T_{PIDC}	7.0	ns
TBUF driving a Horizontal Longline (L.L.)[1]			
I to L.L. while T is Low (buffer active)	T_{IO}	5.0	ns
T↓ to L.L. active and valid with single pull-up resistor	T_{ON}	12.0	ns
T↑ to L.L. High with single pull-up resistor	T_{PUS}	24.0	ns
BIDI			
Bidirectional buffer delay	T_{BIDI}	2.0	ns

Notes: 1. Timing is based on the XC3042A, for other devices see timing calculator.
2. The use of two pull-up resistors per Longline, available on other XC3000 devices, is not a valid option for XC3000L devices.

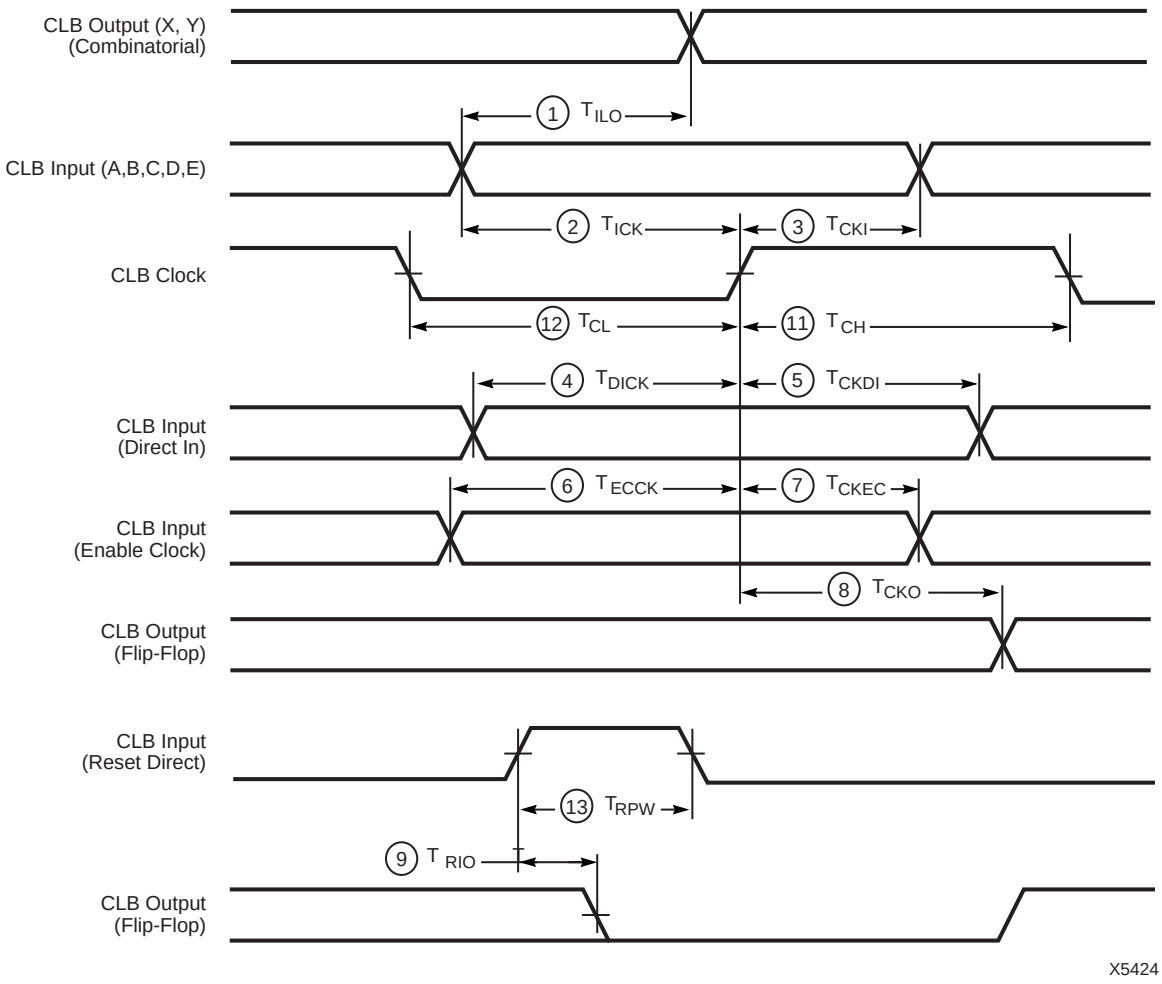
XC3000L CLB Switching Characteristics Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Since many internal timing parameters cannot be measured directly, they are derived from benchmark timing patterns. The following guidelines reflect worst-case values over the recommended operating conditions. For more detailed, more precise, and more up-to-date timing information, use the values provided by the timing calculator and used in the simulator.

		Speed Grade		-8		
Description		**Symbol**		**Min**	**Max**	**Units**
Combinatorial Delay						
Logic Variables	A, B, C, D, E, to outputs X or Y					
	FG Mode	1	T_{ILO}		6.7	ns
	F and FGM Mode				7.5	ns
Sequential delay						
Clock k to outputs X or Y		8	T_{CKO}		7.5	ns
Clock k to outputs X or Y when Q is returned through function generators F or G to drive X or Y			T_{QLO}			
	FG Mode				14.0	ns
	F and FGM Mode				14.8	ns
Set-up time before clock K						
Logic Variables	A, B, C, D, E					
	FG Mode	2	T_{ICK}	5.0		ns
	F and FGM Mode			5.8		ns
Data In	DI	4	T_{DICK}	5.0		ns
Enable Clock	EC	6	T_{ECCK}	6.0		ns
Hold Time after clock K						
Logic Variables	A, B, C, D, E	3	T_{CKI}	0		ns
Data In	DI[2]	5	T_{CKDI}	2.0		ns
Enable Clock	EC	7	T_{CKEC}	2.0		ns
Clock						
Clock High time		11	T_{CH}	5.0		ns
Clock Low time		12	T_{CL}	5.0		ns
Max. flip-flop toggle rate			F_{CLK}	80.0		MHz
Reset Direct (RD)						
RD width		13	T_{RPW}	7.0		ns
delay from RD to outputs X or Y		9	T_{RIO}	7.0		ns
Global Reset ($\overline{\text{RESET}}$ Pad)[1]						
$\overline{\text{RESET}}$ width (Low)			T_{MRW}	16.0		ns
delay from $\overline{\text{RESET}}$ pad to outputs X or Y			T_{MRQ}		23.0	ns

Notes: 1. Timing is based on the XC3042L, for other devices see timing calculator.
2. The CLB K to Q output delay (T_{CKO}, #8) of any CLB, plus the shortest possible interconnect delay, is always longer than the Data In hold time requirement (T_{CKDI}, #5) of any CLB on the same die.

XC3000L CLB Switching Characteristics Guidelines (continued)



XC3000L IOB Switching Characteristics Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Since many internal timing parameters cannot be measured directly, they are derived from benchmark timing patterns. The following guidelines reflect worst-case values over the recommended operating conditions. For more detailed, more precise, and more up-to-date timing information, use the values provided by the timing calculator and used in the simulator.

		Speed Grade	-8		
Description		**Symbol**		**Min**	**Max**	**Units**
Propagation Delays (Input)						
Pad to Direct In (I)		3	T_{PID}		5.0	ns
Pad to Registered In (Q) with latch transparent			T_{PTG}		24.0	ns
Clock (IK) to Registered In (Q)		4	T_{IKRI}		6.0	ns
Set-up Time (Input)						
Pad to Clock (IK) set-up time		1	T_{PICK}	22.0		ns
Propagation Delays (Output)						
Clock (OK) to Pad	(fast)	7	T_{OKPO}		12.0	ns
same	(slew rate limited)	7	T_{OKPO}		28.0	ns
Output (O) to Pad	(fast)	10	T_{OPF}		9.0	ns
same	(slew-rate limited)	10	T_{OPS}		25.0	ns
3-state to Pad begin hi-Z	(fast)	9	T_{TSHZ}		12.0	ns
same	(slew-rate limited)	9	T_{TSHZ}		28.0	ns
3-state to Pad active and valid	(fast)	8	T_{TSON}		16.0	ns
same	(slew -rate limited)	8	T_{TSON}		32.0	ns
Set-up and Hold Times (Output)						
Output (O) to clock (OK) set-up time		5	T_{OOK}	12.0		ns
Output (O) to clock (OK) hold time		6	T_{OKO}	0		ns
Clock						
Clock High time		11	T_{IOH}	5.0		ns
Clock Low time		12	T_{IOL}	5.0		ns
Max. flip-flop toggle rate			F_{CLK}	80.0		MHz
Global Reset Delays (based on XC3042L)						
$\overline{\text{RESET}}$ Pad to Registered In	(Q)	13	T_{RRI}		25.0	ns
$\overline{\text{RESET}}$ Pad to output pad	(fast)	15	T_{RPO}		35.0	ns
	(slew-rate limited)	15	T_{RPO}		51.0	ns

Notes: 1. Timing is measured at pin threshold, with 50 pF external capacitive loads (incl. test fixture). Typical slew rate limited output rise/fall times are approximately four times longer.
2. Voltage levels of unused (bonded and unbonded) pads must be valid logic levels. Each can be configured with the internal pull-up resistor or alternatively configured as a driven output or driven from an external source.
3. Input pad set-up time is specified with respect to the internal clock (ik). In order to calculate system set-up time, subtract clock delay (pad to ik) from the input pad set-up time value. Input pad holdtime with respect to the internal clock (ik) is negative. This means that pad level changes immediately before the internal clock edge (ik) will not be recognized.
4. T_{PID}, T_{PTG}, and T_{PICK} are 3 ns higher for XTL2 when the pin is configured as a user input.

XC3100L Switching Characteristics

Xilinx maintains test specifications for each product as controlled documents. To insure the use of the most recently released device performance parameters, please request a copy of the current test-specification revision.

XC3100L Operating Conditions

Symbol	Description	Min	Max	Units
V_{CC}	Supply voltage relative to GND Commercial 0°C to +85°C junction	3.0	3.6	V
V_{IH}	High-level input voltage	2.0	V_{CC} + 0.3	V
V_{IL}	Low-level input voltage	-0.3	0.8	V
T_{IN}	Input signal transition time		250	ns

Notes: 1. At junction temperatures above those listed as Operating Conditions, all delay parameters increase by 0.3% per °C.
2. Although the present (1996) devices operate over the full supply voltage range from 3.0 V to 5.25 V, Xilinx reserves the right to restrict operation to the 3.0 and 3.6 V range later, when smaller device geometries might preclude operation @ 5 V. Operating conditions are guaranteed in the 3.0 – 3.6 V V_{CC} range.

XC3100L DC Characteristics Over Operating Conditions

Symbol	Description	Min	Max	Units
V_{OH}	High-level output voltage (@ I_{OH} = -4.0 mA, V_{CC} min)	2.4		V
	High-level output voltage (@ I_{OH} = -100.0 µA, V_{CC} min)	V_{CC} -0.2		V
V_{OL}	Low-level output voltage (@ I_{OH} = 4.0 mA, V_{CC} min)		0.40	V
	Low-level output voltage (@ I_{OH} = +100.0 µA, V_{CC} min)		0.2	V
V_{CCPD}	Power-down supply voltage (PWRDWN must be Low)	2.30		V
I_{CCO}	Quiescent FPGA supply current Chip thresholds programmed as CMOS levels[1]		1.5	mA
I_{IL}	Input Leakage Current	-10	+10	µA
C_{IN}	Input capacitance (sample tested) All pins except XTL1 and XTL2 XTL1 and XTL2		 10 15	 pF pF
I_{RIN}	Pad pull-up (when selected) @ V_{IN} = 0 V [3]	0.02	0.17	mA
I_{RLL}	Horizontal long line pull-up (when selected) @ logic Low	0.20	2.80	mA

Notes: 1. With no output current loads, no active input or long line pull-up resistors, all package pins at V_{CC} or GND, and the FPGA configured with a tie option.
2. Total continuous output sink current may not exceed 100 mA per ground pin. Total continuous output source current may not exceed 100 mA per V_{CC} pin. The number of ground pins varies from the XC3142L to the XC3190L.
3. Not tested. Allows undriven pins to float High. For any other purpose, use an external pull-up.

XC3100L CLB Switching Characteristics Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Since many internal timing parameters cannot be measured directly, they are derived from benchmark timing patterns. The following guidelines reflect worst-case values over the recommended operating conditions. For more detailed, more precise, and more up-to-date timing information, use the values provided by the timing calculator and used in the simulator.

	Speed Grade		-3		-2		
Description	**Symbol**		**Min**	**Max**	**Min**	**Max**	**Units**
Combinatorial Delay							
Logic Variables A, B, C, D, E, to outputs X or Y	1	T_{ILO}		2.7		2.2	ns
Sequential delay							
Clock k to outputs X or Y	8	T_{CKO}		2.1		1.7	ns
Clock k to outputs X or Y when Q is returned through function generators F or G to drive X or Y		T_{QLO}		4.3		3.5	ns
Set-up time before clock K							
Logic Variables A, B, C, D, E	2	T_{ICK}	2.1		1.8		ns
Data In DI	4	T_{DICK}	1.4		1.3		ns
Enable Clock EC	6	T_{ECCK}	2.7		2.5		ns
Reset Direct Inactive RD			1.0		1.0		ns
Hold Time after clock K							
Logic Variables A, B, C, D, E	3	T_{CKI}	0		0		ns
Data In DI	5	T_{CKDI}	0.9		0.9		ns
Enable Clock EC	7	T_{CKEC}	0.7		0.7		ns
Clock							
Clock High time	11	T_{CH}	1.6		1.3		ns
Clock Low time	12	T_{CL}	1.6		1.3		ns
Max. flip-flop toggle rate		F_{CLK}	270		325		MHz
Reset Direct (RD)							
RD width	13	T_{RPW}	2.7		2.3		ns
delay from RD to outputs X or Y	9	T_{RIO}		3.1		2.7	ns
Global Reset ($\overline{\text{RESET}}$ Pad)							
$\overline{\text{RESET}}$ width (Low)							ns
(XC3142L)		T_{MRW}	12.0		12.0		ns
delay from $\overline{\text{RESET}}$ pad to outputs X or Y		T_{MRQ}		12.0		12.0	
			Advance				

Notes: 1. The CLB K to Q delay (T_{CKO}, #8) of any CLB, plus the shortest possible interconnect delay, is always longer than the Data In hold time requirement (T_{CKDI}, #5) of any CLB on the same die.
2. T_{ILO}, T_{QLO} and T_{ICK} are specified for 4-input functions. For 5-input functions or base FGM functions, each of these specifications for the XC3100L family increase by 0.35 ns (-3) and 0.29 ns (-2).

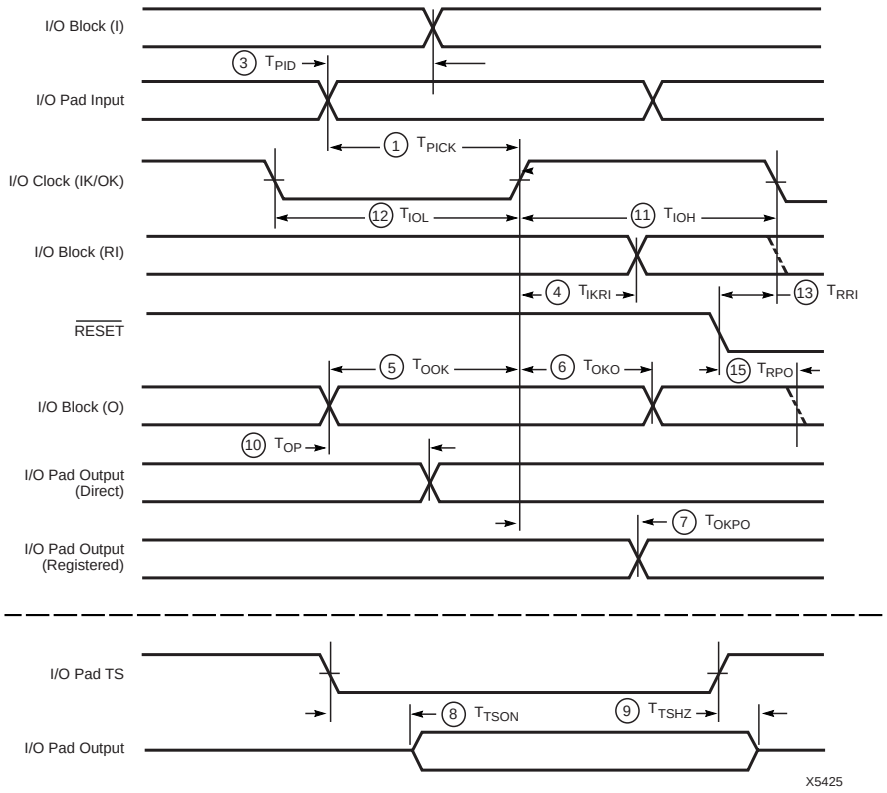
XC3100L IOB Switching Characteristics Guidelines

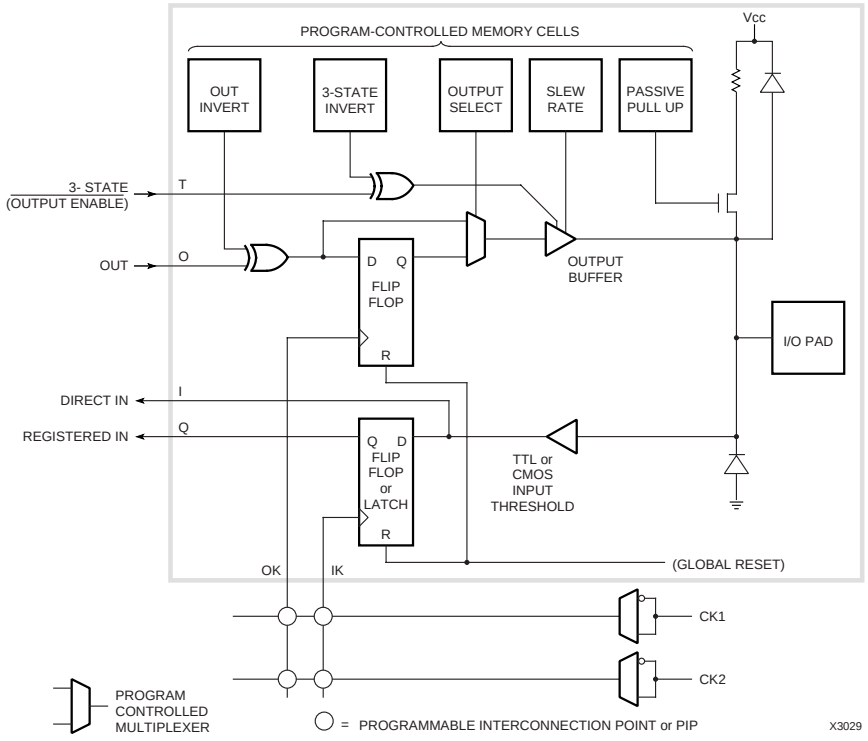
Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Since many internal timing parameters cannot be measured directly, they are derived from benchmark timing patterns. The following guidelines reflect worst-case values over the recommended operating conditions. For more detailed, more precise, and more up-to-date timing information, use the values provided by the timing calculator and used in the simulator.

	Speed Grade		-3		-2		
Description	**Symbol**		**Min**	**Max**	**Min**	**Max**	**Units**
Propagation Delays (Input)							
Pad to Direct In (I)	3	T_{PID}		2.2		2.0	ns
Pad to Registered In (Q) with latch (XC3100L) transparent		T_{PTG}		11.0		11.0	ns
Clock (IK) to Registered In (Q)	4	T_{IKRI}		2.2		1.9	ns
Set-up Time (Input)							
Pad to Clock (IK) set-up time	1	T_{PICK}					
XC3142L			9.5		9.0		ns
XC3190L			9.9		9.4		ns
Propagation Delays (Output)							
Clock (OK) to Pad (fast)	7	T_{OKPO}		4.4		4.0	ns
same (slew rate limited)	7	T_{OK} PO		10.0		9.7	ns
Output (O) to Pad (fast)	10	T_{OPF}		3.3		3.0	ns
same (slew-rate limited)(XC3100L)	10	T_{OPF}		9.0		8.7	ns
3-state to Pad begin hi-Z (fast)	9	T_{TSHZ}		5.5		5.0	ns
same (slew-rate limited)	9	T_{TSHZ}		5.5		5.0	ns
3-state to Pad active and valid (fast)(XC3100L)	8	T_{TSON}		9.0		8.5	ns
same (slew -rate limited)	8	T_{TSON}		15.0		14.2	ns
Set-up and Hold Times (Output)							
Output (O) to clock (OK) set-up time (XC3100L)	5	T_{OOK}	4.0		3.6		ns
Output (O) to clock (OK) hold time	6	T_{OKO}	0		0		ns
Clock							
Clock High time	11	T_{IOH}	1.6		1.3		ns
Clock Low time	12	T_{IOL}	1.6		1.3		ns
Export Control Maximum flip-flop toggle rate		F_{TOG}	270		325		MHz
Global Reset Delays							
$\overline{\text{RESET}}$ Pad to Registered In (Q)							
(XC3142L)	13	T_{RRI}		16.0		16.0	ns
(XC3190L)				21.0		21.0	ns
$\overline{\text{RESET}}$ Pad to output pad (fast)	15	T_{RPO}		17.0		17.0	ns
(slew-rate limited)	15	T_{RPO}		23.0		23.0	ns
			Advance				

Notes: 1. Timing is measured at pin threshold, with 50 pF external capacitive loads (incl. test fixture). Typical slew rate limited output rise/fall times are approximately four times longer.
2. Voltage levels of unused (bonded and unbonded) pads must be valid logic levels. Each can be configured with the internal pull-up resistor or alternatively configured as a driven output or driven from an external source.
3. Input pad set-up time is specified with respect to the internal clock (IK). In order to calculate system set-up time, subtract clock delay (pad to ik) from the input pad set-up time value. Input pad holdtime with respect to the internal clock (IK) is negative. This means that pad level changes immediately before the internal clock edge (IK) will not be recognized.

XC3100L IOB Switching Characteristics Guidelines (continued)





XC3064A/XC3090A/XC3195A 84-Pin PLCC Pinouts

XC3000A, XC3000L, XC3100A, and XC3100L families have identical pinouts

PLCC Pin Number	XC3064A, XC3090A, XC3195A
12	PWRDN
13	TCLKIN-I/O
14	I/O
15	I/O
16	I/O
17	I/O
18	I/O
19	I/O
20	I/O
21	GND*
22	VCC
23	I/O
24	I/O
25	I/O
26	I/O
27	I/O
28	I/O
29	I/O
30	I/O
31	M1-RDATA
32	M0-RTRIG
33	M2-I/O
34	HDC-I/O
35	I/O
36	LDC-I/O
37	I/O
38	I/O
39	I/O
40	I/O
41	INIT/I/O*
42	VCC*
43	GND
44	I/O
45	I/O
46	I/O
47	I/O
48	I/O
49	I/O
50	I/O
51	I/O
52	I/O
53	XTL2(IN)-I/O

PLCC Pin Number	XC3064A, XC3090A, XC3195A
54	RESET
55	DONE-PG
56	D7-I/O
57	XTL1(OUT)-BCLKIN-I/O
58	D6-I/O
59	I/O
60	D5-I/O
61	CS0-I/O
62	D4-I/O
63	I/O
64	VCC
65	GND*
66	D3-I/O*
67	CS1-I/O*
68	D2-I/O*
69	I/O
70	D1-I/O
71	RDY/BUSY-RCLK-I/O
72	D0-DIN-I/O
73	DOUT-I/O
74	CCLK
75	A0-WS-I/O
76	A1-CS2-I/O
77	A2-I/O
78	A3-I/O
79	I/O
80	I/O
81	A15-I/O
82	A4-I/O
83	A14-I/O
84	A5-I/O
1	GND
2	VCC*
3	A13-I/O*
4	A6-I/O*
5	A12-I/O*
6	A7-I/O*
7	I/O
8	A11-I/O
9	A8-I/O
10	A10-I/O
11	A9-I/O

Unprogrammed IOBs have a default pull-up. This prevents an undefined pad level for unbonded or unused IOBs. Programmed outputs are default slew-rate limited.

* In the PC84 package, XC3064A, XC3090A and XC3195A have additional VCC and GND pins and thus a different pin definition than XC3020A/XC3030A/XC3042A.

XC3000 Series 100-Pin QFP Pinouts

XC3000A, XC3000L, XC3100A, and XC3100L families have identical pinouts

Pin No.		XC3020A XC3030A XC3042A
PQFP	TQFP VQFP	
16	13	GND
17	14	A13-I/O
18	15	A6-I/O
19	16	A12-I/O
20	17	A7-I/O
21	18	I/O*
22	19	I/O*
23	20	A11-I/O
24	21	A8-I/O
25	22	A10-I/O
26	23	A9-I/O
27	24	VCC*
28	25	GND*
29	26	$\overline{\text{PWRDN}}$
30	27	TCLKIN-I/O
31	28	I/O**
32	29	I/O*
33	30	I/O*
34	31	I/O
35	32	I/O
36	33	I/O
37	34	I/O
38	35	I/O
39	36	I/O
40	37	I/O
41	38	VCC
42	39	I/O
43	40	I/O
44	41	I/O
45	42	I/O
46	43	I/O
47	44	I/O
48	45	I/O
49	46	I/O

Pin No.		XC3020A XC3030A XC3042A
PQFP	TQFP VQFP	
50	47	I/O*
51	48	I/O*
52	49	M1-$\overline{\text{RD}}$
53	50	GND*
54	51	MO-RT
55	52	VCC*
56	53	M2-I/O
57	54	HDC-I/O
58	55	I/O
59	56	$\overline{\text{LDC}}$-I/O
60	57	I/O*
61	58	I/O*
62	59	I/O
63	60	I/O
64	61	I/O
65	62	$\overline{\text{INIT}}$-I/O
66	63	GND
67	64	I/O
68	65	I/O
69	66	I/O
70	67	I/O
71	68	I/O
72	69	I/O
73	70	I/O
74	71	I/O*
75	72	I/O*
76	73	XTL2-I/O
77	74	GND*
78	75	$\overline{\text{RESET}}$
79	76	VCC*
80	77	DONE-$\overline{\text{PG}}$
81	78	D7-I/O
82	79	BCLKIN-XTL1-I/O
83	80	D6-I/O

Pin No.		XC3020A XC3030A XC3042A
PQFP	TQFP VQFP	
84	81	I/O*
85	82	I/O*
86	83	I/O
87	84	D5-I/O
88	85	$\overline{\text{CS0}}$-I/O
89	86	D4-I/O
90	87	I/O
91	88	VCC
92	89	D3-I/O
93	90	$\overline{\text{CS1}}$-I/O
94	91	D2-I/O
95	92	I/O
96	93	I/O*
97	94	I/O*
98	95	D1-I/O
99	96	RDY/$\overline{\text{BUSY}}$-RCLK-I/O
100	97	DO-DIN-I/O
1	98	DOUT-I/O
2	99	CCLK
3	100	VCC*
4	1	GND*
5	2	AO-$\overline{\text{WS}}$-I/O
6	3	A1-CS2-I/O
7	4	I/O**
8	5	A2-I/O
9	6	A3-I/O
10	7	I/O*
11	8	I/O*
12	9	A15-I/O
13	10	A4-I/O
14	11	A14-I/O
15	12	A5-I/O

Unprogrammed IOBs have a default pull-up. This prevents an undefined pad level for unbonded or unused IOBs. Programmed outputs are default slew-rate limited.

* This table describes the pinouts of three different chips in three different packages. The pin-description column lists 100 of the 118 pads on the XC3042A that are connected to the 100 package pins. Two pads, indicated by double asterisks, do not exist on the XC3030A, which has 98 pads; therefore the corresponding pins have no connections. Twenty-six pads, indicated by single or double asterisks, do not exist on the XC3020A, which has 74 pads; therefore, the corresponding pins have no connections. (See table on page 65.)

XC3000 Series 132-Pin Ceramic and Plastic PGA Pinouts

XC3000A, XC3000L, XC3100A, and XC3100L families have identical pinouts

PGA Pin Number	XC3042A XC3064A	PGA Pin Number	XC3042A XC3064A	PGA Pin Number	XC3042A XC3064A	PGA Pin Number	XC3042A XC3064A
C4	GND	B13	M1-RD	P14	RESET	M3	DOUT-I/O
A1	PWRDN	C11	GND	M11	VCC	P1	CCLK
C3	I/O-TCLKIN	A14	M0-RT	N13	DONE-PG	M4	VCC
B2	I/O	D12	VCC	M12	D7-I/O	L3	GND
B3	I/O	C13	M2-I/O	P13	XTL1-I/O-BCLKIN	M2	A0-WS-I/O
A2	I/O*	B14	HDC-I/O	N12	I/O	N1	A1-CS2-I/O
B4	I/O	C14	I/O	P12	I/O	M1	I/O
C5	I/O	E12	I/O	N11	D6-I/O	K3	I/O
A3	I/O*	D13	I/O	M10	I/O	L2	A2-I/O
A4	I/O	D14	LDC-I/O	P11	I/O*	L1	A3-I/O
B5	I/O	E13	I/O*	N10	I/O	K2	I/O
C6	I/O	F12	I/O	P10	I/O	J3	I/O
A5	I/O	E14	I/O	M9	D5-I/O	K1	A15-I/O
B6	I/O	F13	I/O	N9	CS0-I/O	J2	A4-I/O
A6	I/O	F14	I/O	P9	I/O*	J1	I/O*
B7	I/O	G13	I/O	P8	I/O*	H1	A14-I/O
C7	GND	G14	INIT-I/O	N8	D4-I/O	H2	A5-I/O
C8	VCC	G12	VCC	P7	I/O	H3	GND
A7	I/O	H12	GND	M8	VCC	G3	VCC
B8	I/O	H14	I/O	M7	GND	G2	A13-I/O
A8	I/O	H13	I/O	N7	D3-I/O	G1	A6-I/O
A9	I/O	J14	I/O	P6	CS1-I/O	F1	I/O*
B9	I/O	J13	I/O	N6	I/O*	F2	A12-I/O
C9	I/O	K14	I/O	P5	I/O*	E1	A7-I/O
A10	I/O	J12	I/O	M6	D2-I/O	F3	I/O
B10	I/O	K13	I/O	N5	I/O	E2	I/O
A11	I/O*	L14	I/O*	P4	I/O	D1	A11-I/O
C10	I/O	L13	I/O	P3	I/O	D2	A8-I/O
B11	I/O	K12	I/O	M5	D1-I/O	E3	I/O
A12	I/O*	M14	I/O	N4	RDY/BUSY-RCLK-I/O	C1	I/O
B12	I/O	N14	I/O	P2	I/O	B1	A10-I/O
A13	I/O*	M13	XTL2(IN)-I/O	N3	I/O	C2	A9-I/O
C12	I/O	L12	GND	N2	D0-DIN-I/O	D3	VCC

Unprogrammed IOBs have a default pull-up. This prevents an undefined pad level for unbonded or unused IOBs. Programmed outputs are default slew-rate limited.

* Indicates unconnected package pins (14) for the XC3042A.

XC3000 Series 208-Pin PQFP Pinouts

XC3000A, and XC3000L families have identical pinouts

Pin Number	XC3090A
1	–
2	GND
3	$\overline{\text{PWRDWN}}$
4	TCLKIN-I/O
5	I/O
6	I/O
7	I/O
8	I/O
9	I/O
10	I/O
11	I/O
12	I/O
13	I/O
14	I/O
15	–
16	I/O
17	I/O
18	I/O
19	I/O
20	I/O
21	I/O
22	I/O
23	I/O
24	I/O
25	GND
26	VCC
27	I/O
28	I/O
29	I/O
30	I/O
31	I/O
32	I/O
33	I/O
34	I/O
35	I/O
36	I/O
37	–
38	I/O
39	I/O
40	I/O
41	I/O
42	I/O
43	I/O
44	I/O
45	I/O
46	I/O
47	I/O
48	M1-$\overline{\text{RDATA}}$
49	GND
50	M0-RTRIG
51	–
52	–

Pin Number	XC3090A
53	–
54	–
55	VCC
56	M2-I/O
57	HDC-I/O
58	I/O
59	I/O
60	I/O
61	$\overline{\text{LDC}}$-I/O
62	I/O
63	I/O
64	–
65	–
66	–
67	–
68	I/O
69	I/O
70	I/O
71	I/O
72	–
73	–
74	I/O
75	I/O
76	I/O
77	$\overline{\text{INIT}}$-I/O
78	VCC
79	GND
80	I/O
81	I/O
82	I/O
83	–
84	–
85	I/O
86	I/O
87	I/O
88	I/O
89	I/O
90	–
91	–
92	–
93	I/O
94	I/O
95	I/O
96	I/O
97	I/O
98	I/O
99	I/O
100	XTL2-I/O
101	GND
102	$\overline{\text{RESET}}$
103	–
104	–

Pin Number	XC3090A
105	–
106	VCC
107	D/$\overline{\text{P}}$
108	–
109	D7-I/O
110	XTL1-BCLKIN-I/O
111	I/O
112	I/O
113	I/O
114	I/O
115	D6-I/O
116	I/O
117	I/O
118	I/O
119	–
120	I/O
121	I/O
122	D5-I/O
123	$\overline{\text{CS0}}$-I/O
124	I/O
125	I/O
126	I/O
127	I/O
128	D4-I/O
129	I/O
130	VCC
131	GND
132	D3-I/O
133	$\overline{\text{CS1}}$-I/O
134	I/O
135	I/O
136	I/O
137	I/O
138	D2-I/O
139	I/O
140	I/O
141	I/O
142	–
143	I/O
144	I/O
145	D1-I/O
146	RDY/$\overline{\text{BUSY}}$-$\overline{\text{RCLK}}$-I/O
147	I/O
148	I/O
149	I/O
150	I/O
151	DIN-D0-I/O
152	DOUT-I/O
153	CCLK
154	VCC
155	–
156	–

Pin Number	XC3090A
157	–
158	–
159	–
160	GND
161	$\overline{\text{WS}}$-A0-I/O
162	CS2-A1-I/O
163	I/O
164	I/O
165	A2-I/O
166	A3-I/O
167	I/O
168	I/O
169	–
170	–
171	–
172	A15-I/O
173	A4-I/O
174	I/O
175	I/O
176	–
177	–
178	A14-I/O
179	A5-I/O
180	I/O
181	I/O
182	GND
183	VCC
184	A13-I/O
185	A6-I/O
186	I/O
187	I/O
188	–
189	–
190	I/O
191	I/O
192	A12-I/O
193	A7-I/O
194	–
195	–
196	–
197	I/O
198	I/O
199	A11-I/O
200	A8-I/O
201	I/O
202	I/O
203	A10-I/O
204	A9-I/O
205	VCC
206	–
207	–
208	–

Unprogrammed IOBs have a default pull-up. This prevents an undefined pad level for unbonded or unused IOBs. Programmed outputs are default slew-rate limited.

* In PQ208, XC3090A and XC3195A have different pinouts.

XC3195A PQ208 Pinouts

Pin Description	PQ208
A9-I/O	206
A10-I/O	205
I/O	204
I/O	203
I/O	202
I/O	201
A8-I/O	200
A11-I/O	199
I/O	198
I/O	197
I/O	196
I/O	194
A7-I/O	193
A12-I/O	192
I/O	191
I/O	190
I/O	189
I/O	188
I/O	187
I/O	186
A6-I/O	185
A13-I/O	184
VCC	183
GND	182
I/O	181
I/O	180
A5-I/O	179
A14-I/O	178
I/O	177
I/O	176
I/O	175
I/O	174
A4-I/O	173
A15-I/O	172
I/O	171
I/O	169
I/O	168
I/O	167
A3-I/O	166
A2-I/O	165
I/O	164
I/O	163
I/O	162
I/O	161
A1-CS2-I/O	160
A0-$\overline{WS}$-I/O	159
GND	158
VCC	157
CCLK	156
DOUT-I/O	155

Pin Description	PQ208
D0-DIN-I/O	154
I/O	153
I/O	152
I/O	151
I/O	150
RDY/BUSY-RCLK-I/O	149
D1-I/O	148
I/O	147
I/O	146
I/O	145
I/O	144
I/O	141
I/O	140
I/O	139
D2-I/O	138
I/O	137
I/O	136
I/O	135
I/O	134
$\overline{CS1}$-I/O	133
D3-I/O	132
GND	131
VCC	130
I/O	129
D4-I/O	128
I/O	127
I/O	126
I/O	125
I/O	124
$\overline{CS0}$-I/O	123
D5-I/O	122
I/O	121
I/O	120
I/O	119
I/O	118
I/O	117
I/O	116
I/O	115
D6-I/O	114
I/O	113
I/O	112
I/O	111
I/O	110
XTLX1(OUT)BCLKN-I/O	109
D7-I/O	108
D/$\overline{P}$	107
VCC	106
$\overline{RESET}$	105
GND	104
XTL2(IN)-I/O	103

Pin Description	PQ208
I/O	102
I/O	101
I/O	100
I/O	99
I/O	98
I/O	97
I/O	96
I/O	95
I/O	94
I/O	93
I/O	92
I/O	89
I/O	88
I/O	87
I/O	86
I/O	85
I/O	84
I/O	83
I/O	82
I/O	81
I/O	80
GND	79
VCC	78
$\overline{INIT}$	77
I/O	76
I/O	75
I/O	74
I/O	73
I/O	72
I/O	71
I/O	70
I/O	69
I/O	68
I/O	67
I/O	66
I/O	63
I/O	62
I/O	61
I/O	60
$\overline{LDC}$-I/O	59
I/O	58
I/O	57
I/O	56
HDC-I/O	55
M2-I/O	54
VCC	53
M0-RTIG	52
GND	51
M1/$\overline{RDATA}$	50
I/O	49

Pin Description	PQ208
I/O	48
I/O	47
I/O	46
I/O	45
I/O	44
I/O	43
I/O	42
I/O	41
I/O	40
I/O	39
I/O	38
I/O	37
I/O	36
I/O	35
I/O	34
I/O	33
I/O	32
I/O	31
I/O	30
I/O	29
I/O	28
VCC	27
GND	26
I/O	25
I/O	24
I/O	23
I/O	22
I/O	21
I/O	20
I/O	19
I/O	18
I/O	17
I/O	14
I/O	13
I/O	12
I/O	11
I/O	10
I/O	9
I/O	8
I/O	7
I/O	6
I/O	5
I/O	4
I/O	3
TCLKIN-I/O	2
$\overline{PWRDN}$	1
GND	208
VCC	207

Unprogrammed IOBs have a default pull-up. This prevents an undefined pad level for unbonded or unused IOBs. Programmed outputs are default slew-rate limited.
In the PQ208 package, pins 15, 16, 64, 65, 90, 91, 142, 143, 170 and 195 are not connected.
* In PQ208, XC3090A and XC3195A have different pinouts.