E·XFL



Welcome to E-XFL.COM

Understanding <u>Embedded - FPGAs (Field</u> <u>Programmable Gate Array)</u>

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	320
Number of Logic Elements/Cells	-
Total RAM Bits	64160
Number of I/O	70
Number of Gates	6000
Voltage - Supply	4.75V ~ 5.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	84-LCC (J-Lead)
Supplier Device Package	84-PLCC (29.31x29.31)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc3090a-7pc84c

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong





Longlines

The Longlines bypass the switch matrices and are intended primarily for signals that must travel a long distance, or must have minimum skew among multiple destinations. Longlines, shown in Figure 14, run vertically and horizontally the height or width of the interconnect area. Each interconnection column has three vertical Longlines, and each interconnection row has two horizontal Longlines. Two additional Longlines are located adjacent to the outer sets of switching matrices. In devices larger than the XC3020A and XC3120A FPGAs, two vertical Longlines in each column are connectable half-length lines. On the XC3020A and XC3120A FPGAs, only the outer Longlines are connectable half-length lines.

Longlines can be driven by a logic block or IOB output on a column-by-column basis. This capability provides a common low skew control or clock line within each column of logic blocks. Interconnections of these Longlines are shown in Figure 15. Isolation buffers are provided at each input to a Longline and are enabled automatically by the development system when a connection is made.



Figure 14: Horizontal and Vertical Longlines. These Longlines provide high fan-out, low-skew signal distribution in each row and column. The global buffer in the upper left die corner drives a common line throughout the FPGA.

A buffer in the upper left corner of the FPGA chip drives a global net which is available to all K inputs of logic blocks. Using the global buffer for a clock signal provides a skew-free, high fan-out, synchronized clock for use at any or all of the IOBs and CLBs. Configuration bits for the K input to each logic block can select this global line or another routing resource as the clock source for its flip-flops. This net may also be programmed to drive the die edge clock lines for IOB use. An enhanced speed, CMOS threshold, direct access to this buffer is available at the second pad from the top of the left die edge.

A buffer in the lower right corner of the array drives a horizontal Longline that can drive programmed connections to a vertical Longline in each interconnection column. This alternate buffer also has low skew and high fan-out. The network formed by this alternate buffer's Longlines can be selected to drive the K inputs of the CLBs. CMOS threshold, high speed access to this buffer is available from the third pad from the bottom of the right die edge.

Internal Busses

A pair of 3-state buffers, located adjacent to each CLB, permits logic to drive the horizontal Longlines. Logic operation

A of the 3-state buffer controls allows them to implement wide multiplexing functions. Any 3-state buffer input can be

multiplexing functions. Any 3-state buffer input can be selected as drive for the horizontal long-line bus by applying a Low logic level on its 3-state control line. See Figure 16. The user is required to avoid contention which can result from multiple drivers with opposing logic levels. Control of the 3-state input by the same signal that drives the buffer input, creates an open-drain wired-AND function. A logic High on both buffer inputs creates a high impedance, which represents no contention. A logic Low enables the buffer to drive the Longline Low. See Figure 17. Pull-up resistors are available at each end of the Longline to provide a High output when all connected buffers are non-conducting. This forms fast, wide gating functions. When data drives the inputs, and separate signals drive the 3-state control lines, these buffers form multiplexers (3-state busses). In this case, care must be used to prevent contention through multiple active buffers of conflicting levels on a common line. Each horizontal Longline is also driven by a weak keeper circuit that prevents undefined floating levels by maintaining the previous logic level when the line is not driven by an active buffer or a pull-up resistor. Figure 18 shows 3-state buffers, Longlines and pull-up resistors.



Figure 18: Design Editor.

An extra large view of possible interconnections in the lower right corner of the XC3020A.

Product Obsolete or Under Obsolescence

XC3000 Series Field Programmable Gate Arrays



	Description	Symbol		Symbol		Min	Max	Units
	To address valid	1	T _{RAC}	0	200	ns		
	To data setup	2	T _{DRC}	60		ns		
RCLK	To data hold	3	T _{RCD}	0		ns		
	RCLK High		T _{RCH}	600		ns		
	RCLK Low		T _{RCL}	4.0		μs		

Notes: 1. At power-up, V_{CC} must rise from 2.0 V to V_{CC} min in less than 25 ms. If this is not possible, configuration can be delayed by holding RESET Low until VCC has reached 4.0 V (2.5 V for the XC3000L). A very long V_{CC} rise time of >100 ms, or a non-monotonically rising V_{CC} may require a >6-μs High level on RESET, followed by a >6-μs Low level on RESET and D/P after V_{CC} has reached 4.0 V (2.5 V for the XC3000L).
2. Configuration can be controlled by holding RESET Low with or until after the INIT of all daisy-chain slave-mode devices is

High.

This timing diagram shows that the EPROM requirements are extremely relaxed: EPROM access time can be longer than 4000 ns. EPROM data output has no hold time requirements.

Figure 26: Master Parallel Mode Programming Switching Characteristics



Description Symbol Min Units Max Effective Write time required 1 100 ns T_{CA} (Assertion of $\overline{CS0}$, $\overline{CS1}$, $\overline{CS2}$, \overline{WS}) **DIN Setup time required** 2 TDC 60 ns WRITE **DIN Hold time required** 3 T_{CD} 0 ns RDY/BUSY delay after end of WS 4 60 ns TWTRB Earliest next WS after end of BUSY 5 0 T_{RBWT} ns RDY **BUSY** Low time generated CCLK 6 2.5 9 TBUSY periods

Notes: 1. At powe<u>r-up, V_{CC}</u> must rise from 2.0 V to V_{CC} min in less than 25 ms. If this is not possible, configuration can be delayed by holding RESET Low until V_{CC} has reached 4.0 V (2.5 V for the X<u>C3000L</u>). A very long V_{CC} rise time of >10<u>0 ms</u>, or a non-monotonically rising V_{CC} may require a >6- μ s High level on RESET, followed by a >6- μ s Low level on RESET and D/P after V_{CC} has reached 4.0 V (2.5 V for th<u>e X</u>C3000L).

2. Configuration must be delayed until the INIT of all FPGAs is High.

- 3. Time from end of WS to CCLK cycle for the new byte of data depends on completion of previous byte processing and the phase of the internal timing generator for CCLK.
- 4. CCLK and DOUT timing is tested in slave mode.

5. T_{BUSY} indicates that the double-buffered parallel-to-serial converter is not yet ready to receive new data. The shortest T_{BUSY} occurs when a byte is loaded into an empty parallel-to-serial converter. The longest TBUSY occurs when a new word is loaded into the input register before the second-level buffer has started shifting out data.

Note: This timing diagram shows very relaxed requirements: Data need not be held beyond the rising edge of \overline{WS} . \overline{BUSY} will go active within 60 ns after the end of \overline{WS} . \overline{BUSY} will stay active for several microseconds. \overline{WS} may be asserted immediately after the end of \overline{BUSY} .

Figure 28: Peripheral Mode Programming Switching Characteristics



XC3000A IOB Switching Characteristics Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Since many internal timing parameters cannot be measured directly, they are derived from benchmark timing patterns. The following guidelines reflect worst-case values over the recommended operating conditions. For more detailed, more precise, and more up-to-date timing information, use the values provided by the timing calculator and used in the simulator.

(Sp	eed Grade	-	7	-	6	
Description		S	ymbol	Min	Max	Min	Max	Units
Propagation Delays (Input)								
Pad to Direct In (I)		3	T _{PID}		4.0		3.0	ns
Pad to Registered In (Q) with la	tch transparent		T _{PTG}		15.0		14.0	ns
Clock (IK) to Registered In (Q)		4	T _{IKRI}		3.0		2.5	ns
Set-up Time (Input)								
Pad to Clock (IK) set-up time		1	T _{PICK}	14.0		12.0		ns
Propagation Delays (Output)								
Clock (OK) to Pad	(fast)	7	Т _{ОКРО}		8.0		7.0	ns
same	(slew rate limited)	7	Т _{ОКРО}		18.0		15.0	ns
Output (O) to Pad	(fast)	10	T _{OPF}		6.0		5.0	ns
same	(slew-rate limited)	10	T _{OPS}		16.0		13.0	ns
3-state to Pad begin hi-Z	(fast)	9	T _{TSHZ}		10.0		9.0	ns
same	(slew-rate limited)	9	T _{TSHZ}		20.0		12.0	ns
3-state to Pad active and valid	(fast)	8	T _{TSON}		11.0		10.0	ns
same	(slew -rate limited)	8	T _{TSON}		21.0		18.0	ns
Set-up and Hold Times (Output)								
Output (O) to clock (OK) set-up	time	5	Т _{ООК}	8.0		7.0		ns
Output (O) to clock (OK) hold tin	me	6	т _{око}	0		0		ns
Clock								
Clock High time		11	T _{IOH}	4.0		3.5		ns
Clock Low time		12	T _{IOL}	4.0		3.5		ns
Max. flip-flop toggle rate			F _{CLK}	113.0		135.0		MHz
Global Reset Delays (based on XC3042A)								
RESET Pad to Registered In	(Q)	13	T _{RRI}		24.0		23.0	ns
RESET Pad to output pad	(fast)	15	T _{RPO}		33.0		29.0	ns
	(slew-rate limited)	15	T _{RPO}		43.0		37.0	ns

Notes: 1. Timing is measured at pin threshold, with 50 pF external capacitive loads (incl. test fixture). Typical slew rate limited output rise/fall times are approximately four times longer.

2. Voltage levels of unused (bonded and unbonded) pads must be valid logic levels. Each can be configured with the internal pull-up resistor or alternatively configured as a driven output or driven from an external source.

3. Input pad set-up time is specified with respect to the internal clock (ik). In order to calculate system set-up time, subtract clock delay (pad to ik) from the input pad set-up time value. Input pad holdtime with respect to the internal clock (ik) is negative. This means that pad level changes immediately before the internal clock edge (ik) will not be recognized.

4. T_{PID} , T_{PTG} , and T_{PICK} are 3 ns higher for XTL2 when the pin is configured as a user input.

XILINX[®]

XC3000A IOB Switching Characteristics Guidelines (continued)







XC3000L Switching Characteristics

Xilinx maintains test specifications for each product as controlled documents. To insure the use of the most recently released device performance parameters, please request a copy of the current test-specification revision.

XC3000L Operating Conditions

Symbol	Description	Min	Max	Units
V _{CC}	Supply voltage relative to GND Commercial 0°C to +85°C junction	3.0	3.6	V
V _{IH}	High-level input voltage — TTL configuration	2.0	V _{CC} +0.3	V
V _{IL}	Low-level input voltage — TTL configuration	-0.3	0.8	V
T _{IN}	Input signal transition time		250	ns

Notes: 1. At junction temperatures above those listed as Operating Conditions, all delay parameters increase by 0.3% per °C. 2. Although the present (1996) devices operate over the full supply voltage range from 3.0 to 5.25 V, Xilinx reserves the right to restrict operation to the 3.0 to 3.6 V range later, when smaller device geometries might preclude operation at 5V. Operating conditions are guaranteed in the $3.0 - 3.6 \text{ V V}_{CC}$ range.

XC3000L DC Characteristics Over Operating Conditions

Symbol	Description	Min	Max	Units
V _{OH}	High-level output voltage (@ I _{OH} = -4.0 mA, V _{CC} min)	2.40		V
V _{OL}	Low-level output voltage (@ I _{OL} = 4.0 mA, V _{CC} min)		0.40	V
V _{OH}	High-level output voltage (@ $I_{OH} = -4.0 \text{ mA}, V_{CC} \text{ min}$)	V _{CC} -0.2		V
V _{OL}	Low-level output voltage (@ I _{OL} = 4.0 mA, V _{CC} min)		0.2	V
V _{CCPD}	Power-down supply voltage (PWRDWN must be Low)	2.30		V
I _{CCPD}	Power-down supply current (V _{CC(MAX)} @ T _{MAX})		10	μA
Icco	Quiescent FPGA supply current in addition to I _{CCPD} ¹ Chip thresholds programmed as CMOS levels		20	μA
IIL	Input Leakage Current	-10	+10	μA
6	Input capacitance, all packages except PGA175 (sample tested) All Pins except XTL1 and XTL2 XTL1 and XTL2		10 15	pF pF
C _{IN}	Input capacitance, PGA 175 (sample tested) All Pins except XTL1 and XTL2 XTL1 and XTL2		15 20	pF pF
I _{RIN}	Pad pull-up (when selected) @ $V_{IN} = 0 V^3$	0.01	0.17	mA
I _{RLL}	Horizontal Longline pull-up (when selected) @ logic Low		2.50	mA

Notes: 1. With no output current loads, no active input or Longline pull-up resistors, all package pins at V_{CC} or GND, and the FPGA

device configured with a tie option. I_{CCO} is in addition to I_{CCPD}.
2. Total continuous output sink current may not exceed 100 mA per ground pin. Total continuous output source may not exceed 100 mA per V_{CC} pin. The number of ground pins varies from the XC3020L to the XC3090L.

3. Not tested. Allows an undriven pin to float High. For any other purpose, use an external pull-up.

XC3000L Absolute Maximum Ratings

Symbol	Description		Units
V _{CC}	Supply voltage relative to GND	-0.5 to +7.0	V
V _{IN}	Input voltage with respect to GND	–0.5 to V _{CC} +0.5	V
V _{TS}	Voltage applied to 3-state output	–0.5 to V _{CC} +0.5	V
T _{STG}	Storage temperature (ambient)	-65 to +150	°C
T _{SOL}	Maximum soldering temperature (10 s @ 1/16 in.)	+260	°C
т	Junction temperature plastic	+125	°C
١٦	Junction temperature ceramic	+150	°C

Note: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

XC3000L Global Buffer Switching Characteristics Guidelines

	Speed Grade	-8	
Description	Symbol	Max	Units
Global and Alternate Clock Distribution ¹			
Either: Normal IOB input pad through clock buffer			
to any CLB or IOB clock input	T _{PID}	9.0	ns
Or: Fast (CMOS only) input pad through clock			
buffer to any CLB or IOB clock input	T _{PIDC}	7.0	ns
TBUF driving a Horizontal Longline (L.L.) ¹			
I to L.L. while T is Low (buffer active)	T _{IO}	5.0	ns
T \downarrow to L.L. active and valid with single pull-up resistor	T _{ON}	12.0	ns
T↑ to L.L. High with single pull-up resistor	T _{PUS}	24.0	ns
BIDI			
Bidirectional buffer delay	T _{BIDI}	2.0	ns

Notes: 1. Timing is based on the XC3042A, for other devices see timing calculator.

2. The use of two pull-up resistors per Longline, available on other XC3000 devices, is not a valid option for XC3000L devices.

XC3000L CLB Switching Characteristics Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Since many internal timing parameters cannot be measured directly, they are derived from benchmark timing patterns. The following guidelines reflect worst-case values over the recommended operating conditions. For more detailed, more precise, and more up-to-date timing information, use the values provided by the timing calculator and used in the simulator.

		S	beed Grade	-	·8	
	Description	S	Symbol	Min	Max	Units
Combinatorial Delay						
Logic Variables	A, B, C, D, E, to outputs X or Y					
	FG Mode	1	T _{ILO}		6.7	ns
	F and FGM Mode		.20		7.5	ns
Sequential delay						
Clock k to outputs	s X or Y	8	Тско		7.5	ns
Clock k to outputs	s X or Y when Q is returned		one			
through function g	generators F or G to drive X or Y					
	FG Mode		T _{QLO}		14.0	ns
	F and FGM Mode				14.8	ns
Set-up time before clo	ck K					
Logic Variables	A, B, C, D, E					
	FG Mode	2	TICK	5.0		ns
	F and FGM Mode			5.8		ns
Data In	DI	4	TDICK	5.0		ns
Enable Clock	EC	6	T _{ECCK}	6.0		ns
Hold Time after clock	K					
Logic Variables	A, B, C, D, E	3	Тскі	0		ns
Data In	DI ²	5	T _{CKDI}	2.0		ns
Enable Clock	EC	7	T _{CKEC}	2.0		ns
Clock						
Clock High time		11	T _{CH}	5.0		ns
Clock Low time		12	T _{CL}	5.0		ns
Max. flip-flop togg	le rate		F _{CLK}	80.0		MHz
Reset Direct (RD)			_			
RD width		13	T _{RPW}	7.0		ns
delay from RD to	outputs X or Y	9	T _{RIO}	7.0		ns
Global Reset (RESET	Pad) ¹					
RESET width (Lo	<u>w</u>)		T _{MRW}	16.0		ns
delay from RESE	T pad to outputs X or Y		T _{MRQ}		23.0	ns

Notes: 1. Timing is based on the XC3042L, for other devices see timing calculator.

The CLB K to Q output delay (T_{CKO}, #8) of any CLB, plus the shortest possible interconnect delay, is always longer than the Data In hold time requirement (T_{CKDI}, #5) of any CLB on the same die.

∑XILINX[®]

XC3000L CLB Switching Characteristics Guidelines (continued)





XC3000L IOB Switching Characteristics Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Since many internal timing parameters cannot be measured directly, they are derived from benchmark timing patterns. The following guidelines reflect worst-case values over the recommended operating conditions. For more detailed, more precise, and more up-to-date timing information, use the values provided by the timing calculator and used in the simulator.

		Speed Grade			-		
Des	scription		S	ymbol	Min	Max	Units
Propagation Delays (Input)							
Pad to Direct In (I)			3	T _{PID}		5.0	ns
Pad to Registered In (Q) with la	tch transparent			T _{PTG}		24.0	ns
Clock (IK) to Registered In (Q)			4	T _{IKRI}		6.0	ns
Set-up Time (Input)							
Pad to Clock (IK) set-up time			1	T _{PICK}	22.0		ns
Propagation Delays (Output)							
Clock (OK) to Pad	(fast)		7	Т _{ОКРО}		12.0	ns
same	(slew rate limited)		7	Т _{ОКРО}		28.0	ns
Output (O) to Pad	(fast)		10	T _{OPF}		9.0	ns
same	(slew-rate limited)		10	T _{OPS}		25.0	ns
3-state to Pad begin hi-Z	(fast)		9	T _{TSHZ}		12.0	ns
same	(slew-rate limited)		9	T _{TSHZ}		28.0	ns
3-state to Pad active and valid	(fast)		8	T _{TSON}		16.0	ns
same	(slew -rate limited)		8	T _{TSON}		32.0	ns
Set-up and Hold Times (Output)							
Output (O) to clock (OK) set-up	time		5	Т _{ООК}	12.0		ns
Output (O) to clock (OK) hold tin	ne		6	Т _{око}	0		ns
Clock							
Clock High time			11	T _{IOH}	5.0		ns
Clock Low time			12	T _{IOL}	5.0		ns
Max. flip-flop toggle rate				F _{CLK}	80.0		MHz
Global Reset Delays (based on XC	:3042L)						
RESET Pad to Registered In	(Q)		13	T _{RRI}		25.0	ns
RESET Pad to output pad	(fast)		15	T _{RPO}		35.0	ns
	(slew-rate limited)		15	T _{RPO}		51.0	ns

Notes: 1. Timing is measured at pin threshold, with 50 pF external capacitive loads (incl. test fixture). Typical slew rate limited output rise/fall times are approximately four times longer.

2. Voltage levels of unused (bonded and unbonded) pads must be valid logic levels. Each can be configured with the internal pull-up resistor or alternatively configured as a driven output or driven from an external source.

3. Input pad set-up time is specified with respect to the internal clock (ik). In order to calculate system set-up time, subtract clock delay (pad to ik) from the input pad set-up time value. Input pad holdtime with respect to the internal clock (ik) is negative. This means that pad level changes immediately before the internal clock edge (ik) will not be recognized.

4. T_{PID}, T_{PTG}, and T_{PICK} are 3 ns higher for XTL2 when the pin is configured as a user input.



XC3100L Switching Characteristics

Xilinx maintains test specifications for each product as controlled documents. To insure the use of the most recently released device performance parameters, please request a copy of the current test-specification revision.

XC3100L Operating Conditions

Symbol	Description	Min	Max	Units
V _{CC}	Supply voltage relative to GND Commercial 0°C to +85°C junction	3.0	3.6	V
V _{IH}	High-level input voltage	2.0	V _{CC} + 0.3	V
V _{IL}	Low-level input voltage	-0.3	0.8	V
T _{IN}	Input signal transition time		250	ns

Notes: 1. At junction temperatures above those listed as Operating Conditions, all delay parameters increase by 0.3% per °C. 2. Although the present (1996) devices operate over the full supply voltage range from 3.0 V to 5.25 V, Xilinx reserves the right to restrict operation to the 3.0 and 3.6 V range later, when smaller device geometries might preclude operation @ 5 V. Operating conditions are guaranteed in the $3.0 - 3.6 \vee V_{CC}$ range.

XC3100L DC Characteristics Over Operating Conditions

Symbol	Description	Min	Max	Units
V	High-level output voltage (@ I _{OH} = -4.0 mA, V _{CC} min)	2.4		V
⊻ОН	High-level output voltage (@ I_{OH} = -100.0 μ A, V _{CC} min)	V _{CC} -0.2		V
V.	Low-level output voltage (@ I _{OH} = 4.0 mA, V _{CC} min)		0.40	V
V OL	Low-level output voltage (@ I_{OH} = +100.0 μ A, V _{CC} min)		0.2	V
V _{CCPD}	Power-down supply voltage (PWRDWN must be Low)	2.30		V
I _{CCO}	Quiescent FPGA supply current		1.5	mA
	Chip thresholds programmed as CMOS levels ¹			
۱ _{IL}	Input Leakage Current	-10	+10	μΑ
	Input capacitance			
Curr	(sample tested)			
CIN	All pins except XTL1 and XTL2		10	pF
	XTL1 and XTL2		15	pF
I _{RIN}	Pad pull-up (when selected) @ V_{IN} = 0 V ³	0.02	0.17	mA
I _{RLL}	Horizontal long line pull-up (when selected) @ logic Low	0.20	2.80	mA

Notes: 1. With no output current loads, no active input or long line pull-up resistors, all package pins at V_{CC} or GND, and the FPGA configured with a tie option.

2. Total continuous output sink current may not exceed 100 mA per ground pin. Total continuous output source current may not exceed 100 mA per V_{CC} pin. The number of ground pins varies from the XC3142L to the XC3190L. 3. Not tested. Allows undriven pins to float High. For any other purpose, use an external pull-up.



XC3100L CLB Switching Characteristics Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Since many internal timing parameters cannot be measured directly, they are derived from benchmark timing patterns. The following guidelines reflect worst-case values over the recommended operating conditions. For more detailed, more precise, and more up-to-date timing information, use the values provided by the timing calculator and used in the simulator.

Speed Grade		-3		-2			
Description	S	symbol	Min	Max	Min	Max	Units
Combinatorial Delay							
Logic Variables A, B, C, D, E, to outputs X or Y	1	T _{ILO}		2.7		2.2	ns
Sequential delay							
Clock k to outputs X or Y	8	т _{ско}		2.1		1.7	ns
Clock k to outputs X or Y when Q is returned							
through function generators F or G to drive X or Y		T _{QLO}		4.3		3.5	ns
Set-up time before clock K							
Logic Variables A, B, C, D, E	2	T _{ICK}	2.1		1.8		ns
Data In DI	4	T _{DICK}	1.4		1.3		ns
Enable Clock EC	6	T _{ECCK}	2.7		2.5		ns
Reset Direct Inactive RD			1.0		1.0		ns
Hold Time after clock K							
Logic Variables A, B, C, D, E	3	тскі	0		0		ns
Data In DI	5	T _{CKDI}	0.9		0.9		ns
Enable Clock EC	7	T _{CKEC}	0.7		0.7		ns
Clock							
Clock High time	11	T _{CH}	1.6		1.3		ns
Clock Low time	12	T _{CL}	1.6		1.3		ns
Max. flip-flop toggle rate		F _{CLK}	270		325		MHz
Reset Direct (RD)							
RD width	13	T _{RPW}	2.7		2.3		ns
delay from RD to outputs X or Y	9	T _{RIO}		3.1		2.7	ns
Global Reset (RESET Pad)							
RESET width (Low)							ns
(XC3142L)		T _{MRW}	12.0		12.0		ns
delay from RESET pad to outputs X or Y		T _{MRQ}		12.0		12.0	
				Adv	ance		

Notes: 1. The CLB K to Q delay (T_{CKO}, #8) of any CLB, plus the shortest possible interconnect delay, is always longer than the Data

In hold time requirement (T_{CKDI}, #5) of any CLB on the same die. 2. T_{ILO}, T_{QLO} and T_{ICK} are specified for 4-input functions. For 5-input functions or base FGM functions, each of these specifications for the XC3100L family increase by 0.35 ns (-3) and 0.29 ns (-2).

XC3100L IOB Switching Characteristics Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Since many internal timing parameters cannot be measured directly, they are derived from benchmark timing patterns. The following guidelines reflect worst-case values over the recommended operating conditions. For more detailed, more precise, and more up-to-date timing information, use the values provided by the timing calculator and used in the simulator.

		Speed Grade				-		
Description	S	Symbol	Min	Max	Min	Max	Units	
Propagation Delays (Input)								
Pad to Direct In (I)		3	T _{PID}		2.2		2.0	ns
Pad to Registered In (Q) wit	h latch (XC3100L)		T _{PTG}		11.0		11.0	ns
transparent								
Clock (IK) to Registered In (Q)	4	T _{IKRI}		2.2		1.9	ns
Set-up Time (Input)								
Pad to Clock (IK) set-up time	e	1	T _{PICK}					
	XC3142L			9.5		9.0		ns
	XC3190L			9.9		9.4		ns
Propagation Delays (Output)								
Clock (OK) to Pad	(fast)	7	T _{OKPO} T _{OK}		4.4		4.0	ns
same	(slew rate limited)	7	PO		10.0		9.7	ns
Output (O) to Pad	(fast)	10	T _{OPF}		3.3		3.0	ns
same (slew-ra	ate limited)(XC3100L)	10	T _{OPF}		9.0		8.7	ns
3-state to Pad begin hi-Z	(fast)	9	T _{TSHZ}		5.5		5.0	ns
same	(slew-rate limited)	9	T _{TSHZ}		5.5		5.0	ns
3-state to Pad active and va	lid (fast) (XC3100L)	8	T _{TSON}		9.0		8.5	ns
same	(slew -rate limited)	8	T _{TSON}		15.0		14.2	ns
Set-up and Hold Times (Output)								
Output (O) to clock (OK) set	-up time (XC3100L)	5	Т _{ООК}	4.0		3.6		ns
Output (O) to clock (OK) hold time			Токо	0		0		ns
Clock								
Clock High time		11	T _{IOH}	1.6		1.3		ns
Clock Low time		12	TIOL	1.6		1.3		ns
Export Control Maximum flip	o-flop toggle rate		F _{TOG}	270		325		MHz
Global Reset Delays								
RESET Pad to Registered In (Q)								
	(XC3142L)	13	T _{RRI}		16.0		16.0	ns
	(XC3190L)				21.0		21.0	ns
RESET Pad to output pad	(fast)	15	T _{RPO}		17.0		17.0	ns
	(slew-rate limited)	15	T _{RPO}		23.0		23.0	ns
			-!		Adv	ance		

Notes: 1. Timing is measured at pin threshold, with 50 pF external capacitive loads (incl. test fixture). Typical slew rate limited output rise/fall times are approximately four times longer.

2. Voltage levels of unused (bonded and unbonded) pads must be valid logic levels. Each can be configured with the internal pull-up resistor or alternatively configured as a driven output or driven from an external source.

3. Input pad set-up time is specified with respect to the internal clock (IK). In order to calculate system set-up time, subtract clock delay (pad to ik) from the input pad set-up time value. Input pad holdtime with respect to the internal clock (IK) is negative. This means that pad level changes immediately before the internal clock edge (IK) will not be recognized.

XC3100L IOB Switching Characteristics Guidelines (continued)





XC3064A/XC3090A/XC3195A 84-Pin PLCC Pinouts

XC3000A, XC3000L, XC3100A, and XC3100L families have identical pinouts

PLCC Pin Number	XC3064A, XC3090A, XC3195A	P
12	PWRDN	
13	TCLKIN-I/O	
14	I/O	
15	I/O	
16	I/O	
17	I/O	
18	I/O	
19	I/O	
20	I/O	
21	GND*	
22	VCC	
23	I/O	
24	I/O	
25	I/O	
26	I/O	
27	I/O	
28	I/O	
29	I/O	
30	I/O	
31	M1-RDATA	
32	M0-RTRIG	
33	M2-I/O	
34	HDC-I/O	
35	I/O	
36	LDC-I/O	
37	I/O	
38	I/O	
39	I/O	
40	I/O	
41	INIT/I/O*	
42	VCC*	
43	GND	
44	I/O	
45	I/O	
46	I/O	
47	I/O	
48	I/O	
49	I/O	
50	I/O	
51	I/O	
52	I/O	
53	XTL2(IN)-I/O	

PLCC Pin Number	XC3064A, XC3090A, XC3195A
54	RESET
55	DONE-PG
56	D7-I/O
57	XTL1(OUT)-BCLKIN-I/O
58	D6-I/O
59	I/O
60	D5-I/O
61	CS0-I/O
62	D4-I/O
63	I/O
64	VCC
65	GND*
66	D3-I/O*
67	CS1-I/O*
68	D2-I/O*
69	I/O
70	D1-I/O
71	RDY/BUSY-RCLK-I/O
72	D0-DIN-I/O
73	DOUT-I/O
74	CCLK
75	A0-WS-I/O
76	A1-CS2-I/O
77	A2-I/O
78	A3-I/O
79	I/O
80	I/O
81	A15-I/O
82	A4-I/O
83	A14-I/O
84	A5-I/O
1	GND
2	VCC*
3	A13-I/O*
4	A6-I/O*
5	A12-I/O*
6	A7-I/O*
7	I/O
8	A11-I/O
9	A8-I/O
10	A10-I/O
11	A9-I/O

Unprogrammed IOBs have a default pull-up. This prevents an undefined pad level for unbonded or unused IOBs. Programmed outputs are default slew-rate limited.

* In the PC84 package, XC3064A, XC3090A and XC3195A have additional VCC and GND pins and thus a different pin definition than XC3020A/XC3030A/XC3042A.



XC3000 Series 100-Pin QFP Pinouts

XC3000A, XC3000L, XC3100A, and XC3100L families have identical pinouts

Pin No.		XC3020A	Pin No. XC3020A		XC3020A	Pin No.		XC3020A	
PQFP	TQFP VQFP	XC3030A XC3042A	PQFP	TQFP VQFP	XC3030A XC3042A	PQFP	TQFP VQFP	XC3030A XC3042A	
16	13	GND	50	47	I/O*	84	81	I/O*	
17	14	A13-I/O	51	48	I/O*	85	82	I/O*	
18	15	A6-I/O	52	49	M1-RD	86	83	I/O	
19	16	A12-I/O	53	50	GND*	87	84	D5-I/O	
20	17	A7-I/O	54	51	MO-RT	88	85	CS0-I/O	
21	18	I/O*	55	52	VCC*	89	86	D4-I/O	
22	19	I/O*	56	53	M2-I/O	90	87	I/O	
23	20	A11-I/O	57	54	HDC-I/O	91	88	VCC	
24	21	A8-I/O	58	55	I/O	92	89	D3-I/O	
25	22	A10-I/O	59	56	LDC-I/O	93	90	CS1-I/O	
26	23	A9-I/O	60	57	I/O*	94	91	D2-I/O	
27	24	VCC*	61	58	I/O*	95	92	I/O	
28	25	GND*	62	59	I/O	96	93	I/O*	
29	26	PWRDN	63	60	I/O	97	94	I/O*	
30	27	TCLKIN-I/O	64	61	I/O	98	95	D1-I/O	
31	28	I/O**	65	62	INIT-I/O	99	96	RDY/BUSY-RCLK-I/O	
32	29	I/O*	66	63	GND	100	97	DO-DIN-I/O	
33	30	I/O*	67	64	I/O	1	98	DOUT-I/O	
34	31	I/O	68	65	I/O	2	99	CCLK	
35	32	I/O	69	66	I/O	3	100	VCC*	
36	33	I/O	70	67	I/O	4	1	GND*	
37	34	I/O	71	68	I/O	5	2	AO-WS-I/O	
38	35	I/O	72	69	I/O	6	3	A1-CS2-I/O	
39	36	I/O	73	70	I/O	7	4	I/O**	
40	37	I/O	74	71	I/O*	8	5	A2-I/O	
41	38	VCC	75	72	I/O*	9	6	A3-I/O	
42	39	I/O	76	73	XTL2-I/O	10	7	I/O*	
43	40	I/O	77	74	GND*	11	8	I/O*	
44	41	I/O	78	75	RESET	12	9	A15-I/O	
45	42	I/O	79	76	VCC*	13	10	A4-I/O	
46	43	I/O	80	77	DONE-PG	14	11	A14-I/O	
47	44	I/O	81	78	D7-I/O	15	12	A5-I/O	
48	45	I/O	82	79	BCLKIN-XTL1-I/O				
49	46	I/O	83	80	D6-I/O				

Unprogrammed IOBs have a default pull-up. This prevents an undefined pad level for unbonded or unused IOBs. Programmed outputs are default slew-rate limited.

* This table describes the pinouts of three different chips in three different packages. The pin-description column lists 100 of the 118 pads on the XC3042A that are connected to the 100 package pins. Two pads, indicated by double asterisks, do not exist on the XC3030A, which has 98 pads; therefore the corresponding pins have no connections. Twenty-six pads, indicated by single or double asterisks, do not exist on the XC3020A, which has 74 pads; therefore, the corresponding pins have no connections. (See table on page 65.)

XC3000 Series 132-Pin Ceramic and Plastic PGA Pinouts

XC3000A, XC3000L, XC3100A, and XC3100L families have identical pinouts

PGA		PGA		PGA		PGA	
Pin	XC3042A	Pin	XC3042A	Pin	XC3042A	Pin	XC3042A
Number	XC3064A	Number	XC3064A	Number	XC3064A	Number	XC3064A
C4	GND	B13	M1-RD	P14	RESET	M3	DOUT-I/O
A1	PWRDN	C11	GND	M11	VCC	P1	CCLK
C3	I/O-TCLKIN	A14	M0-RT	N13	DONE-PG	M4	VCC
B2	I/O	D12	VCC	M12	D7-I/O	L3	GND
B3	I/O	C13	M2-I/O	P13	XTL1-I/O-BCLKIN	M2	A0-WS-I/O
A2	I/O*	B14	HDC-I/O	N12	I/O	N1	A1-CS2-I/O
B4	I/O	C14	I/O	P12	I/O	M1	I/O
C5	I/O	E12	I/O	N11	D6-I/O	K3	I/O
A3	I/O*	D13	I/O	M10	I/O	L2	A2-I/O
A4	I/O	D14	LDC-I/O	P11	I/O*	L1	A3-I/O
B5	I/O	E13	I/O*	N10	I/O	K2	I/O
C6	I/O	F12	I/O	P10	I/O	J3	I/O
A5	I/O	E14	I/O	M9	D5-I/O	K1	A15-I/O
B6	I/O	F13	I/O	N9	CS0-I/O	J2	A4-I/O
A6	I/O	F14	I/O	P9	I/O*	J1	I/O*
B7	I/O	G13	I/O	P8	I/O*	H1	A14-I/O
C7	GND	G14	INIT-I/O	N8	D4-I/O	H2	A5-I/O
C8	VCC	G12	VCC	P7	I/O	H3	GND
A7	I/O	H12	GND	M8	VCC	G3	VCC
B8	I/O	H14	I/O	M7	GND	G2	A13-I/O
A8	I/O	H13	I/O	N7	D3-I/O	G1	A6-I/O
A9	I/O	J14	I/O	P6	CS1-I/O	F1	I/O*
B9	I/O	J13	I/O	N6	I/O*	F2	A12-I/O
C9	I/O	K14	I/O	P5	I/O*	E1	A7-I/O
A10	I/O	J12	I/O	M6	D2-I/O	F3	I/O
B10	I/O	K13	I/O	N5	I/O	E2	I/O
A11	I/O*	L14	I/O*	P4	I/O	D1	A11-I/O
C10	I/O	L13	I/O	P3	I/O	D2	A8-I/O
B11	I/O	K12	I/O	M5	D1-I/O	E3	I/O
A12	I/O*	M14	I/O	N4	RDY/BUSY-RCLK-I/O	C1	I/O
B12	I/O	N14	I/O	P2	I/O	B1	A10-I/O
A13	I/O*	M13	XTL2(IN)-I/O	N3	I/O	C2	A9-I/O
C12	I/O	L12	GND	N2	D0-DIN-I/O	D3	VCC

Unprogrammed IOBs have a default pull-up. This prevents an undefined pad level for unbonded or unused IOBs. Programmed outputs are default slew-rate limited.

* Indicates unconnected package pins (14) for the XC3042A.



XC3000 Series 208-Pin PQFP Pinouts

XC3000A, and XC3000L families have identical pinouts

Pin Number	XC3090A	Pin Number	XC3090A	Pin Number	XC3090A	Pin Number	XC3090A
1	-	53	-	105	-	157	-
2	GND	54	-	106	VCC	158	-
3	PWRDWN	55	VCC	107	D/P	159	-
4	TCLKIN-I/O	56	M2-I/O	108	-	160	GND
5	I/O	57	HDC-I/O	109	D7-I/O	161	WS-A0-I/O
6	I/O	58	I/O	110	XTL1-BCLKIN-I/O	162	CS2-A1-I/O
7	I/O	59	I/O	111	I/O	163	I/O
8	I/O	60	I/O	112	I/O	164	I/O
9	I/O	61	LDC-I/O	113	I/O	165	A2-I/O
10	I/O	62	I/O	114	I/O	166	A3-I/O
11	I/O	63	I/O	115	D6-I/O	167	I/O
12	I/O	64	-	116	I/O	168	I/O
13	I/O	65	-	117	I/O	169	-
14	I/O	66	-	118	I/O	170	-
15	-	67	-	119	-	171	_
16	I/O	68	I/O	120	I/O	172	A15-I/O
17	I/O	69	I/O	121	I/O	173	A4-I/O
18	I/O	70	I/O	122	D5-I/O	174	I/O
19	I/O	71	I/O	123	CS0-I/O	175	I/O
20	I/O	72	-	124	I/O	176	_
21	I/O	73	-	125	I/O	177	-
22	I/O	74	I/O	126	I/O	178	A14-I/O
23	I/O	75	I/O	127	I/O	179	A5-I/O
24	I/O	76	I/O	128	D4-I/O	180	I/O
25	GND	77	INIT-I/O	129	I/O	181	I/O
26	VCC	78	VCC	130	VCC	182	GND
27	I/O	79	GND	131	GND	183	VCC
28	I/O	80	I/O	132	D3-I/O	184	A13-I/O
29	I/O	81	I/O	133	CS1-I/O	185	A6-I/O
30	I/O	82	I/O	134	I/O	186	I/O
31	I/O	83	-	135	I/O	187	I/O
32	I/O	84	-	136	I/O	188	_
33	I/O	85	I/O	137	I/O	189	-
34	I/O	86	I/O	138	D2-I/O	190	I/O
35	I/O	87	I/O	139	I/O	191	I/O
36	I/O	88	I/O	140	I/O	192	A12-I/O
37	-	89	I/O	141	I/O	193	A7-I/O
38	I/O	90	-	142	-	194	-
39	I/O	91	-	143	I/O	195	-
40	I/O	92	-	144	I/O	196	-
41	I/O	93	I/O	145	D1-I/O	197	I/O
42	I/O	94	I/O	146	RDY/BUSY-RCLK-I/O	198	I/O
43	I/O	95	I/O	147	I/O	199	A11-I/O
44	I/O	96	I/O	148	I/O	200	A8-I/O
45	I/O	97	I/O	149	I/O	201	I/O
46	I/O	98	I/O	150	I/O	202	I/O
47	I/O	99	I/O	151	DIN-D0-I/O	203	A10-I/O
48	M1-RDATA	100	XTL2-I/O	152	DOUT-I/O	204	A9-I/O
49	GND	101	GND	153	CCLK	205	VCC
50	M0-RTRIG	102	RESET	154	VCC	206	-
51	-	103	-	155	-	207	-
52	-	104	-	156	-	208	-
1		L			1		

Unprogrammed IOBs have a default pull-up. This prevents an undefined pad level for unbonded or unused IOBs. Programmed outputs are default slew-rate limited.

* In PQ208, XC3090A and XC3195A have different pinouts.

XC3195A PQ208 Pinouts

AA10-0 206 Do-DIN-NO 154 I/O 102 100 48 A10-00 205 I/O 152 I/O 100 100 100 100 48 I/O 201 I/O 151 I/O 100 98 I/O 48 I/O 201 R/MUSV-RCLK-10 148 I/O 97 I/O 445 I/O 198 I/O 144 I/O 95 I/O 43 I/O 198 I/O 144 I/O 95 I/O 44 I/O 194 I/O 144 I/O 90 100 37 I/O 194 I/O 138 I/O 86 I/O 38 I/O 197 I/O 138 I/O 86 I/O 31 I/O 198 I/O 131 I/O 86 I/O 32 I/O 198 I/O 132	Pin Description	PQ208	Pin Description	PQ208	Pin Description	PQ208	Pin Description	PQ208
Att-No 205 VO 153 VO 101 VO 47 VO 203 VO 151 VO 100 99 VO 45 VO 202 VO 156 VO 99 VO 45 VO 199 VO 148 VO 96 VO 42 VO 198 VO 146 VO 96 VO 42 VO 198 VO 146 VO 96 VO 42 VO 198 VO 146 VO 96 VO 42 VO 193 VO 146 VO 92 VO 38 VO 33 VO	A9-I/O	206	D0-DIN-I/O	154	I/O	102	I/O	48
I/O 204 I/O 152 I/O 100 100 I/O 202 I/O 151 I/O 98 I/O 44 I/O 202 I/O 150 I/O 98 I/O 44 I/O 202 I/O 141 I/O 96 I/O 43 AA1/O 199 I/O 144 I/O 96 I/O 43 I/O 197 I/O 144 I/O 96 I/O 43 I/O 198 I/O 144 I/O 93 I/O 39 I/O 192 I/O 138 I/O 89 I/O 36 I/O 198 I/O 136 I/O 81 I/O 31 I/O 198 I/O 134 I/O 81 I/O 31 I/O 198 I/O 132 I/O 81 I/O 32 I/O </td <td>A10-I/O</td> <td>205</td> <td>I/O</td> <td>153</td> <td>I/O</td> <td>101</td> <td>I/O</td> <td>47</td>	A10-I/O	205	I/O	153	I/O	101	I/O	47
I/O 203 I/O 151 I/O 99 I/O 451 I/O 202 I/O 160 140 100 99 I/O 44 I/O 203 D1-I/O 148 I/O 96 I/O 43 I/O 198 I/O 146 I/O 96 I/O 43 I/O 198 I/O 146 I/O 93 I/O 43 I/O 198 I/O 144 I/O 92 I/O 33 I/O 191 I/O 144 I/O 88 I/O 38 I/O 191 I/O 136 I/O 84 I/O 38 I/O 186 I/O 136 I/O 83 I/O 38 I/O 186 I/O 132 I/O 81 I/O 32 I/O 186 I/O 128 I/O 76 I/O 32	I/O	204	I/O	152	I/O	100	I/O	46
I/O 202 I/O 150 I/O 98 I/O 44 I/O 201 D1 1/O 1/O 1/O 43 AB-I/O 200 D1 1/O 1/A 1/O 98 1/O 43 I/O 198 I/O 1/A 1/O 98 1/O 43 I/O 197 I/O 1/A 1/O 98 1/O 43 I/O 198 I/O 1/A 1/O 98 1/O 42 I/O 197 I/O 1/A 1/O 98 1/O 42 I/O 198 I/O 1/A 1/O 88 1/O 38 I/O 198 I/O 138 I/O 88 1/O 38 I/O 189 I/O 136 I/O 84 I/O 32 I/O 187 I/O 138 I/O 81 I/O 32 <tr< td=""><td>I/O</td><td>203</td><td>I/O</td><td>151</td><td>I/O</td><td>99</td><td>I/O</td><td>45</td></tr<>	I/O	203	I/O	151	I/O	99	I/O	45
I/O 201 RDVRUSY-RCLK-IO 149 I/O 97 I/O 43 AB-IO 200 11/O 146 I/O 97 I/O 42 I/O 198 I/O 146 I/O 93 I/O 43 I/O 197 I/O 146 I/O 93 I/O 43 I/O 198 I/O 144 I/O 92 I/O 43 I/O 198 I/O 144 I/O 92 I/O 38 I/O 191 I/O 143 I/O 86 I/O 38 I/O 191 I/O 137 I/O 86 I/O 38 I/O 188 I/O 133 I/O 86 I/O 38 I/O 186 D3-I/O 132 I/O 80 I/O 38 I/O 186 D3-I/O 132 I/O 80 I/O 38 <td>I/O</td> <td>202</td> <td>I/O</td> <td>150</td> <td>I/O</td> <td>98</td> <td>I/O</td> <td>44</td>	I/O	202	I/O	150	I/O	98	I/O	44
AR-I/O 200 D1-I/O 148 I/O 96 I/O 42 A11-I/O 199 I/O 146 I/O 95 I/O 42 I/O 197 I/O 144 I/O 95 I/O 42 I/O 197 I/O 144 I/O 92 I/O 42 I/O 194 I/O 144 I/O 93 I/O 42 I/O 194 I/O 144 I/O 93 I/O 38 I/O 192 I/O 138 I/O 86 I/O 38 I/O 187 I/O 133 I/O 84 I/O 32 I/O 188 I/O 122 I/O 81 I/O 28 I/O 181 D4/O 133 I/O 81 I/O 28 I/O 181 D4/O 122 I/O 75 I/O 22 <td>I/O</td> <td>201</td> <td>RDY/BUSY-RCLK-I/O</td> <td>149</td> <td>I/O</td> <td>97</td> <td>I/O</td> <td>43</td>	I/O	201	RDY/BUSY-RCLK-I/O	149	I/O	97	I/O	43
A11-1/0 199 1/0 147 1/0 96 1/0 197 1/0 146 1/0 93 1/0 196 1/0 144 1/0 93 1/0 196 1/0 144 1/0 93 1/0 193 1/0 144 1/0 92 1/0 193 1/0 144 1/0 92 1/0 191 1/0 144 1/0 92 1/0 191 1/0 139 1/0 88 1/0 189 1/0 135 1/0 84 1/0 188 1/0 134 1/0 82 1/0 186 0/0 131 1/0 81 1/0 28 1/0 186 0/0 127 1/0 80 1/0 28 1/0 181 1/0 122 1/0 77 1/0 28 1/0 176	A8-I/O	200	D1-I/O	148	I/O	96	I/O	42
I/O 198 I/O 146 I/O 94 I/O 196 I/O 145 I/O 94 I/O 196 I/O 144 I/O 92 I/O 194 I/O 144 I/O 92 I/O 193 I/O 144 I/O 88 I/O 191 D2-I/O 138 I/O 88 I/O 192 D2-I/O 138 I/O 86 I/O 188 I/O 137 I/O 81 I/O 188 I/O 132 I/O 81 I/O 188 I/O 132 I/O 81 I/O 184 I/O 122 I/O 76 I/O 181 D4-I/O 128 I/O 77 I/O 177 I/O 124 I/O 71 I/O 174 I/O 124 I/O 71 <t< td=""><td>A11-I/O</td><td>199</td><td>I/O</td><td>147</td><td>I/O</td><td>95</td><td>I/O</td><td>41</td></t<>	A11-I/O	199	I/O	147	I/O	95	I/O	41
I/O 197 I/O 145 I/O 93 I/O 194 I/O 144 I/O 92 I/O 194 I/O 144 I/O 92 I/O 194 I/O 144 I/O 89 I/O 191 I/O 144 I/O 89 I/O 191 I/O 144 I/O 89 I/O 191 I/O 137 I/O 86 I/O 188 I/O 136 I/O 86 I/O 186 I/O 133 I/O 81 I/O 186 I/O 133 I/O 81 I/O 181 GND 131 GND 77 I/O 181 I/O 125 I/O 73 I/O 177 I/O 126 I/O 74 I/O 174 I/O 121 I/O 76 I/O <td>I/O</td> <td>198</td> <td>I/O</td> <td>146</td> <td>I/O</td> <td>94</td> <td>I/O</td> <td>40</td>	I/O	198	I/O	146	I/O	94	I/O	40
$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$	I/O	197	I/O	145	I/O	93	I/O	39
I/O 194 A7-I/O I/O 141 I/O I/O 141 I/O I/O 88 I/O I/O 37 I/O A72-I/O 193 I/O 141 I/O 100 88 I/O I/O 37 I/O 191 D2-I/O 138 I/O I/O 87 I/O 36 I/O 198 I/O 137 I/O 85 I/O 31 I/O 188 I/O 133 I/O 85 I/O 32 I/O 186 D3-I/O 132 I/O 81 I/O 32 I/O 188 I/O 128 I/O 81 I/O 32 I/O 181 D4-I/O 128 I/O 76 I/O 22 I/O 181 I/O 128 I/O 77 I/O 24 I/O 181 I/O 128 I/O 73 I/O 22 I/O 177 I/O 128	I/O	196	I/O	144	I/O	92	I/O	38
A7-VO 193 VO 140 VO 87 A12-VO 193 VO 139 VO 138 VO 87 VO 191 D2-V/O 138 VO 86 VO 35 VO 198 VO 137 VO 86 VO 35 VO 188 VO 137 VO 86 VO 33 VO 187 VO 133 VO 81 VO 32 VO 186 D3-VO 132 VO 80 VO 22 A6-VO 188 VO 122 VO 80 VO 28 A14-VO 188 VO 128 VO 77 VO 24 VO 176 VO 122 VO 74 VO 22 VO 177 VO 122 VO 71 VO 21 VO 177 VO	I/O	194	I/O	141	I/O	89	I/O	37
A12-VO 192 VO 139 VO 87 VO 191 D2-VO 138 VO 87 VO 189 VO 137 VO 86 VO 189 VO 136 VO 86 VO 187 VO 136 VO 84 VO 187 VO 132 VO 84 VO 186 CS1-VO 133 VO 81 VO 186 D3-VO 132 VO 81 VCC 183 VCC 130 VCC 77 VCC 183 VC 132 VO 77 VCC 183 VC 128 VO 78 VO 180 VO 128 VO 74 VO 24 VO 176 CS0-VO 122 VO 71 VO 18 VO 176 D5-VO 122 VO	A7-I/O	193	I/O	140	I/O	88	I/O	36
I/O 191 D2-I/O 138 I/O 86 I/O 189 I/O 137 I/O 86 I/O 188 I/O 136 I/O 86 I/O 188 I/O 135 I/O 83 I/O 186 CS1-I/O 133 I/O 82 I/O 186 CS1-I/O 133 I/O 82 I/O 186 CS1-I/O 132 I/O 80 A6-I/O 185 D3-I/O 132 I/O 80 VCC 183 VCC 130 I/O 80 V/O 181 D4-I/O 128 I/O 76 I/O 174 I/O 122 I/O 76 I/O 174 I/O 122 I/O 71 I/O 174 I/O 174 I/O 18 I/O 177 I/O 122 I/O 71	A12-I/O	192	I/O	139	I/O	87	I/O	35
$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$	I/O	191	D2-I/O	138	I/O	86	I/O	34
VO 189 $ VO $ 136 $ VO $ 84 $ VO $ 187 $ VO $ 136 $ VO $ 83 $ VO $ 186 $ VO $ 133 $ VO $ 83 $ VO $ 186 $ DS /O $ 133 $ VO $ 81 $ VO $ 186 $ DS /O $ 133 $ VO $ 81 $ VO $ 186 $ VO $ 131 $ VO $ 81 $ VO $ 181 $ VO $ 128 $ VO $ 80 $ VO $ 181 $ VO $ 128 $ VO $ 75 $ VO $ 180 $ VO $ 127 $ VO $ 75 $ VO $ 177 $ VO $ 126 $ VO $ 76 $ VO $ 177 $ VO $ 121 $ VO $ 72 $ VO $ 171 $ VO $ 121 $ VO $ 72 $ VO $ 171 $ VO $ 118 $ VO $ 71 $ VO $ 1	I/O	190	I/O	137	I/O	85	I/O	33
IO 188 IO 135 IO 135 IO 31 I/O 187 IO 133 IO 134 IO 82 IO 31 I/O 186 IO 133 IO 82 IO 82 IO 82 A6-I/O 185 D3-I/O 132 IO 81 IO 82 VCC 183 IO 129 VCC 78 IO 76 I/O 180 IO 126 IO 76 IO 76 I/O 180 IO 125 IO 73 IO 72 I/O 177 IO 122 IO 73 IO 22 I/O 177 IO 122 IO 70 IO 22 I/O 171 IO 122 IO 70 IO 13 I/O 166 IO 111 IO 663	I/O	189	I/O	136	I/O	84	I/O	32
$ VO $ 187 $ VO $ 134 $ VO $ 82 $ VO $ 186 $\overline{CS}I \cdot VO $ 133 $ VO $ 81 $A6 \cdot VO $ 185 $D3 \cdot VO $ 131 $ VO $ 81 $VCC $ 183 $OVCC $ 183 $ VO $ 129 $VCC $ 183 $ VO $ 129 $ VO $ 73 $VCC $ 183 $ VO $ 129 $ VO $ 76 $ VO $ 181 $D4 \cdot VO $ 128 $ VO $ 76 $ VO $ 178 $ VO $ 122 $ VO $ 73 $ VO $ 176 $D5 \cdot VO $ 123 $ VO $ 71 $ VO $ 172 $ VO $ 121 $ VO $ 72 $ VO $ 173 $ VO $ 119 $ VO $ 68 $ VO $ 171 $ VO $ 118 $ VO $ 16 $ VO $ 171 $ VO $ 116 $ VO $ 16 $ $	I/O	188	I/O	135	I/O	83	I/O	31
I/O 186 $\overline{CS1}$ -I/O 133 I/O 81 I/O 29 A6-I/O 185 $D3-I/O$ 132 ORD 80 ORD 80 A13-I/O 184 OCC 183 OCC 78 ORD 77 VCC 183 VO 129 VCC 78 I/O 28 I/O 181 VO 129 I/O 75 I/O 24 I/O 180 I/O 126 I/O 74 I/O 24 I/O 178 I/O 122 I/O 74 I/O 21 I/O 176 I/O 123 I/O 71 I/O 21 I/O 176 $D5-I/O$ 122 I/O 71 I/O 18 I/O 171 I/O 112 I/O 66 I/O 11 I/O 116 I/O 116	I/O	187	I/O	134	I/O	82	I/O	30
A6-I/O 185 D3-I/O 132 I/O 80 A13-I/O 184 GND 131 GND 79 VCC 183 V/O 130 V/O 79 VCC 183 V/O 129 V/O 78 I/O 181 V/O 129 V/O 76 I/O 181 V/O 128 V/O 76 I/O 181 V/O 128 V/O 76 V/O 170 V/O 125 V/O 74 V/O 176 V/O 123 V/O 71 V/O 176 D5-V/O 122 V/O 70 V/O 171 V/O 121 V/O 68 V/O 171 V/O 181 V/O 66 V/O 171 V/O 181 V/O 66 V/O 111 V/O 66 V/O 114	I/O	186	CS1-I/O	133	I/O	81	I/O	29
A13-I/O 184 GND 131 GND 79 VCC 183 VCC 130 VCC 78 GND 182 V/O 129 N/O 76 I/O 181 D4-I/O 128 V/O 76 I/O 180 V/O 127 V/O 76 I/O 179 V/O 126 V/O 75 A14-VO 178 V/O 122 V/O 73 V/O 176 CS0-V/O 123 V/O 71 V/O 173 V/O 122 V/O 70 V/O 173 V/O 122 V/O 70 V/O 171 V/O 120 V/O 66 V/O 171 V/O 180 V/O 61 V/O 166 V/O 116 V/O 66 V/O 166 V/O 111 V/O 57	A6-I/O	185	D3-I/O	132	I/O	80	I/O	28
VCC 183 VCC 130 VCC 78 GND 182 I/O 129 I/O 181 VOC 130 I/O 181 UO 129 I/O 76 I/O 25 A5-I/O 179 I/O 127 I/O 74 I/O 23 I/O 177 I/O 123 I/O 73 I/O 21 I/O 176 I/O 123 I/O 71 I/O 19 I/O 171 I/O 121 I/O 70 I/O 19 I/O 173 I/O 110 100 18 I/O 14 I/O 171 I/O 118 I/O 66 I/O 14 I/O 166 I/O 111 I/O 68 I/O 11 I/O 163 I/O 111 I/O 58 I/O 10 I/O 161	A13-I/O	184	GND	131	GND	79	VCC	27
GND 182 I/O 129 INIT 77 I/O 181 D4-I/O 128 I/O 76 I/O 180 I/O 127 I/O 76 A5-I/O 179 I/O 126 I/O 74 I/O 177 I/O 126 I/O 73 I/O 176 I/O 121 I/O 73 I/O 176 CSO-I/O 123 I/O 71 I/O 173 I/O 121 I/O 70 I/O 173 I/O 121 I/O 70 I/O 173 I/O 121 I/O 70 I/O 171 I/O 121 I/O 70 I/O 169 I/O 117 I/O 66 I/O 168 I/O 111 I/O 66 I/O 164 I/O 111 I/O 58	VCC	183	VCC	130	VCC	78	GND	26
I/O 181 D4-I/O 128 I/O 76 I/O 24 I/O 180 I/O 127 I/O 127 I/O 76 I/O 23 A14-I/O 178 I/O 126 I/O 74 I/O 22 A14-I/O 177 I/O 126 I/O 74 I/O 22 I/O 176 I/O 122 I/O 72 I/O 20 I/O 176 D5-I/O 122 I/O 71 I/O 20 I/O 174 I/O 120 I/O 17 I/O 18 I/O 171 I/O 112 I/O 166 I/O 11 I/O 168 I/O 116 I/O 162 I/O 11 I/O 166 I/O 111 I/O 162 I/O 10 I/O 163 I/O 112 I/O 56	GND	182	I/O	129	INIT	77	I/O	25
I/O 180 I/O 127 I/O 75 I/O 75 A5-I/O 179 I/O 126 I/O 74 I/O 22 A14-I/O 177 I/O 126 I/O 74 I/O 22 I/O 176 I/O 123 I/O 71 I/O 20 I/O 176 I/O 123 I/O 71 I/O 20 I/O 174 I/O 121 I/O 70 I/O 19 I/O 171 I/O 112 I/O 66 I/O 17 I/O 169 I/O 118 I/O 66 I/O 12 I/O 166 I/O 116 I/O 166 I/O 11 I/O 163 I/O 113 I/O 10 10 10 I/O 161 I/O 111 I/O 55 I/O 10	I/O	181	D4-I/O	128	I/O	76	I/O	24
A5-I/O 179 A14-I/O 178 I/O 177 I/O 177 I/O 176 I/O 174 I/O 174 I/O 171 I/O 121 I/O 171 I/O 172 I/O 171 I/O 172 I/O 171 I/O 171 I/O 118 I/O 116 I/O 110 I/O	I/O	180	I/O	127	I/O	75	I/O	23
Å14-I/O 178 I/O 125 I/O 177 I/O 124 I/O 176 I/O 124 I/O 176 I/O 124 I/O 176 I/O 123 I/O 174 I/O 121 I/O 174 I/O 121 I/O 173 I/O 121 I/O 173 I/O 121 I/O 173 I/O 120 I/O 171 I/O 120 I/O 171 I/O 119 I/O 168 I/O 116 I/O 166 I/O 114 I/O 165 I/O 114 I/O 165 I/O 114 I/O 166 I/O 111 I/O 161 I/O 110 I/O 162 I/O 111 I/O 161 I/O 102 I/O 162 I/O 103 I/O <	A5-I/O	179	I/O	126	I/O	74	I/O	22
$ VO $ 177 $ VO $ 124 $ VO $ 72 $ VO $ 120 $ VO $ 176 $\overline{CSO} \cdot VO $ 123 $ VO $ 71 $ VO $ 19 $ VO $ 174 $ VO $ 121 $ VO $ 69 $ VO $ 18 $ VO $ 171 $ VO $ 110 $ VO $ 110 $ VO $ 66 $ VO $ 168 $ VO $ 111 $ VO $ 66 $ VO $ 111 $ VO $ 166 $ VO $ 115 $ VO $ 66 $ VO $ 111 $ VO $ 166 $ VO $ 116 $ VO $ 66 $ VO $ 111 $ VO $ 166 $ VO $ 111 $ VO $ 66 $ VO $ 7 $ VO $ 166 $ VO $ 1111 $ VO $ 57 $ VO $ 8 $ VO $ 166 $ VO $ 110 $ VO $ 56 $ VO $ 7 $ VO $ 160 $D7$ $D7$ $D06$ $M2$ <td>A14-I/O</td> <td>178</td> <td>I/O</td> <td>125</td> <td>I/O</td> <td>73</td> <td>I/O</td> <td>21</td>	A14-I/O	178	I/O	125	I/O	73	I/O	21
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $	I/O	177	I/O	124	I/O	72	I/O	20
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $	I/O	176	CS0-I/O	123	I/O	71	I/O	19
I/O 174 A4-I/O 173 A4-I/O 173 A15-I/O 172 I/O 171 I/O 171 I/O 171 I/O 171 I/O 119 I/O 161 I/O 167 I/O 166 I/O 166 I/O 163 I/O 163 I/O 161 I/O 163 I/O 161 I/O 163 I/O 161 I/O 163 I/O 110 I/O 163 I/O 110 I/O 163 I/O 109 A1-CS2-I/O 160 D/P 107 GND 158 VCC 163 VCC 164 D/P 107 D/P 107	I/O	175	D5-I/O	122	I/O	70	I/O	18
A4-I/O 173 I/O 120 A15-I/O 172 I/O 119 I/O 169 I/O 118 I/O 168 I/O 116 I/O 166 I/O 115 A2-I/O 166 I/O 113 I/O 166 I/O 113 I/O 163 I/O 112 I/O 163 I/O 111 I/O 163 I/O 111 I/O 161 I/O 112 I/O 161 I/O 112 I/O 161 I/O 110 I/O 161 I/O 110 I/O 161 I/O 109 D7-I/O 109 D7-I/O 56 I/O 107 108 M2-I/O 54 I/O 159 VCC 106 M0-RTIG 52 VCC 157 GND 104 I/	I/O	174	I/O	121	I/O	69	I/O	17
A15-I/O 172 I/O 171 I/O 169 I/O 169 I/O 168 I/O 167 I/O 166 I/O 166 I/O 165 I/O 165 I/O 163 I/O 163 I/O 161 I/O 162 I/O 161 I/O 162 I/O 111 I/O 162 I/O 111 I/O 163 I/O 111 I/O 164 I/O 111 I/O 163 I/O 111 I/O 164 I/O 111 I/O 165 I/O 109 MO-WS-I/O	A4-I/O	173	I/O	120	I/O	68	I/O	14
I/O 171 I/O 169 I/O 169 I/O 168 I/O 167 I/O 166 A3-I/O 166 A2-I/O 165 I/O 114 I/O 163 I/O 111 I/O 163 I/O 161 I/O 109 M1/DC-I/O 55 I/O 108 D/P 107 VCC 106 NO-WS-I/O 159 D/P 107 VCC 106 RESET 105 GND 104 V/O 49	A15-I/O	172	I/O	119	I/O	67	I/O	13
I/O 169 I/O 117 I/O 168 I/O 167 A3-I/O 166 A2-I/O 165 I/O 114 I/O 113 I/O 161 I/O 113 I/O 163 I/O 114 I/O 163 I/O 113 I/O 163 I/O 111 I/O 163 I/O 111 I/O 163 I/O 111 I/O 161 I/O 111 I/O 163 I/O 111 I/O 163 I/O 111 I/O 56 I/O 109 M1/ED-I/O 55 I/O 4 M2-I/O 54 D/P 107 VCC 106 M0-RTIG 52 GND 50 VCC	I/O	171	I/O	118	I/O	66	I/O	12
I/O 168 I/O 167 I/O 167 A3-I/O 166 I/O 115 D6-I/O 114 I/O 165 I/O 165 I/O 163 I/O 163 I/O 111 I/O 163 I/O 111 I/O 163 I/O 111 I/O 161 I/O 111 I/O 161 I/O 111 I/O 163 I/O 110 I/O 163 I/O 110 XTLX1(OUT)BCLKN-I/O 109 M1/C 55 I/O 4 I/O 55 I/O 3 A1-CS2-I/O 160 D/P 107 VCC 106 MO-RTIG 52 GND 51 VCC 103 VCC 103	I/O	169	I/O	117	I/O	63	I/O	11
I/O 167 A3-I/O 166 A2-I/O 165 I/O 114 I/O 165 I/O 164 I/O 163 I/O 163 I/O 163 I/O 163 I/O 111 I/O 59 I/O 161 I/O 111 I/O 56 I/O 109 M1/O 56 I/O 109 M1/O 56 I/O 109 M1/O 56 I/O 3 A1-CS2-I/O 160 D/P 107 VCC 108 VCC 106 M0-WS-I/O 159 VCC 106 RESET 105 GND 50 VCC 103 I/O 49	I/O	168	I/O	116	I/O	62	I/O	10
A3-I/O 166 A2-I/O 165 I/O 165 I/O 164 I/O 164 I/O 163 I/O 163 I/O 163 I/O 163 I/O 161 I/O 111 I/O 161 I/O 110 XTLX1(OUT)BCLKN-I/O 109 M1/C 55 I/O 160 XTLX1(OUT)BCLKN-I/O 109 M2-I/O 54 D/P 107 VCC 106 MO-WS-I/O 159 O/P 107 VCC 106 M0-RTIG 52 GND 51 VCC 103 M1/RDATA 50 VCC 207	I/O	167	I/O	115	I/O	61	I/O	9
A2-I/O 165 I/O 113 I/O 164 I/O 163 I/O 163 I/O 163 I/O 161 I/O 161 I/O 161 I/O 161 I/O 161 I/O 109 M1/CO 55 I/O 160 M1/O 160 M1/O 109 M1/CO 55 I/O 3 M2-I/O 54 D/P 107 VCC 106 MO-WS-I/O 159 VCC 106 MO-WS-I/O 159 VCC 106 MO-RTIG 52 GND 51 VCC 207 CCLK 156 DOUT-I/O 153	A3-I/O	166	D6-I/O	114	I/O	60	I/O	8
I/O 164 I/O 163 I/O 163 I/O 163 I/O 162 I/O 161 I/O 161 I/O 161 I/O 160 I/O 161 XTLX1(OUT)BCLKN-I/O 109 M1/CD-I/O 55 I/O 3 M2-I/O 54 D/P 107 VCC 106 MO-WS-I/O 159 VCC 106 VCC 106 RESET 105 GND 51 VCC 207 CCLK 156 DOUT-I/O 103	A2-I/O	165	I/O	113	LDC-I/O	59	I/O	7
I/O 163 I/O 111 I/O 162 I/O 161 I/O 161 I/O 161 XTLX1(OUT)BCLKN-I/O 109 D7-I/O 108 D7-I/O 108 D/P 107 VCC 159 VCC 106 VCC 106 NO-WS-I/O 159 VCC 106 MO-RTIG 52 GND 154 VCC 106 M0-RTIG 52 GND 104 M1/RDATA 50 VCC 103	I/O	164	I/O	112	I/O	58	I/O	6
I/O 162 I/O 161 I/O 161 I/O 161 XTLX1(OUT)BCLKN-I/O 109 A1-CS2-I/O 160 A0-WS-I/O 159 GND 158 VCC 106 NCC 106 MO-RTIG 52 OLK 156 GND 104 M1/RDATA 50 DOUT-I/O 103	I/O	163	I/O	111	I/O	57	I/O	5
I/O 161 XTLX1(0UT)BCLKN-I/O 109 HDC-I/O 55 A1-CS2-I/O 160 D7-I/O 108 M2-I/O 54 A0-WS-I/O 159 D/P 107 VCC 53 GND 158 VCC 106 M0-RTIG 52 VCC 157 RESET 105 GND 51 DOUT-I/O 155 XTL2(IN)-I/O 103 I/O 49	I/O	162	I/O	110	I/O	56	I/O	4
A1-CS2-I/O 160 A0-WS-I/O 159 GND 158 VCC 106 RESET 105 GND 157 CCLK 156 DUP-I/O 104 M1/RDATA 50 VCC 103	I/O	161	XTLX1(OUT)BCLKN-I/O	109	HDC-I/O	55	I/O	3
A0-WS-I/O 159 GND 158 VCC 106 NCC 105 RESET 105 GND 157 CCLK 156 DOUT-I/O 155	A1-CS2-I/O	160	D7-I/O	108	M2-I/O	54	TCLKIN-I/O	2
GND 158 VCC 106 M0-RTIG 52 GND 208 VCC 157 RESET 105 GND 51 VCC 207 CCLK 156 GND 104 M1/RDATA 50 VCC 207 DOUT-I/O 155 XTL2(IN)-I/O 103 I/O 49 VCC 208	A0-WS-I/O	159	D/P	107	VCC	53	PWRDN	1
VCC 157 RESET 105 GND 51 VCC 207 CCLK 156 GND 104 M1/RDATA 50 VCC 207 DOUT-I/O 155 XTL2(IN)-I/O 103 I/O 49 VCC 207	GND	158	VCC	106	M0-RTIG	52	GND	208
CCLK 156 GND 104 M1/RDATA 50 DOUT-I/O 155 XTL2(IN)-I/O 103 I/O 49	VCC	157	RESET	105	GND	51	VCC	207
DOUT-I/O 155 XTL2(IN)-I/O 103 I/O 49	CCLK	156	GND	104	M1/RDATA	50		
	DOUT-I/O	155	XTL2(IN)-I/O	103	I/O	49		

Unprogrammed IOBs have a default pull-up. This prevents an undefined pad level for unbonded or unused IOBs. Programmed outputs are default slew-rate limited.

In the PQ208 package, pins 15, 16, 64, 65, 90, 91, 142, 143, 170 and 195 are not connected. * In PQ208, XC3090A and XC3195A have different pinouts.

XILINX[®]