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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	320
Number of Logic Elements/Cells	-
Total RAM Bits	64160
Number of I/O	144
Number of Gates	6000
Voltage - Supply	4.75V ~ 5.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	176-LQFP
Supplier Device Package	176-TQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc3090a-7tq176c

The input-buffer portion of each IOB provides threshold detection to translate external signals applied to the package pin to internal logic levels. The global input-buffer threshold of the IOBs can be programmed to be compatible with either TTL or CMOS levels. The buffered input signal drives the data input of a storage element, which may be configured as either a flip-flop or a latch. The clocking polarity (rising/falling edge-triggered flip-flop, High/Low transparent latch) is programmable for each of the two clock lines on each of the four die edges. Note that a clock line driving a *rising* edge-triggered flip-flop makes any latch driven by the same line on the same edge Low-level transparent and vice versa (*falling* edge, *High* transparent). All Xilinx primitives in the supported schematic-entry packages, however, are positive edge-triggered flip-flops or High transparent latches. When one clock line must drive flip-flops as well as latches, it is necessary to compensate for the difference in clocking polarities with an additional inverter either in the flip-flop clock input or the latch-enable input. I/O storage elements are reset during configuration or by the active-Low chip $\overline{\text{RESET}}$ input. Both direct input (from IOB pin I) and registered input (from IOB pin Q) signals are available for interconnect.

For reliable operation, inputs should have transition times of less than 100 ns and should not be left floating. Floating CMOS input-pin circuits might be at threshold and produce oscillations. This can produce additional power dissipation and system noise. A typical hysteresis of about 300 mV reduces sensitivity to input noise. Each user IOB includes a programmable high-impedance pull-up resistor, which may be selected by the program to provide a constant High for otherwise undriven package pins. Although the Field Programmable Gate Array provides circuitry to provide input protection for electrostatic discharge, normal CMOS handling precautions should be observed.

Flip-flop loop delays for the IOB and logic-block flip-flops are short, providing good performance under asynchronous clock and data conditions. Short loop delays minimize the probability of a metastable condition that can result from assertion of the clock during data transitions. Because of the short-loop-delay characteristic in the Field Programmable Gate Array, the IOB flip-flops can be used to synchronize external signals applied to the device. Once synchronized in the IOB, the signals can be used internally without further consideration of their clock relative timing, except as it applies to the internal logic and routing-path delays.

IOB output buffers provide CMOS-compatible 4-mA source-or-sink drive for high fan-out CMOS or TTL- compatible signal levels (8 mA in the XC3100A family). The network driving IOB pin O becomes the registered or direct data source for the output buffer. The 3-state control signal (IOB) pin T can control output activity. An open-drain output may be obtained by using the same signal for driving the output and 3-state signal nets so that the buffer output is enabled only for a Low.

Configuration program bits for each IOB control features such as optional output register, logic signal inversion, and 3-state and slew-rate control of the output.

The program-controlled memory cells of Figure 4 control the following options.

- Logic inversion of the output is controlled by one configuration program bit per IOB.
- Logic 3-state control of each IOB output buffer is determined by the states of configuration program bits that turn the buffer on, or off, or select the output buffer 3-state control interconnection (IOB pin T). When this IOB output control signal is High, a logic one, the buffer is disabled and the package pin is high impedance. When this IOB output control signal is Low, a logic zero, the buffer is enabled and the package pin is active. Inversion of the buffer 3-state control-logic sense (output enable) is controlled by an additional configuration program bit.
- Direct or registered output is selectable for each IOB. The register uses a positive-edge, clocked flip-flop. The clock source may be supplied (IOB pin OK) by either of two metal lines available along each die edge. Each of these lines is driven by an invertible buffer.
- Increased output transition speed can be selected to improve critical timing. Slower transitions reduce capacitive-load peak currents of non-critical outputs and minimize system noise.
- An internal high-impedance pull-up resistor (active by default) prevents unconnected inputs from floating.

Unlike the original XC3000 series, the XC3000A, XC3000L, XC3100A, and XC3100L families include the Soft Startup feature. When the configuration process is finished and the device starts up in user mode, the first activation of the outputs is automatically slew-rate limited. This feature avoids potential ground bounce when all outputs are turned on simultaneously. After start-up, the slew rate of the individual outputs is determined by the individual configuration option.

Summary of I/O Options

- Inputs
  - Direct
  - Flip-flop/latch
  - CMOS/TTL threshold (chip inputs)
  - Pull-up resistor/open circuit
- Outputs
  - Direct/registered
  - Inverted/not
  - 3-state/on/off
  - Full speed/slew limited
  - 3-state/output enable (inverse)

Configurable Logic Block

The array of CLBs provides the functional elements from which the user's logic is constructed. The logic blocks are arranged in a matrix within the perimeter of IOBs. For example, the XC3020A has 64 such blocks arranged in 8 rows and 8 columns. The development system is used to compile the configuration data which is to be loaded into the internal configuration memory to define the operation and interconnection of each block. User definition of CLBs and their interconnecting networks may be done by automatic translation from a schematic-capture logic diagram or optionally by installing library or user macros.

Each CLB has a combinatorial logic section, two flip-flops, and an internal control section. See Figure 5. There are: five logic inputs (A, B, C, D and E); a common clock input (K); an asynchronous direct RESET input (RD); and an enable clock (EC). All may be driven from the interconnect resources adjacent to the blocks. Each CLB also has two outputs (X and Y) which may drive interconnect networks.

Data input for either flip-flop within a CLB is supplied from the function F or G outputs of the combinatorial logic, or the block input, DI. Both flip-flops in each CLB share the asynchronous RD which, when enabled and High, is dominant over clocked inputs. All flip-flops are reset by the active-Low chip input, RESET, or during the configuration process. The flip-flops share the enable clock (EC) which, when Low, recirculates the flip-flops' present states and inhibits response to the data-in or combinatorial function inputs on a CLB. The user may enable these control inputs and select their sources. The user may also select the clock net input (K), as well as its active sense within each CLB. This programmable inversion eliminates the need to route both phases of a clock signal throughout the device.

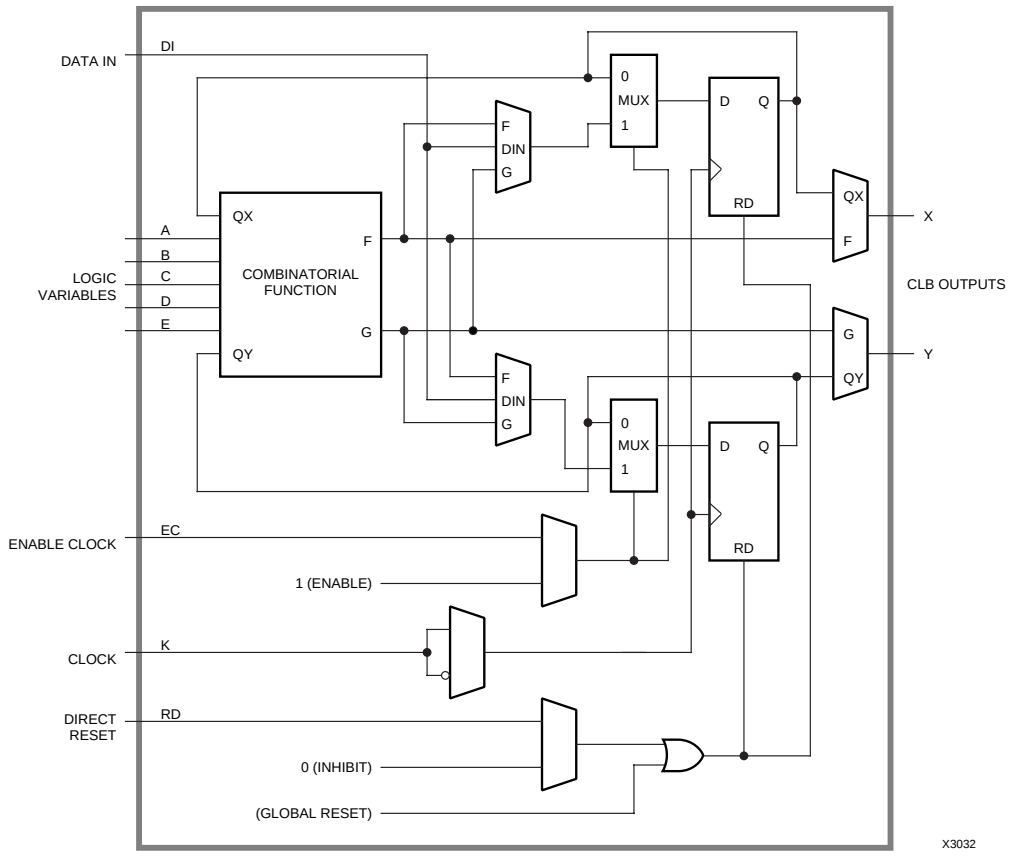

Figure 5: Configurable Logic Block.

Each CLB includes a combinatorial logic section, two flip-flops and a program memory controlled multiplexer selection of function. It has the following:

- five logic variable inputs A, B, C, D, and E
- a direct data in DI
- an enable clock EC
- a clock (invertible) K
- an asynchronous direct RESET RD
- two outputs X and Y

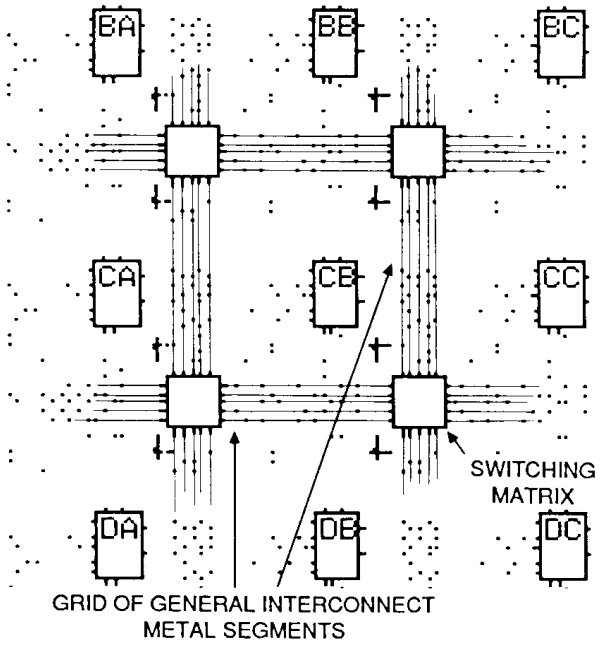

Figure 10: FPGA General-Purpose Interconnect.
Composed of a grid of metal segments that may be interconnected through switch matrices to form networks for CLB and IOB inputs and outputs.

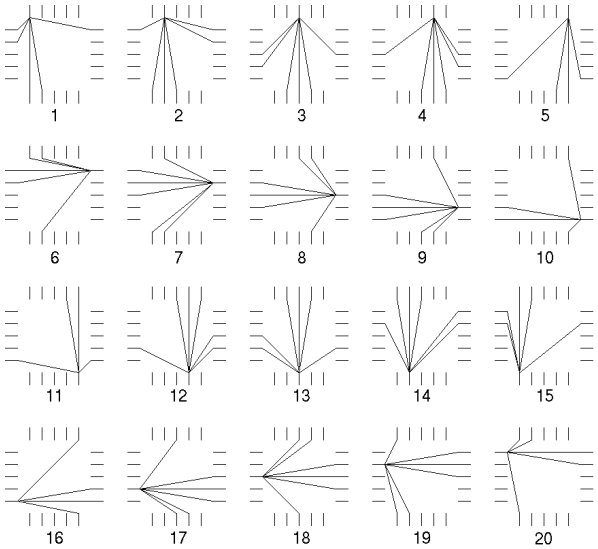

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Figure 11: Switch Matrix Interconnection Options for Each Pin.
Switch matrices on the edges are different.

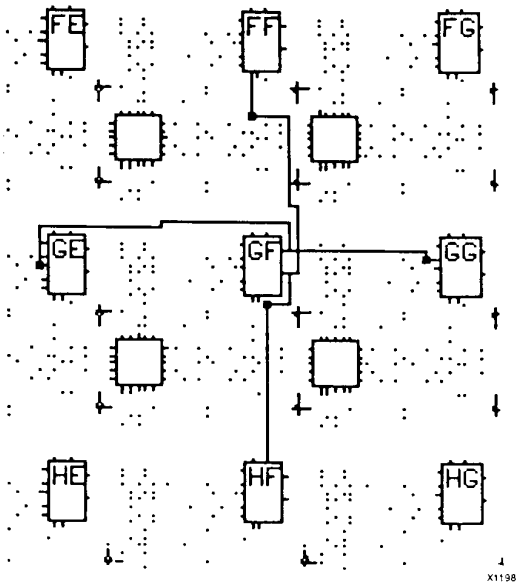

Figure 12: CLB X and Y Outputs.
The X and Y outputs of each CLB have single contact, direct access to inputs of adjacent CLBs

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Longlines

The Longlines bypass the switch matrices and are intended primarily for signals that must travel a long distance, or must have minimum skew among multiple destinations. Longlines, shown in Figure 14, run vertically and horizontally the height or width of the interconnect area. Each interconnection column has three vertical Longlines, and each interconnection row has two horizontal Longlines. Two additional Longlines are located adjacent to the outer sets of switching matrices. In devices larger than the XC3020A and XC3120A FPGAs, two vertical Longlines in each column are connectable half-length lines. On the XC3020A and XC3120A FPGAs, only the outer Longlines are connectable half-length lines.

Longlines can be driven by a logic block or IOB output on a column-by-column basis. This capability provides a common low skew control or clock line within each column of logic blocks. Interconnections of these Longlines are shown in Figure 15. Isolation buffers are provided at each input to a Longline and are enabled automatically by the development system when a connection is made.

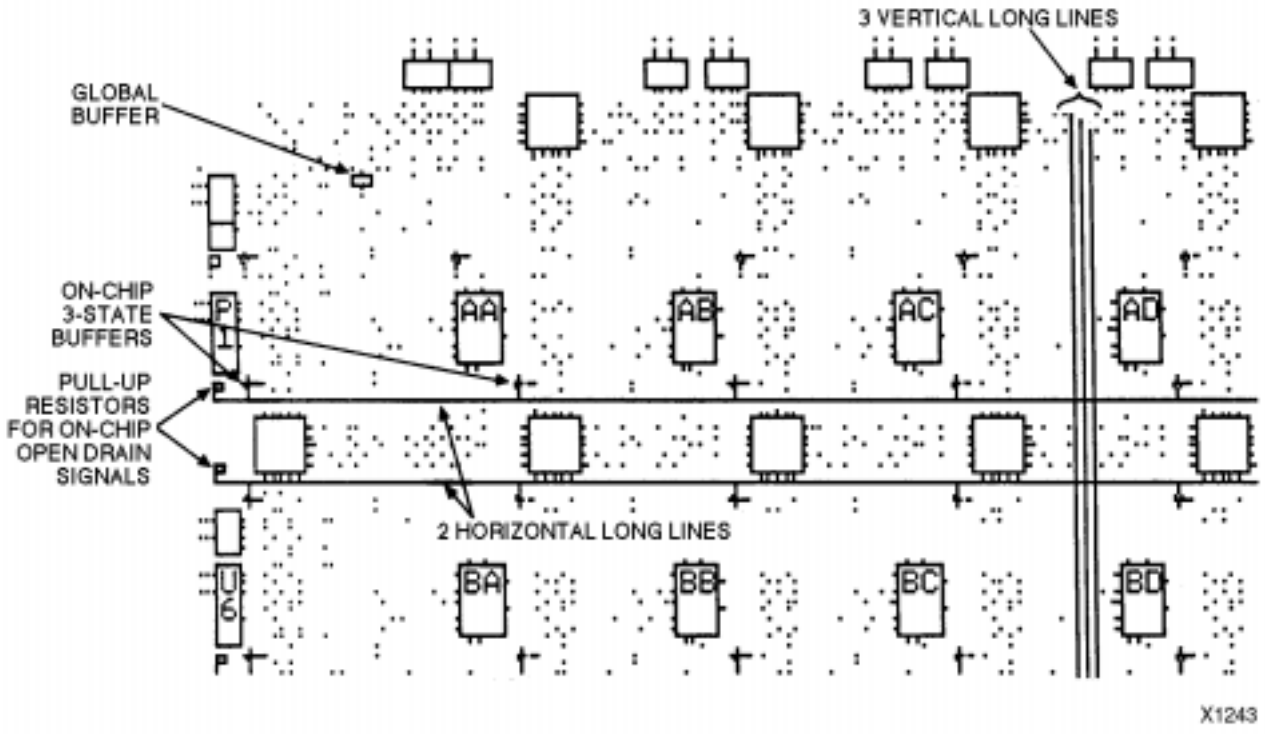

Figure 14: Horizontal and Vertical Longlines. These Longlines provide high fan-out, low-skew signal distribution in each row and column. The global buffer in the upper left die corner drives a common line throughout the FPGA.

A buffer in the upper left corner of the FPGA chip drives a global net which is available to all K inputs of logic blocks. Using the global buffer for a clock signal provides a skew-free, high fan-out, synchronized clock for use at any or all of the IOBs and CLBs. Configuration bits for the K input to each logic block can select this global line or another routing resource as the clock source for its flip-flops. This net may also be programmed to drive the die edge clock lines for IOB use. An enhanced speed, CMOS threshold, direct access to this buffer is available at the second pad from the top of the left die edge.

A buffer in the lower right corner of the array drives a horizontal Longline that can drive programmed connections to a vertical Longline in each interconnection column. This alternate buffer also has low skew and high fan-out. The network formed by this alternate buffer's Longlines can be selected to drive the K inputs of the CLBs. CMOS threshold, high speed access to this buffer is available from the third pad from the bottom of the right die edge.

Internal Busses

A pair of 3-state buffers, located adjacent to each CLB, permits logic to drive the horizontal Longlines. Logic operation of the 3-state buffer controls allows them to implement wide multiplexing functions. Any 3-state buffer input can be selected as drive for the horizontal long-line bus by applying a Low logic level on its 3-state control line. See Figure 16. The user is required to avoid contention which can result from multiple drivers with opposing logic levels. Control of the 3-state input by the same signal that drives the buffer input, creates an open-drain wired-AND function. A logic High on both buffer inputs creates a high impedance, which represents no contention. A logic Low enables the buffer to drive the Longline Low. See Figure 17. Pull-up resistors are available at each end of the Longline to provide a High output when all connected buffers are non-conducting. This forms fast, wide gating functions. When data drives the inputs, and separate signals drive the 3-state control lines, these buffers form multiplexers (3-state busses). In this case, care must be used to prevent contention through multiple active buffers of conflicting levels on a common line. Each horizontal Longline is also driven by a weak keeper circuit that prevents undefined floating levels by maintaining the previous logic level when the line is not driven by an active buffer or a pull-up resistor. Figure 18 shows 3-state buffers, Longlines and pull-up resistors.

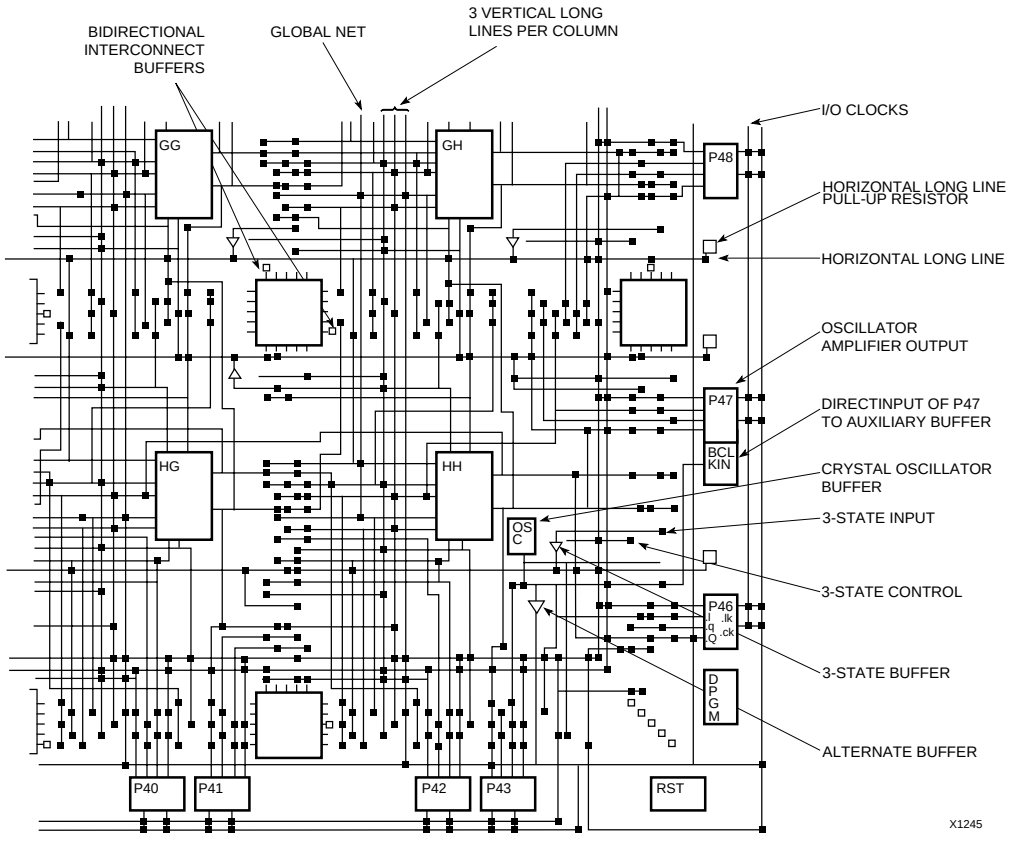

Figure 18: Design Editor.
An extra large view of possible interconnections in the lower right corner of the XC3020A.

Master Parallel Mode

In Master Parallel mode, the lead FPGA directly addresses an industry-standard byte-wide EPROM and accepts eight data bits right before incrementing (or decrementing) the address outputs.

The eight data bits are serialized in the lead FPGA, which then presents the preamble data (and all data that overflows the lead device) on the DOUT pin. There is an internal delay of 1.5 CCLK periods, after the rising CCLK edge that accepts a byte of data, and also changes the EPROM address, until the falling CCLK edge that makes the LSB (D0) of this byte appear at DOUT. This means that DOUT changes on the falling CCLK edge, and the next device in the daisy chain accepts data on the subsequent rising CCLK edge.

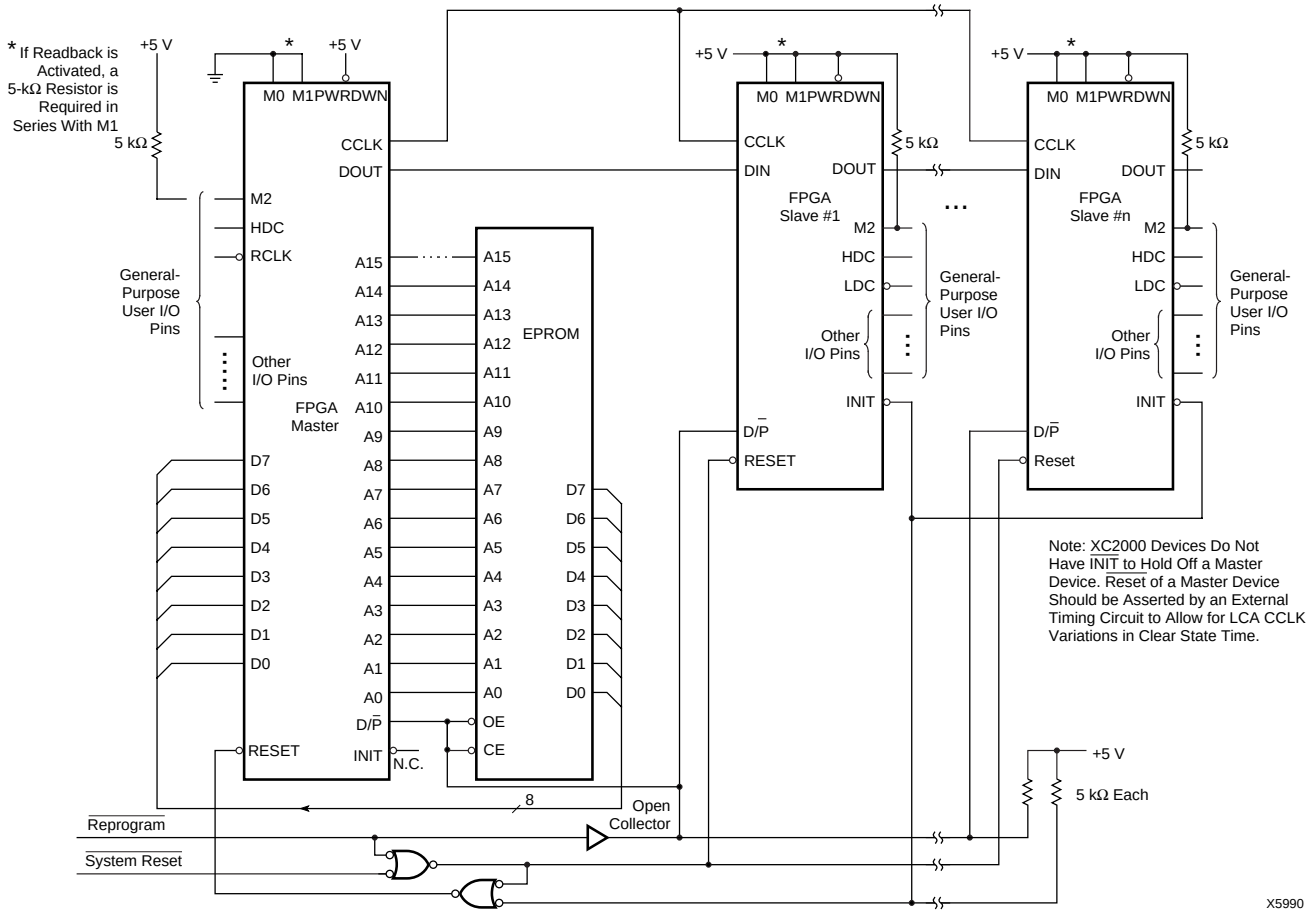

Figure 25: Master Parallel Mode Circuit Diagram

Pin Descriptions

Permanently Dedicated Pins

V_{CC}

Two to eight (depending on package type) connections to the positive V supply voltage. All must be connected.

GND

Two to eight (depending on package type) connections to ground. All must be connected.

$\overline{\text{PWRDWN}}$

A Low on this CMOS-compatible input stops all internal activity, but retains configuration. All flip-flops and latches are reset, all outputs are 3-stated, and all inputs are interpreted as High, independent of their actual level. When $\overline{\text{PWDWN}}$ returns High, the FPGA becomes operational with DONE Low for two cycles of the internal 1-MHz clock. Before and during configuration, $\overline{\text{PWRDWN}}$ must be High. If not used, $\overline{\text{PWRDWN}}$ must be tied to V_{CC}.

$\overline{\text{RESET}}$

This is an active Low input which has three functions.

Prior to the start of configuration, a Low input will delay the start of the configuration process. An internal circuit senses the application of power and begins a minimal time-out cycle. When the time-out and $\overline{\text{RESET}}$ are complete, the levels of the M lines are sampled and configuration begins.

If $\overline{\text{RESET}}$ is asserted during a configuration, the FPGA is re-initialized and restarts the configuration at the termination of $\overline{\text{RESET}}$.

If $\overline{\text{RESET}}$ is asserted after configuration is complete, it provides a global asynchronous $\overline{\text{RESET}}$ of all IOB and CLB storage elements of the FPGA.

CCLK

During configuration, Configuration Clock is an output of an FPGA in Master mode or Peripheral mode, but an input in Slave mode. During Readback, CCLK is a clock input for shifting configuration data out of the FPGA.

CCLK drives dynamic circuitry inside the FPGA. The Low time may, therefore, not exceed a few microseconds. When used as an input, CCLK must be “parked High”. An internal pull-up resistor maintains High when the pin is not being driven.

DONE/$\overline{\text{PROG}}$ (D/$\overline{\text{P}}$)

DONE is an open-drain output, configurable with or without an internal pull-up resistor of 2 to 8 k Ω. At the completion of configuration, the FPGA circuitry becomes active in a synchronous order; DONE is programmed to go active High one cycle either before or after the outputs go active.

Once configuration is done, a High-to-Low transition of this pin will cause an initialization of the FPGA and start a reconfiguration.

M0/RTRIG

As Mode 0, this input is sampled on power-on to determine the power-on delay (2^{14} cycles if M0 is High, 2^{16} cycles if M0 is Low). Before the start of configuration, this input is again sampled together with M1, M2 to determine the configuration mode to be used.

A Low-to-High input transition, after configuration is complete, acts as a Read Trigger and initiates a Readback of configuration and storage-element data clocked by CCLK. By selecting the appropriate Readback option when generating the bitstream, this operation may be limited to a single Readback, or be inhibited altogether.

M1/$\overline{\text{RDATA}}$

As Mode 1, this input and M0, M2 are sampled before the start of configuration to establish the configuration mode to be used. If Readback is never used, M1 can be tied directly to ground or V_{CC}. If Readback is ever used, M1 must use a 5-kΩ resistor to ground or V_{CC}, to accommodate the RDATA output.

As an active-Low Read Data, after configuration is complete, this pin is the output of the Readback data.

User I/O Pins That Can Have Special Functions

M2

During configuration, this input has a weak pull-up resistor. Together with M0 and M1, it is sampled before the start of configuration to establish the configuration mode to be used. After configuration, this pin is a user-programmable I/O pin.

HDC

During configuration, this output is held at a High level to indicate that configuration is not yet complete. After configuration, this pin is a user-programmable I/O pin.

$\overline{\text{LDC}}$

During Configuration, this output is held at a Low level to indicate that the configuration is not yet complete. After configuration, this pin is a user-programmable I/O pin. $\overline{\text{LDC}}$ is particularly useful in Master mode as a Low enable for an EPROM, but it must then be programmed as a High after configuration.

$\overline{\text{INIT}}$

This is an active Low open-drain output with a weak pull-up and is held Low during the power stabilization and internal clearing of the configuration memory. It can be used to indicate status to a configuring microprocessor or, as a wired

AND of several slave mode devices, a hold-off signal for a master mode device. After configuration this pin becomes a user-programmable I/O pin.

BCLKIN

This is a direct CMOS level input to the alternate clock buffer (Auxiliary Buffer) in the lower right corner.

XTL1

This user I/O pin can be used to operate as the output of an amplifier driving an external crystal and bias circuitry.

XTL2

This user I/O pin can be used as the input of an amplifier connected to an external crystal and bias circuitry. The I/O Block is left unconfigured. The oscillator configuration is activated by routing a net from the oscillator buffer symbol output and by the MakeBits program.

$\overline{CS0}$, $\overline{CS1}$, CS2, $\overline{WS}$

These four inputs represent a set of signals, three active Low and one active High, that are used to control configuration-data entry in the Peripheral mode. Simultaneous assertion of all four inputs generates a Write to the internal data buffer. The removal of any assertion clocks in the D0-D7 data. In Master-Parallel mode, WS and CS2 are the A0 and A1 outputs. After configuration, these pins are user-programmable I/O pins.

RDY/$\overline{BUSY}$

During Peripheral Parallel mode configuration this pin indicates when the chip is ready for another byte of data to be written to it. After configuration is complete, this pin becomes a user-programmed I/O pin.

$\overline{RCLK}$

During Master Parallel mode configuration, each change on the A0-15 outputs is preceded by a rising edge on $\overline{RCLK}$, a redundant output signal. After configuration is complete, this pin becomes a user-programmed I/O pin.

D0-D7

This set of eight pins represents the parallel configuration byte for the parallel Master and Peripheral modes. After configuration is complete, they are user-programmed I/O pins.

A0-A15

During Master Parallel mode, these 16 pins present an address output for a configuration EPROM. After configuration, they are user-programmable I/O pins.

DIN

During Slave or Master Serial configuration, this pin is used as a serial-data input. In the Master or Peripheral configuration, this is the Data 0 input. After configuration is complete, this pin becomes a user-programmed I/O pin.

DOUT

During configuration this pin is used to output serial-configuration data to the DIN pin of a daisy-chained slave. After configuration is complete, this pin becomes a user-programmed I/O pin.

TCLKIN

This is a direct CMOS-level input to the global clock buffer. This pin can also be configured as a user programmable I/O pin. However, since TCLKIN is the preferred input to the global clock net, and the global clock net should be used as the primary clock source, this pin is usually the clock input to the chip.

Unrestricted User I/O Pins

I/O

An I/O pin may be programmed by the user to be an Input or an Output pin following configuration. All unrestricted I/O pins, plus the special pins mentioned on the following page, have a weak pull-up resistor that becomes active as soon as the device powers up, and stays active until the end of configuration.

Note: *Before and during configuration, all outputs that are not used for the configuration process are 3-stated with a weak pull-up resistor.*

XC3000A CLB Switching Characteristics Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Since many internal timing parameters cannot be measured directly, they are derived from benchmark timing patterns. The following guidelines reflect worst-case values over the recommended operating conditions. For more detailed, more precise, and more up-to-date timing information, use the values provided by the timing calculator and used in the simulator.

		Speed Grade		-7		-6		
Description		**Symbol**		**Min**	**Max**	**Min**	**Max**	**Units**
Combinatorial Delay								
Logic Variables	A, B, C, D, E, to outputs X or Y							
	FG Mode	1	T_{ILO}		5.1		4.1	ns
	F and FGM Mode				5.6		4.6	ns
Sequential delay								
Clock k to outputs X or Y		8	T_{CKO}		4.5		4.0	ns
Clock k to outputs X or Y when Q is returned through function generators F or G to drive X or Y								
	FG Mode		T_{QLO}		9.5		8.0	ns
	F and FGM Mode				10.0		8.5	ns
Set-up time before clock K								
Logic Variables	A, B, C, D, E							
	FG Mode	2	T_{ICK}	4.5		3.5		ns
	F and FGM Mode			5.0		4.0		ns
Data In	DI	4	T_{DICK}	4.0		3.0		ns
Enable Clock	EC	6	T_{ECCK}	4.5		4.0		ns
Hold Time after clock K								
Logic Variables	A, B, C, D, E	3	T_{CKI}	0		0		ns
Data In	DI[2]	5	T_{CKDI}	1.0		1.0		ns
Enable Clock	EC	7	T_{CKEC}	2.0		2.0		ns
Clock								
Clock High time		11	T_{CH}	4.0		3.5		ns
Clock Low time		12	T_{CL}	4.0		3.5		ns
Max. flip-flop toggle rate			F_{CLK}	113.0		135.0		MHz
Reset Direct (RD)								
RD width		13	T_{RPW}	6.0		5.0		ns
delay from RD to outputs X or Y		9	T_{RIO}		6.0		5.0	ns
Global Reset ($\overline{\text{RESET}}$ Pad)[1]								
$\overline{\text{RESET}}$ width (Low)			T_{MRW}	16.0		14.0		ns
delay from $\overline{\text{RESET}}$ pad to outputs X or Y			T_{MRQ}		19.0		17.0	ns

Notes: 1. Timing is based on the XC3042A, for other devices see timing calculator.
2. The CLB K to Q output delay (T_{CKO}, #8) of any CLB, plus the shortest possible interconnect delay, is always longer than the Data In hold time requirement (T_{CKDI}, #5) of any CLB on the same die.

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XC3000L Switching Characteristics

Xilinx maintains test specifications for each product as controlled documents. To insure the use of the most recently released device performance parameters, please request a copy of the current test-specification revision.

XC3000L Operating Conditions

Symbol	Description	Min	Max	Units
V_{CC}	Supply voltage relative to GND Commercial 0°C to +85°C junction	3.0	3.6	V
V_{IH}	High-level input voltage — TTL configuration	2.0	V_{CC}+0.3	V
V_{IL}	Low-level input voltage — TTL configuration	-0.3	0.8	V
T_{IN}	Input signal transition time		250	ns

Notes: 1. At junction temperatures above those listed as Operating Conditions, all delay parameters increase by 0.3% per °C.
2. Although the present (1996) devices operate over the full supply voltage range from 3.0 to 5.25 V, Xilinx reserves the right to restrict operation to the 3.0 to 3.6 V range later, when smaller device geometries might preclude operation at 5V. Operating conditions are guaranteed in the 3.0 – 3.6 V V_{CC} range.

XC3000L DC Characteristics Over Operating Conditions

Symbol	Description	Min	Max	Units
V_{OH}	High-level output voltage (@ I_{OH} = –4.0 mA, V_{CC} min)	2.40		V
V_{OL}	Low-level output voltage (@ I_{OL} = 4.0 mA, V_{CC} min)		0.40	V
V_{OH}	High-level output voltage (@ I_{OH} = –4.0 mA, V_{CC} min)	V_{CC} -0.2		V
V_{OL}	Low-level output voltage (@ I_{OL} = 4.0 mA, V_{CC} min)		0.2	V
V_{CCPD}	Power-down supply voltage (PWRDWN must be Low)	2.30		V
I_{CCPD}	Power-down supply current ($V_{CC(MAX)}$ @ T_{MAX})		10	µA
I_{CCO}	Quiescent FPGA supply current in addition to I_{CCPD}[1] Chip thresholds programmed as CMOS levels		 20	 µA
I_{IL}	Input Leakage Current	–10	+10	µA
C_{IN}	Input capacitance, all packages except PGA175 (sample tested) All Pins except XTL1 and XTL2 XTL1 and XTL2		 10 15	 pF pF
	Input capacitance, PGA 175 (sample tested) All Pins except XTL1 and XTL2 XTL1 and XTL2		 15 20	 pF pF
I_{RIN}	Pad pull-up (when selected) @ V_{IN} = 0 V[3]	0.01	0.17	mA
I_{RLL}	Horizontal Longline pull-up (when selected) @ logic Low		2.50	mA

Notes: 1. With no output current loads, no active input or Longline pull-up resistors, all package pins at V_{CC} or GND, and the FPGA device configured with a tie option. I_{CCO} is in addition to I_{CCPD}.
2. Total continuous output sink current may not exceed 100 mA per ground pin. Total continuous output source may not exceed 100 mA per V_{CC} pin. The number of ground pins varies from the XC3020L to the XC3090L.
3. Not tested. Allows an undriven pin to float High. For any other purpose, use an external pull-up.

XC3000L Absolute Maximum Ratings

Symbol	Description		Units
V_{CC}	Supply voltage relative to GND	–0.5 to +7.0	V
V_{IN}	Input voltage with respect to GND	–0.5 to V_{CC} +0.5	V
V_{TS}	Voltage applied to 3-state output	–0.5 to V_{CC} +0.5	V
T_{STG}	Storage temperature (ambient)	–65 to +150	°C
T_{SOL}	Maximum soldering temperature (10 s @ 1/16 in.)	+260	°C
T_J	Junction temperature plastic	+125	°C
	Junction temperature ceramic	+150	°C

Note: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

XC3000L Global Buffer Switching Characteristics Guidelines

	Speed Grade	-8	
Description	**Symbol**	**Max**	**Units**
Global and Alternate Clock Distribution[1]			
Either: **Normal** IOB input pad through clock buffer to any CLB or IOB clock input	T_{PID}	9.0	ns
Or: **Fast** (CMOS only) input pad through clock buffer to any CLB or IOB clock input	T_{PIDC}	7.0	ns
TBUF driving a Horizontal Longline (L.L.)[1]			
I to L.L. while T is Low (buffer active)	T_{IO}	5.0	ns
T↓ to L.L. active and valid with single pull-up resistor	T_{ON}	12.0	ns
T↑ to L.L. High with single pull-up resistor	T_{PUS}	24.0	ns
BIDI			
Bidirectional buffer delay	T_{BIDI}	2.0	ns

Notes: 1. Timing is based on the XC3042A, for other devices see timing calculator.
2. The use of two pull-up resistors per Longline, available on other XC3000 devices, is not a valid option for XC3000L devices.

XC3100A Switching Characteristics

Xilinx maintains test specifications for each product as controlled documents. To insure the use of the most recently released device performance parameters, please request a copy of the current test-specification revision.

XC3100A Operating Conditions

Symbol	Description	Min	Max	Units
V_{CC}	Supply voltage relative to GND Commercial 0°C to +85°C junction	4.25	5.25	V
	Supply voltage relative to GND Industrial -40°C to +100°C junction	4.5	5.5	V
V_{IHT}	High-level input voltage — TTL configuration	2.0	V_{CC}	V
V_{ILT}	Low-level input voltage — TTL configuration	0	0.8	V
V_{IHC}	High-level input voltage — CMOS configuration	70%	100%	V_{CC}
V_{ILC}	Low-level input voltage — CMOS configuration	0	20%	V_{CC}
T_{IN}	Input signal transition time		250	ns

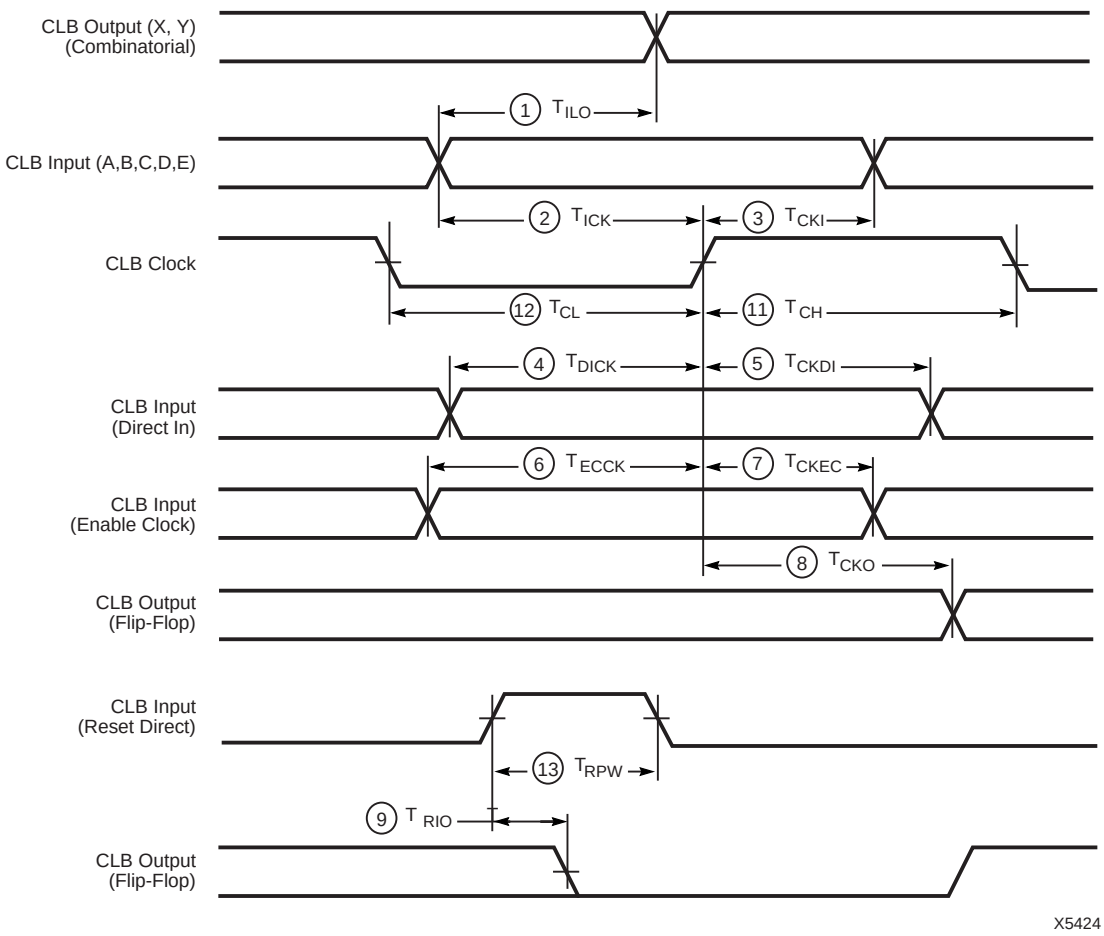
Note: At junction temperatures above those listed as Operating Conditions, all delay parameters increase by 0.3% per °C.

XC3100A DC Characteristics Over Operating Conditions

Symbol	Description		Min	Max	Units
V_{OH}	High-level output voltage (@ I_{OH} = –8.0 mA, V_{CC} min)	Commercial	3.86		V
V_{OL}	Low-level output voltage (@ I_{OL} = 8.0 mA, V_{CC} min)			0.40	V
V_{OH}	High-level output voltage (@ I_{OH} = –8.0 mA, V_{CC} min)	Industrial	3.76		V
V_{OL}	Low-level output voltage (@ I_{OL} = 8.0 mA, V_{CC} min)			0.40	V
V_{CCPD}	Power-down supply voltage (PWRDWN must be Low)		2.30		V
I_{CCO}	Quiescent LCA supply current in addition to I_{CCPD}[1] Chip thresholds programmed as CMOS levels Chip thresholds programmed as TTL levels			 8 14	 mA mA
I_{IL}	Input Leakage Current		–10	+10	µA
C_{IN}	Input capacitance, all packages except PGA175 (sample tested) All Pins except XTL1 and XTL2 XTL1 and XTL2			 10 15	 pF pF
	Input capacitance, PGA 175 (sample tested) All Pins except XTL1 and XTL2 XTL1 and XTL2			 15 20	 pF pF
I_{RIN}	Pad pull-up (when selected) @ V_{IN} = 0 V[3]		0.02	0.17	mA
I_{RLL}	Horizontal Longline pull-up (when selected) @ logic Low		0.20	2.80	mA

Notes: 1. With no output current loads, no active input or Longline pull-up resistors, all package pins at V_{CC} or GND, and the LCA device configured with a tie option.
2. Total continuous output sink current may not exceed 100 mA per ground pin. The number of ground pins varies from two for the XC3120A in the PC84 package, to eight for the XC3195A in the PQ208 package.
3. Not tested. Allows an undriven pin to float High. For any other purpose, use an external pull-up.

XC3100A CLB Switching Characteristics Guidelines (continued)



XC3100L Switching Characteristics

Xilinx maintains test specifications for each product as controlled documents. To insure the use of the most recently released device performance parameters, please request a copy of the current test-specification revision.

XC3100L Operating Conditions

Symbol	Description	Min	Max	Units
V_{CC}	Supply voltage relative to GND Commercial 0°C to +85°C junction	3.0	3.6	V
V_{IH}	High-level input voltage	2.0	V_{CC} + 0.3	V
V_{IL}	Low-level input voltage	-0.3	0.8	V
T_{IN}	Input signal transition time		250	ns

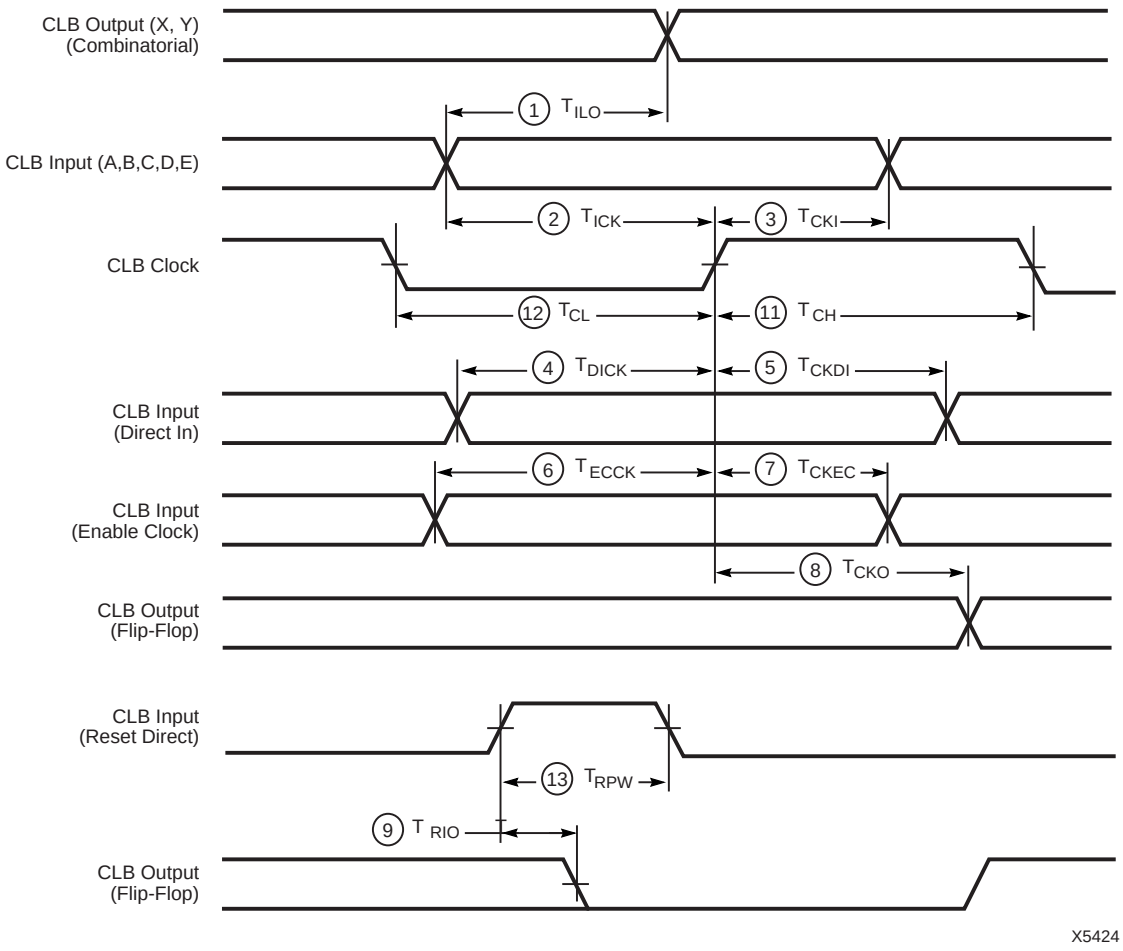
Notes: 1. At junction temperatures above those listed as Operating Conditions, all delay parameters increase by 0.3% per °C.
2. Although the present (1996) devices operate over the full supply voltage range from 3.0 V to 5.25 V, Xilinx reserves the right to restrict operation to the 3.0 and 3.6 V range later, when smaller device geometries might preclude operation @ 5 V. Operating conditions are guaranteed in the 3.0 – 3.6 V V_{CC} range.

XC3100L DC Characteristics Over Operating Conditions

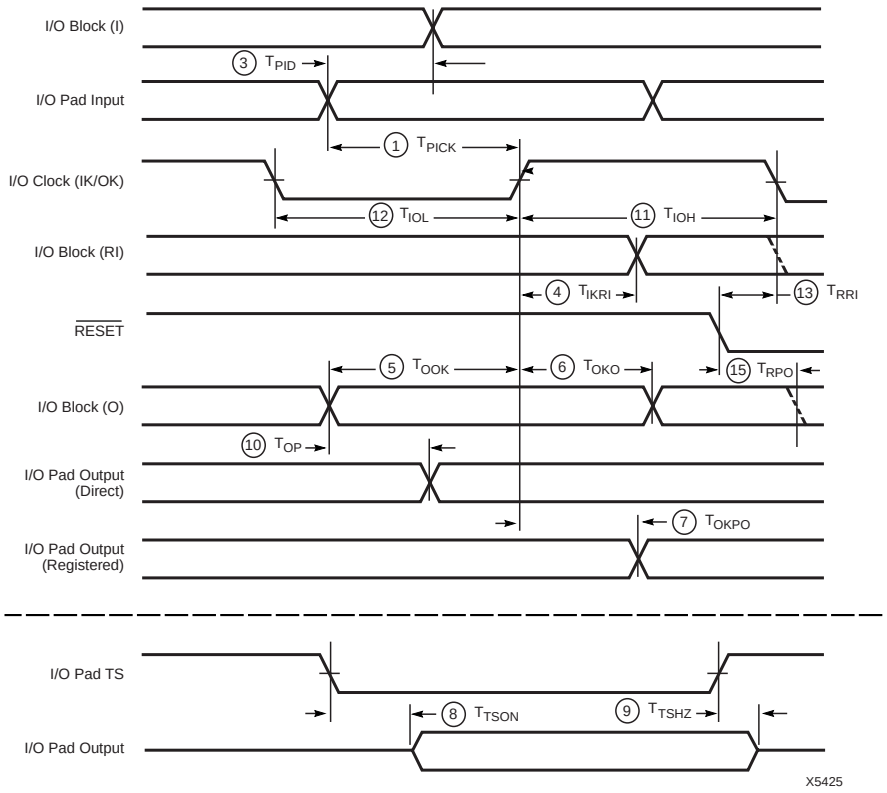
Symbol	Description	Min	Max	Units
V_{OH}	High-level output voltage (@ I_{OH} = -4.0 mA, V_{CC} min)	2.4		V
	High-level output voltage (@ I_{OH} = -100.0 µA, V_{CC} min)	V_{CC} -0.2		V
V_{OL}	Low-level output voltage (@ I_{OH} = 4.0 mA, V_{CC} min)		0.40	V
	Low-level output voltage (@ I_{OH} = +100.0 µA, V_{CC} min)		0.2	V
V_{CCPD}	Power-down supply voltage (PWRDWN must be Low)	2.30		V
I_{CCO}	Quiescent FPGA supply current Chip thresholds programmed as CMOS levels[1]		1.5	mA
I_{IL}	Input Leakage Current	-10	+10	µA
C_{IN}	Input capacitance (sample tested) All pins except XTL1 and XTL2 XTL1 and XTL2		 10 15	 pF pF
I_{RIN}	Pad pull-up (when selected) @ V_{IN} = 0 V [3]	0.02	0.17	mA
I_{RLL}	Horizontal long line pull-up (when selected) @ logic Low	0.20	2.80	mA

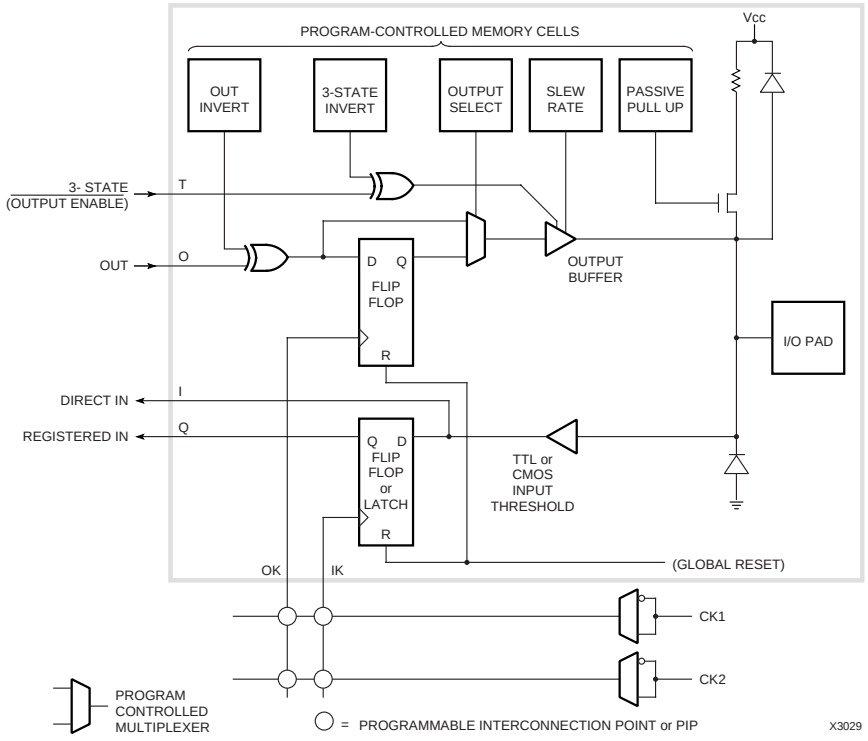
Notes: 1. With no output current loads, no active input or long line pull-up resistors, all package pins at V_{CC} or GND, and the FPGA configured with a tie option.
2. Total continuous output sink current may not exceed 100 mA per ground pin. Total continuous output source current may not exceed 100 mA per V_{CC} pin. The number of ground pins varies from the XC3142L to the XC3190L.
3. Not tested. Allows undriven pins to float High. For any other purpose, use an external pull-up.

XC3100L CLB Switching Characteristics Guidelines (continued)



XC3100L IOB Switching Characteristics Guidelines (continued)





XC3000 Series 64-Pin Plastic VQFP Pinouts

XC3000A, XC3000L, and XC3100A families have identical pinouts

Pin No.	XC3030A
1	A0-WS-I/O
2	A1-CS2-I/O
3	A2-I/O
4	A3-I/O
5	A4-I/O
6	A14-I/O
7	A5-I/O
8	**GND**
9	A13-I/O
10	A6-I/O
11	A12-I/O
12	A7-I/O
13	A11-I/O
14	A8-I/O
15	A10-I/O
16	A9-I/O
17	PWRDN
18	TCLKIN-I/O
19	I/O
20	I/O
21	I/O
22	I/O
23	I/O
24	**VCC**
25	I/O
26	I/O
27	I/O
28	I/O
29	I/O
30	I/O
31	M1-$\overline{\text{RDATA}}$
32	M0-RTRIG

Pin No.	XC3030A
33	M2-I/O
34	HDC-I/O
35	I/O
36	$\overline{\text{LDC}}$-I/O
37	I/O
38	I/O
39	I/O
40	$\overline{\text{INIT}}$-I/O
41	**GND**
42	I/O
43	I/O
44	I/O
45	I/O
46	I/O
47	XTAL2(IN)-I/O
48	$\overline{\text{RESET}}$
49	DONE-PG
50	D7-I/O
51	XTAL1(OUT)-BCLKIN-I/O
52	D6-I/O
53	D5-I/O
54	$\overline{\text{CS0}}$-I/O
55	D4-I/O
56	VCC
57	D3-I/O
58	$\overline{\text{CS1}}$-I/O
59	D2-I/O
60	D1-I/O
61	RDY/$\overline{\text{BUSY}}$-RCLK-I/O
62	D0-DIN-I/O
63	DOUT-I/O
64	CCLK

XC3000 Series 100-Pin QFP Pinouts

XC3000A, XC3000L, XC3100A, and XC3100L families have identical pinouts

Pin No.		XC3020A XC3030A XC3042A
PQFP	TQFP VQFP	
16	13	GND
17	14	A13-I/O
18	15	A6-I/O
19	16	A12-I/O
20	17	A7-I/O
21	18	I/O*
22	19	I/O*
23	20	A11-I/O
24	21	A8-I/O
25	22	A10-I/O
26	23	A9-I/O
27	24	VCC*
28	25	GND*
29	26	$\overline{\text{PWRDN}}$
30	27	TCLKIN-I/O
31	28	I/O**
32	29	I/O*
33	30	I/O*
34	31	I/O
35	32	I/O
36	33	I/O
37	34	I/O
38	35	I/O
39	36	I/O
40	37	I/O
41	38	VCC
42	39	I/O
43	40	I/O
44	41	I/O
45	42	I/O
46	43	I/O
47	44	I/O
48	45	I/O
49	46	I/O

Pin No.		XC3020A XC3030A XC3042A
PQFP	TQFP VQFP	
50	47	I/O*
51	48	I/O*
52	49	M1-$\overline{\text{RD}}$
53	50	GND*
54	51	MO-RT
55	52	VCC*
56	53	M2-I/O
57	54	HDC-I/O
58	55	I/O
59	56	$\overline{\text{LDC}}$-I/O
60	57	I/O*
61	58	I/O*
62	59	I/O
63	60	I/O
64	61	I/O
65	62	$\overline{\text{INIT}}$-I/O
66	63	GND
67	64	I/O
68	65	I/O
69	66	I/O
70	67	I/O
71	68	I/O
72	69	I/O
73	70	I/O
74	71	I/O*
75	72	I/O*
76	73	XTL2-I/O
77	74	GND*
78	75	$\overline{\text{RESET}}$
79	76	VCC*
80	77	DONE-$\overline{\text{PG}}$
81	78	D7-I/O
82	79	BCLKIN-XTL1-I/O
83	80	D6-I/O

Pin No.		XC3020A XC3030A XC3042A
PQFP	TQFP VQFP	
84	81	I/O*
85	82	I/O*
86	83	I/O
87	84	D5-I/O
88	85	$\overline{\text{CS0}}$-I/O
89	86	D4-I/O
90	87	I/O
91	88	VCC
92	89	D3-I/O
93	90	$\overline{\text{CS1}}$-I/O
94	91	D2-I/O
95	92	I/O
96	93	I/O*
97	94	I/O*
98	95	D1-I/O
99	96	RDY/$\overline{\text{BUSY}}$-RCLK-I/O
100	97	DO-DIN-I/O
1	98	DOUT-I/O
2	99	CCLK
3	100	VCC*
4	1	GND*
5	2	AO-$\overline{\text{WS}}$-I/O
6	3	A1-CS2-I/O
7	4	I/O**
8	5	A2-I/O
9	6	A3-I/O
10	7	I/O*
11	8	I/O*
12	9	A15-I/O
13	10	A4-I/O
14	11	A14-I/O
15	12	A5-I/O

Unprogrammed IOBs have a default pull-up. This prevents an undefined pad level for unbonded or unused IOBs. Programmed outputs are default slew-rate limited.

* This table describes the pinouts of three different chips in three different packages. The pin-description column lists 100 of the 118 pads on the XC3042A that are connected to the 100 package pins. Two pads, indicated by double asterisks, do not exist on the XC3030A, which has 98 pads; therefore the corresponding pins have no connections. Twenty-six pads, indicated by single or double asterisks, do not exist on the XC3020A, which has 74 pads; therefore, the corresponding pins have no connections. (See table on page 65.)

XC3000 Series 176-Pin TQFP Pinouts

XC3000A, XC3000L, XC3100A, and XC3100L families have identical pinouts

Pin Number	XC3090A
1	$\overline{\text{PWRDWN}}$
2	TCLKIN-I/O
3	I/O
4	I/O
5	I/O
6	I/O
7	I/O
8	I/O
9	I/O
10	I/O
11	I/O
12	I/O
13	I/O
14	I/O
15	I/O
16	I/O
17	I/O
18	I/O
19	I/O
20	I/O
21	I/O
22	GND
23	VCC
24	I/O
25	I/O
26	I/O
27	I/O
28	I/O
29	I/O
30	I/O
31	I/O
32	I/O
33	I/O
34	I/O
35	I/O
36	I/O
37	I/O
38	I/O
39	I/O
40	I/O
41	I/O
42	I/O
43	I/O
44	–

Pin Number	XC3090A
45	M1-$\overline{\text{RDATA}}$
46	GND
47	M0-RTRIG
48	VCC
49	M2-I/O
50	HDC-I/O
51	I/O
52	I/O
53	I/O
54	$\overline{\text{LDC}}$-I/O
55	–
56	I/O
57	I/O
58	I/O
59	I/O
60	I/O
61	I/O
62	I/O
63	I/O
64	I/O
65	$\overline{\text{INIT}}$-I/O
66	VCC
67	GND
68	I/O
69	I/O
70	I/O
71	I/O
72	I/O
73	I/O
74	I/O
75	I/O
76	I/O
77	I/O
78	I/O
79	I/O
80	I/O
81	I/O
82	–
83	–
84	I/O
85	XTAL2(IN)-I/O
86	GND
87	$\overline{\text{RESET}}$
88	VCC

Pin Number	XC3090A
89	DONE-$\overline{\text{PG}}$
90	D7-I/O
91	XTAL1(OUT)-BCLKIN-I/O
92	I/O
93	I/O
94	I/O
95	I/O
96	D6-I/O
97	I/O
98	I/O
99	I/O
100	I/O
101	I/O
102	D5-I/O
103	$\overline{\text{CS0}}$-I/O
104	I/O
105	I/O
106	I/O
107	I/O
108	D4-I/O
109	I/O
110	VCC
111	GND
112	D3-I/O
113	$\overline{\text{CS1}}$-I/O
114	I/O
115	I/O
116	I/O
117	I/O
118	D2-I/O
119	I/O
120	I/O
121	I/O
122	I/O
123	I/O
124	D1-I/O
125	RDY/$\overline{\text{BUSY}}$-$\overline{\text{RCLK}}$-I/O
126	I/O
127	I/O
128	I/O
129	I/O
130	D0-DIN-I/O
131	DOUT-I/O
132	CCLK

Pin Number	XC3090A
133	VCC
134	GND
135	A0-$\overline{\text{WS}}$-I/O
136	A1-CS2-I/O
137	–
138	I/O
139	I/O
140	A2-I/O
141	A3-I/O
142	–
143	–
144	I/O
145	I/O
146	A15-I/O
147	A4-I/O
148	I/O
149	I/O
150	A14-I/O
151	A5-I/O
152	I/O
153	I/O
154	GND
155	VCC
156	A13-I/O
157	A6-I/O
158	I/O
159	I/O
160	–
161	–
162	I/O
163	I/O
164	A12-I/O
165	A7-I/O
166	I/O
167	I/O
168	–
169	A11-I/O
170	A8-I/O
171	I/O
172	I/O
173	A10-I/O
174	A9-I/O
175	VCC
176	GND

Unprogrammed IOBs have a default pull-up. This prevents an undefined pad level for unbonded or unused IOBs. Programmed outputs are default slew-rate limited.

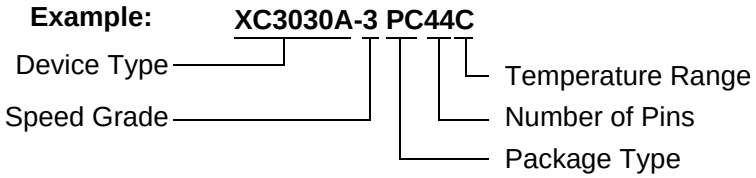
Pins		44	64	68	84		100			132		144	160	175		176	208
Type		Plast. PLCC	Plast. VQFP	Plast. PLCC	Plast. PLCC	Cer. PGA	Plast. PQFP	Plast. TQFP	Plast. VQFP	Plast. PGA	Cer. PGA	Plast. TQFP	Plast. PQFP	Plast. PGA	Cer. PGA	Plast. TQFP	Plast. PQFP
Code		PC44	VQ64	PC68	PC84	PG84	PQ100	TQ100	VQ100	PP132	PG132	TQ144	PQ160	PP175	PG175	TQ176	PQ208
XC3142L					C				C			C					
					C				C			C					
XC3190L					C							C				C	
					C							C				C	

Notes: C = Commercial, T_J= 0° to +85°C I = Industrial, T_J = -40° to +100°C

Number of Available I/O Pins

		Number of Package Pins										
	Max I/O	44	64	68	84	100	132	144	160	175	176	208
XC3020A/XC3120A	64			58	64	64						
XC3030A/XC3130A	80	34	54	58	74	80						
XC3042A/3142A	96				74	82	96	96				
XC2064A/XC3164A	120				70		110	120	120			
XC3090A/XC3190A	144				70			122	138	144	144	144
XC3195A	176				70				138	144		176

Ordering Information



Revision History

Date	Revision
11/98	Revised version number to 3.1, removed XC3100A-5 obsolete packages.