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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	320
Number of Logic Elements/Cells	-
Total RAM Bits	64160
Number of I/O	70
Number of Gates	6000
Voltage - Supply	3V ~ 3.6V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	84-LCC (J-Lead)
Supplier Device Package	84-PLCC (29.31x29.31)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc3090l-8pc84c

Introduction

XC3000-Series Field Programmable Gate Arrays (FPGAs) provide a group of high-performance, high-density, digital integrated circuits. Their regular, extendable, flexible, user-programmable array architecture is composed of a configuration program store plus three types of configurable elements: a perimeter of I/O Blocks (IOBs), a core array of Configurable Logic Bocks (CLBs) and resources for interconnection. The general structure of an FPGA is shown in Figure 2. The development system provides schematic capture and auto place-and-route for design entry. Logic and timing simulation, and in-circuit emulation are available as design verification alternatives. The design editor is used for interactive design optimization, and to compile the data pattern that represents the configuration program.

The FPGA user logic functions and interconnections are determined by the configuration program data stored in internal static memory cells. The program can be loaded in any of several modes to accommodate various system requirements. The program data resides externally in an EEPROM, EPROM or ROM on the application circuit board, or on a floppy disk or hard disk. On-chip initialization logic provides for optional automatic loading of program data at power-up. The companion XC17XX Serial Configuration PROMs provide a very simple serial configuration program storage in a one-time programmable package.

The XC3000 Field Programmable Gate Array families provide a variety of logic capacities, package styles, temperature ranges and speed grades.

XC3000 Series Overview

There are now four distinct family groupings within the XC3000 Series of FPGA devices:

- XC3000A Family
- XC3000L Family
- XC3100A Family
- XC3100L Family

All four families share a common architecture, development software, design and programming methodology, and also common package pin-outs. An extensive Product Description covers these common aspects.

Detailed parametric information for the XC3000A, XC3000L, XC3100A, and XC3100L product families is then provided. (The XC3000 and XC3100 families are not recommended for new designs.)

Here is a simple overview of those XC3000 products currently emphasized:

- **XC3000A Family** — The XC3000A is an enhanced version of the basic XC3000 family, featuring additional interconnect resources and other user-friendly enhancements.
- **XC3000L Family** — The XC3000L is identical in architecture and features to the XC3000A family, but operates at a nominal supply voltage of 3.3 V. The XC3000L is the right solution for battery-operated and low-power applications.
- **XC3100A Family** — The XC3100A is a performance-optimized relative of the XC3000A family. While both families are bitstream and footprint compatible, the XC3100A family extends toggle rates to 370 MHz and in-system performance to over 80 MHz. The XC3100A family also offers one additional array size, the XC3195A.
- **XC3100L Family** — The XC3100L is identical in architectures and features to the XC3100A family, but operates at a nominal supply voltage of 3.3V.

Figure 1 illustrates the relationships between the families. Compared to the original XC3000 family, XC3000A offers additional functionality and increased speed. The XC3000L family offers the same additional functionality, but reduced speed due to its lower supply voltage of 3.3 V. The XC3100A family offers substantially higher speed and higher density with the XC3195A.

New XC3000 Series Compared to Original XC3000 Family

For readers already familiar with the original XC3000 family of FPGAs, the major new features in the XC3000A, XC3000L, XC3100A, and XC3100L families are listed in this section.

All of these new families are upward-compatible extensions of the original XC3000 FPGA architecture. Any bitstream used to configure an XC3000 device will configure the corresponding XC3000A, XC3000L, XC3100A, or XC3100L device exactly the same way.

The XC3100A and XC3100L FPGA architectures are upward-compatible extensions of the XC3000A and XC3000L architectures. Any bitstream used to configure an XC3000A or XC3000L device will configure the corresponding XC3100A or XC3100L device exactly the same way.

Configurable Logic Block

The array of CLBs provides the functional elements from which the user's logic is constructed. The logic blocks are arranged in a matrix within the perimeter of IOBs. For example, the XC3020A has 64 such blocks arranged in 8 rows and 8 columns. The development system is used to compile the configuration data which is to be loaded into the internal configuration memory to define the operation and interconnection of each block. User definition of CLBs and their interconnecting networks may be done by automatic translation from a schematic-capture logic diagram or optionally by installing library or user macros.

Each CLB has a combinatorial logic section, two flip-flops, and an internal control section. See Figure 5. There are: five logic inputs (A, B, C, D and E); a common clock input (K); an asynchronous direct RESET input (RD); and an enable clock (EC). All may be driven from the interconnect resources adjacent to the blocks. Each CLB also has two outputs (X and Y) which may drive interconnect networks.

Data input for either flip-flop within a CLB is supplied from the function F or G outputs of the combinatorial logic, or the block input, DI. Both flip-flops in each CLB share the asynchronous RD which, when enabled and High, is dominant over clocked inputs. All flip-flops are reset by the active-Low chip input, RESET, or during the configuration process. The flip-flops share the enable clock (EC) which, when Low, recirculates the flip-flops' present states and inhibits response to the data-in or combinatorial function inputs on a CLB. The user may enable these control inputs and select their sources. The user may also select the clock net input (K), as well as its active sense within each CLB. This programmable inversion eliminates the need to route both phases of a clock signal throughout the device.

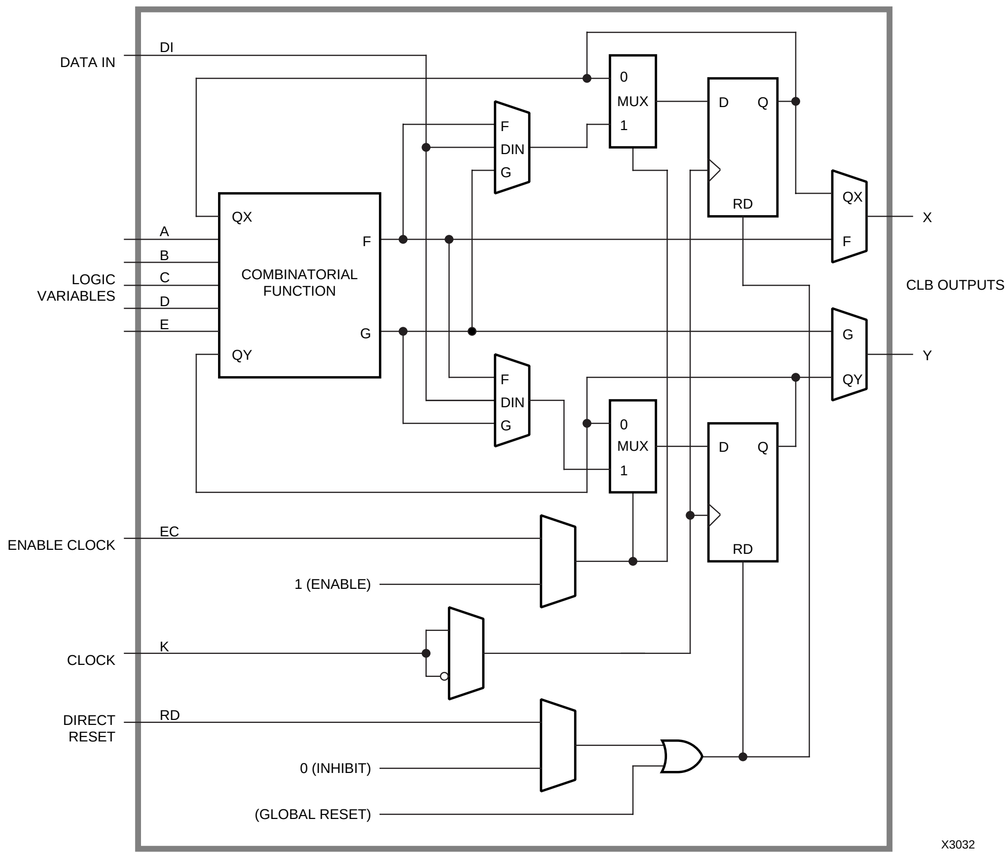


Figure 5: Configurable Logic Block.
Each CLB includes a combinatorial logic section, two flip-flops and a program memory controlled multiplexer selection of function. It has the following:

- five logic variable inputs A, B, C, D, and E
- a direct data in DI
- an enable clock EC
- a clock (invertible) K
- an asynchronous direct RESET RD
- two outputs X and Y

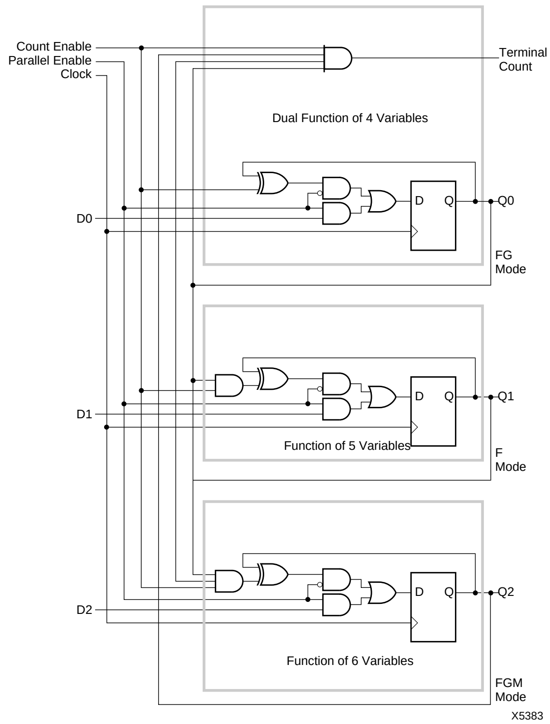


Figure 7: Counter.
The modulo-8 binary counter with parallel enable and clock enable uses one combinatorial logic block of each option.

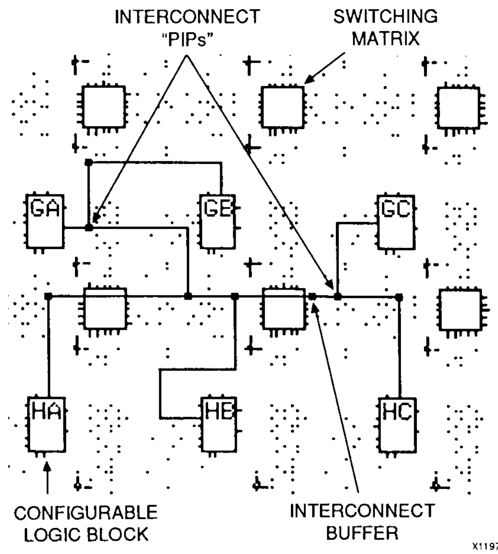


Figure 8: A Design Editor view of routing resources used to form a typical interconnection network from CLB GA.

General Purpose Interconnect

General purpose interconnect, as shown in Figure 10, consists of a grid of five horizontal and five vertical metal segments located between the rows and columns of logic and IOBs. Each segment is the height or width of a logic block. Switching matrices join the ends of these segments and allow programmed interconnections between the metal grid segments of adjoining rows and columns. The switches of an unprogrammed device are all non-conducting. The connections through the switch matrix may be established by the automatic routing or by selecting the desired pairs of matrix pins to be connected or disconnected. The legitimate switching matrix combinations for each pin are indicated in Figure 11.

Special buffers within the general interconnect areas provide periodic signal isolation and restoration for improved performance of lengthy nets. The interconnect buffers are available to propagate signals in either direction on a given general interconnect segment. These bidirectional (bidi) buffers are found adjacent to the switching matrices, above and to the right. The other PIPs adjacent to the matrices are accessed to or from Longlines. The development system automatically defines the buffer direction based on the location of the interconnection network source. The delay calculator of the development system automatically calculates and displays the block, interconnect and buffer delays for any paths selected. Generation of the simulation netlist with a worst-case delay model is provided.

Direct Interconnect

Direct interconnect, shown in Figure 12, provides the most efficient implementation of networks between adjacent CLBs or I/O Blocks. Signals routed from block to block using the direct interconnect exhibit minimum interconnect propagation and use no general interconnect resources. For each CLB, the X output may be connected directly to the B input of the CLB immediately to its right and to the C input of the CLB to its left. The Y output can use direct interconnect to drive the D input of the block immediately above and the A input of the block below. Direct interconnect should be used to maximize the speed of high-performance portions of logic. Where logic blocks are adjacent to IOBs, direct connect is provided alternately to the IOB inputs (I) and outputs (O) on all four edges of the die. The right edge provides additional direct connects from CLB outputs to adjacent IOBs. Direct interconnections of IOBs with CLBs are shown in Figure 13.

7

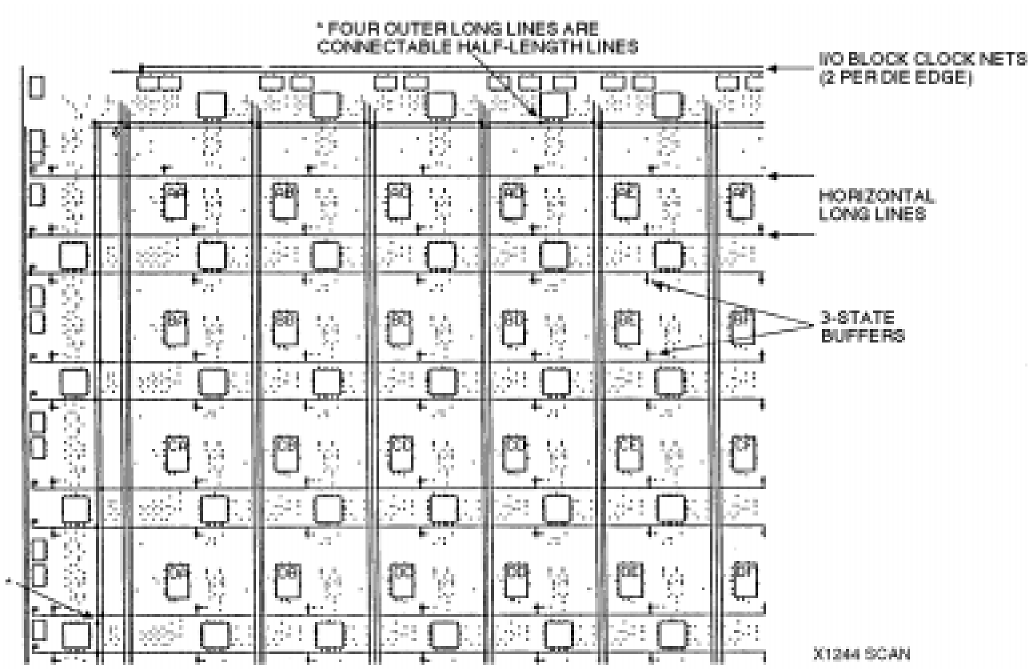


Figure 15: Programmable Interconnection of Longlines. This is provided at the edges of the routing area. Three-state buffers allow the use of horizontal Longlines to form on-chip wired AND and multiplexed buses. The left two non-clock vertical Longlines per column (except XC3020A) and the outer perimeter Longlines may be programmed as connectable half-length lines.

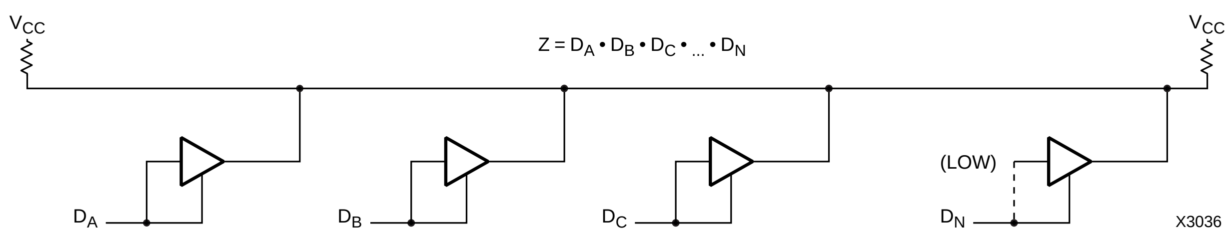


Figure 16: 3-State Buffers Implement a Wired-AND Function. When all the buffer 3-state lines are High, (high impedance), the pull-up resistor(s) provide the High output. The buffer inputs are driven by the control signals or a Low.

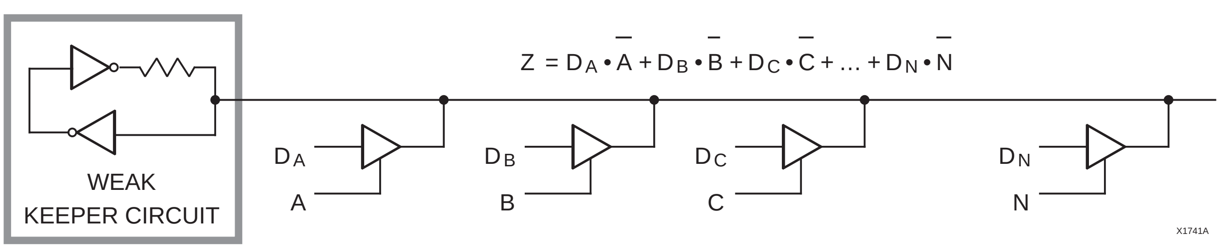


Figure 17: 3-State Buffers Implement a Multiplexer. The selection is accomplished by the buffer 3-state signal.

Peripheral Mode

Peripheral mode uses the trailing edge of the logic AND condition of the CS0, CS1, CS2, and WS inputs to accept byte-wide data from a microprocessor bus. In the lead FPGA, this data is loaded into a double-buffered UART-like parallel-to-serial converter and is serially shifted into the internal logic. The lead FPGA presents the preamble data (and all data that overflows the lead device) on the DOUT pin.

The Ready/Busy output from the lead device acts as a handshake signal to the microprocessor. RDY/BUSY goes Low when a byte has been received, and goes High again when the byte-wide input buffer has transferred its information into the shift register, and the buffer is ready to receive new data. The length of the BUSY signal depends on the activity in the UART. If the shift register had been empty when the new byte was received, the BUSY signal lasts for only two CCLK periods. If the shift register was still full when the new byte was received, the BUSY signal can be as long as nine CCLK periods.

Note that after the last byte has been entered, only seven of its bits are shifted out. CCLK remains High with DOUT equal to bit 6 (the next-to-last bit) of the last byte entered.

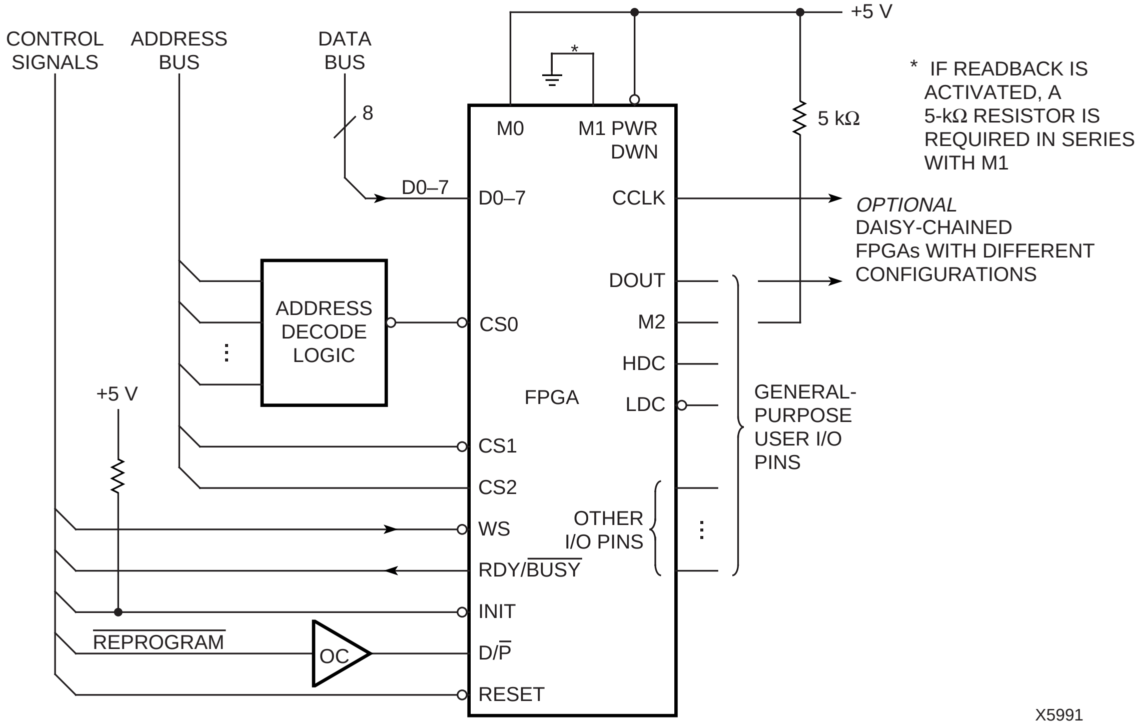
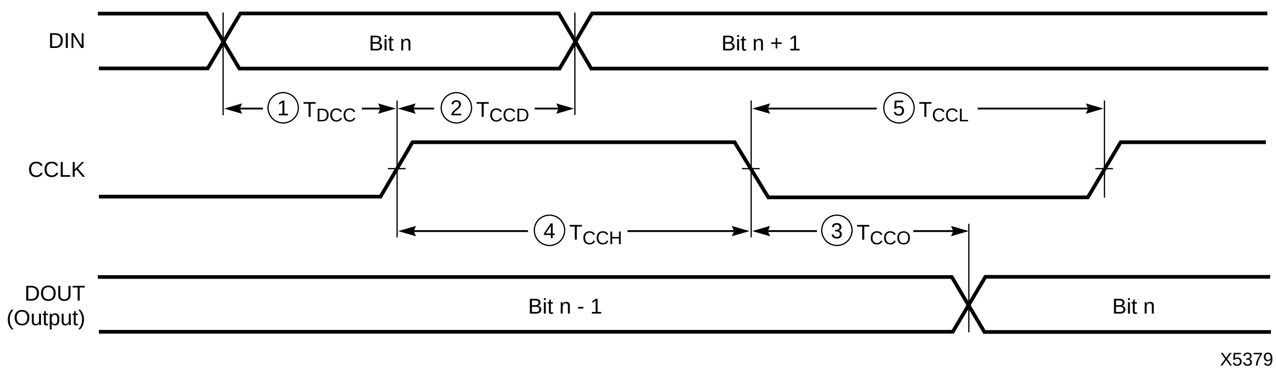


Figure 27: Peripheral Mode Circuit Diagram



	Description		Symbol	Min	Max	Units
CCLK	To DOUT	3	T_{CCO}		100	ns
	DIN setup	1	T_{DCC}	60		ns
	DIN hold	2	T_{CCD}	0		ns
	High time	4	T_{CCH}	0.05		µs
	Low time (Note 1)	5	T_{CCL}	0.05	5.0	µs
	Frequency		F_{CC}		10	MHz

Notes:
1. The max limit of CCLK Low time is caused by dynamic circuitry inside the FPGA.
2. Configuration must be delayed until the $\overline{\text{INIT}}$ of all FPGAs is High.
3. At power-up, V_{CC} must rise from 2.0 V to V_{CC} min in less than 25 ms. If this is not possible, configuration can be delayed by holding $\overline{\text{RESET}}$ Low until VCC has reached 4.0 V (2.5 V for the XC3000L). A very long V_{CC} rise time of >100 ms, or a non-monotonically rising V_{CC} may require a >6-µs High level on $\overline{\text{RESET}}$, followed by a >6-µs Low level on $\overline{\text{RESET}}$ and D/$\overline{\text{P}}$ after V_{CC} has reached 4.0 V (2.5 V for the XC3000L).

Figure 30: Slave Serial Mode Programming Switching Characteristics

Device Performance

The XC3000 families of FPGAs can achieve very high performance. This is the result of

- A sub-micron manufacturing process, developed and continuously being enhanced for the production of state-of-the-art CMOS SRAMs.
- Careful optimization of transistor geometries, circuit design, and lay-out, based on years of experience with the XC3000 family.
- A look-up table based, coarse-grained architecture that can collapse multiple-layer combinatorial logic into a single function generator. One CLB can implement up to four layers of conventional logic in as little as 1.5 ns.

Actual system performance is determined by the timing of critical paths, including the delay through the combinatorial and sequential logic elements within CLBs and IOBs, plus the delay in the interconnect routing. The AC-timing specifications state the worst-case timing parameters for the various logic resources available in the XC3000-families architecture. Figure 31 shows a variety of elements involved in determining system performance.

Logic block performance is expressed as the propagation time from the interconnect point at the input to the block to the output of the block in the interconnect area. Since combinatorial logic is implemented with a memory lookup table within a CLB, the combinatorial delay through the CLB, called T_{ILO}, is always the same, regardless of the function being implemented. For the combinatorial logic function driving the data input of the storage element, the critical timing is data set-up relative to the clock edge provided to the flip-flop element. The delay from the clock source to the output of the logic block is critical in the timing signals produced by storage elements. Loading of a logic-block output is limited only by the resulting propagation delay of the larger interconnect network. Speed performance of the logic block is a function of supply voltage and temperature. See Figure 32.

Interconnect performance depends on the routing resources used to implement the signal path. Direct interconnects to the neighboring CLB provide an extremely fast path. Local interconnects go through switch matrices (magic boxes) and suffer an RC delay, equal to the resistance of the pass transistor multiplied by the capacitance of the driven metal line. Longlines carry the signal across the length or breadth of the chip with only one access delay. Generous on-chip signal buffering makes performance relatively insensitive to signal fan-out; increasing fan-out from 1 to 8 changes the CLB delay by only 10%. Clocks can be distributed with two low-skew clock distribution networks.

The tools in the Development System used to place and route a design in an XC3000 FPGA automatically calculate the actual maximum worst-case delays along each signal path. This timing information can be back-annotated to the design's netlist for use in timing simulation or examined with, a static timing analyzer.

Actual system performance is applications dependent. The maximum clock rate that can be used in a system is determined by the critical path delays within that system. These delays are combinations of incremental logic and routing delays, and vary from design to design. In a synchronous system, the maximum clock rate depends on the number of combinatorial logic layers between re-synchronizing flip-flops. Figure 33 shows the achievable clock rate as a function of the number of CLB layers.

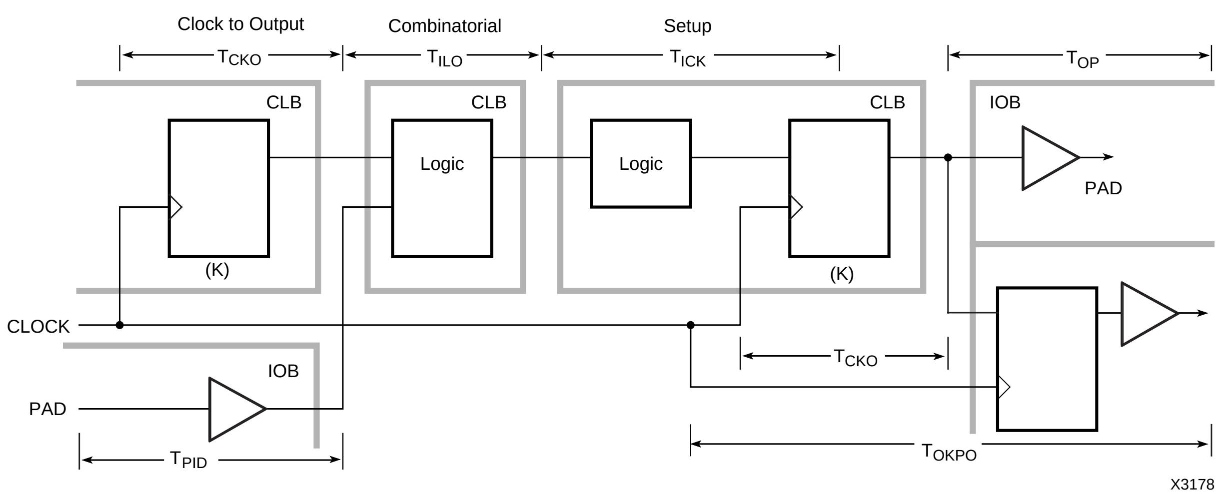


Figure 31: Primary Block Speed Factors. Actual timing is a function of various block factors combined with routing. factors. Overall performance can be evaluated with the timing calculator or by an optional simulation.

Dynamic Power Consumption

	XC3042A	XC3042L	XC3142A	
One CLB driving three local interconnects	0.25	0.17	0.25	mW per MHz
One global clock buffer and clock line	2.25	1.40	1.70	mW per MHz
One device output with a 50 pF load	1.25	1.25	1.25	mW per MHz

Power Consumption

The Field Programmable Gate Array exhibits the low power consumption characteristic of CMOS ICs. For any design, the configuration option of TTL chip input threshold requires power for the threshold reference. The power required by the static memory cells that hold the configuration data is very low and may be maintained in a power-down mode.

Typically, most of power dissipation is produced by external capacitive loads on the output buffers. This load and frequency dependent power is 25 µW/pF/MHz per output. Another component of I/O power is the external dc loading on all output pins.

Internal power dissipation is a function of the number and size of the nodes, and the frequency at which they change. In an FPGA, the fraction of nodes changing on a given clock is typically low (10-20%). For example, in a long binary counter, the total activity of all counter flip-flops is equivalent to that of only two CLB outputs toggling at the clock frequency. Typical global clock-buffer power is between 2.0 mW/MHz for the XC3020A and 3.5 mW/MHz for the XC3090A. The internal capacitive load is more a function of interconnect than fan-out. With a typical load of three general interconnect segments, each CLB output requires about 0.25 mW per MHz of its output frequency.

Because the control storage of the FPGA is CMOS static memory, its cells require a very low standby current for data retention. In some systems, this low data retention current characteristic can be used as a method of preserving configurations in the event of a primary power loss. The FPGA has built in powerdown logic which, when activated, will disable normal operation of the device and retain only the configuration data. All internal operation is suspended and output buffers are placed in their high-impedance state with no pull-ups. Different from the XC3000 family which can be powered down to a current consumption of a few microamps, the XC3100A draws 5 mA, even in power-down. This makes power-down operation less meaningful. In contrast, I_{CCPD} for the XC3000L is only 10 µA.

To force the FPGA into the Powerdown state, the user must pull the $\overline{\text{PWRDWN}}$ pin Low and continue to supply a retention voltage to the V_{CC} pins. When normal power is restored, V_{CC} is elevated to its normal operating voltage and $\overline{\text{PWRDWN}}$ is returned to a High. The FPGA resumes operation with the same internal sequence that occurs at the conclusion of configuration. Internal-I/O and logic-block storage elements will be reset, the outputs will become enabled and the DONE/$\overline{\text{PROG}}$ pin will be released.

When V_{CC} is shut down or disconnected, some power might unintentionally be supplied from an incoming signal driving an I/O pin. The conventional electrostatic input protection is implemented with diodes to the supply and ground. A positive voltage applied to an input (or output) will cause the positive protection diode to conduct and drive the V_{CC} connection. This condition can produce invalid power conditions and should be avoided. A large series resistor might be used to limit the current or a bipolar buffer may be used to isolate the input signal.

7

XC3000A CLB Switching Characteristics Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Since many internal timing parameters cannot be measured directly, they are derived from benchmark timing patterns. The following guidelines reflect worst-case values over the recommended operating conditions. For more detailed, more precise, and more up-to-date timing information, use the values provided by the timing calculator and used in the simulator.

Description			Speed Grade	-7 Min	-7 Max	-6 Min	-6 Max	Units
Combinatorial Delay								
Logic Variables	A, B, C, D, E, to outputs X or Y							
	FG Mode	1	T_{ILO}		5.1		4.1	ns
	F and FGM Mode				5.6		4.6	ns
Sequential delay								
Clock k to outputs X or Y		8	T_{CKO}		4.5		4.0	ns
Clock k to outputs X or Y when Q is returned through function generators F or G to drive X or Y								
	FG Mode		T_{QLO}		9.5		8.0	ns
	F and FGM Mode				10.0		8.5	ns
Set-up time before clock K								
Logic Variables	A, B, C, D, E							
	FG Mode	2	T_{ICK}	4.5		3.5		ns
	F and FGM Mode			5.0		4.0		ns
Data In	DI	4	T_{DICK}	4.0		3.0		ns
Enable Clock	EC	6	T_{ECCK}	4.5		4.0		ns
Hold Time after clock K								
Logic Variables	A, B, C, D, E	3	T_{CKI}	0		0		ns
Data In	DI[2]	5	T_{CKDI}	1.0		1.0		ns
Enable Clock	EC	7	T_{CKEC}	2.0		2.0		ns
Clock								
Clock High time		11	T_{CH}	4.0		3.5		ns
Clock Low time		12	T_{CL}	4.0		3.5		ns
Max. flip-flop toggle rate			F_{CLK}	113.0		135.0		MHz
Reset Direct (RD)								
RD width		13	T_{RPW}	6.0		5.0		ns
delay from RD to outputs X or Y		9	T_{RIO}		6.0		5.0	ns
Global Reset ($\overline{RESET}$ Pad)[1]								
$\overline{RESET}$ width (Low)			T_{MRW}	16.0		14.0		ns
delay from $\overline{RESET}$ pad to outputs X or Y			T_{MRQ}		19.0		17.0	ns

Notes: 1. Timing is based on the XC3042A, for other devices see timing calculator.
2. The CLB K to Q output delay (T_{CKO}, #8) of any CLB, plus the shortest possible interconnect delay, is always longer than the Data In hold time requirement (T_{CKDI}, #5) of any CLB on the same die.

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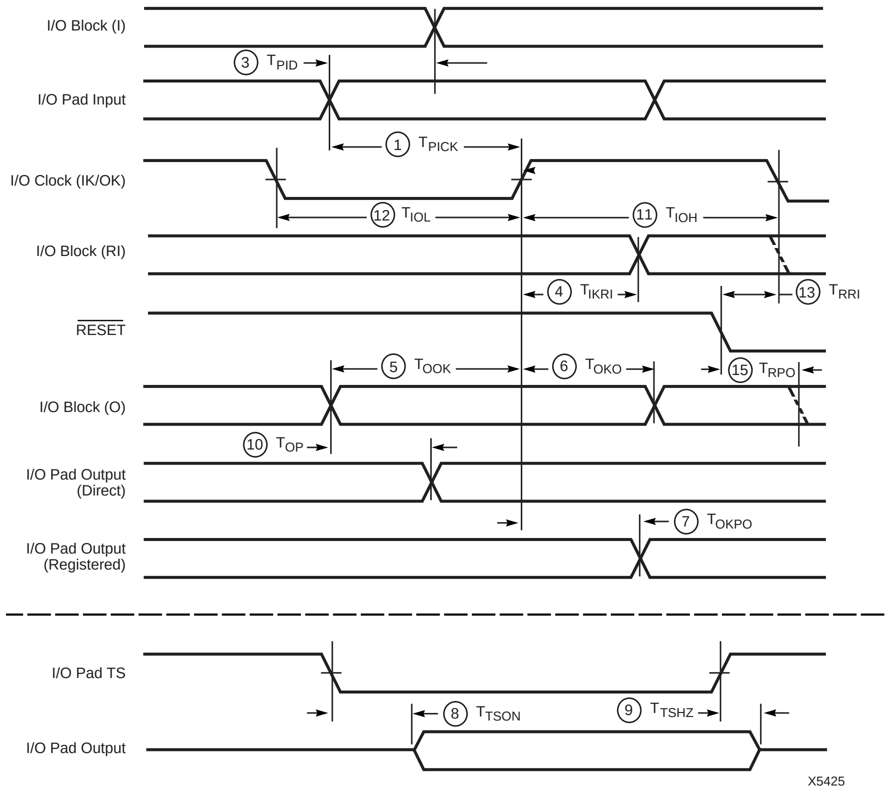
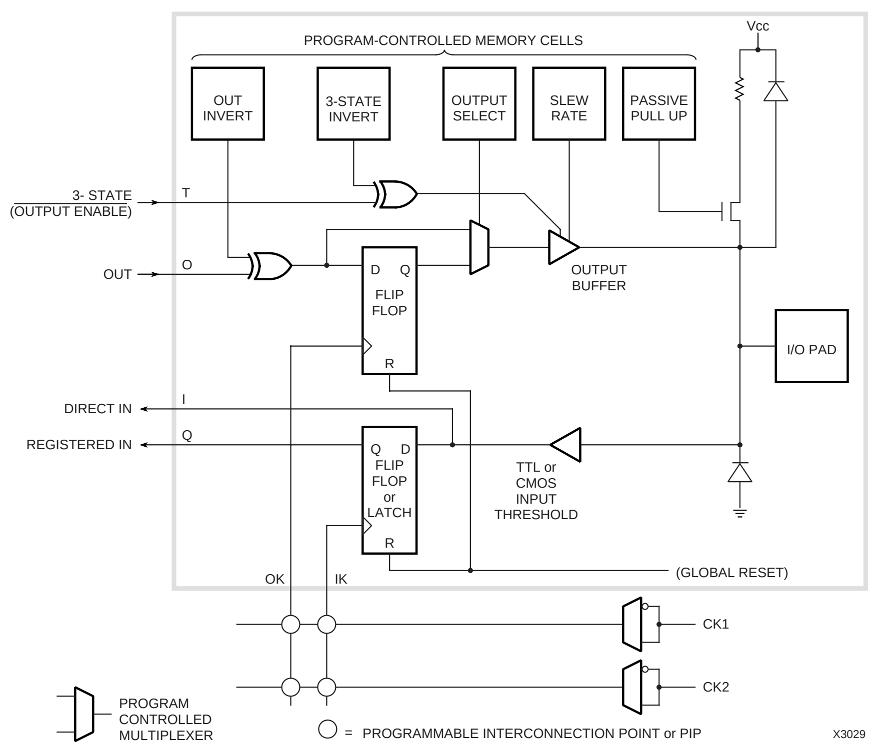
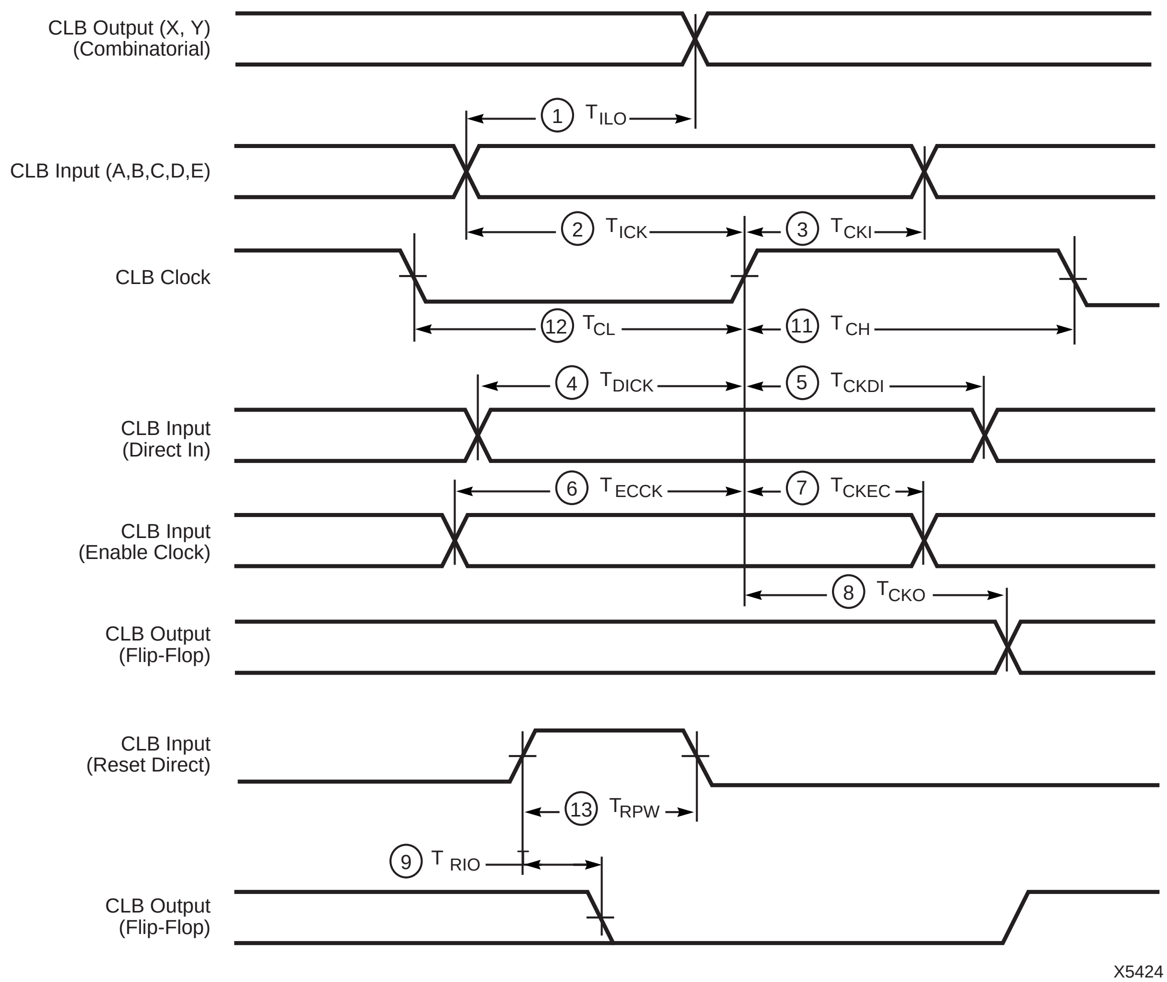
XC3000A IOB Switching Characteristics Guidelines (continued)





XC3000L CLB Switching Characteristics Guidelines (continued)



XC3100A Switching Characteristics

Xilinx maintains test specifications for each product as controlled documents. To insure the use of the most recently released device performance parameters, please request a copy of the current test-specification revision.

XC3100A Operating Conditions

Symbol	Description	Min	Max	Units
V_{CC}	Supply voltage relative to GND Commercial 0°C to +85°C junction	4.25	5.25	V
	Supply voltage relative to GND Industrial -40°C to +100°C junction	4.5	5.5	V
V_{IHT}	High-level input voltage — TTL configuration	2.0	V_{CC}	V
V_{ILT}	Low-level input voltage — TTL configuration	0	0.8	V
V_{IHC}	High-level input voltage — CMOS configuration	70%	100%	V_{CC}
V_{ILC}	Low-level input voltage — CMOS configuration	0	20%	V_{CC}
T_{IN}	Input signal transition time		250	ns

Note: At junction temperatures above those listed as Operating Conditions, all delay parameters increase by 0.3% per °C.

XC3100A DC Characteristics Over Operating Conditions

Symbol	Description		Min	Max	Units
V_{OH}	High-level output voltage (@ I_{OH} = –8.0 mA, V_{CC} min)	Commercial	3.86		V
V_{OL}	Low-level output voltage (@ I_{OL} = 8.0 mA, V_{CC} min)			0.40	V
V_{OH}	High-level output voltage (@ I_{OH} = –8.0 mA, V_{CC} min)	Industrial	3.76		V
V_{OL}	Low-level output voltage (@ I_{OL} = 8.0 mA, V_{CC} min)			0.40	V
V_{CCPD}	Power-down supply voltage (PWRDWN must be Low)		2.30		V
I_{CCO}	Quiescent LCA supply current in addition to I_{CCPD}[1] Chip thresholds programmed as CMOS levels Chip thresholds programmed as TTL levels			 8 14	 mA mA
I_{IL}	Input Leakage Current		–10	+10	µA
C_{IN}	Input capacitance, all packages except PGA175 (sample tested) All Pins except XTL1 and XTL2 XTL1 and XTL2			 10 15	 pF pF
	Input capacitance, PGA 175 (sample tested) All Pins except XTL1 and XTL2 XTL1 and XTL2			 15 20	 pF pF
I_{RIN}	Pad pull-up (when selected) @ V_{IN} = 0 V[3]		0.02	0.17	mA
I_{RLL}	Horizontal Longline pull-up (when selected) @ logic Low		0.20	2.80	mA

Notes:
1. With no output current loads, no active input or Longline pull-up resistors, all package pins at V_{CC} or GND, and the LCA device configured with a tie option.
2. Total continuous output sink current may not exceed 100 mA per ground pin. The number of ground pins varies from two for the XC3120A in the PC84 package, to eight for the XC3195A in the PQ208 package.
3. Not tested. Allows an undriven pin to float High. For any other purpose, use an external pull-up.

XC3100A Absolute Maximum Ratings

Symbol	Description		Units
V_{CC}	Supply voltage relative to GND	–0.5 to +7.0	V
V_{IN}	Input voltage with respect to GND	–0.5 to V_{CC} +0.5	V
V_{TS}	Voltage applied to 3-state output	–0.5 to V_{CC} +0.5	V
T_{STG}	Storage temperature (ambient)	–65 to +150	°C
T_{SOL}	Maximum soldering temperature (10 s @ 1/16 in.)	+260	°C
T_J	Junction temperature plastic	+125	°C
	Junction temperature ceramic	+150	°C

Note: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

XC3100A Global Buffer Switching Characteristics Guidelines

	Speed Grade	-4	-3	-2	-1	-09	
Description	**Symbol**	**Max**	**Max**	**Max**	**Max**	**Max**	**Units**
Global and Alternate Clock Distribution[1]							
Either: **Normal** IOB input pad through clock buffer to any CLB or IOB clock input	T_{PID}	6.5	5.6	4.7	4.3	3.9	ns
Or: **Fast** (CMOS only) input pad through clock buffer to any CLB or IOB clock input	T_{PIDC}	5.1	4.3	3.7	3.5	3.1	ns
TBUF driving a Horizontal Longline (L.L.)[1]							
I to L.L. while T is Low (buffer active) (XC3100)	T_{IO}	3.7	3.1				ns
(XC3100A)	T_{IO}	3.6	3.1	3.1	2.9	2.1	ns
T↓ to L.L. active and valid with single pull-up resistor	T_{ON}	5.0	4.2	4.2	4.0	3.1	ns
T↓ to L.L. active and valid with pair of pull-up resistors	T_{ON}	6.5	5.7	5.7	5.5	4.6	ns
T↑ to L.L. High with single pull-up resistor	T_{PUS}	13.5	11.4	11.4	10.4	8.9	ns
T↑ to L.L. High with pair of pull-up resistors	T_{PUF}	10.5	8.8	8.1	7.1	5.9	ns
BIDI							
Bidirectional buffer delay	T_{BIDI}	1.2	1.0	0.9	0.85	0.75	ns
						Prelim	

Note: 1. Timing is based on the XC3142A, for other devices see timing calculator.
The use of two pull-up resistors per longline, available on other XC3000 devices, is not a valid design option for XC3100A devices.

XC3100A CLB Switching Characteristics Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Since many internal timing parameters cannot be measured directly, they are derived from benchmark timing patterns. The following guidelines reflect worst-case values over the recommended operating conditions. For more detailed, more precise, and more up-to-date timing information, use the values provided by the timing calculator and used in the simulator.

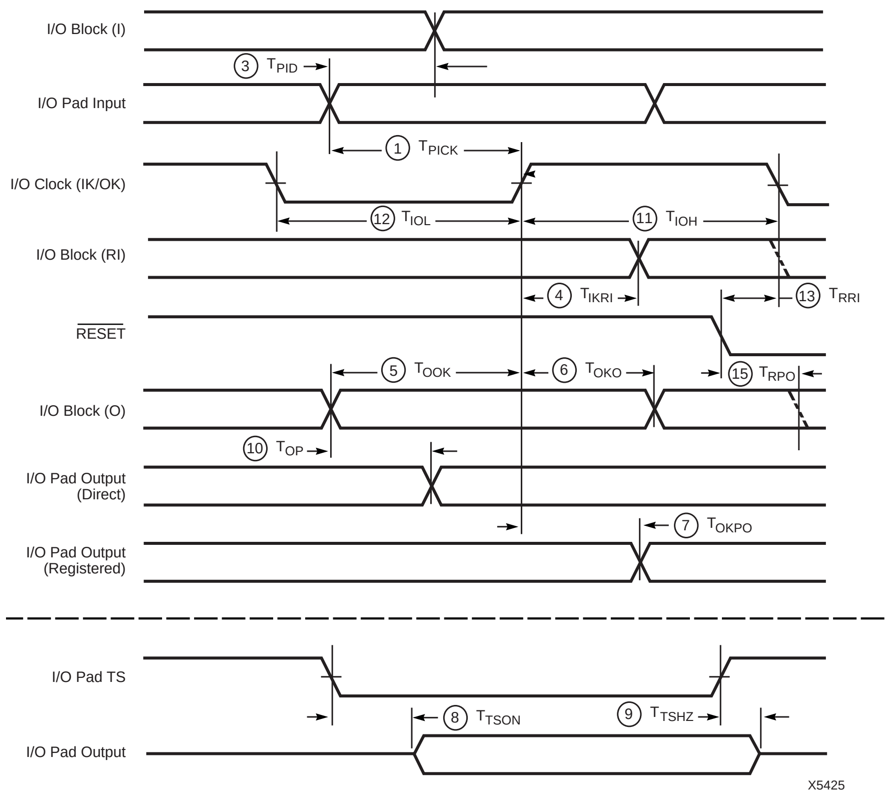
Speed Grade			-4		-3		-2		-1		-09		
Description	**Symbol**		**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**
Combinatorial Delay													
Logic Variables A, B, C, D, E, to outputs X or Y	1	T_{ILO}		3.3		2.7		2.2		1.75		1.5	ns
Sequential delay													
Clock k to outputs X or Y	8	T_{CKO}		2.5		2.1		1.7		1.4		1.25	ns
Clock k to outputs X or Y when Q is returned through function generators F or G to drive X or Y		T_{QLO}		5.2		4.3		3.5		3.1		2.7	ns
Set-up time before clock K													
Logic Variables A, B, C, D, E	2	T_{ICK}	2.5		2.1		1.8		1.7		1.5		ns
Data In DI	4	T_{DICK}	1.6		1.4		1.3		1.2		1.0		ns
Enable Clock EC	6	T_{ECCK}	3.2		2.7		2.5		2.3		2.05		ns
Reset Direct inactive RD			1.0		1.0		1.0		1.0		1.0		ns
Hold Time after clock K													
Logic Variables A, B, C, D, E	3	T_{CKI}	0		0		0		0		0		ns
Data In DI	5	T_{CKDI}	1.0		0.9		0.9		0.8		0.7		ns
Enable Clock EC	7	T_{CKEC}	0.8		0.7		0.7		0.6		0.55		ns
Clock													
Clock High time	11	T_{CH}	2.0		1.6		1.3		1.3		1.3		ns
Clock Low time	12	T_{CL}	2.0		1.6		1.3		1.3		1.3		ns
Max. flip-flop toggle rate		F_{CLK}	227		270		323		323		370		MHz
Reset Direct (RD)													
RD width	13	T_{RPW}	3.2		2.7		2.3		2.3		2.05		ns
delay from RD to outputs X or Y	9	T_{RIO}		3.7		3.1		2.7		2.4		2.15	ns
Global Reset ($\overline{\text{RESET}}$ Pad)[1]													
$\overline{\text{RESET}}$ width (Low) (XC3142A)		T_{MRW}	14.0		12.0		12.0		12.0		12.0		ns
delay from $\overline{\text{RESET}}$ pad to outputs X or Y		T_{MRQ}		14.0		12.0		12.0		12.0		12.0	ns
											Prelim		

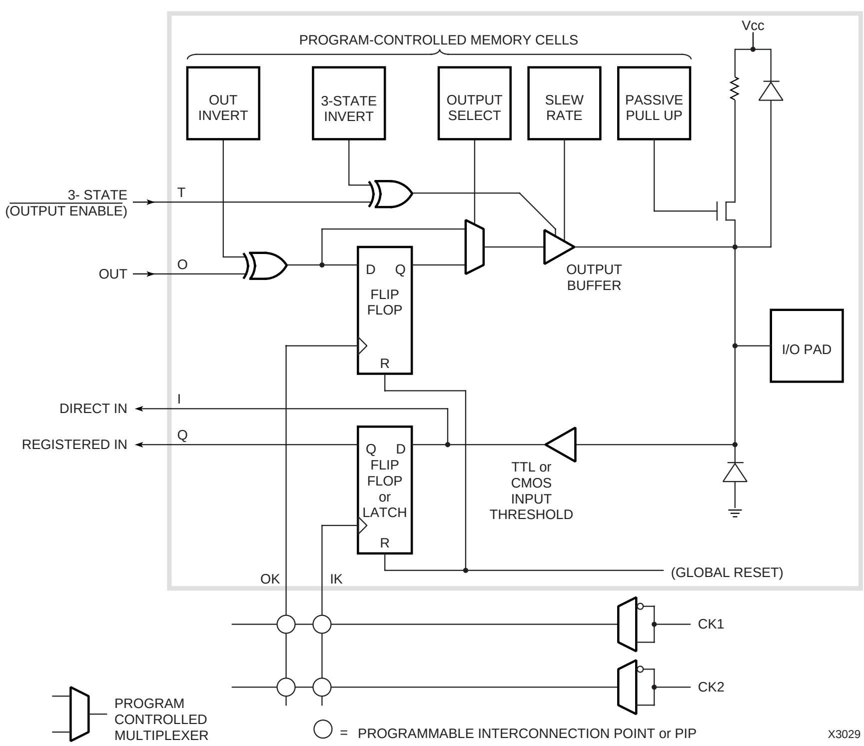
Notes: 1. The CLB K to Q output delay (T_{CKO}, #8) of any CLB, plus the shortest possible interconnect delay, is always longer than the Data In hold time requirement (T_{CKDI}, #5) of any CLB on the same die.

2. T_{ILO}, T_{QLO} and T_{ICK} are specified for 4-input functions. For 5-input functions or base FGM functions, each of these specifications for the XC3100A family increases by 0.50 ns (-5), 0.42 ns (-4) and 0.35 ns (-3), 0.35 ns (-2), 0.30 ns (-1), and 0.30 ns (-09).

7

XC3100A IOB Switching Characteristics Guidelines (continued)





XC3100L Absolute Maximum Ratings

Symbol	Description		Units
V_{CC}	Supply voltage relative to GND	–0.5 to +7.0	V
V_{IN}	Input voltage with respect to GND	–0.5 to V_{CC} +0.5	V
V_{TS}	Voltage applied to 3-state output	–0.5 to V_{CC} +0.5	V
T_{STG}	Storage temperature (ambient)	–65 to +150	°C
T_{SOL}	Maximum soldering temperature (10 s @ 1/16 in.)	+260	°C
T_J	Junction temperature plastic	+125	°C
	Junction temperature ceramic	+150	°C

Note: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

XC3100L Global Buffer Switching Characteristics Guidelines

	Speed Grade	-3	-2	
Description	**Symbol**	**Max**	**Max**	**Units**
Global and Alternate Clock Distribution[1]				
Either: **Normal** IOB input pad through clock buffer to any CLB or IOB clock input	T_{PID}	5.6	4.7	ns
Or: **Fast** (CMOS only) input pad through clock buffer to any CLB or IOB clock input	T_{PIDC}	4.3	3.7	ns
TBUF driving a Horizontal Longline (L.L.)[1]				
I to L.L. while T is Low (buffer active)	T_{IO}	3.1	3.1	ns
T↓ to L.L. active and valid with single pull-up resistor	T_{ON}	4.2	4.2	ns
T↑ to L.L. High with single pull-up resistor	T_{PUS}	11.4	11.4	ns
BIDI				
Bidirectional buffer delay	T_{BIDI}	1.0	0.9	ns
		Advance		

Notes: 1. Timing is based on the XC3142L, for other devices see timing calculator.
2. The use of two pull-up resistors per longline, available on other XC3000 devices, is not a valid option for XC3100L devices.

XC3000 Series 68-Pin PLCC, 84-Pin PLCC and PGA Pinouts

XC3000A, XC3000L, XC3100A, and XC3100L families have identical pinouts

68 PLCC		XC3020A, XC3030A, XC3042A	84 PLCC
XC3030A	XC3020A		
10	10	$\overline{\text{PWRDN}}$	12
11	11	TCLKIN-I/O	13
12	—	I/O*	14
13	12	I/O	15
14	13	I/O	16
—	—	I/O	17
15	14	I/O	18
16	15	I/O	19
—	16	I/O	20
17	17	I/O	21
18	18	VCC	22
19	19	I/O	23
—	—	I/O	24
20	20	I/O	25
—	21	I/O	26
21	22	I/O	27
22	—	I/O	28
23	23	I/O	29
24	24	I/O	30
25	25	M1-$\overline{\text{RDATA}}$	31
26	26	M0-RTRIG	32
27	27	M2-I/O	33
28	28	HDC-I/O	34
29	29	I/O	35
30	30	$\overline{\text{LDC}}$-I/O	36
—	31	I/O	37
—		I/O*	38
31	32	I/O	39
32	33	I/O	40
33	—	I/O*	41
34	34	$\overline{\text{INIT}}$-I/O	42
35	35	GND	43
36	36	I/O	44
37	37	I/O	45
38	38	I/O	46
39	39	I/O	47
—	40	I/O	48
—	41	I/O	49
40		I/O*	50
41		I/O*	51
42	42	I/O	52
43	43	XTL2(IN)-I/O	53

68 PLCC		XC3020A, XC3030A, XC3042A	84 PLCC
XC3030A	XC3020A		
44	44	$\overline{\text{RESET}}$	54
45	45	DONE-$\overline{\text{PG}}$	55
46	46	D7-I/O	56
47	47	XTL1(OUT)-BCLKIN-I/O	57
48	48	D6-I/O	58
—	—	I/O	59
49	49	D5-I/O	60
50	50	$\overline{\text{CS0}}$-I/O	61
51	51	D4-I/O	62
—	—	I/O	63
52	52	VCC	64
53	53	D3-I/O	65
54	54	$\overline{\text{CS1}}$-I/O	66
55	55	D2-I/O	67
—	—	I/O	68
—	—	I/O*	69
56	56	D1-I/O	70
57	57	RDY/$\overline{\text{BUSY}}$-$\overline{\text{RCLK}}$-I/O	71
58	58	D0-DIN-I/O	72
59	59	DOUT-I/O	73
60	60	CCLK	74
61	61	A0-$\overline{\text{WS}}$-I/O	75
62	62	A1-CS2-I/O	76
63	63	A2-I/O	77
64	64	A3-I/O	78
—	—	I/O*	79
—	—	I/O*	80
65	65	A15-I/O	81
66	66	A4-I/O	82
67	67	A14-I/O	83
68	68	A5-I/O	84
1	1	GND	1
2	2	A13-I/O	2
3	3	A6-I/O	3
4	4	A12-I/O	4
5	5	A7-I/O	5
—	—	I/O*	6
—	—	I/O*	7
6	6	A11-I/O	8
7	7	A8-I/O	9
8	8	A10-I/O	10
9	9	A9-I/O	11

Unprogrammed IOBs have a default pull-up. This prevents an undefined pad level for unbonded or unused IOBs. Programmed outputs are default slew-rate limited.

This table describes the pinouts of three different chips in three different packages. The pin-description column lists 84 of the 118 pads on the XC3042A (and 84 of the 98 pads on the XC3030A) that are connected to the 84 package pins. Ten pads, indicated by an asterisk, do not exist on the XC3020A, which has 74 pads; therefore the corresponding pins on the 84-pin packages have no connections to an XC3020A. Six pads on the XC3020A and 16 pads on the XC3030A, indicated by a dash (—) in the 68 PLCC column, have no connection to the 68 PLCC, but are connected to the 84-pin packages.

XC3064A/XC3090A/XC3195A 84-Pin PLCC Pinouts

XC3000A, XC3000L, XC3100A, and XC3100L families have identical pinouts

PLCC Pin Number	XC3064A, XC3090A, XC3195A
12	$\overline{\text{PWRDN}}$
13	TCLKIN-I/O
14	I/O
15	I/O
16	I/O
17	I/O
18	I/O
19	I/O
20	I/O
21	GND*
22	VCC
23	I/O
24	I/O
25	I/O
26	I/O
27	I/O
28	I/O
29	I/O
30	I/O
31	M1-$\overline{\text{RDATA}}$
32	M0-RTRIG
33	M2-I/O
34	HDC-I/O
35	I/O
36	$\overline{\text{LDC}}$-I/O
37	I/O
38	I/O
39	I/O
40	I/O
41	INIT/I/O*
42	VCC*
43	GND
44	I/O
45	I/O
46	I/O
47	I/O
48	I/O
49	I/O
50	I/O
51	I/O
52	I/O
53	XTL2(IN)-I/O

PLCC Pin Number	XC3064A, XC3090A, XC3195A
54	$\overline{\text{RESET}}$
55	DONE-$\overline{\text{PG}}$
56	D7-I/O
57	XTL1(OUT)-BCLKIN-I/O
58	D6-I/O
59	I/O
60	D5-I/O
61	$\overline{\text{CS0}}$-I/O
62	D4-I/O
63	I/O
64	VCC
65	GND*
66	D3-I/O*
67	$\overline{\text{CS1}}$-I/O*
68	D2-I/O*
69	I/O
70	D1-I/O
71	RDY/$\overline{\text{BUSY}}$-$\overline{\text{RCLK}}$-I/O
72	D0-DIN-I/O
73	DOUT-I/O
74	CCLK
75	A0-$\overline{\text{WS}}$-I/O
76	A1-CS2-I/O
77	A2-I/O
78	A3-I/O
79	I/O
80	I/O
81	A15-I/O
82	A4-I/O
83	A14-I/O
84	A5-I/O
1	GND
2	VCC*
3	A13-I/O*
4	A6-I/O*
5	A12-I/O*
6	A7-I/O*
7	I/O
8	A11-I/O
9	A8-I/O
10	A10-I/O
11	A9-I/O

Unprogrammed IOBs have a default pull-up. This prevents an undefined pad level for unbonded or unused IOBs. Programmed outputs are default slew-rate limited.

* In the PC84 package, XC3064A, XC3090A and XC3195A have additional VCC and GND pins and thus a different pin definition than XC3020A/XC3030A/XC3042A.

XC3000 Series 175-Pin Ceramic and Plastic PGA Pinouts

XC3000A, XC3000L, XC3100A, and XC3100L families have identical pinouts

PGA Pin Number	XC3090A, XC3195A
B2	$\overline{\text{PWRDN}}$
D4	TCLKIN-I/O
B3	I/O
C4	I/O
B4	I/O
A4	I/O
D5	I/O
C5	I/O
B5	I/O
A5	I/O
C6	I/O
D6	I/O
B6	I/O
A6	I/O
B7	I/O
C7	I/O
D7	I/O
A7	I/O
A8	I/O
B8	I/O
C8	I/O
D8	GND
D9	VCC
C9	I/O
B9	I/O
A9	I/O
A10	I/O
D10	I/O
C10	I/O
B10	I/O
A11	I/O
B11	I/O
D11	I/O
C11	I/O
A12	I/O
B12	I/O
C12	I/O
D12	I/O
A13	I/O
B13	I/O
C13	I/O
A14	I/O

PGA Pin Number	XC3090A, XC3195A
D13	I/O
B14	M1-$\overline{\text{RDATA}}$
C14	GND
B15	M0-RTRIG
D14	VCC
C15	M2-I/O
E14	HDC-I/O
B16	I/O
D15	I/O
C16	I/O
D16	$\overline{\text{LDC}}$-I/O
F14	I/O
E15	I/O
E16	I/O
F15	I/O
F16	I/O
G14	I/O
G15	I/O
G16	I/O
H16	I/O
H15	$\overline{\text{INIT}}$-I/O
H14	VCC
J14	GND
J15	I/O
J16	I/O
K16	I/O
K15	I/O
K14	I/O
L16	I/O
L15	I/O
M16	I/O
M15	I/O
L14	I/O
N16	I/O
P16	I/O
N15	I/O
R16	I/O
M14	I/O
P15	XTL2(IN)-I/O
N14	GND
R15	$\overline{\text{RESET}}$
P14	VCC

PGA Pin Number	XC3090A, XC3195A
R14	DONE-$\overline{\text{PG}}$
N13	D7-I/O
T14	XTL1(OUT)-BCLKIN-I/O
P13	I/O
R13	I/O
T13	I/O
N12	I/O
P12	D6-I/O
R12	I/O
T12	I/O
P11	I/O
N11	I/O
R11	I/O
T11	D5-I/O
R10	$\overline{\text{CS0}}$-I/O
P10	I/O
N10	I/O
T10	I/O
T9	I/O
R9	D4-I/O
P9	I/O
N9	VCC
N8	GND
P8	D3-I/O
R8	$\overline{\text{CS1}}$-I/O
T8	I/O
T7	I/O
N7	I/O
P7	I/O
R7	D2-I/O
T6	I/O
R6	I/O
N6	I/O
P6	I/O
T5	I/O
R5	D1-I/O
P5	RDY/$\overline{\text{BUSY}}$-$\overline{\text{RCLK}}$-I/O
N5	I/O
T4	I/O
R4	I/O
P4	I/O
R3	D0-DIN-I/O

PGA Pin Number	XC3090A, XC3195A
N4	DOUT-I/O
R2	CCLK
P3	VCC
N3	GND
P2	A0-$\overline{\text{WS}}$-I/O
M3	A1-CS2-I/O
R1	I/O
N2	I/O
P1	A2-I/O
N1	A3-I/O
L3	I/O
M2	I/O
M1	A15-I/O
L2	A4-I/O
L1	I/O
K3	I/O
K2	A14-I/O
K1	A5-I/O
J1	I/O
J2	I/O
J3	GND
H3	VCC
H2	A13-I/O
H1	A6-I/O
G1	I/O
G2	I/O
G3	I/O
F1	I/O
F2	A12-I/O
E1	A7-I/O
E2	I/O
F3	I/O
D1	A11-I/O
C1	A8-I/O
D2	I/O
B1	I/O
E3	A10-I/O
C2	A9-I/O
D3	VCC
C3	GND

Unprogrammed IOBs have a default pull-up. This prevents an undefined pad level for unbonded or unused IOBs. Programmed outputs are default slew-rate limited.

Pins A2, A3, A15, A16, T1, T2, T3, T15 and T16 are not connected. Pin A1 does not exist.

XC3000 Series 176-Pin TQFP Pinouts

XC3000A, XC3000L, XC3100A, and XC3100L families have identical pinouts

Pin Number	XC3090A	Pin Number	XC3090A	Pin Number	XC3090A	Pin Number	XC3090A
1	$\overline{PWRDWN}$	45	M1-$\overline{RDATA}$	89	DONE-$\overline{PG}$	133	VCC
2	TCLKIN-I/O	46	GND	90	D7-I/O	134	GND
3	I/O	47	M0-RTRIG	91	XTAL1(OUT)-BCLKIN-I/O	135	A0-$\overline{WS}$-I/O
4	I/O	48	VCC	92	I/O	136	A1-CS2-I/O
5	I/O	49	M2-I/O	93	I/O	137	–
6	I/O	50	HDC-I/O	94	I/O	138	I/O
7	I/O	51	I/O	95	I/O	139	I/O
8	I/O	52	I/O	96	D6-I/O	140	A2-I/O
9	I/O	53	I/O	97	I/O	141	A3-I/O
10	I/O	54	$\overline{LDC}$-I/O	98	I/O	142	–
11	I/O	55	–	99	I/O	143	–
12	I/O	56	I/O	100	I/O	144	I/O
13	I/O	57	I/O	101	I/O	145	I/O
14	I/O	58	I/O	102	D5-I/O	146	A15-I/O
15	I/O	59	I/O	103	$\overline{CS0}$-I/O	147	A4-I/O
16	I/O	60	I/O	104	I/O	148	I/O
17	I/O	61	I/O	105	I/O	149	I/O
18	I/O	62	I/O	106	I/O	150	A14-I/O
19	I/O	63	I/O	107	I/O	151	A5-I/O
20	I/O	64	I/O	108	D4-I/O	152	I/O
21	I/O	65	$\overline{INIT}$-I/O	109	I/O	153	I/O
22	GND	66	VCC	110	VCC	154	GND
23	VCC	67	GND	111	GND	155	VCC
24	I/O	68	I/O	112	D3-I/O	156	A13-I/O
25	I/O	69	I/O	113	$\overline{CS1}$-I/O	157	A6-I/O
26	I/O	70	I/O	114	I/O	158	I/O
27	I/O	71	I/O	115	I/O	159	I/O
28	I/O	72	I/O	116	I/O	160	–
29	I/O	73	I/O	117	I/O	161	–
30	I/O	74	I/O	118	D2-I/O	162	I/O
31	I/O	75	I/O	119	I/O	163	I/O
32	I/O	76	I/O	120	I/O	164	A12-I/O
33	I/O	77	I/O	121	I/O	165	A7-I/O
34	I/O	78	I/O	122	I/O	166	I/O
35	I/O	79	I/O	123	I/O	167	I/O
36	I/O	80	I/O	124	D1-I/O	168	–
37	I/O	81	I/O	125	RDY/$\overline{BUSY}$-$\overline{RCLK}$-I/O	169	A11-I/O
38	I/O	82	–	126	I/O	170	A8-I/O
39	I/O	83	–	127	I/O	171	I/O
40	I/O	84	I/O	128	I/O	172	I/O
41	I/O	85	XTAL2(IN)-I/O	129	I/O	173	A10-I/O
42	I/O	86	GND	130	D0-DIN-I/O	174	A9-I/O
43	I/O	87	$\overline{RESET}$	131	DOUT-I/O	175	VCC
44	–	88	VCC	132	CCLK	176	GND

Unprogrammed IOBs have a default pull-up. This prevents an undefined pad level for unbonded or unused IOBs. Programmed outputs are default slew-rate limited.