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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	100
Number of Logic Elements/Cells	-
Total RAM Bits	22176
Number of I/O	74
Number of Gates	2000
Voltage - Supply	4.25V ~ 5.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	84-LCC (J-Lead)
Supplier Device Package	84-PLCC (29.31x29.31)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc3130a-3pc84c

A buffer in the upper left corner of the FPGA chip drives a global net which is available to all K inputs of logic blocks. Using the global buffer for a clock signal provides a skew-free, high fan-out, synchronized clock for use at any or all of the IOBs and CLBs. Configuration bits for the K input to each logic block can select this global line or another routing resource as the clock source for its flip-flops. This net may also be programmed to drive the die edge clock lines for IOB use. An enhanced speed, CMOS threshold, direct access to this buffer is available at the second pad from the top of the left die edge.

A buffer in the lower right corner of the array drives a horizontal Longline that can drive programmed connections to a vertical Longline in each interconnection column. This alternate buffer also has low skew and high fan-out. The network formed by this alternate buffer's Longlines can be selected to drive the K inputs of the CLBs. CMOS threshold, high speed access to this buffer is available from the third pad from the bottom of the right die edge.

Internal Busses

A pair of 3-state buffers, located adjacent to each CLB, permits logic to drive the horizontal Longlines. Logic operation of the 3-state buffer controls allows them to implement wide multiplexing functions. Any 3-state buffer input can be selected as drive for the horizontal long-line bus by applying a Low logic level on its 3-state control line. See Figure 16. The user is required to avoid contention which can result from multiple drivers with opposing logic levels. Control of the 3-state input by the same signal that drives the buffer input, creates an open-drain wired-AND function. A logic High on both buffer inputs creates a high impedance, which represents no contention. A logic Low enables the buffer to drive the Longline Low. See Figure 17. Pull-up resistors are available at each end of the Longline to provide a High output when all connected buffers are non-conducting. This forms fast, wide gating functions. When data drives the inputs, and separate signals drive the 3-state control lines, these buffers form multiplexers (3-state busses). In this case, care must be used to prevent contention through multiple active buffers of conflicting levels on a common line. Each horizontal Longline is also driven by a weak keeper circuit that prevents undefined floating levels by maintaining the previous logic level when the line is not driven by an active buffer or a pull-up resistor. Figure 18 shows 3-state buffers, Longlines and pull-up resistors.

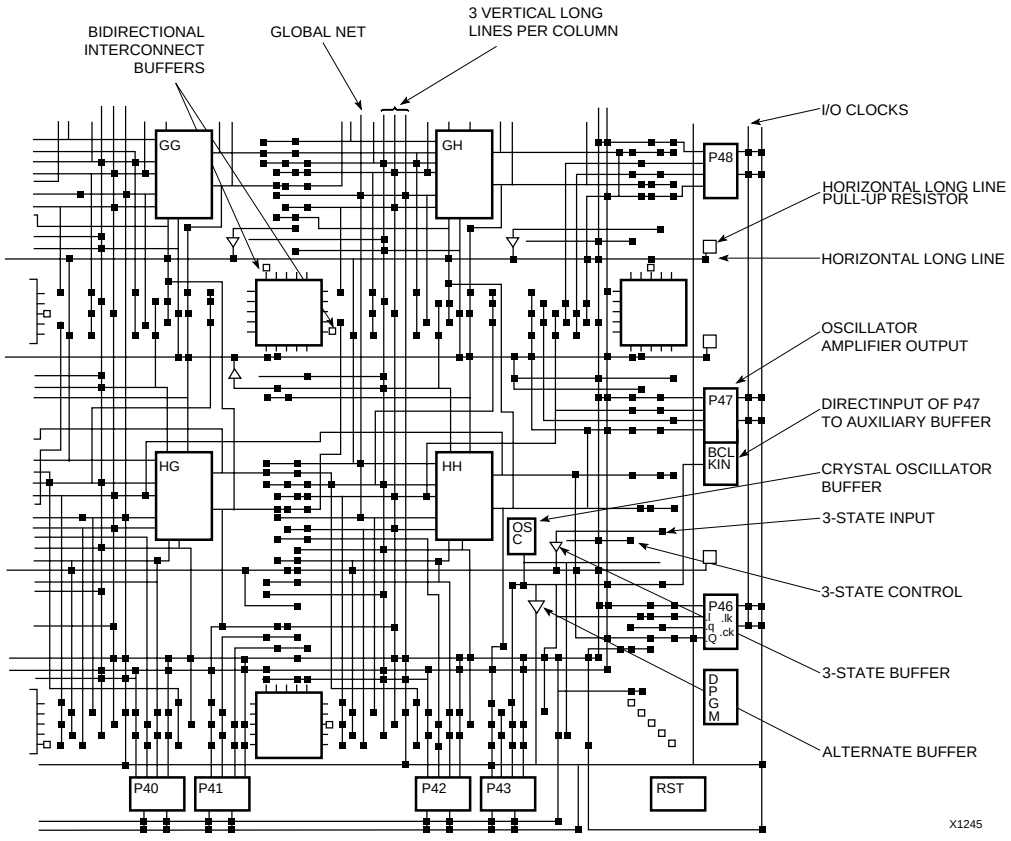


Figure 18: Design Editor.
An extra large view of possible interconnections in the lower right corner of the XC3020A.

Special Configuration Functions

The configuration data includes control over several special functions in addition to the normal user logic functions and interconnect.

- Input thresholds
- Readback disable
- DONE pull-up resistor
- DONE timing
- RESET timing
- Oscillator frequency divided by two

Each of these functions is controlled by configuration data bits which are selected as part of the normal development system bitstream generation process.

Input Thresholds

Prior to the completion of configuration all FPGA input thresholds are TTL compatible. Upon completion of configuration, the input thresholds become either TTL or CMOS compatible as programmed. The use of the TTL threshold option requires some additional supply current for threshold shifting. The exception is the threshold of the PWRDWN input and direct clocks which always have a CMOS input. Prior to the completion of configuration the user I/O pins each have a high impedance pull-up. The configuration program can be used to enable the IOB pull-up resistors in the Operational mode to act either as an input load or to avoid a floating input on an otherwise unused pin.

Readback

The contents of a Field Programmable Gate Array may be read back if it has been programmed with a bitstream in which the Readback option has been enabled. Readback may be used for verification of configuration and as a method of determining the state of internal logic nodes during debugging. There are three options in generating the configuration bitstream.

- “Never” inhibits the Readback capability.
- “One-time,” inhibits Readback after one Readback has been executed to verify the configuration.
- “On-command” allows unrestricted use of Readback.

Readback is accomplished without the use of any of the user I/O pins; only M0, M1 and CCLK are used. The initiation of Readback is produced by a Low to High transition of the M0/RTRIG (Read Trigger) pin. The CCLK input must then be driven by external logic to read back the configuration data. The first three Low-to-High CCLK transitions clock out dummy data. The subsequent Low-to-High CCLK transitions shift the data frame information out on the M1/RDATA (Read Data) pin. Note that the logic polarity is always inverted, a zero in configuration becomes a one in Readback, and vice versa. Note also that each Readback frame has one Start bit (read back as a one) but, unlike in configuration, each Readback frame has only one Stop bit (read back as a zero). The third leading dummy bit mentioned above can be considered the Start bit of the first frame. All data frames must be read back to complete the process and return the Mode Select and CCLK pins to their normal functions.

Readback data includes the current state of each CLB flip-flop, each input flip-flop or latch, and each device pad. These data are imbedded into unused configuration bit positions during Readback. This state information is used by the development system In-Circuit Verifier to provide visibility into the internal operation of the logic while the system is operating. To readback a uniform time-sample of all storage elements, it may be necessary to inhibit the system clock.

Reprogram

To initiate a re-programming cycle, the dual-function pin DONE/PROG must be given a High-to-Low transition. To reduce sensitivity to noise, the input signal is filtered for two cycles of the FPGA internal timing generator. When reprogram begins, the user-programmable I/O output buffers are disabled and high-impedance pull-ups are provided for the package pins. The device returns to the Clear state and clears the configuration memory before it indicates ‘initialized’. Since this Clear operation uses chip-individual internal timing, the master might complete the Clear operation and then start configuration before the slave has completed the Clear operation. To avoid this problem, the slave INIT pins must be AND-wired and used to force a RESET on the master (see Figure 25). Reprogram control is often implemented using an external open-collector driver which pulls DONE/PROG Low. Once a stable request is recognized, the DONE/PROG pin is held Low until the new configuration has been completed. Even if the re-program request is externally held Low beyond the configuration period, the FPGA will begin operation upon completion of configuration.

DONE Pull-up

DONE/PROG is an open-drain I/O pin that indicates the FPGA is in the operational state. An optional internal pull-up resistor can be enabled by the user of the development system. The DONE/PROG pins of multiple FPGAs in a daisy-chain may be connected together to indicate all are DONE or to direct them all to reprogram.

DONE Timing

The timing of the DONE status signal can be controlled by a selection to occur either a CCLK cycle before, or after, the outputs going active. See Figure 22. This facilitates control of external functions such as a PROM enable or holding a system in a wait state.

Master Parallel Mode

In Master Parallel mode, the lead FPGA directly addresses an industry-standard byte-wide EPROM and accepts eight data bits right before incrementing (or decrementing) the address outputs.

The eight data bits are serialized in the lead FPGA, which then presents the preamble data (and all data that overflows the lead device) on the DOUT pin. There is an internal delay of 1.5 CCLK periods, after the rising CCLK edge that accepts a byte of data, and also changes the EPROM address, until the falling CCLK edge that makes the LSB (D0) of this byte appear at DOUT. This means that DOUT changes on the falling CCLK edge, and the next device in the daisy chain accepts data on the subsequent rising CCLK edge.

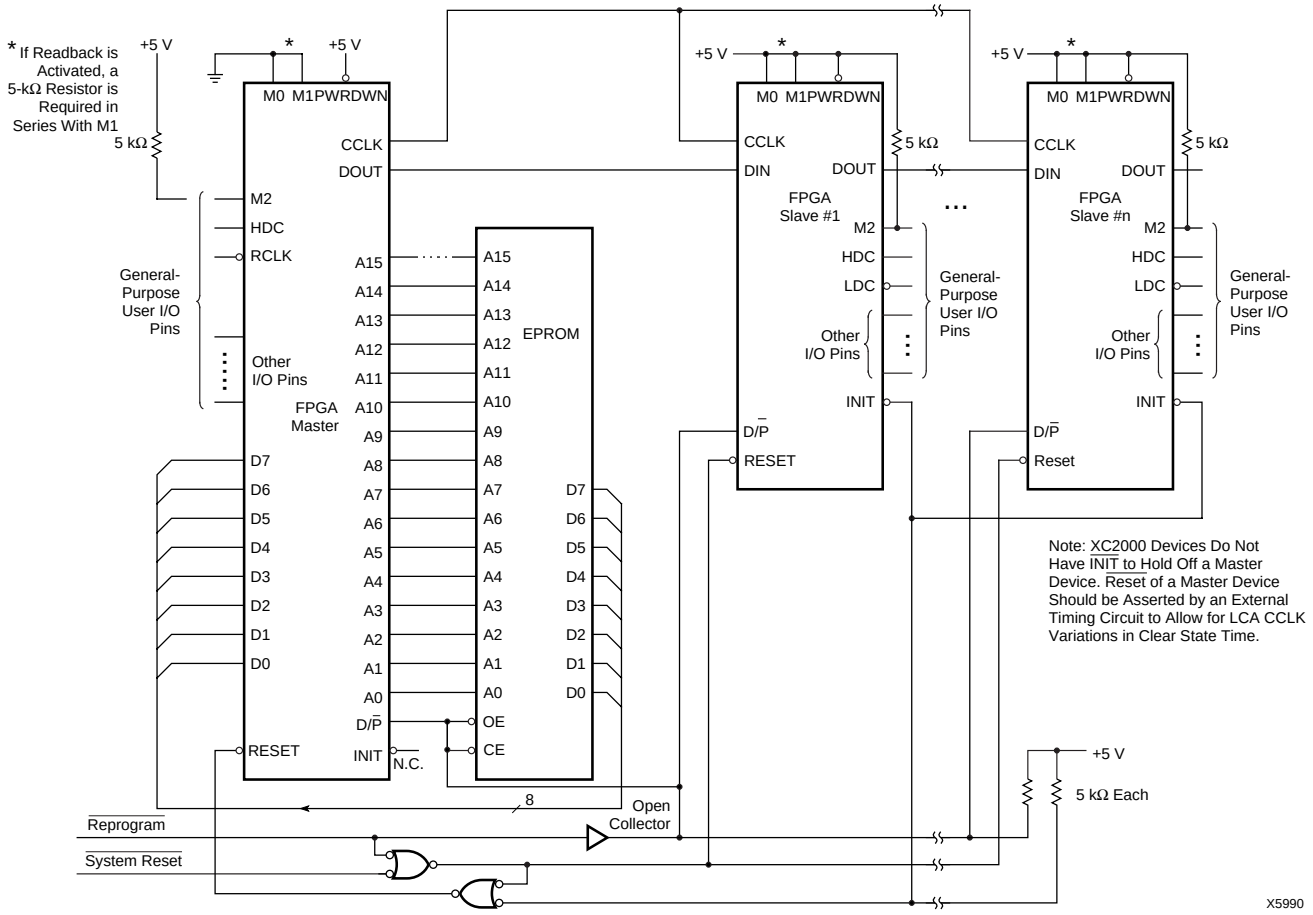
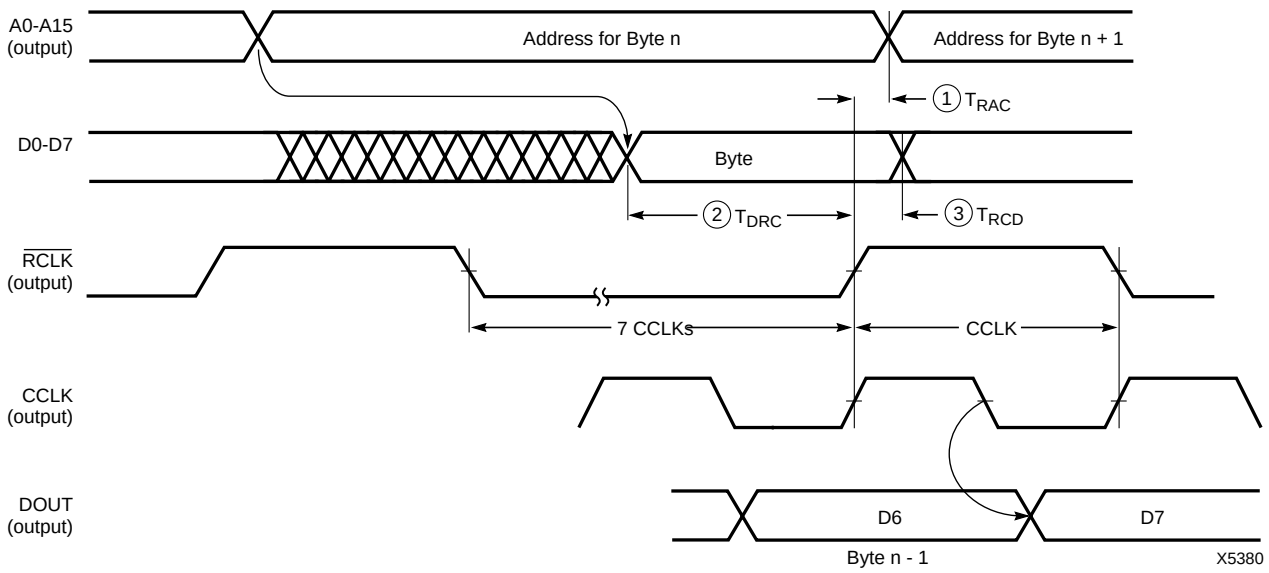


Figure 25: Master Parallel Mode Circuit Diagram



	Description	Symbol		Min	Max	Units
RCLK	To address valid	1	T_{RAC}	0	200	ns
	To data setup	2	T_{DRC}	60		ns
	To data hold	3	T_{RCD}	0		ns
	RCLK High		T_{RCH}	600		ns
	RCLK Low		T_{RCL}	4.0		µs

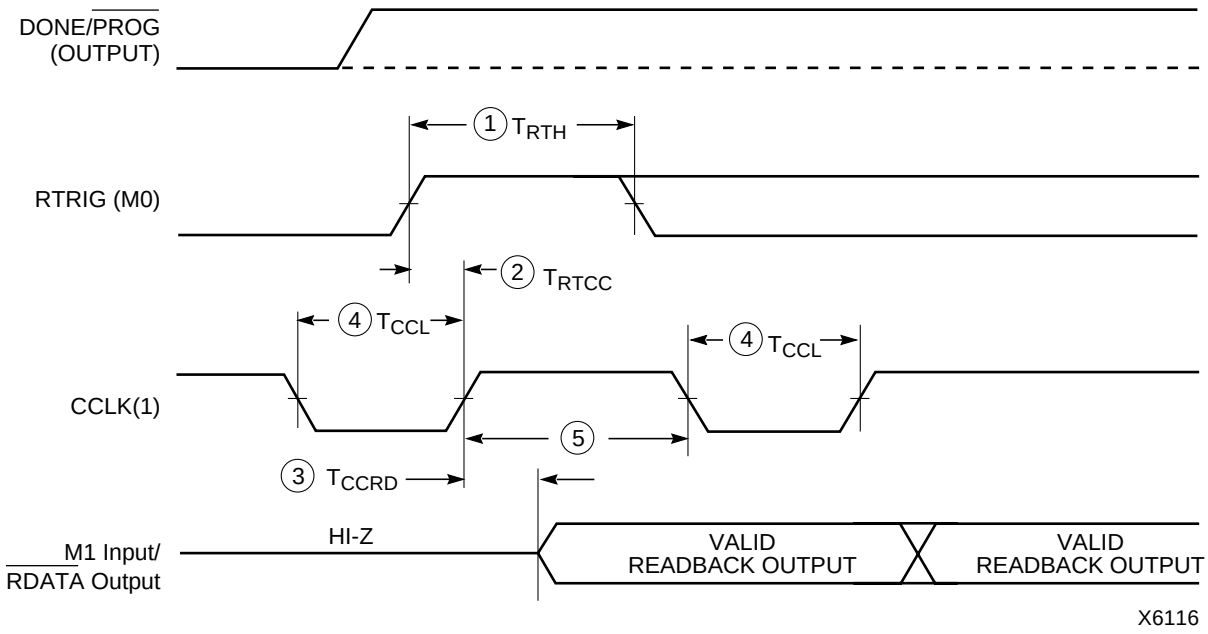
Notes: 1. At power-up, V_{CC} must rise from 2.0 V to V_{CC} min in less than 25 ms. If this is not possible, configuration can be delayed by holding $\overline{\text{RESET}}$ Low until VCC has reached 4.0 V (2.5 V for the XC3000L). A very long V_{CC} rise time of >100 ms, or a non-monotonically rising V_{CC} may require a >6-µs High level on $\overline{\text{RESET}}$, followed by a >6-µs Low level on $\overline{\text{RESET}}$ and D/P after V_{CC} has reached 4.0 V (2.5 V for the XC3000L).

2. Configuration can be controlled by holding $\overline{\text{RESET}}$ Low with or until after the $\overline{\text{INIT}}$ of all daisy-chain slave-mode devices is High.

This timing diagram shows that the EPROM requirements are extremely relaxed:
EPROM access time can be longer than 4000 ns. EPROM data output has no hold time requirements.

Figure 26: Master Parallel Mode Programming Switching Characteristics

Program Readback Switching Characteristics



	Description	Symbol		Min	Max	Units
RTRIG	RTRIG High	1	T_{RTH}	250		ns
CCLK	RTRIG setup	2	T_{RTCC}	200		ns
	RDATA delay	3	T_{CCRD}		100	ns
	High time	4	T_{CCHR}	0.5		µs
	Low time	5	T_{CCLR}	0.5	5	µs

Notes: 1. During Readback, CCLK frequency may not exceed 1 MHz.
2. RETRIG (M0 positive transition) shall not be done until after one clock following active I/O pins.
3. Readback should not be initiated until configuration is complete.
4. T_{CCLR} is 5 µs min to 15 µs max for XC3000L.

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Device Performance

The XC3000 families of FPGAs can achieve very high performance. This is the result of

- A sub-micron manufacturing process, developed and continuously being enhanced for the production of state-of-the-art CMOS SRAMs.
- Careful optimization of transistor geometries, circuit design, and lay-out, based on years of experience with the XC3000 family.
- A look-up table based, coarse-grained architecture that can collapse multiple-layer combinatorial logic into a single function generator. One CLB can implement up to four layers of conventional logic in as little as 1.5 ns.

Actual system performance is determined by the timing of critical paths, including the delay through the combinatorial and sequential logic elements within CLBs and IOBs, plus the delay in the interconnect routing. The AC-timing specifications state the worst-case timing parameters for the various logic resources available in the XC3000-families architecture. Figure 31 shows a variety of elements involved in determining system performance.

Logic block performance is expressed as the propagation time from the interconnect point at the input to the block to the output of the block in the interconnect area. Since combinatorial logic is implemented with a memory lookup table within a CLB, the combinatorial delay through the CLB, called T_{ILO}, is always the same, regardless of the function being implemented. For the combinatorial logic function driving the data input of the storage element, the critical timing is data set-up relative to the clock edge provided to the flip-flop element. The delay from the clock source to the output of the logic block is critical in the timing signals produced by storage elements. Loading of a logic-block output is limited only by the resulting propagation delay of the larger interconnect network. Speed performance of the logic block is a function of supply voltage and temperature. See Figure 32.

Interconnect performance depends on the routing resources used to implement the signal path. Direct interconnects to the neighboring CLB provide an extremely fast path. Local interconnects go through switch matrices (magic boxes) and suffer an RC delay, equal to the resistance of the pass transistor multiplied by the capacitance of the driven metal line. Longlines carry the signal across the length or breadth of the chip with only one access delay. Generous on-chip signal buffering makes performance relatively insensitive to signal fan-out; increasing fan-out from 1 to 8 changes the CLB delay by only 10%. Clocks can be distributed with two low-skew clock distribution networks.

The tools in the Development System used to place and route a design in an XC3000 FPGA automatically calculate the actual maximum worst-case delays along each signal path. This timing information can be back-annotated to the design's netlist for use in timing simulation or examined with, a static timing analyzer.

Actual system performance is applications dependent. The maximum clock rate that can be used in a system is determined by the critical path delays within that system. These delays are combinations of incremental logic and routing delays, and vary from design to design. In a synchronous system, the maximum clock rate depends on the number of combinatorial logic layers between re-synchronizing flip-flops. Figure 33 shows the achievable clock rate as a function of the number of CLB layers.

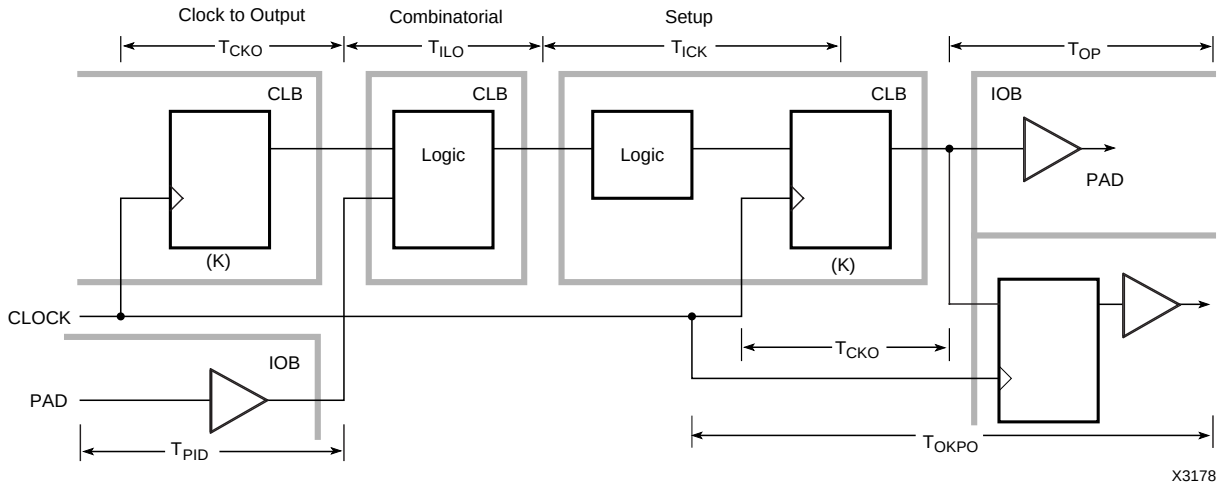


Figure 31: Primary Block Speed Factors. Actual timing is a function of various block factors combined with routing. factors. Overall performance can be evaluated with the timing calculator or by an optional simulation.

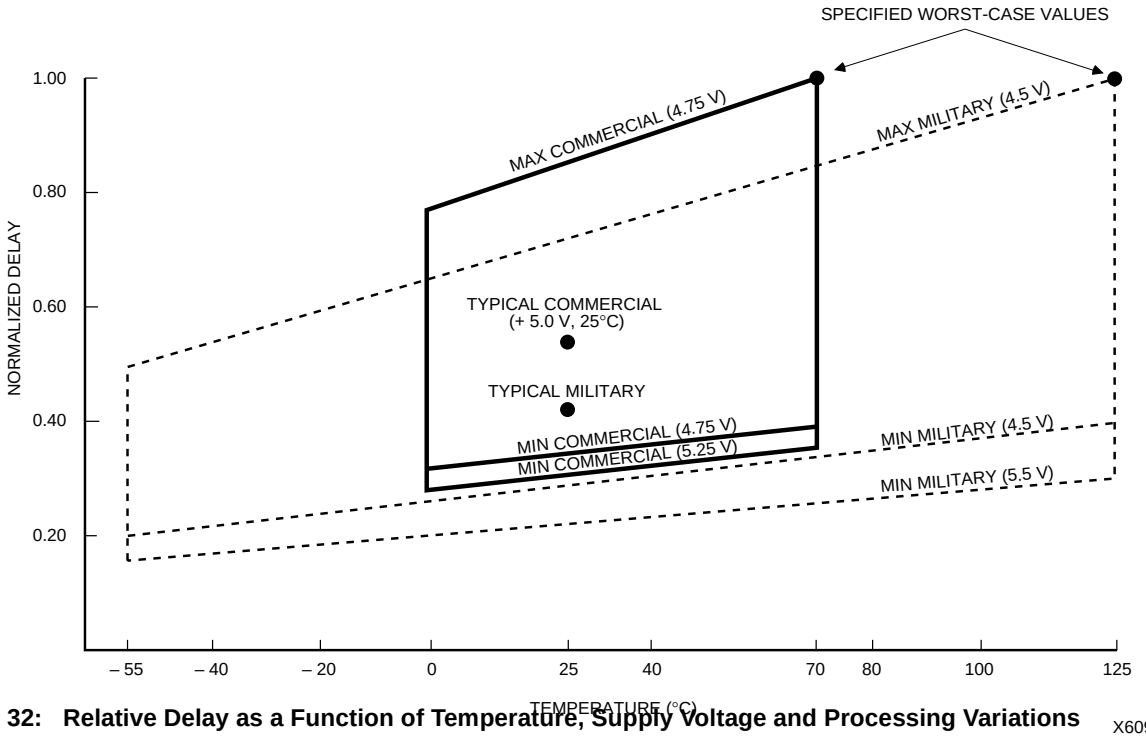


Figure 32: Relative Delay as a Function of Temperature, Supply Voltage and Processing Variations

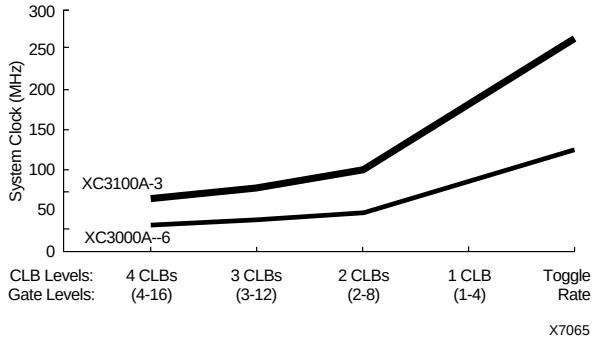


Figure 33: Clock Rate as a Function of Logic Complexity (Number of Combinational Levels between Flip-Flops)

Power

Power Distribution

Power for the FPGA is distributed through a grid to achieve high noise immunity and isolation between logic and I/O. Inside the FPGA, a dedicated V_{CC} and ground ring surrounding the logic array provides power to the I/O drivers. An independent matrix of V_{CC} and groundlines supplies the interior logic of the device. This power distribution grid provides a stable supply and ground for all internal logic, providing the external package power pins are all connected and appropriately decoupled. Typically a 0.1-µF capacitor connected near the V_{CC} and ground pins will provide adequate decoupling.

Output buffers capable of driving the specified 4- or 8-mA loads under worst-case conditions may be capable of driving as much as 25 to 30 times that current in a best case. Noise can be reduced by minimizing external load capacitance and reducing simultaneous output transitions in the same direction. It may also be beneficial to locate heavily loaded output buffers near the ground pads. The I/O Block output buffers have a slew-limited mode which should be used where output rise and fall times are not speed critical. Slew-limited outputs maintain their dc drive capability, but generate less external reflections and internal noise.

Dynamic Power Consumption

	XC3042A	XC3042L	XC3142A	
One CLB driving three local interconnects	0.25	0.17	0.25	mW per MHz
One global clock buffer and clock line	2.25	1.40	1.70	mW per MHz
One device output with a 50 pF load	1.25	1.25	1.25	mW per MHz

Power Consumption

The Field Programmable Gate Array exhibits the low power consumption characteristic of CMOS ICs. For any design, the configuration option of TTL chip input threshold requires power for the threshold reference. The power required by the static memory cells that hold the configuration data is very low and may be maintained in a power-down mode.

Typically, most of power dissipation is produced by external capacitive loads on the output buffers. This load and frequency dependent power is 25 µW/pF/MHz per output. Another component of I/O power is the external dc loading on all output pins.

Internal power dissipation is a function of the number and size of the nodes, and the frequency at which they change. In an FPGA, the fraction of nodes changing on a given clock is typically low (10-20%). For example, in a long binary counter, the total activity of all counter flip-flops is equivalent to that of only two CLB outputs toggling at the clock frequency. Typical global clock-buffer power is between 2.0 mW/MHz for the XC3020A and 3.5 mW/MHz for the XC3090A. The internal capacitive load is more a function of interconnect than fan-out. With a typical load of three general interconnect segments, each CLB output requires about 0.25 mW per MHz of its output frequency.

Because the control storage of the FPGA is CMOS static memory, its cells require a very low standby current for data retention. In some systems, this low data retention current characteristic can be used as a method of preserving configurations in the event of a primary power loss. The FPGA has built in powerdown logic which, when activated, will disable normal operation of the device and retain only the configuration data. All internal operation is suspended and output buffers are placed in their high-impedance state with no pull-ups. Different from the XC3000 family which can be powered down to a current consumption of a few microamps, the XC3100A draws 5 mA, even in power-down. This makes power-down operation less meaningful. In contrast, I_{CCPD} for the XC3000L is only 10 µA.

To force the FPGA into the Powerdown state, the user must pull the $\overline{\text{PWRDWN}}$ pin Low and continue to supply a retention voltage to the V_{CC} pins. When normal power is restored, V_{CC} is elevated to its normal operating voltage and $\overline{\text{PWRDWN}}$ is returned to a High. The FPGA resumes operation with the same internal sequence that occurs at the conclusion of configuration. Internal-I/O and logic-block storage elements will be reset, the outputs will become enabled and the DONE/$\overline{\text{PROG}}$ pin will be released.

When V_{CC} is shut down or disconnected, some power might unintentionally be supplied from an incoming signal driving an I/O pin. The conventional electrostatic input protection is implemented with diodes to the supply and ground. A positive voltage applied to an input (or output) will cause the positive protection diode to conduct and drive the V_{CC} connection. This condition can produce invalid power conditions and should be avoided. A large series resistor might be used to limit the current or a bipolar buffer may be used to isolate the input signal.

Pin Descriptions

Permanently Dedicated Pins

V_{CC}

Two to eight (depending on package type) connections to the positive V supply voltage. All must be connected.

GND

Two to eight (depending on package type) connections to ground. All must be connected.

$\overline{\text{PWRDWN}}$

A Low on this CMOS-compatible input stops all internal activity, but retains configuration. All flip-flops and latches are reset, all outputs are 3-stated, and all inputs are interpreted as High, independent of their actual level. When $\overline{\text{PWDWN}}$ returns High, the FPGA becomes operational with DONE Low for two cycles of the internal 1-MHz clock. Before and during configuration, $\overline{\text{PWRDWN}}$ must be High. If not used, $\overline{\text{PWRDWN}}$ must be tied to V_{CC}.

$\overline{\text{RESET}}$

This is an active Low input which has three functions.

Prior to the start of configuration, a Low input will delay the start of the configuration process. An internal circuit senses the application of power and begins a minimal time-out cycle. When the time-out and $\overline{\text{RESET}}$ are complete, the levels of the M lines are sampled and configuration begins.

If $\overline{\text{RESET}}$ is asserted during a configuration, the FPGA is re-initialized and restarts the configuration at the termination of $\overline{\text{RESET}}$.

If $\overline{\text{RESET}}$ is asserted after configuration is complete, it provides a global asynchronous $\overline{\text{RESET}}$ of all IOB and CLB storage elements of the FPGA.

CCLK

During configuration, Configuration Clock is an output of an FPGA in Master mode or Peripheral mode, but an input in Slave mode. During Readback, CCLK is a clock input for shifting configuration data out of the FPGA.

CCLK drives dynamic circuitry inside the FPGA. The Low time may, therefore, not exceed a few microseconds. When used as an input, CCLK must be “parked High”. An internal pull-up resistor maintains High when the pin is not being driven.

DONE/$\overline{\text{PROG}}$ (D/$\overline{\text{P}}$)

DONE is an open-drain output, configurable with or without an internal pull-up resistor of 2 to 8 k Ω. At the completion of configuration, the FPGA circuitry becomes active in a synchronous order; DONE is programmed to go active High one cycle either before or after the outputs go active.

Once configuration is done, a High-to-Low transition of this pin will cause an initialization of the FPGA and start a reconfiguration.

M0/RTRIG

As Mode 0, this input is sampled on power-on to determine the power-on delay (2^{14} cycles if M0 is High, 2^{16} cycles if M0 is Low). Before the start of configuration, this input is again sampled together with M1, M2 to determine the configuration mode to be used.

A Low-to-High input transition, after configuration is complete, acts as a Read Trigger and initiates a Readback of configuration and storage-element data clocked by CCLK. By selecting the appropriate Readback option when generating the bitstream, this operation may be limited to a single Readback, or be inhibited altogether.

M1/$\overline{\text{RDATA}}$

As Mode 1, this input and M0, M2 are sampled before the start of configuration to establish the configuration mode to be used. If Readback is never used, M1 can be tied directly to ground or V_{CC}. If Readback is ever used, M1 must use a 5-kΩ resistor to ground or V_{CC}, to accommodate the RDATA output.

As an active-Low Read Data, after configuration is complete, this pin is the output of the Readback data.

User I/O Pins That Can Have Special Functions

M2

During configuration, this input has a weak pull-up resistor. Together with M0 and M1, it is sampled before the start of configuration to establish the configuration mode to be used. After configuration, this pin is a user-programmable I/O pin.

HDC

During configuration, this output is held at a High level to indicate that configuration is not yet complete. After configuration, this pin is a user-programmable I/O pin.

$\overline{\text{LDC}}$

During Configuration, this output is held at a Low level to indicate that the configuration is not yet complete. After configuration, this pin is a user-programmable I/O pin. $\overline{\text{LDC}}$ is particularly useful in Master mode as a Low enable for an EPROM, but it must then be programmed as a High after configuration.

$\overline{\text{INIT}}$

This is an active Low open-drain output with a weak pull-up and is held Low during the power stabilization and internal clearing of the configuration memory. It can be used to indicate status to a configuring microprocessor or, as a wired

XC3000A Absolute Maximum Ratings

Symbol	Description		Units
V_{CC}	Supply voltage relative to GND	–0.5 to +7.0	V
V_{IN}	Input voltage with respect to GND	–0.5 to V_{CC} +0.5	V
V_{TS}	Voltage applied to 3-state output	–0.5 to V_{CC} +0.5	V
T_{STG}	Storage temperature (ambient)	–65 to +150	°C
T_{SOL}	Maximum soldering temperature (10 s @ 1/16 in.)	+260	°C
T_J	Junction temperature plastic	+125	°C
	Junction temperature ceramic	+150	°C

Note: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

XC3000A Global Buffer Switching Characteristics Guidelines

	Speed Grade	-7	-6	
Description	**Symbol**	**Max**	**Max**	**Units**
Global and Alternate Clock Distribution[1]				
Either: **Normal** IOB input pad through clock buffer to any CLB or IOB clock input	T_{PID}	7.5	7.0	ns
Or: **Fast** (CMOS only) input pad through clock buffer to any CLB or IOB clock input	T_{PIDC}	6.0	5.7	ns
TBUF driving a Horizontal Longline (L.L.)[1]				
I to L.L. while T is Low (buffer active)	T_{IO}	4.5	4.0	ns
T↓ to L.L. active and valid with single pull-up resistor	T_{ON}	9.0	8.0	ns
T↓ to L.L. active and valid with pair of pull-up resistors	T_{ON}	11.0	10.0	ns
T↑ to L.L. High with single pull-up resistor	T_{PUS}	16.0	14.0	ns
T↑ to L.L. High with pair of pull-up resistors	T_{PUF}	10.0	8.0	ns
BIDI Bidirectional buffer delay	T_{BIDI}	1.7	1.5	ns

Note: 1. Timing is based on the XC3042A, for other devices see timing calculator.

XC3000A IOB Switching Characteristics Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Since many internal timing parameters cannot be measured directly, they are derived from benchmark timing patterns. The following guidelines reflect worst-case values over the recommended operating conditions. For more detailed, more precise, and more up-to-date timing information, use the values provided by the timing calculator and used in the simulator.

		Speed Grade		-7		-6		
Description		**Symbol**		**Min**	**Max**	**Min**	**Max**	**Units**
Propagation Delays (Input)								
Pad to Direct In (I)		3	T_{PID}		4.0		3.0	ns
Pad to Registered In (Q) with latch transparent			T_{PTG}		15.0		14.0	ns
Clock (IK) to Registered In (Q)		4	T_{IKRI}		3.0		2.5	ns
Set-up Time (Input)								
Pad to Clock (IK) set-up time		1	T_{PICK}	14.0		12.0		ns
Propagation Delays (Output)								
Clock (OK) to Pad	(fast)	7	T_{OKPO}		8.0		7.0	ns
same	(slew rate limited)	7	T_{OKPO}		18.0		15.0	ns
Output (O) to Pad	(fast)	10	T_{OPF}		6.0		5.0	ns
same	(slew-rate limited)	10	T_{OPS}		16.0		13.0	ns
3-state to Pad begin hi-Z	(fast)	9	T_{TSHZ}		10.0		9.0	ns
same	(slew-rate limited)	9	T_{TSHZ}		20.0		12.0	ns
3-state to Pad active and valid	(fast)	8	T_{TSON}		11.0		10.0	ns
same	(slew -rate limited)	8	T_{TSON}		21.0		18.0	ns
Set-up and Hold Times (Output)								
Output (O) to clock (OK) set-up time		5	T_{OOK}	8.0		7.0		ns
Output (O) to clock (OK) hold time		6	T_{OKO}	0		0		ns
Clock								
Clock High time		11	T_{IOH}	4.0		3.5		ns
Clock Low time		12	T_{IOL}	4.0		3.5		ns
Max. flip-flop toggle rate			F_{CLK}	113.0		135.0		MHz
Global Reset Delays (based on XC3042A)								
$\overline{\text{RESET}}$ Pad to Registered In	(Q)	13	T_{RRI}		24.0		23.0	ns
$\overline{\text{RESET}}$ Pad to output pad	(fast)	15	T_{RPO}		33.0		29.0	ns
	(slew-rate limited)	15	T_{RPO}		43.0		37.0	ns

Notes:
1. Timing is measured at pin threshold, with 50 pF external capacitive loads (incl. test fixture). Typical slew rate limited output rise/fall times are approximately four times longer.
2. Voltage levels of unused (bonded and unbonded) pads must be valid logic levels. Each can be configured with the internal pull-up resistor or alternatively configured as a driven output or driven from an external source.
3. Input pad set-up time is specified with respect to the internal clock (ik). In order to calculate system set-up time, subtract clock delay (pad to ik) from the input pad set-up time value. Input pad holdtime with respect to the internal clock (ik) is negative. This means that pad level changes immediately before the internal clock edge (ik) will not be recognized.
4. T_{PID}, T_{PTG}, and T_{PICK} are 3 ns higher for XTL2 when the pin is configured as a user input.

XC3000L Switching Characteristics

Xilinx maintains test specifications for each product as controlled documents. To insure the use of the most recently released device performance parameters, please request a copy of the current test-specification revision.

XC3000L Operating Conditions

Symbol	Description	Min	Max	Units
V_{CC}	Supply voltage relative to GND Commercial 0°C to +85°C junction	3.0	3.6	V
V_{IH}	High-level input voltage — TTL configuration	2.0	V_{CC}+0.3	V
V_{IL}	Low-level input voltage — TTL configuration	-0.3	0.8	V
T_{IN}	Input signal transition time		250	ns

Notes: 1. At junction temperatures above those listed as Operating Conditions, all delay parameters increase by 0.3% per °C.
2. Although the present (1996) devices operate over the full supply voltage range from 3.0 to 5.25 V, Xilinx reserves the right to restrict operation to the 3.0 to 3.6 V range later, when smaller device geometries might preclude operation at 5V. Operating conditions are guaranteed in the 3.0 – 3.6 V V_{CC} range.

XC3000L DC Characteristics Over Operating Conditions

Symbol	Description	Min	Max	Units
V_{OH}	High-level output voltage (@ I_{OH} = –4.0 mA, V_{CC} min)	2.40		V
V_{OL}	Low-level output voltage (@ I_{OL} = 4.0 mA, V_{CC} min)		0.40	V
V_{OH}	High-level output voltage (@ I_{OH} = –4.0 mA, V_{CC} min)	V_{CC} -0.2		V
V_{OL}	Low-level output voltage (@ I_{OL} = 4.0 mA, V_{CC} min)		0.2	V
V_{CCPD}	Power-down supply voltage (PWRDWN must be Low)	2.30		V
I_{CCPD}	Power-down supply current ($V_{CC(MAX)}$ @ T_{MAX})		10	µA
I_{CCO}	Quiescent FPGA supply current in addition to I_{CCPD}[1] Chip thresholds programmed as CMOS levels		 20	 µA
I_{IL}	Input Leakage Current	–10	+10	µA
C_{IN}	Input capacitance, all packages except PGA175 (sample tested) All Pins except XTL1 and XTL2 XTL1 and XTL2		 10 15	 pF pF
	Input capacitance, PGA 175 (sample tested) All Pins except XTL1 and XTL2 XTL1 and XTL2		 15 20	 pF pF
I_{RIN}	Pad pull-up (when selected) @ V_{IN} = 0 V[3]	0.01	0.17	mA
I_{RLL}	Horizontal Longline pull-up (when selected) @ logic Low		2.50	mA

Notes: 1. With no output current loads, no active input or Longline pull-up resistors, all package pins at V_{CC} or GND, and the FPGA device configured with a tie option. I_{CCO} is in addition to I_{CCPD}.
2. Total continuous output sink current may not exceed 100 mA per ground pin. Total continuous output source may not exceed 100 mA per V_{CC} pin. The number of ground pins varies from the XC3020L to the XC3090L.
3. Not tested. Allows an undriven pin to float High. For any other purpose, use an external pull-up.

XC3000L Absolute Maximum Ratings

Symbol	Description		Units
V_{CC}	Supply voltage relative to GND	–0.5 to +7.0	V
V_{IN}	Input voltage with respect to GND	–0.5 to V_{CC} +0.5	V
V_{TS}	Voltage applied to 3-state output	–0.5 to V_{CC} +0.5	V
T_{STG}	Storage temperature (ambient)	–65 to +150	°C
T_{SOL}	Maximum soldering temperature (10 s @ 1/16 in.)	+260	°C
T_J	Junction temperature plastic	+125	°C
	Junction temperature ceramic	+150	°C

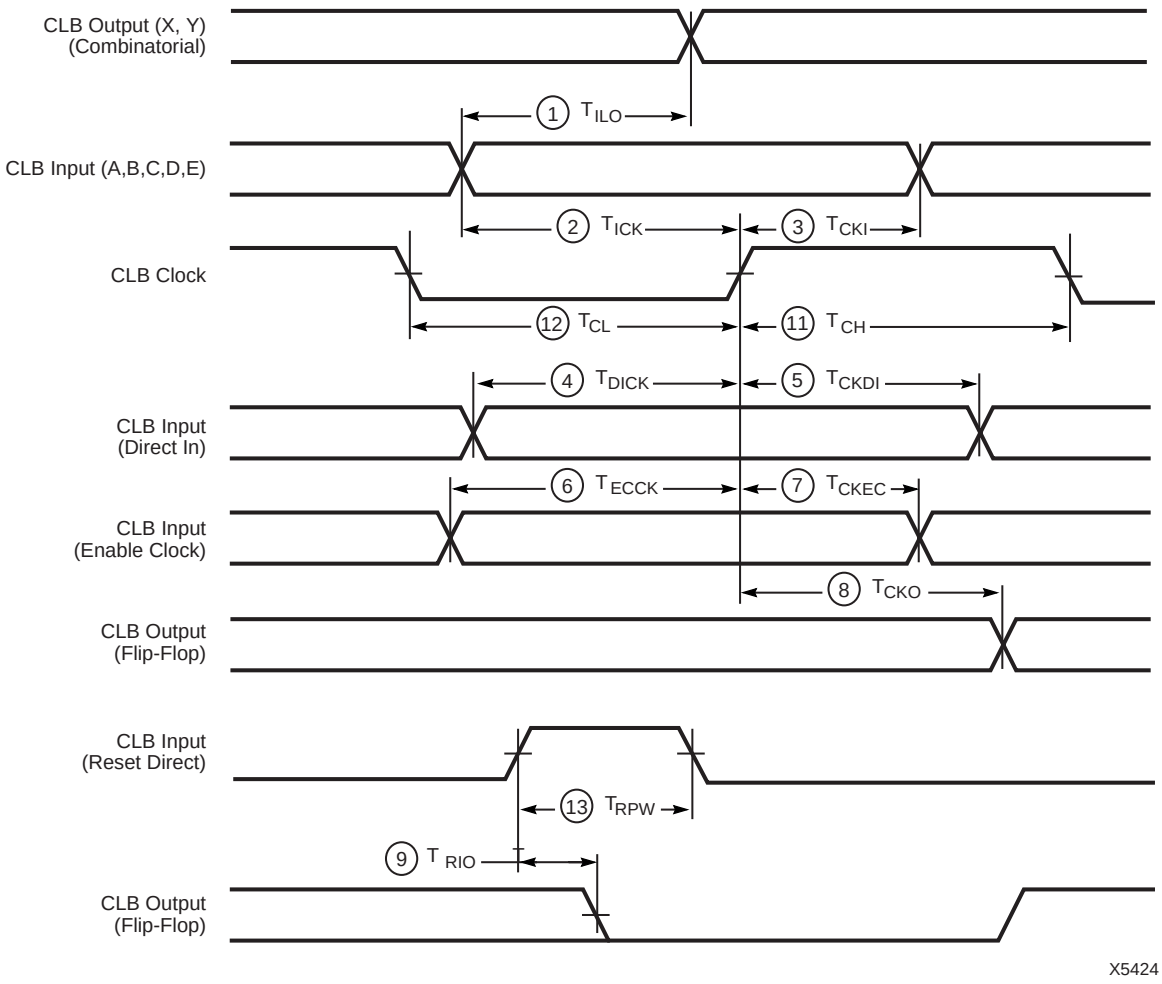
Note: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

XC3000L Global Buffer Switching Characteristics Guidelines

	Speed Grade	-8	
Description	**Symbol**	**Max**	**Units**
Global and Alternate Clock Distribution[1]			
Either: **Normal** IOB input pad through clock buffer to any CLB or IOB clock input	T_{PID}	9.0	ns
Or: **Fast** (CMOS only) input pad through clock buffer to any CLB or IOB clock input	T_{PIDC}	7.0	ns
TBUF driving a Horizontal Longline (L.L.)[1]			
I to L.L. while T is Low (buffer active)	T_{IO}	5.0	ns
T↓ to L.L. active and valid with single pull-up resistor	T_{ON}	12.0	ns
T↑ to L.L. High with single pull-up resistor	T_{PUS}	24.0	ns
BIDI			
Bidirectional buffer delay	T_{BIDI}	2.0	ns

Notes: 1. Timing is based on the XC3042A, for other devices see timing calculator.
2. The use of two pull-up resistors per Longline, available on other XC3000 devices, is not a valid option for XC3000L devices.

XC3000L CLB Switching Characteristics Guidelines (continued)



XC3100A Absolute Maximum Ratings

Symbol	Description		Units
V_{CC}	Supply voltage relative to GND	–0.5 to +7.0	V
V_{IN}	Input voltage with respect to GND	–0.5 to V_{CC} +0.5	V
V_{TS}	Voltage applied to 3-state output	–0.5 to V_{CC} +0.5	V
T_{STG}	Storage temperature (ambient)	–65 to +150	°C
T_{SOL}	Maximum soldering temperature (10 s @ 1/16 in.)	+260	°C
T_J	Junction temperature plastic	+125	°C
	Junction temperature ceramic	+150	°C

Note: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

XC3100A Global Buffer Switching Characteristics Guidelines

Speed Grade		-4	-3	-2	-1	-09	
Description	**Symbol**	**Max**	**Max**	**Max**	**Max**	**Max**	**Units**
Global and Alternate Clock Distribution[1]							
Either: **Normal** IOB input pad through clock buffer to any CLB or IOB clock input	T_{PID}	6.5	5.6	4.7	4.3	3.9	ns
Or: **Fast** (CMOS only) input pad through clock buffer to any CLB or IOB clock input	T_{PIDC}	5.1	4.3	3.7	3.5	3.1	ns
TBUF driving a Horizontal Longline (L.L.)[1]							
I to L.L. while T is Low (buffer active) (XC3100)	T_{IO}	3.7	3.1				ns
(XC3100A)	T_{IO}	3.6	3.1	3.1	2.9	2.1	ns
T↓ to L.L. active and valid with single pull-up resistor	T_{ON}	5.0	4.2	4.2	4.0	3.1	ns
T↓ to L.L. active and valid with pair of pull-up resistors	T_{ON}	6.5	5.7	5.7	5.5	4.6	ns
T↑ to L.L. High with single pull-up resistor	T_{PUS}	13.5	11.4	11.4	10.4	8.9	ns
T↑ to L.L. High with pair of pull-up resistors	T_{PUF}	10.5	8.8	8.1	7.1	5.9	ns
BIDI							
Bidirectional buffer delay	T_{BIDI}	1.2	1.0	0.9	0.85	0.75	ns
						Prelim	

Note: 1. Timing is based on the XC3142A, for other devices see timing calculator.
The use of two pull-up resistors per longline, available on other XC3000 devices, is not a valid design option for XC3100A devices.

XC3100L Switching Characteristics

Xilinx maintains test specifications for each product as controlled documents. To insure the use of the most recently released device performance parameters, please request a copy of the current test-specification revision.

XC3100L Operating Conditions

Symbol	Description	Min	Max	Units
V_{CC}	Supply voltage relative to GND Commercial 0°C to +85°C junction	3.0	3.6	V
V_{IH}	High-level input voltage	2.0	V_{CC} + 0.3	V
V_{IL}	Low-level input voltage	-0.3	0.8	V
T_{IN}	Input signal transition time		250	ns

Notes: 1. At junction temperatures above those listed as Operating Conditions, all delay parameters increase by 0.3% per °C.
2. Although the present (1996) devices operate over the full supply voltage range from 3.0 V to 5.25 V, Xilinx reserves the right to restrict operation to the 3.0 and 3.6 V range later, when smaller device geometries might preclude operation @ 5 V. Operating conditions are guaranteed in the 3.0 – 3.6 V V_{CC} range.

XC3100L DC Characteristics Over Operating Conditions

Symbol	Description	Min	Max	Units
V_{OH}	High-level output voltage (@ I_{OH} = -4.0 mA, V_{CC} min)	2.4		V
	High-level output voltage (@ I_{OH} = -100.0 µA, V_{CC} min)	V_{CC} -0.2		V
V_{OL}	Low-level output voltage (@ I_{OH} = 4.0 mA, V_{CC} min)		0.40	V
	Low-level output voltage (@ I_{OH} = +100.0 µA, V_{CC} min)		0.2	V
V_{CCPD}	Power-down supply voltage (PWRDWN must be Low)	2.30		V
I_{CCO}	Quiescent FPGA supply current Chip thresholds programmed as CMOS levels[1]		1.5	mA
I_{IL}	Input Leakage Current	-10	+10	µA
C_{IN}	Input capacitance (sample tested) All pins except XTL1 and XTL2 XTL1 and XTL2		 10 15	 pF pF
I_{RIN}	Pad pull-up (when selected) @ V_{IN} = 0 V [3]	0.02	0.17	mA
I_{RLL}	Horizontal long line pull-up (when selected) @ logic Low	0.20	2.80	mA

Notes: 1. With no output current loads, no active input or long line pull-up resistors, all package pins at V_{CC} or GND, and the FPGA configured with a tie option.
2. Total continuous output sink current may not exceed 100 mA per ground pin. Total continuous output source current may not exceed 100 mA per V_{CC} pin. The number of ground pins varies from the XC3142L to the XC3190L.
3. Not tested. Allows undriven pins to float High. For any other purpose, use an external pull-up.

XC3000 Series Pin Assignments

Xilinx offers the six different array sizes in the XC3000 families in a variety of surface-mount and through-hole package types, with pin counts from 44 to 208.

Each chip is offered in several package types to accommodate the available PC board space and manufacturing technology. Most package types are also offered with different chips to accommodate design changes without the need for PC board changes.

Note that there is no perfect match between the number of bonding pads on the chip and the number of pins on a package. In some cases, the chip has more pads than there are pins on the package, as indicated by the information (“unused” pads) below the line in the following table. The IOBs of the unconnected pads can still be used as storage elements if the specified propagation delays and set-up times are acceptable.

In other cases, the chip has fewer pads than there are pins on the package; therefore, some package pins are not connected (n.c.), as shown above the line in the following table.

XC3000 Series 44-Pin PLCC Pinouts

XC3000A, XC3000L, and XC3100A families have identical pinouts

Pin No.	XC3030A
1	GND
2	I/O
3	I/O
4	I/O
5	I/O
6	I/O
7	PWRDWN
8	TCLKIN-I/O
9	I/O
10	I/O
11	I/O
12	VCC
13	I/O
14	I/O
15	I/O
16	M1-RDATA
17	M0-RTRIG
18	M2-I/O
19	HDC-I/O
20	LDC-I/O
21	I/O
22	$\overline{\text{INIT}}$-I/O

Pin No.	XC3030A
23	GND
24	I/O
25	I/O
26	XTL2(IN)-I/O
27	RESET
28	DONE-PGM
29	I/O
30	XTL1(OUT)-BCLK-I/O
31	I/O
32	I/O
33	I/O
34	**VCC**
35	I/O
36	I/O
37	I/O
38	DIN-I/O
39	DOUT-I/O
40	CCLK
41	I/O
42	I/O
43	I/O
44	I/O

Peripheral mode and Master Parallel mode are not supported in the PC44 package

XC3000 Series 64-Pin Plastic VQFP Pinouts

XC3000A, XC3000L, and XC3100A families have identical pinouts

Pin No.	XC3030A
1	A0-WS-I/O
2	A1-CS2-I/O
3	A2-I/O
4	A3-I/O
5	A4-I/O
6	A14-I/O
7	A5-I/O
8	**GND**
9	A13-I/O
10	A6-I/O
11	A12-I/O
12	A7-I/O
13	A11-I/O
14	A8-I/O
15	A10-I/O
16	A9-I/O
17	PWRDN
18	TCLKIN-I/O
19	I/O
20	I/O
21	I/O
22	I/O
23	I/O
24	**VCC**
25	I/O
26	I/O
27	I/O
28	I/O
29	I/O
30	I/O
31	M1-$\overline{\text{RDATA}}$
32	M0-RTRIG

Pin No.	XC3030A
33	M2-I/O
34	HDC-I/O
35	I/O
36	$\overline{\text{LDC}}$-I/O
37	I/O
38	I/O
39	I/O
40	$\overline{\text{INIT}}$-I/O
41	**GND**
42	I/O
43	I/O
44	I/O
45	I/O
46	I/O
47	XTAL2(IN)-I/O
48	$\overline{\text{RESET}}$
49	DONE-PG
50	D7-I/O
51	XTAL1(OUT)-BCLKIN-I/O
52	D6-I/O
53	D5-I/O
54	$\overline{\text{CS0}}$-I/O
55	D4-I/O
56	VCC
57	D3-I/O
58	$\overline{\text{CS1}}$-I/O
59	D2-I/O
60	D1-I/O
61	RDY/$\overline{\text{BUSY}}$-RCLK-I/O
62	D0-DIN-I/O
63	DOUT-I/O
64	CCLK

XC3000 Series 160-Pin PQFP Pinouts

XC3000A, XC3000L, XC3100A, and XC3100L families have identical pinouts

PQFP Pin Number	XC3064A, XC3090A, XC3195A
1	I/O*
2	I/O*
3	I/O*
4	I/O
5	I/O
6	I/O
7	I/O
8	I/O
9	I/O
10	I/O
11	I/O
12	I/O
13	I/O
14	I/O
15	I/O
16	I/O
17	I/O
18	I/O
19	GND
20	VCC
21	I/O*
22	I/O
23	I/O
24	I/O
25	I/O
26	I/O
27	I/O
28	I/O
29	I/O
30	I/O
31	I/O
32	I/O
33	I/O
34	I/O
35	I/O
36	I/O
37	I/O
38	I/O*
39	I/O*
40	M1-$\overline{\text{RDATA}}$

PQFP Pin Number	XC3064A, XC3090A, XC3195A
41	GND
42	M0–RTRIG
43	VCC
44	M2-I/O
45	HDC-I/O
46	I/O
47	I/O
48	I/O
49	$\overline{\text{LDC}}$-I/O
50	I/O*
51	I/O*
52	I/O
53	I/O
54	I/O
55	I/O
56	I/O
57	I/O
58	I/O
59	$\overline{\text{INIT}}$-I/O
60	VCC
61	GND
62	I/O
63	I/O
64	I/O
65	I/O
66	I/O
67	I/O
68	I/O
69	I/O
70	I/O
71	I/O
72	I/O
73	I/O
74	I/O
75	I/O*
76	XTL2-I/O
77	GND
78	$\overline{\text{RESET}}$
79	VCC
80	DONE/$\overline{\text{PG}}$

PQFP Pin Number	XC3064A, XC3090A, XC3195A
81	D7-I/O
82	XTL1-I/O-BCLKIN
83	I/O*
84	I/O
85	I/O
86	D6-I/O
87	I/O
88	I/O
89	I/O
90	I/O
91	I/O
92	D5-I/O
93	$\overline{\text{CS0}}$-I/O
94	I/O*
95	I/O*
96	I/O
97	I/O
98	D4-I/O
99	I/O
100	VCC
101	GND
102	D3-I/O
103	$\overline{\text{CS1}}$-I/O
104	I/O
105	I/O
106	I/O*
107	I/O*
108	D2-I/O
109	I/O
110	I/O
111	I/O
112	I/O
113	I/O
114	D1-I/O
115	RDY/$\overline{\text{BUSY}}$-$\overline{\text{RCLK}}$-I/O
116	I/O
117	I/O
118	I/O*
119	D0-DIN-I/O
120	DOUT-I/O

PQFP Pin Number	XC3064A, XC3090A, XC3195A
121	CCLK
122	VCC
123	GND
124	A0-$\overline{\text{WS}}$-I/O
125	A1-CS2-I/O
126	I/O
127	I/O
128	A2-I/O
129	A3-I/O
130	I/O
131	I/O
132	A15-I/O
133	A4-I/O
134	I/O
135	I/O
136	A14-I/O
137	A5-I/O
138	I/O*
139	GND
140	VCC
141	A13-I/O
142	A6-I/O
143	I/O*
144	I/O*
145	I/O
146	I/O
147	A12-I/O
148	A7-I/O
149	I/O
150	I/O
151	A11-I/O
152	A8-I/O
153	I/O
154	I/O
155	A10-I/O
156	A9-I/O
157	VCC
158	GND
159	$\overline{\text{PWRDWN}}$
160	TCLKIN-I/O

Unprogrammed IOBs have a default pull-up. This prevents an undefined pad level for unbonded or unused IOBs. Programmed IOBs are default slew-rate limited.

* Indicates unconnected package pins (18) for the XC3064A.

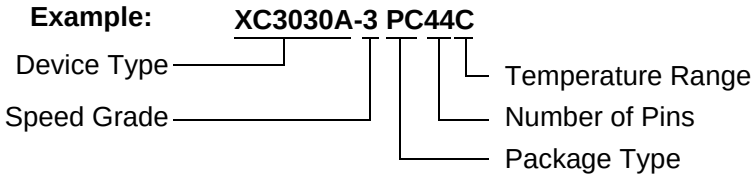
Pins		44	64	68	84		100			132		144	160	175		176	208
Type		Plast. PLCC	Plast. VQFP	Plast. PLCC	Plast. PLCC	Cer. PGA	Plast. PQFP	Plast. TQFP	Plast. VQFP	Plast. PGA	Cer. PGA	Plast. TQFP	Plast. PQFP	Plast. PGA	Cer. PGA	Plast. TQFP	Plast. PQFP
Code		PC44	VQ64	PC68	PC84	PG84	PQ100	TQ100	VQ100	PP132	PG132	TQ144	PQ160	PP175	PG175	TQ176	PQ208
XC3142L					C				C			C					
					C				C			C					
XC3190L					C							C				C	
					C							C				C	

Notes: C = Commercial, T_J= 0° to +85°C I = Industrial, T_J = -40° to +100°C

Number of Available I/O Pins

		Number of Package Pins										
	Max I/O	44	64	68	84	100	132	144	160	175	176	208
XC3020A/XC3120A	64			58	64	64						
XC3030A/XC3130A	80	34	54	58	74	80						
XC3042A/3142A	96				74	82	96	96				
XC2064A/XC3164A	120				70		110	120	120			
XC3090A/XC3190A	144				70			122	138	144	144	144
XC3195A	176				70				138	144		176

Ordering Information



Revision History

Date	Revision
11/98	Revised version number to 3.1, removed XC3100A-5 obsolete packages.