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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	100
Number of Logic Elements/Cells	-
Total RAM Bits	22176
Number of I/O	80
Number of Gates	2000
Voltage - Supply	4.25V ~ 5.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	100-BQFP
Supplier Device Package	100-PQFP (20x14)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc3130a-3pq100c

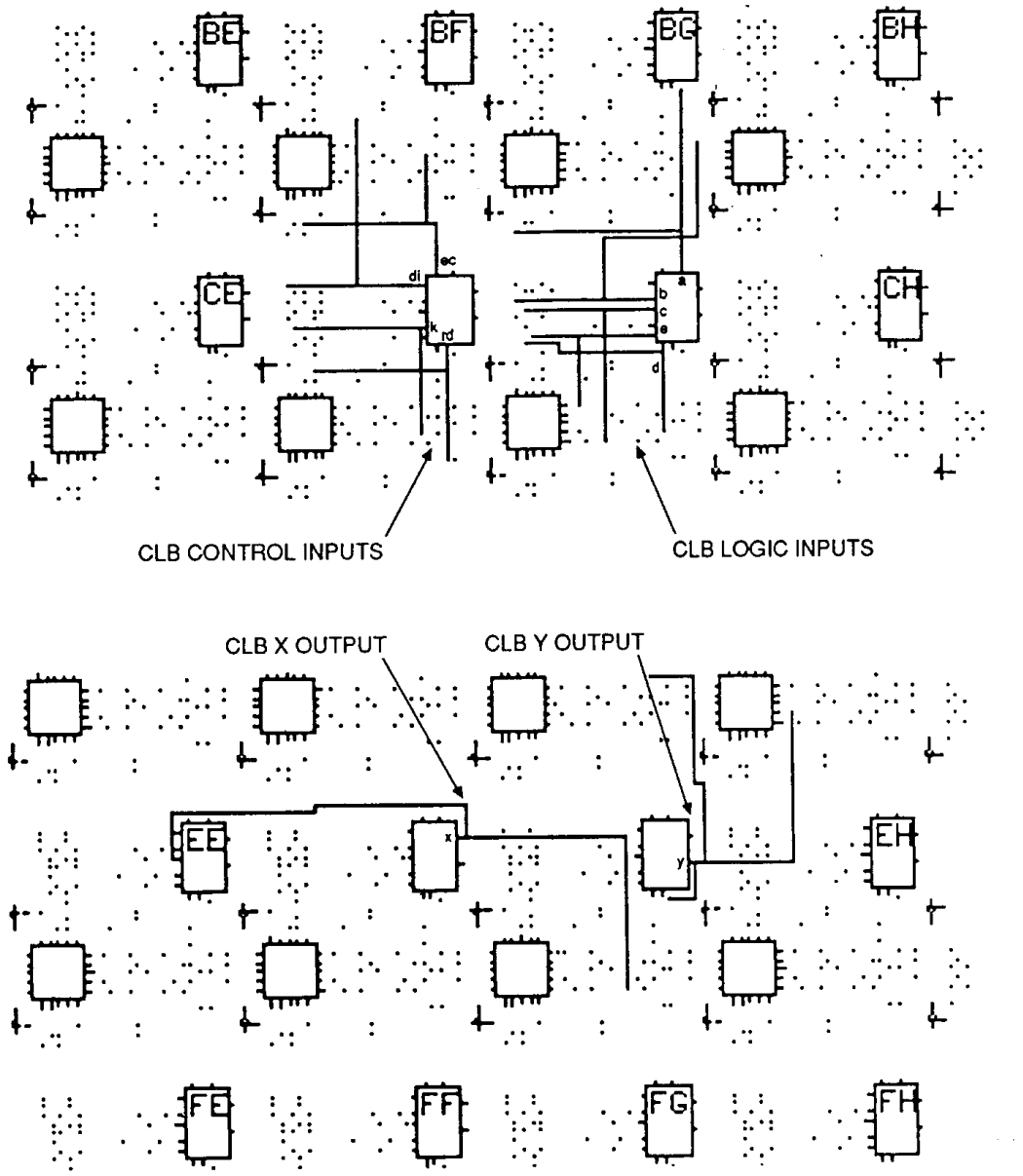


Figure 9: Design Editor Locations of interconnect access, CLB control inputs, logic inputs and outputs. The dot pattern represents the available programmable interconnection points (PIPs).

Some of the interconnect PIPs are directional.

Configuration

Initialization Phase

An internal power-on-reset circuit is triggered when power is applied. When V_{CC} reaches the voltage at which portions of the FPGA device begin to operate (nominally 2.5 to 3 V), the programmable I/O output buffers are 3-stated and a high-impedance pull-up resistor is provided for the user I/O pins. A time-out delay is initiated to allow the power supply voltage to stabilize. During this time the power-down mode is inhibited. The Initialization state time-out (about 11 to 33 ms) is determined by a 14-bit counter driven by a self-generated internal timer. This nominal 1-MHz timer is subject to variations with process, temperature and power supply. As shown in Table 1, five configuration mode choices are available as determined by the input levels of three mode pins; M0, M1 and M2.

Table 1: Configuration Mode Choices

M0	M1	M2	CCLK	Mode	Data
0	0	0	output	Master	Bit Serial
0	0	1	output	Master	Byte Wide Addr. = 0000 up
0	1	0	—	reserved	—
0	1	1	output	Master	Byte Wide Addr. = FFFF down
1	0	0	—	reserved	—
1	0	1	output	Peripheral	Byte Wide
1	1	0	—	reserved	—
1	1	1	input	Slave	Bit Serial

In Master configuration modes, the device becomes the source of the Configuration Clock (CCLK). The beginning of configuration of devices using Peripheral or Slave modes must be delayed long enough for their initialization to be completed. An FPGA with mode lines selecting a Master configuration mode extends its initialization state using four times the delay (43 to 130 ms) to assure that all daisy-chained slave devices, which it may be driving, will be ready even if the master is very fast, and the slave(s) very slow. Figure 20 shows the state sequences. At the end of Initialization, the device enters the Clear state where it clears the configuration memory. The active Low, open-drain initialization signal $\overline{\text{INIT}}$ indicates when the Initialization and Clear states are complete. The FPGA tests for the absence of an external active Low $\overline{\text{RESET}}$ before it makes a final sample of the mode lines and enters the Configuration state. An external wired-AND of one or more $\overline{\text{INIT}}$ pins can be used to control configuration by the assertion of the active-Low $\overline{\text{RESET}}$ of a master mode device or to signal a processor that the FPGAs are not yet initialized.

If a configuration has begun, a re-assertion of $\overline{\text{RESET}}$ for a minimum of three internal timer cycles will be recognized and the FPGA will initiate an abort, returning to the Clear state to clear the partially loaded configuration memory words. The FPGA will then resample $\overline{\text{RESET}}$ and the mode lines before re-entering the Configuration state.

During configuration, the XC3000A, XC3000L, XC3100A, and XC3100L devices check the bit-stream format for stop bits in the appropriate positions. Any error terminates the configuration and pulls INIT Low.

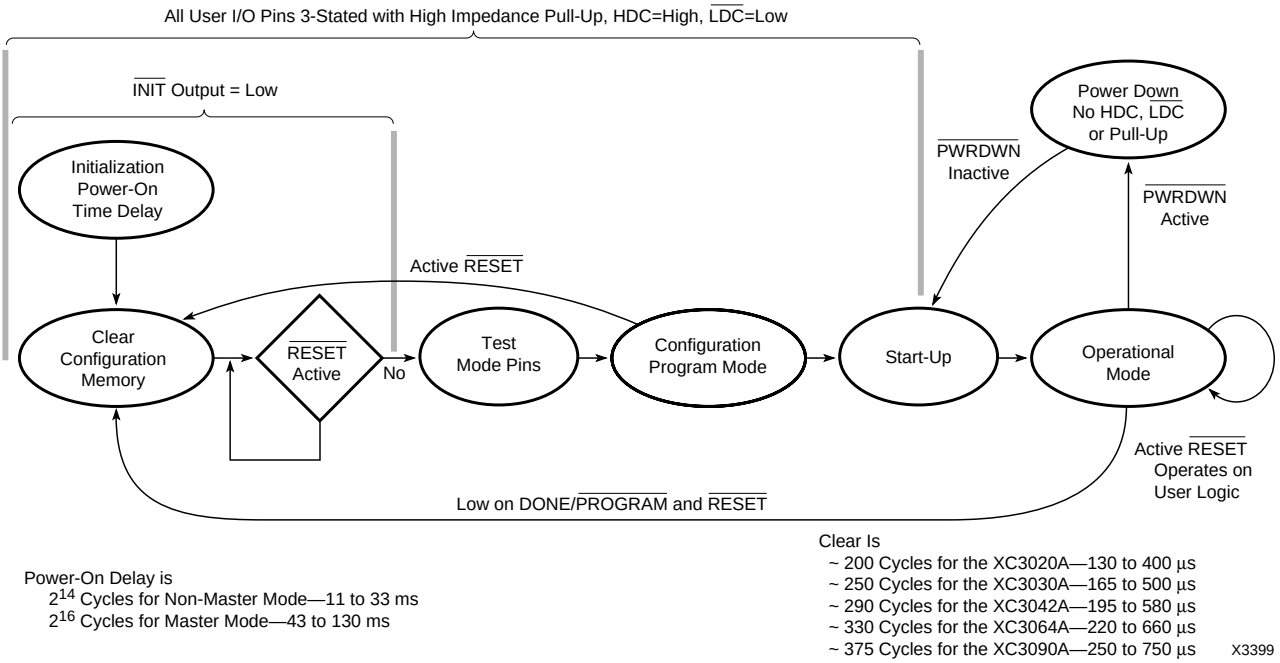
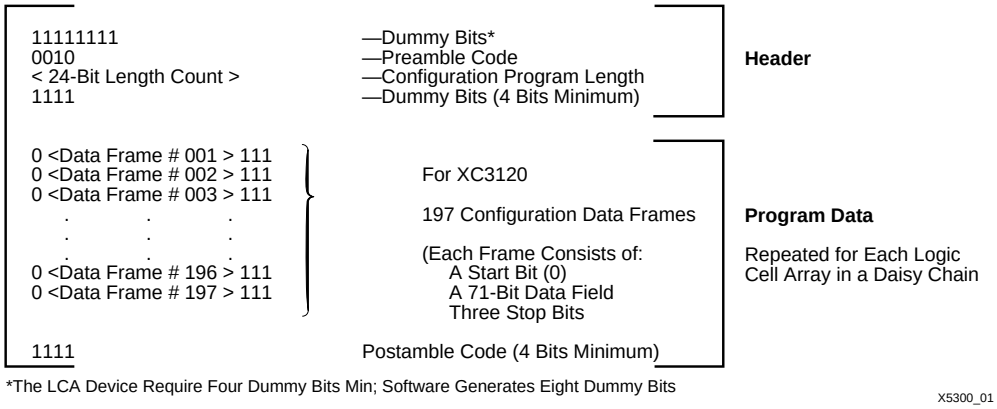


Figure 20: A State Diagram of the Configuration Process for Power-up and Reprogram.

A re-program is initiated.when a configured XC3000 series device senses a High-to-Low transition and subsequent >6 µs Low level on the DONE/PROG package pin, or, if this pin is externally held permanently Low, a High-to-Low transition and subsequent >6 µs Low time on the RESET package pin.

The device returns to the Clear state where the configuration memory is cleared and mode lines re-sampled, as for an aborted configuration. The complete configuration program is cleared and loaded during each configuration program cycle.

Length count control allows a system of multiple Field Programmable Gate Arrays, of assorted sizes, to begin operation in a synchronized fashion. The configuration program generated by the development system begins with a preamble of 111111110010 followed by a 24-bit length count representing the total number of configuration clocks needed to complete loading of the configuration program(s). The data framing is shown in Figure 21. All FPGAs connected in series read and shift preamble and length count in on positive and out on negative configuration clock edges. A device which has received the preamble and length count then presents a High Data Out until it has intercepted the appropriate number of data frames. When the configuration program memory of an FPGA is full and the length count does not yet compare, the device shifts any additional data through, as it did for preamble and length count. When the FPGA configuration memory is full and the length count compares, the device will execute



Device	XC3020A XC3020L XC3120A	XC3030A XC3030L XC3130A	XC3042A XC3042L XC3142A XC3142L	XC3064A XC3064L XC3164A	XC3090A XC3090L XC3190A XC3190L	XC3195A
Gates	1,000 to 1,500	1,500 to 2,000	2,000 to 3,000	3,500 to 4,500	5,000 to 6,000	6,500 to 7,500
CLBs	64	100	144	224	320	484
Row x Col	(8 x 8)	(10 x 10)	(12 x 12)	(16 x 14)	(20 x 16)	(22 x 22)
IOBs	64	80	96	120	144	176
Flip-flops	256	360	480	688	928	1,320
Horizontal Longlines	16	20	24	32	40	44
TBUFs/Horizontal LL	9	11	13	15	17	23
Bits per Frame (including1 start and 3 stop bits)	75	92	108	140	172	188
Frames	197	241	285	329	373	505
Program Data = Bits x Frames + 4 bits (excludes header)	14,779	22,176	30,784	46,064	64,160	94,944
PROM size (bits) = Program Data + 40-bit Header	14,819	22,216	30,824	46,104	64,200	94,984

Figure 21: Internal Configuration Data Structure for an FPGA. This shows the preamble, length count and data frames generated by the Development System.

The Length Count produced by the program = [(40-bit preamble + sum of program data + 1 per daisy chain device) rounded up to multiple of 8] – ($2 \le K \le 4$) where K is a function of DONE and RESET timing selected. An additional 8 is added if roundup increment is less than K. K additional clocks are needed to complete start-up after length count is reached.

Special Configuration Functions

The configuration data includes control over several special functions in addition to the normal user logic functions and interconnect.

- Input thresholds
- Readback disable
- DONE pull-up resistor
- DONE timing
- RESET timing
- Oscillator frequency divided by two

Each of these functions is controlled by configuration data bits which are selected as part of the normal development system bitstream generation process.

Input Thresholds

Prior to the completion of configuration all FPGA input thresholds are TTL compatible. Upon completion of configuration, the input thresholds become either TTL or CMOS compatible as programmed. The use of the TTL threshold option requires some additional supply current for threshold shifting. The exception is the threshold of the PWRDWN input and direct clocks which always have a CMOS input. Prior to the completion of configuration the user I/O pins each have a high impedance pull-up. The configuration program can be used to enable the IOB pull-up resistors in the Operational mode to act either as an input load or to avoid a floating input on an otherwise unused pin.

Readback

The contents of a Field Programmable Gate Array may be read back if it has been programmed with a bitstream in which the Readback option has been enabled. Readback may be used for verification of configuration and as a method of determining the state of internal logic nodes during debugging. There are three options in generating the configuration bitstream.

- “Never” inhibits the Readback capability.
- “One-time,” inhibits Readback after one Readback has been executed to verify the configuration.
- “On-command” allows unrestricted use of Readback.

Readback is accomplished without the use of any of the user I/O pins; only M0, M1 and CCLK are used. The initiation of Readback is produced by a Low to High transition of the M0/RTRIG (Read Trigger) pin. The CCLK input must then be driven by external logic to read back the configuration data. The first three Low-to-High CCLK transitions clock out dummy data. The subsequent Low-to-High CCLK transitions shift the data frame information out on the M1/RDATA (Read Data) pin. Note that the logic polarity is always inverted, a zero in configuration becomes a one in Readback, and vice versa. Note also that each Readback frame has one Start bit (read back as a one) but, unlike in configuration, each Readback frame has only one Stop bit (read back as a zero). The third leading dummy bit mentioned above can be considered the Start bit of the first frame. All data frames must be read back to complete the process and return the Mode Select and CCLK pins to their normal functions.

Readback data includes the current state of each CLB flip-flop, each input flip-flop or latch, and each device pad. These data are imbedded into unused configuration bit positions during Readback. This state information is used by the development system In-Circuit Verifier to provide visibility into the internal operation of the logic while the system is operating. To readback a uniform time-sample of all storage elements, it may be necessary to inhibit the system clock.

Reprogram

To initiate a re-programming cycle, the dual-function pin DONE/PROG must be given a High-to-Low transition. To reduce sensitivity to noise, the input signal is filtered for two cycles of the FPGA internal timing generator. When reprogram begins, the user-programmable I/O output buffers are disabled and high-impedance pull-ups are provided for the package pins. The device returns to the Clear state and clears the configuration memory before it indicates ‘initialized’. Since this Clear operation uses chip-individual internal timing, the master might complete the Clear operation and then start configuration before the slave has completed the Clear operation. To avoid this problem, the slave INIT pins must be AND-wired and used to force a RESET on the master (see Figure 25). Reprogram control is often implemented using an external open-collector driver which pulls DONE/PROG Low. Once a stable request is recognized, the DONE/PROG pin is held Low until the new configuration has been completed. Even if the re-program request is externally held Low beyond the configuration period, the FPGA will begin operation upon completion of configuration.

DONE Pull-up

DONE/PROG is an open-drain I/O pin that indicates the FPGA is in the operational state. An optional internal pull-up resistor can be enabled by the user of the development system. The DONE/PROG pins of multiple FPGAs in a daisy-chain may be connected together to indicate all are DONE or to direct them all to reprogram.

DONE Timing

The timing of the DONE status signal can be controlled by a selection to occur either a CCLK cycle before, or after, the outputs going active. See Figure 22. This facilitates control of external functions such as a PROM enable or holding a system in a wait state.

RESET Timing

As with DONE timing, the timing of the release of the internal reset can be controlled to occur either a CCLK cycle before, or after, the outputs going active. See Figure 22. This reset keeps all user programmable flip-flops and latches in a zero state during configuration.

Crystal Oscillator Division

A selection allows the user to incorporate a dedicated divide-by-two flip-flop between the crystal oscillator and the alternate clock line. This guarantees a symmetrical clock signal. Although the frequency stability of a crystal oscillator is very good, the symmetry of its waveform can be affected by bias or feedback drive.

Bitstream Error Checking

Bitstream error checking protects against erroneous configuration.

Each Xilinx FPGA bitstream consists of a 40-bit preamble, followed by a device-specific number of data frames. The number of bits per frame is also device-specific; however, each frame ends with three stop bits (111) followed by a start bit for the next frame (0).

All devices in all XC3000 families start reading in a new frame when they find the first 0 after the end of the previous frame. An original XC3000 device does not check for the correct stop bits, but XC3000A, XC3100A, XC3000L, and XC3100L devices check that the last three bits of any frame are actually 111.

Under normal circumstances, all these FPGAs behave the same way; however, if the bitstream is corrupted, an XC3000 device will always start a new frame as soon as it finds the first 0 after the end of the previous frame, even if the data is completely wrong or out-of-sync. Given sufficient zeros in the data stream, the device will also go Done, but with incorrect configuration and the possibility of internal contention.

An XC3000A/XC3100A/XC3000L/XC3100L device starts any new frame only if the three preceding bits are all ones. If this check fails, it pulls $\overline{\text{INIT}}$ Low and stops the internal configuration, although the Master CCLK keeps running. The user must then start a new configuration by applying a >6 µs Low level on $\overline{\text{RESET}}$.

This simple check does not protect against random bit errors, but it offers almost 100 percent protection against erroneous configuration files, defective configuration data sources, synchronization errors between configuration source and FPGA, or PC-board level defects, such as broken lines or solder-bridges.

Reset Spike Protection

A separate modification slows down the $\overline{\text{RESET}}$ input before configuration by using a two-stage shift register driven from the internal clock. It tolerates submicrosecond High spikes on $\overline{\text{RESET}}$ before configuration. The XC3000 master can be connected like an XC4000 master, but with its $\overline{\text{RESET}}$ input used instead of $\overline{\text{INIT}}$. (On XC3000, $\overline{\text{INIT}}$ is output only).

Soft Start-up

After configuration, the outputs of all FPGAs in a daisy-chain become active simultaneously, as a result of the same CCLK edge. In the original XC3000/3100 devices, each output becomes active in either fast or slew-rate limited mode, depending on the way it is configured. This can lead to large ground-bounce signals. In XC3000A, XC3000L, XC3100A, and XC3100L devices, all outputs become active first in slew-rate limited mode, reducing the ground bounce. After this soft start-up, each individual output slew rate is again controlled by the respective configuration bit.

Master Parallel Mode

In Master Parallel mode, the lead FPGA directly addresses an industry-standard byte-wide EPROM and accepts eight data bits right before incrementing (or decrementing) the address outputs.

The eight data bits are serialized in the lead FPGA, which then presents the preamble data (and all data that overflows the lead device) on the DOUT pin. There is an internal delay of 1.5 CCLK periods, after the rising CCLK edge that accepts a byte of data, and also changes the EPROM address, until the falling CCLK edge that makes the LSB (D0) of this byte appear at DOUT. This means that DOUT changes on the falling CCLK edge, and the next device in the daisy chain accepts data on the subsequent rising CCLK edge.

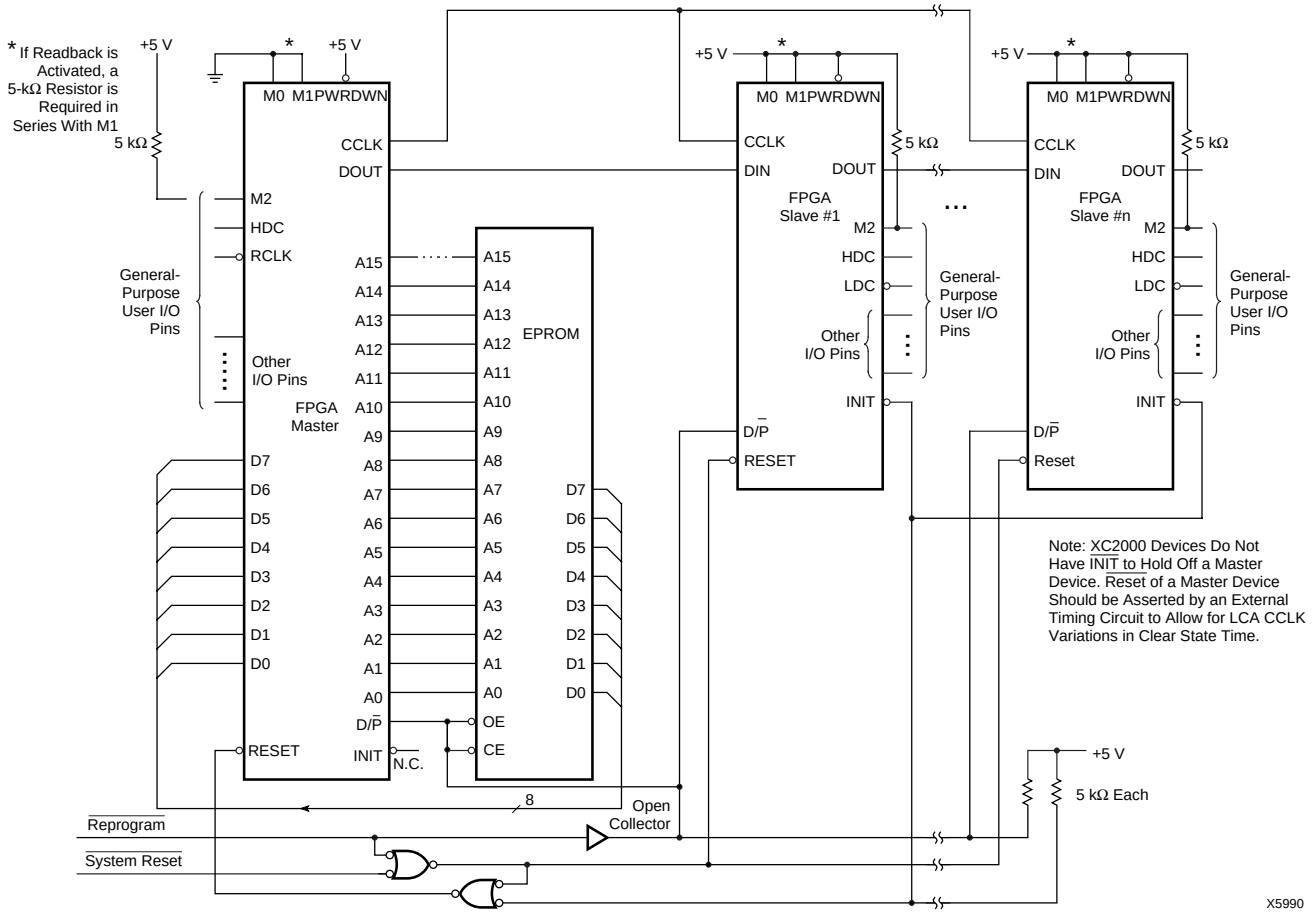
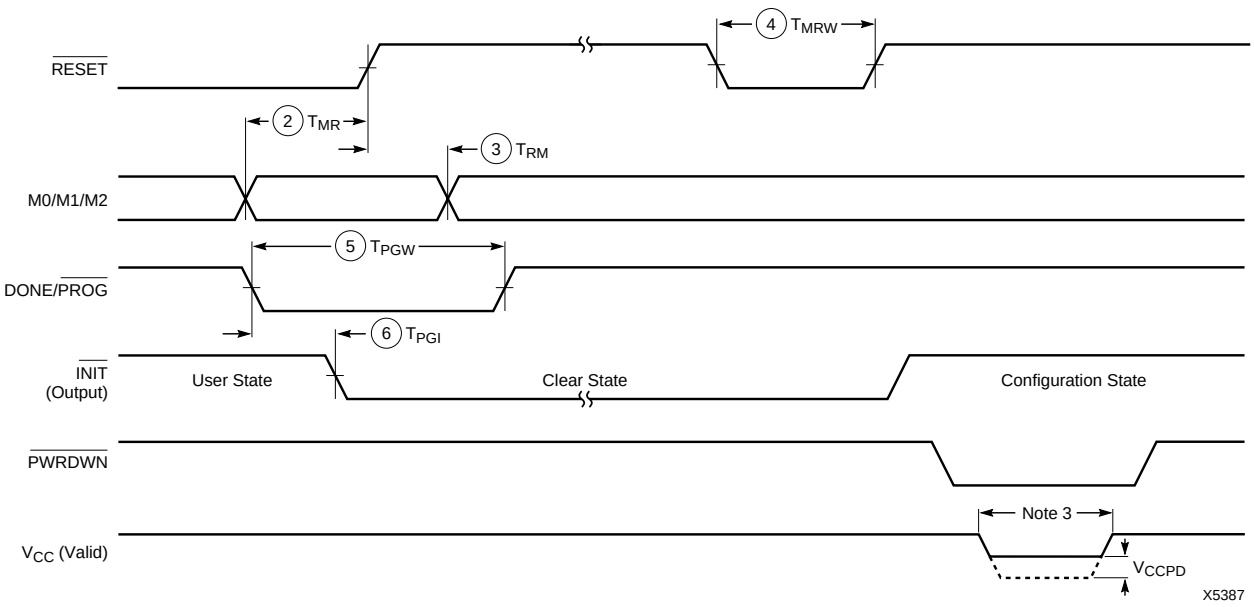


Figure 25: Master Parallel Mode Circuit Diagram

General XC3000 Series Switching Characteristics



	Description		Symbol	Min	Max	Units
RESET (2)	M0, M1, M2 setup time required	2	T_{MR}	1		µs
	M0, M1, M2 hold time required	3	T_{RM}	4.5		µs
	RESET Width (Low) req. for Abort	4	T_{MRW}	6		µs
DONE/PROG	Width (Low) required for Re-config.	5	T_{PGW}	6		µs
	INIT response after D/P is pulled Low	6	T_{PGI}		7	µs
PWRDWN (3)	Power Down V_{CC}		V_{CCPD}	2.3		V

Notes:
1. At power-up, V_{CC} must rise from 2.0 V to V_{CC} min in less than 25 ms. If this is not possible, configuration can be delayed by holding RESET Low until Vcc has reached 4.0 V (2.5 V for XC3000L). A very long Vcc rise time of >100 ms, or a non-monotonically rising V_{CC} may require a >1-µs High level on RESET, followed by a >6-µs Low level on RESET and D/P after Vcc has reached 4.0 V (2.5 V for XC3000L).
2. RESET timing relative to valid mode lines (M0, M1, M2) is relevant when RESET is used to delay configuration. The specified hold time is caused by a shift-register filter slowing down the response to RESET during configuration.
3. PWRDWN transitions must occur while V_{CC} >4.0 V(2.5 V for XC3000L).

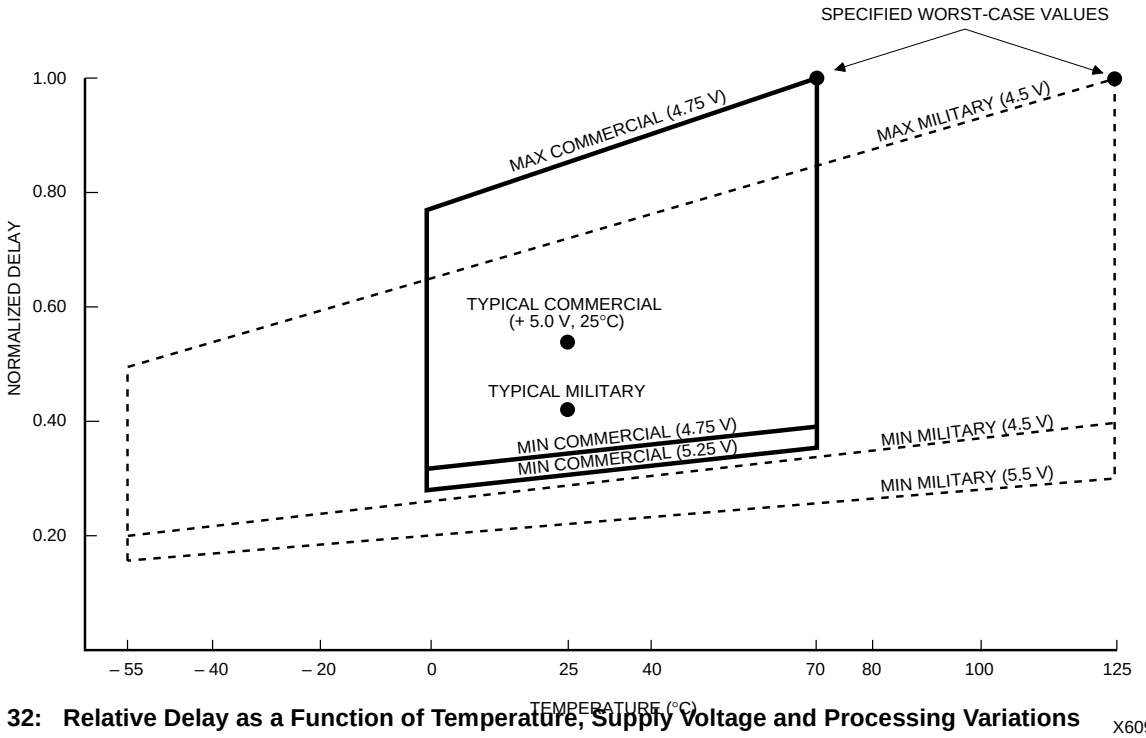


Figure 32: Relative Delay as a Function of Temperature, Supply Voltage and Processing Variations

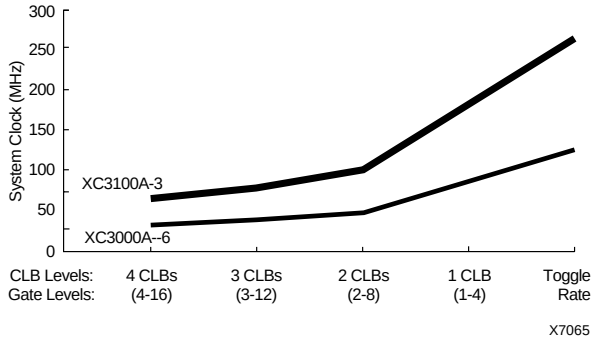


Figure 33: Clock Rate as a Function of Logic Complexity (Number of Combinational Levels between Flip-Flops)

Power

Power Distribution

Power for the FPGA is distributed through a grid to achieve high noise immunity and isolation between logic and I/O. Inside the FPGA, a dedicated V_{CC} and ground ring surrounding the logic array provides power to the I/O drivers. An independent matrix of V_{CC} and groundlines supplies the interior logic of the device. This power distribution grid provides a stable supply and ground for all internal logic, providing the external package power pins are all connected and appropriately decoupled. Typically a 0.1-µF capacitor connected near the V_{CC} and ground pins will provide adequate decoupling.

Output buffers capable of driving the specified 4- or 8-mA loads under worst-case conditions may be capable of driving as much as 25 to 30 times that current in a best case. Noise can be reduced by minimizing external load capacitance and reducing simultaneous output transitions in the same direction. It may also be beneficial to locate heavily loaded output buffers near the ground pads. The I/O Block output buffers have a slew-limited mode which should be used where output rise and fall times are not speed critical. Slew-limited outputs maintain their dc drive capability, but generate less external reflections and internal noise.

Pin Functions During Configuration

Configuration Mode <M2:M1:M0>					***		**										****	
SLAVE SERIAL <1:1:1>	MASTER-SERIAL <0:0:0>	PERIPH <1:0:1>	MASTER-HIGH <1:1:0>	MASTER-LOW <1:0:0>	44 PLCC	64 VQFP	68 PLCC	84 PLCC	84 PGA	100 PQFP	100 VQFP TQFP	132 PGA	144 TQFP	160 PQFP	175 PGA	176 TQFP	208 PQFP	User Function
POWR DWN (I)	POWER DWN (I)	POWER DWN (I)	POWER DWN (I)	POWER DWN (I)	7	17	10	12	B2	29	26	A1	1	159	B2	1	3	POWER DWN (1)
M1 (HIGH) (I)	M1 (LOW) (I)	M1 (LOW) (I)	M1 (HIGH) (I)	M1 (LOW) (I)	16	31	25	31	J2	52	49	B13	36	40	B14	45	48	RDATA
M0 (HIGH) (I)	M0 (LOW) (I)	M0 (HIGH) (I)	M0 (LOW) (I)	M0 (LOW) (I)	17	32	26	32	L1	54	51	A14	38	42	B15	47	50	RTRIG (I)
M2 (HIGH) (I)	M2 (LOW) (I)	M2 (HIGH) (I)	M2 (HIGH) (I)	M2 (HIGH) (I)	18	33	27	33	K2	56	53	C13	40	44	C15	49	56	I/O
HDC (HIGH)	HDC (HIGH)	HDC (HIGH)	HDC (HIGH)	HDC (HIGH)	19	34	28	34	K3	57	54	B14	41	45	E14	50	57	I/O
LDC (LOW)	LDC (LOW)	LDC (LOW)	LDC (LOW)	LDC (LOW)	20	36	30	36	L3	59	56	D14	45	49	D16	54	61	I/O
INIT*	INIT*	INIT*	INIT*	INIT*	22	40	34	42	K6	65	62	G14	53	59	H15	65	77	I/O
GND	GND	GND	GND	GND	23	41	35	43	J6	66	63	H12	55	61	J14	67	79	GND
					26	47	43	53	L11	76	73	M13	69	76	P15	85	100	XTL2 OR I/O
RESET (I)	RESET (I)	RESET (I)	RESET (I)	RESET (I)	27	48	44	54	K10	78	75	P14	71	78	R15	87	102	RESET (I)
DONE	DONE	DONE	DONE	DONE	28	49	45	55	J10	80	77	N13	73	80	R14	89	107	PROGRAM (I)
		DATA 7 (I)	DATA 7 (I)	DATA 7 (I)		50	46	56	K11	81	78	M12	74	81	N13	90	109	I/O
					30	51	47	57	J11	82	79	P13	75	82	T14	91	110	XTL1 OR I/O
		DATA 6 (I)	DATA 6 (I)	DATA 6 (I)		52	48	58	H10	83	80	N11	78	86	P12	96	115	I/O
		DATA 5 (I)	DATA 5 (I)	DATA 5 (I)		53	49	60	F10	87	84	M9	84	92	T11	102	122	I/O
		CS0 (I)				54	50	61	G10	88	85	N9	85	93	R10	103	123	I/O
		DATA 4 (I)	DATA 4 (I)	DATA 4 (I)		55	51	62	G11	89	86	N8	88	96	R9	108	128	I/O
		DATA 3 (I)	DATA 3 (I)	DATA 3 (I)		57	53	65	F11	92	89	N7	92	102	P8	112	132	I/O
		CS1 (I)				58	54	66	E11	93	90	P6	93	103	R8	113	133	I/O
		DATA 2 (I)	DATA 2 (I)	DATA 2 (I)		59	55	67	E10	94	91	M6	96	106	R7	118	138	I/O
		DATA 1 (I)	DATA 1 (I)	DATA 1 (I)		60	56	70	D10	98	95	M5	102	114	R5	124	145	I/O
		RDY/BUSY	$\overline{\text{RCLK}}$	$\overline{\text{RCLK}}$		61	57	71	C11	99	96	N4	103	115	P5	125	146	I/O
DIN (I)	DIN (I)	DATA 0 (I)	DATA 0 (I)	DATA 0 (I)	38	62	58	72	B11	100	97	N2	106	119	R3	130	151	I/O
DOUT	DOUT	DOUT	DOUT	DOUT	39	63	59	73	C10	1	98	M3	107	120	N4	131	152	I/O
CCLK (I)	CCLK (O)	CCLK (O)	CCLK (O)	CCLK (O)	40	64	60	74	A11	2	99	P1	108	121	R2	132	153	CCLK (I)
		WS (I)	A0	A0		1	61	75	B10	5	2	M2	111	124	P2	135	161	I/O
		CS2 (I)	A1	A1		2	62	76	B9	6	3	N1	112	125	M3	136	162	I/O
			A2	A2		3	63	77	A10	8	5	L2	115	128	P1	140	165	I/O
			A3	A3		4	64	78	A9	9	6	L1	116	129	N1	141	166	I/O
			A15	A15			65	81	B6	12	9	K1	119	132	M1	146	172	5
			A4	A4		5	66	82	B7	13	10	J2	120	133	L2	147	173	I/O
			A14	A14		6	67	83	A7	14	11	H1	123	136	K2	150	178	I/O
			A5	A5		7	68	84	C7	15	12	H2	124	137	K1	151	179	I/O
			A13	A13		9	2	2	A6	17	14	G2	128	141	H2	156	184	I/O
			A6	A6		10	3	3	A5	18	15	G1	129	142	H1	157	185	I/O
			A12	A12		11	4	4	B5	19	16	F2	133	147	F2	164	192	I/O
			A7	A7		12	5	5	C5	20	17	E1	134	148	E1	165	193	I/O
			A11	A11		13	6	8	A3	23	20	D1	137	151	D1	169	199	I/O
			A8	A8		14	7	9	A2	24	21	D2	138	152	C1	170	200	I/O
			A10	A10		15	8	10	B3	25	22	B1	141	155	E3	173	203	I/O
			A9	A9		16	9	11	A1	26	26	C2	142	156	C2	174	204	I/O
																		All Others
							X	X	X	X								XC3x20A etc.
					X	X	X	X	X	X	X							XC3x30A etc.
								X	X	X	X	X	X					XC3x42A etc.
								X**				X	X					XC3x64A etc.
								X**					X	X	X	X	X	XC3x90A etc.
								X**						X	X		X	XC3195A

Notes:

Generic I/O pins are not shown.
For a detailed description of the configuration modes, see page 25 through page 34.
For pinout details, see page 65 through page 76.
Represents a weak pull-up before and during configuration.
* INIT is an open drain output during configuration.
(I) Represents an input.
** Pin assignment for the XC3064A/XC3090A and XC3195A differ from those shown.
*** Peripheral mode and master parallel mode are not supported in the PC44 package.
**** Pin assignments for the XC3195A PQ208 differ from those shown.
Pin assignments of PGA Footprint PLCC sockets and PGA packages are not identical.
The information on this page is provided as a convenient summary. For detailed pin descriptions, see the preceding two pages.

Note: Before and during configuration, all outputs that are not used for the configuration process are 3-stated with a weak pull-up resistor.

XC3000A Switching Characteristics

Xilinx maintains test specifications for each product as controlled documents. To insure the use of the most recently released device performance parameters, please request a copy of the current test-specification revision.

XC3000A Operating Conditions

Symbol	Description	Min	Max	Units
V_{CC}	Supply voltage relative to GND Commercial 0°C to +85°C junction	4.75	5.25	V
	Supply voltage relative to GND Industrial -40°C to +100°C junction	4.5	5.5	V
V_{IHT}	High-level input voltage — TTL configuration	2.0	V_{CC}	V
V_{ILT}	Low-level input voltage — TTL configuration	0	0.8	V
V_{IHC}	High-level input voltage — CMOS configuration	70%	100%	V_{CC}
V_{ILC}	Low-level input voltage — CMOS configuration	0	20%	V_{CC}
T_{IN}	Input signal transition time		250	ns

Note: At junction temperatures above those listed as Operating Conditions, all delay parameters increase by 0.3% per °C.

XC3000A DC Characteristics Over Operating Conditions

Symbol	Description		Min	Max	Units
V_{OH}	High-level output voltage (@ I_{OH} = –4.0 mA, V_{CC} min)	Commercial	3.86		V
V_{OL}	Low-level output voltage (@ I_{OL} = 4.0 mA, V_{CC} min)	Commercial		0.40	V
V_{OH}	High-level output voltage (@ I_{OH} = –4.0 mA, V_{CC} min)	Industrial	3.76		V
V_{OL}	Low-level output voltage (@ I_{OL} = 4.0 mA, V_{CC} min)	Industrial		0.40	V
V_{CCPD}	Power-down supply voltage (PWRDWN must be Low)		2.30		V
I_{CCPD}	Power-down supply current ($V_{CC(MAX)}$ @ T_{MAX})				
		3020A		100	µA
		3030A		160	µA
		3042A		240	µA
		3064A		340	µA
		3090A		500	µA
I_{CCO}	Quiescent FPGA supply current in addition to I_{CCPD}				
	Chip thresholds programmed as CMOS levels			500	µA
	Chip thresholds programmed as TTL levels			10	µA
I_{IL}	Input Leakage Current		–10	+10	µA
C_{IN}	Input capacitance, all packages except PGA175 (sample tested)				
	All Pins except XTL1 and XTL2			10	pF
	XTL1 and XTL2			15	pF
	Input capacitance, PGA 175 (sample tested)				
	All Pins except XTL1 and XTL2			16	pF
	XTL1 and XTL2			20	pF
I_{RIN}	Pad pull-up (when selected) @ V_{IN} = 0 V[3]		0.02	0.17	mA
I_{RLL}	Horizontal Longline pull-up (when selected) @ logic Low			3.4	mA

Notes: 1. With no output current loads, no active input or Longline pull-up resistors, all package pins at V_{CC} or GND, and the FPGA device configured with a tie option.
2. Total continuous output sink current may not exceed 100 mA per ground pin. Total continuous output source may not exceed 100 mA per V_{CC} pin. The number of ground pins varies from the XC3020A to the XC3090A.
3. Not tested. Allow an undriven pin to float High. For any other purposes use an external pull-up.

XC3000L Switching Characteristics

Xilinx maintains test specifications for each product as controlled documents. To insure the use of the most recently released device performance parameters, please request a copy of the current test-specification revision.

XC3000L Operating Conditions

Symbol	Description	Min	Max	Units
V_{CC}	Supply voltage relative to GND Commercial 0°C to +85°C junction	3.0	3.6	V
V_{IH}	High-level input voltage — TTL configuration	2.0	V_{CC}+0.3	V
V_{IL}	Low-level input voltage — TTL configuration	-0.3	0.8	V
T_{IN}	Input signal transition time		250	ns

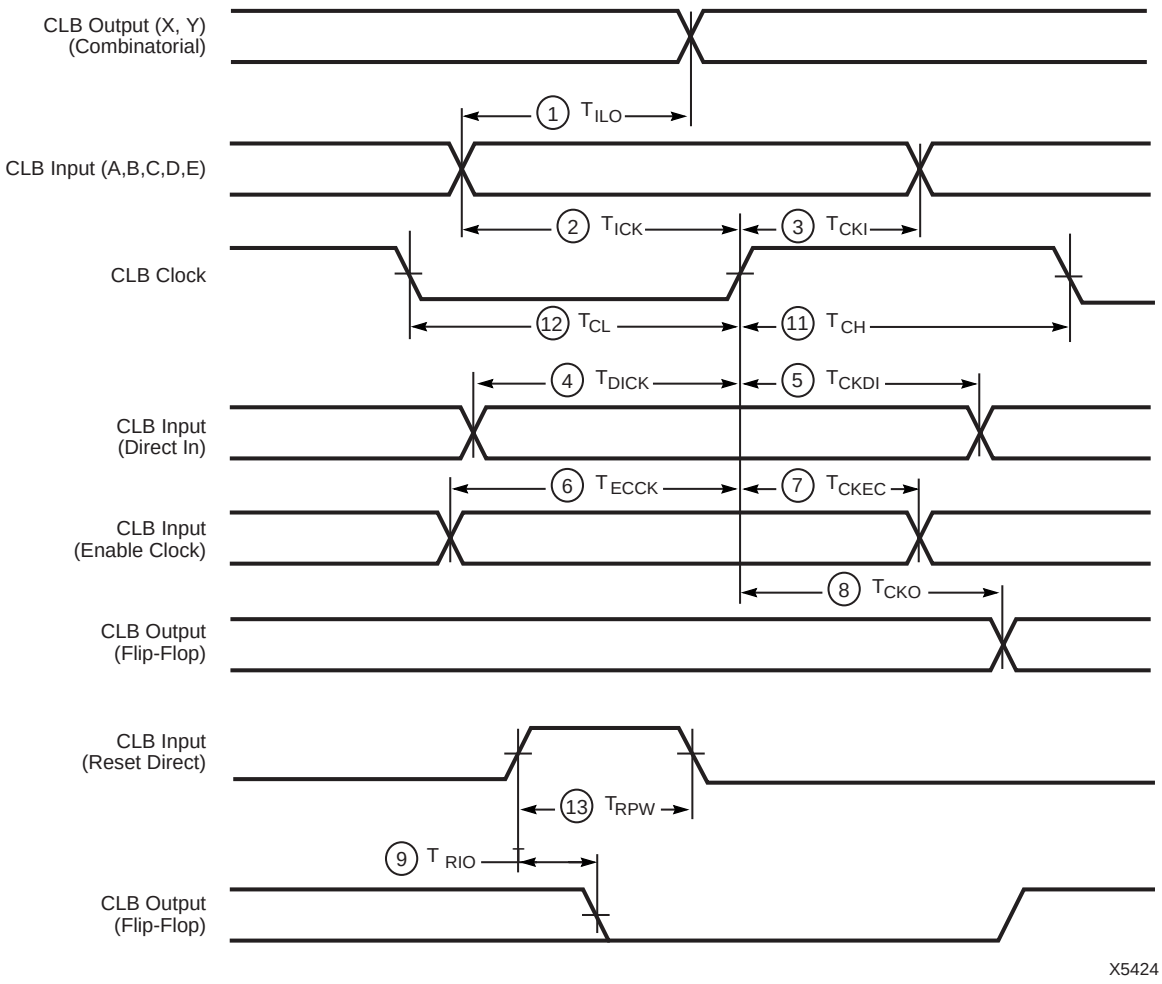
Notes: 1. At junction temperatures above those listed as Operating Conditions, all delay parameters increase by 0.3% per °C.
2. Although the present (1996) devices operate over the full supply voltage range from 3.0 to 5.25 V, Xilinx reserves the right to restrict operation to the 3.0 to 3.6 V range later, when smaller device geometries might preclude operation at 5V. Operating conditions are guaranteed in the 3.0 – 3.6 V V_{CC} range.

XC3000L DC Characteristics Over Operating Conditions

Symbol	Description	Min	Max	Units
V_{OH}	High-level output voltage (@ I_{OH} = –4.0 mA, V_{CC} min)	2.40		V
V_{OL}	Low-level output voltage (@ I_{OL} = 4.0 mA, V_{CC} min)		0.40	V
V_{OH}	High-level output voltage (@ I_{OH} = –4.0 mA, V_{CC} min)	V_{CC} -0.2		V
V_{OL}	Low-level output voltage (@ I_{OL} = 4.0 mA, V_{CC} min)		0.2	V
V_{CCPD}	Power-down supply voltage (PWRDWN must be Low)	2.30		V
I_{CCPD}	Power-down supply current ($V_{CC(MAX)}$ @ T_{MAX})		10	µA
I_{CCO}	Quiescent FPGA supply current in addition to I_{CCPD}[1] Chip thresholds programmed as CMOS levels		 20	 µA
I_{IL}	Input Leakage Current	–10	+10	µA
C_{IN}	Input capacitance, all packages except PGA175 (sample tested) All Pins except XTL1 and XTL2 XTL1 and XTL2		 10 15	 pF pF
	Input capacitance, PGA 175 (sample tested) All Pins except XTL1 and XTL2 XTL1 and XTL2		 15 20	 pF pF
I_{RIN}	Pad pull-up (when selected) @ V_{IN} = 0 V[3]	0.01	0.17	mA
I_{RLL}	Horizontal Longline pull-up (when selected) @ logic Low		2.50	mA

Notes: 1. With no output current loads, no active input or Longline pull-up resistors, all package pins at V_{CC} or GND, and the FPGA device configured with a tie option. I_{CCO} is in addition to I_{CCPD}.
2. Total continuous output sink current may not exceed 100 mA per ground pin. Total continuous output source may not exceed 100 mA per V_{CC} pin. The number of ground pins varies from the XC3020L to the XC3090L.
3. Not tested. Allows an undriven pin to float High. For any other purpose, use an external pull-up.

XC3000L CLB Switching Characteristics Guidelines (continued)



XC3100A CLB Switching Characteristics Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Since many internal timing parameters cannot be measured directly, they are derived from benchmark timing patterns. The following guidelines reflect worst-case values over the recommended operating conditions. For more detailed, more precise, and more up-to-date timing information, use the values provided by the timing calculator and used in the simulator.

	Speed Grade		-4		-3		-2		-1		-09		
Description	**Symbol**		**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**
Combinatorial Delay													
Logic Variables A, B, C, D, E, to outputs X or Y	1	T_{ILO}		3.3		2.7		2.2		1.75		1.5	ns
Sequential delay													
Clock k to outputs X or Y	8	T_{CKO}		2.5		2.1		1.7		1.4		1.25	ns
Clock k to outputs X or Y when Q is returned through function generators F or G to drive X or Y		T_{QLO}		5.2		4.3		3.5		3.1		2.7	ns
Set-up time before clock K													
Logic Variables A, B, C, D, E	2	T_{ICK}	2.5		2.1		1.8		1.7		1.5		ns
Data In DI	4	T_{DICK}	1.6		1.4		1.3		1.2		1.0		ns
Enable Clock EC	6	T_{ECCK}	3.2		2.7		2.5		2.3		2.05		ns
Reset Direct inactive RD			1.0		1.0		1.0		1.0		1.0		ns
Hold Time after clock K													
Logic Variables A, B, C, D, E	3	T_{CKI}	0		0		0		0		0		ns
Data In DI	5	T_{CKDI}	1.0		0.9		0.9		0.8		0.7		ns
Enable Clock EC	7	T_{CKEC}	0.8		0.7		0.7		0.6		0.55		ns
Clock													
Clock High time	11	T_{CH}	2.0		1.6		1.3		1.3		1.3		ns
Clock Low time	12	T_{CL}	2.0		1.6		1.3		1.3		1.3		ns
Max. flip-flop toggle rate		F_{CLK}	227		270		323		323		370		MHz
Reset Direct (RD)													
RD width	13	T_{RPW}	3.2		2.7		2.3		2.3		2.05		ns
delay from RD to outputs X or Y	9	T_{RIO}		3.7		3.1		2.7		2.4		2.15	ns
Global Reset ($\overline{\text{RESET}}$ Pad)[1]													
$\overline{\text{RESET}}$ width (Low) (XC3142A)		T_{MRW}	14.0		12.0		12.0		12.0		12.0		ns
delay from $\overline{\text{RESET}}$ pad to outputs X or Y		T_{MRQ}		14.0		12.0		12.0		12.0		12.0	ns
											Prelim		

Notes: 1. The CLB K to Q output delay (T_{CKO}, #8) of any CLB, plus the shortest possible interconnect delay, is always longer than the Data In hold time requirement (T_{CKDI}, #5) of any CLB on the same die.

2. T_{ILO}, T_{QLO} and T_{ICK} are specified for 4-input functions. For 5-input functions or base FGM functions, each of these specifications for the XC3100A family increases by 0.50 ns (-5), 0.42 ns (-4) and 0.35 ns (-3), 0.35 ns (-2), 0.30 ns (-1), and 0.30 ns (-09).

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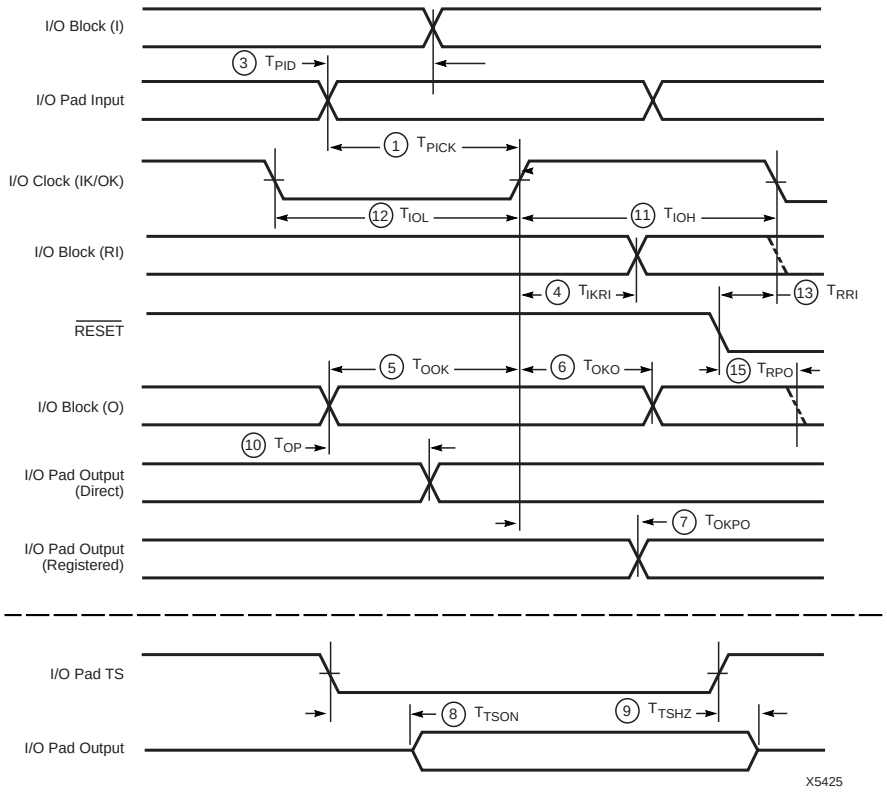
XC3100A IOB Switching Characteristics Guidelines

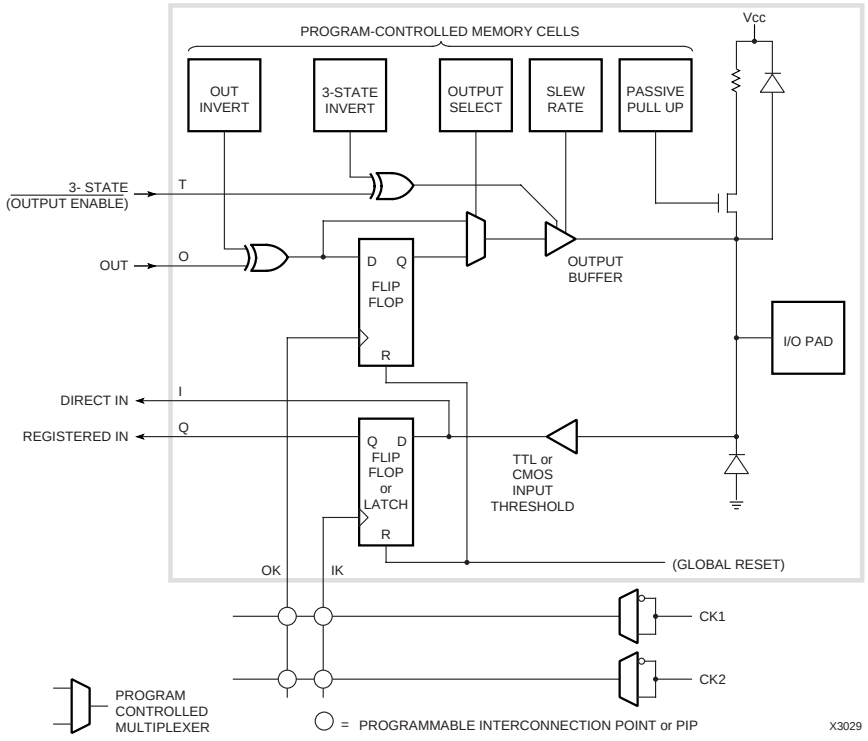
Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Since many internal timing parameters cannot be measured directly, they are derived from benchmark timing patterns. The following guidelines reflect worst-case values over the recommended operating conditions. For more detailed, more precise, and more up-to-date timing information, use the values provided by the timing calculator and used in the simulator.

Speed Grade			-4		-3		-2		-1		-09		
Description	**Symbol**		**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**
Propagation Delays (Input)													
Pad to Direct In (I)	3	T_{PID}		2.5		2.2		2.0		1.7		1.55	ns
Pad to Registered In (Q)													
with latch transparent(XC3100A)Clock (IK)		T_{PTG}		12.0		11.0		11.0		10.0		9.2	ns
to Registered In (Q)	4	T_{IKRI}		2.5		2.2		1.9		1.7		1.55	ns
Set-up Time (Input)													
Pad to Clock (IK) set-up time													
XC3120A, XC3130A	1	T_{PICK}	10.6		9.4		8.9		8.0		7.2		ns
XC3142A			10.7		9.5		9.0		8.1		7.3		ns
XC3164A			11.0		9.7		9.2		8.3		7.5		ns
XC3190A			11.2		9.9		9.4		8.5		7.7		ns
XC3195A			11.6		10.3		9.8		8.9		8.1		ns
Propagation Delays (Output)													
Clock (OK) to Pad (fast)	7	T_{OKPO}		5.0		4.4		3.7		3.4		3.3	ns
same (slew rate limited)	7	T_{OKPO}		12.0		10.0		9.7		8.4		6.9	ns
Output (O) to Pad (fast)	10	T_{OPF}		3.7		3.3		3.0		3.0		2.9	ns
same (slew-rate limited)													ns
(XC3100A)	10	T_{OPS}		11.0		9.0		8.7		8.0		6.5	ns
3-state to Pad													
begin hi-Z (fast)	9	T_{TSHZ}		6.2		5.5		5.0		4.5		4.05	ns
same (slew-rate limited)	9	T_{TSHZ}		6.2		5.5		5.0		4.5		4.05	ns
3-state to Pad													
active and valid (fast) (XC3100A)	8	T_{TSON}		10.0		9.0		8.5		6.5		5.0	ns
same (slew -rate limited)	8	T_{TSON}		17.0		15.0		14.2		11.5		8.6	ns
Set-up and Hold Times (Output)													
Output (O) to clock (OK) set-up time													
(XC3100A)	5	T_{OOK}	4.5				3.6		3.2		2.9		ns
Output (O) to clock (OK) hold time	6	T_{OKO}	0				0		0				ns
Clock													
Clock High time	11	T_{IOH}	2.0		1.6		1.3		1.3		1.3		ns
Clock Low time	12	T_{IOL}	2.0		1.6		1.3		1.3		1.3		ns
Max. flip-flop toggle rate		F_{CLK}	227		270		323		323		370		MHz
Global Reset Delays													
RESET Pad to Registered In (Q)													
(XC3142A)	13	T_{RRI}		15.0		13.0		13.0		13.0		14.4	ns
(XC3190A)				25.5		21.0		21.0		21.0		21.0	ns
RESET Pad to output pad (fast)	15	T_{RPO}		20.0		17.0		17.0		17.0		17.0	ns
(slew-rate limited)	15	T_{RPO}		27.0		23.0		23.0		22.0		21.0	ns
											Preliminary		

Notes: 1. Timing is measured at pin threshold, with 50 pF external capacitive loads (incl. test fixture). For larger capacitive loads, see XAPP024. Typical slew rate limited output rise/fall times are approximately four times longer.
2. Voltage levels of unused (bonded and unbonded) pads must be valid logic levels. Each can be configured with the internal pull-up resistor or alternatively configured as a driven output or driven from an external source.
3. Input pad set-up time is specified with respect to the internal clock (ik). In order to calculate system set-up time, subtract clock delay (pad to ik) from the input pad set-up time value. Input pad holdtime with respect to the internal clock (ik) is negative. This means that pad level changes immediately before the internal clock edge (ik) will not be recognized.
4. T_{PID}, T_{PTG}, and T_{PICK} are 3 ns higher for XTL2 when the pin is configured as a user input.

XC3100A IOB Switching Characteristics Guidelines (continued)





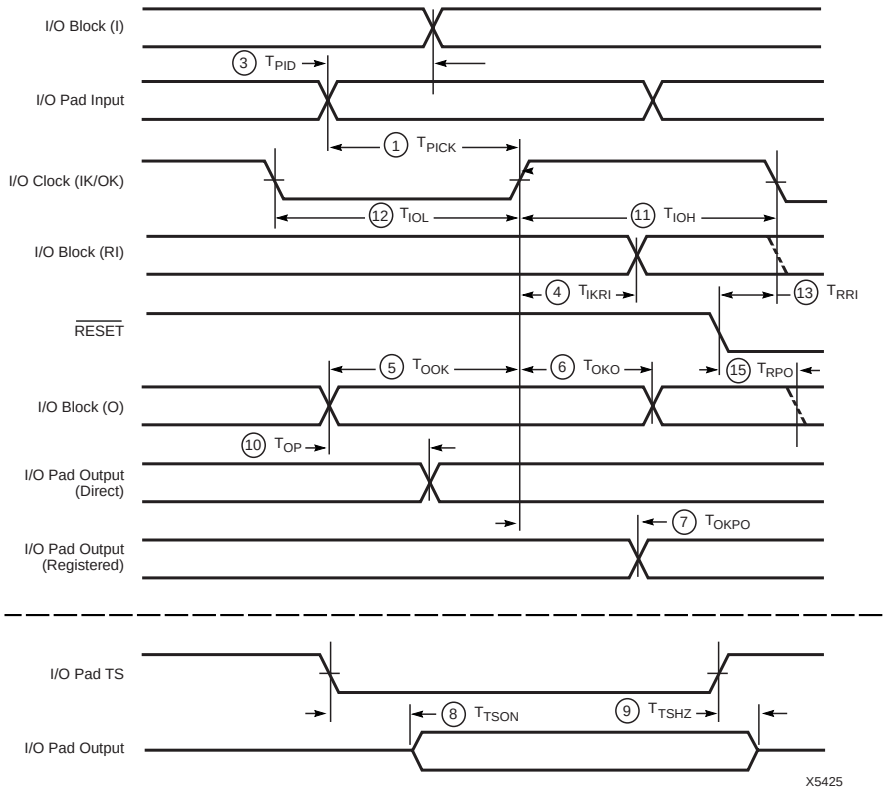
XC3100L IOB Switching Characteristics Guidelines

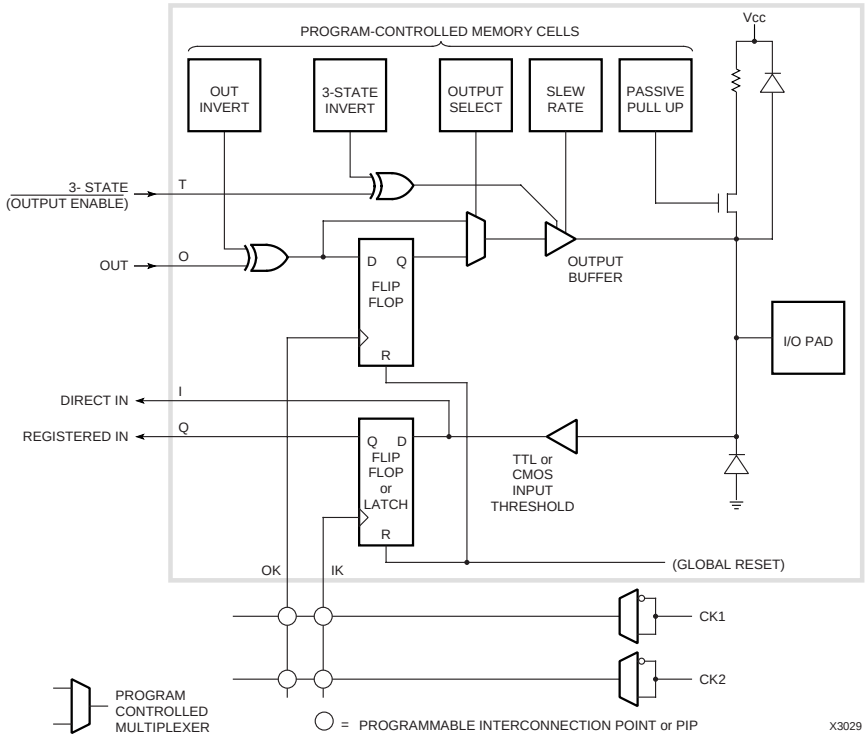
Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Since many internal timing parameters cannot be measured directly, they are derived from benchmark timing patterns. The following guidelines reflect worst-case values over the recommended operating conditions. For more detailed, more precise, and more up-to-date timing information, use the values provided by the timing calculator and used in the simulator.

	Speed Grade		-3		-2		
Description	**Symbol**		**Min**	**Max**	**Min**	**Max**	**Units**
Propagation Delays (Input)							
Pad to Direct In (I)	3	T_{PID}		2.2		2.0	ns
Pad to Registered In (Q) with latch (XC3100L) transparent		T_{PTG}		11.0		11.0	ns
Clock (IK) to Registered In (Q)	4	T_{IKRI}		2.2		1.9	ns
Set-up Time (Input)							
Pad to Clock (IK) set-up time	1	T_{PICK}					
XC3142L			9.5		9.0		ns
XC3190L			9.9		9.4		ns
Propagation Delays (Output)							
Clock (OK) to Pad (fast)	7	T_{OKPO}		4.4		4.0	ns
same (slew rate limited)	7	T_{OK} PO		10.0		9.7	ns
Output (O) to Pad (fast)	10	T_{OPF}		3.3		3.0	ns
same (slew-rate limited)(XC3100L)	10	T_{OPF}		9.0		8.7	ns
3-state to Pad begin hi-Z (fast)	9	T_{TSHZ}		5.5		5.0	ns
same (slew-rate limited)	9	T_{TSHZ}		5.5		5.0	ns
3-state to Pad active and valid (fast)(XC3100L)	8	T_{TSON}		9.0		8.5	ns
same (slew -rate limited)	8	T_{TSON}		15.0		14.2	ns
Set-up and Hold Times (Output)							
Output (O) to clock (OK) set-up time (XC3100L)	5	T_{OOK}	4.0		3.6		ns
Output (O) to clock (OK) hold time	6	T_{OKO}	0		0		ns
Clock							
Clock High time	11	T_{IOH}	1.6		1.3		ns
Clock Low time	12	T_{IOL}	1.6		1.3		ns
Export Control Maximum flip-flop toggle rate		F_{TOG}	270		325		MHz
Global Reset Delays							
$\overline{\text{RESET}}$ Pad to Registered In (Q)							
(XC3142L)	13	T_{RRI}		16.0		16.0	ns
(XC3190L)				21.0		21.0	ns
$\overline{\text{RESET}}$ Pad to output pad (fast)	15	T_{RPO}		17.0		17.0	ns
(slew-rate limited)	15	T_{RPO}		23.0		23.0	ns
			Advance				

Notes: 1. Timing is measured at pin threshold, with 50 pF external capacitive loads (incl. test fixture). Typical slew rate limited output rise/fall times are approximately four times longer.
2. Voltage levels of unused (bonded and unbonded) pads must be valid logic levels. Each can be configured with the internal pull-up resistor or alternatively configured as a driven output or driven from an external source.
3. Input pad set-up time is specified with respect to the internal clock (IK). In order to calculate system set-up time, subtract clock delay (pad to ik) from the input pad set-up time value. Input pad holdtime with respect to the internal clock (IK) is negative. This means that pad level changes immediately before the internal clock edge (IK) will not be recognized.

XC3100L IOB Switching Characteristics Guidelines (continued)





XC3000 Series 132-Pin Ceramic and Plastic PGA Pinouts

XC3000A, XC3000L, XC3100A, and XC3100L families have identical pinouts

PGA Pin Number	XC3042A XC3064A	PGA Pin Number	XC3042A XC3064A	PGA Pin Number	XC3042A XC3064A	PGA Pin Number	XC3042A XC3064A
C4	GND	B13	M1-RD	P14	RESET	M3	DOUT-I/O
A1	PWRDN	C11	GND	M11	VCC	P1	CCLK
C3	I/O-TCLKIN	A14	M0-RT	N13	DONE-PG	M4	VCC
B2	I/O	D12	VCC	M12	D7-I/O	L3	GND
B3	I/O	C13	M2-I/O	P13	XTL1-I/O-BCLKIN	M2	A0-WS-I/O
A2	I/O*	B14	HDC-I/O	N12	I/O	N1	A1-CS2-I/O
B4	I/O	C14	I/O	P12	I/O	M1	I/O
C5	I/O	E12	I/O	N11	D6-I/O	K3	I/O
A3	I/O*	D13	I/O	M10	I/O	L2	A2-I/O
A4	I/O	D14	LDC-I/O	P11	I/O*	L1	A3-I/O
B5	I/O	E13	I/O*	N10	I/O	K2	I/O
C6	I/O	F12	I/O	P10	I/O	J3	I/O
A5	I/O	E14	I/O	M9	D5-I/O	K1	A15-I/O
B6	I/O	F13	I/O	N9	CS0-I/O	J2	A4-I/O
A6	I/O	F14	I/O	P9	I/O*	J1	I/O*
B7	I/O	G13	I/O	P8	I/O*	H1	A14-I/O
C7	GND	G14	INIT-I/O	N8	D4-I/O	H2	A5-I/O
C8	VCC	G12	VCC	P7	I/O	H3	GND
A7	I/O	H12	GND	M8	VCC	G3	VCC
B8	I/O	H14	I/O	M7	GND	G2	A13-I/O
A8	I/O	H13	I/O	N7	D3-I/O	G1	A6-I/O
A9	I/O	J14	I/O	P6	CS1-I/O	F1	I/O*
B9	I/O	J13	I/O	N6	I/O*	F2	A12-I/O
C9	I/O	K14	I/O	P5	I/O*	E1	A7-I/O
A10	I/O	J12	I/O	M6	D2-I/O	F3	I/O
B10	I/O	K13	I/O	N5	I/O	E2	I/O
A11	I/O*	L14	I/O*	P4	I/O	D1	A11-I/O
C10	I/O	L13	I/O	P3	I/O	D2	A8-I/O
B11	I/O	K12	I/O	M5	D1-I/O	E3	I/O
A12	I/O*	M14	I/O	N4	RDY/BUSY-RCLK-I/O	C1	I/O
B12	I/O	N14	I/O	P2	I/O	B1	A10-I/O
A13	I/O*	M13	XTL2(IN)-I/O	N3	I/O	C2	A9-I/O
C12	I/O	L12	GND	N2	D0-DIN-I/O	D3	VCC

Unprogrammed IOBs have a default pull-up. This prevents an undefined pad level for unbonded or unused IOBs. Programmed outputs are default slew-rate limited.

* Indicates unconnected package pins (14) for the XC3042A.

XC3000 Series 160-Pin PQFP Pinouts

XC3000A, XC3000L, XC3100A, and XC3100L families have identical pinouts

PQFP Pin Number	XC3064A, XC3090A, XC3195A
1	I/O*
2	I/O*
3	I/O*
4	I/O
5	I/O
6	I/O
7	I/O
8	I/O
9	I/O
10	I/O
11	I/O
12	I/O
13	I/O
14	I/O
15	I/O
16	I/O
17	I/O
18	I/O
19	GND
20	VCC
21	I/O*
22	I/O
23	I/O
24	I/O
25	I/O
26	I/O
27	I/O
28	I/O
29	I/O
30	I/O
31	I/O
32	I/O
33	I/O
34	I/O
35	I/O
36	I/O
37	I/O
38	I/O*
39	I/O*
40	M1-$\overline{\text{RDATA}}$

PQFP Pin Number	XC3064A, XC3090A, XC3195A
41	GND
42	M0–RTRIG
43	VCC
44	M2-I/O
45	HDC-I/O
46	I/O
47	I/O
48	I/O
49	$\overline{\text{LDC}}$-I/O
50	I/O*
51	I/O*
52	I/O
53	I/O
54	I/O
55	I/O
56	I/O
57	I/O
58	I/O
59	$\overline{\text{INIT}}$-I/O
60	VCC
61	GND
62	I/O
63	I/O
64	I/O
65	I/O
66	I/O
67	I/O
68	I/O
69	I/O
70	I/O
71	I/O
72	I/O
73	I/O
74	I/O
75	I/O*
76	XTL2-I/O
77	GND
78	$\overline{\text{RESET}}$
79	VCC
80	DONE/$\overline{\text{PG}}$

PQFP Pin Number	XC3064A, XC3090A, XC3195A
81	D7-I/O
82	XTL1-I/O-BCLKIN
83	I/O*
84	I/O
85	I/O
86	D6-I/O
87	I/O
88	I/O
89	I/O
90	I/O
91	I/O
92	D5-I/O
93	$\overline{\text{CS0}}$-I/O
94	I/O*
95	I/O*
96	I/O
97	I/O
98	D4-I/O
99	I/O
100	VCC
101	GND
102	D3-I/O
103	$\overline{\text{CS1}}$-I/O
104	I/O
105	I/O
106	I/O*
107	I/O*
108	D2-I/O
109	I/O
110	I/O
111	I/O
112	I/O
113	I/O
114	D1-I/O
115	RDY/$\overline{\text{BUSY}}$-$\overline{\text{RCLK}}$-I/O
116	I/O
117	I/O
118	I/O*
119	D0-DIN-I/O
120	DOUT-I/O

PQFP Pin Number	XC3064A, XC3090A, XC3195A
121	CCLK
122	VCC
123	GND
124	A0-$\overline{\text{WS}}$-I/O
125	A1-CS2-I/O
126	I/O
127	I/O
128	A2-I/O
129	A3-I/O
130	I/O
131	I/O
132	A15-I/O
133	A4-I/O
134	I/O
135	I/O
136	A14-I/O
137	A5-I/O
138	I/O*
139	GND
140	VCC
141	A13-I/O
142	A6-I/O
143	I/O*
144	I/O*
145	I/O
146	I/O
147	A12-I/O
148	A7-I/O
149	I/O
150	I/O
151	A11-I/O
152	A8-I/O
153	I/O
154	I/O
155	A10-I/O
156	A9-I/O
157	VCC
158	GND
159	$\overline{\text{PWRDWN}}$
160	TCLKIN-I/O

Unprogrammed IOBs have a default pull-up. This prevents an undefined pad level for unbonded or unused IOBs. Programmed IOBs are default slew-rate limited.

* Indicates unconnected package pins (18) for the XC3064A.

XC3000 Series 176-Pin TQFP Pinouts

XC3000A, XC3000L, XC3100A, and XC3100L families have identical pinouts

Pin Number	XC3090A
1	$\overline{\text{PWRDWN}}$
2	TCLKIN-I/O
3	I/O
4	I/O
5	I/O
6	I/O
7	I/O
8	I/O
9	I/O
10	I/O
11	I/O
12	I/O
13	I/O
14	I/O
15	I/O
16	I/O
17	I/O
18	I/O
19	I/O
20	I/O
21	I/O
22	GND
23	VCC
24	I/O
25	I/O
26	I/O
27	I/O
28	I/O
29	I/O
30	I/O
31	I/O
32	I/O
33	I/O
34	I/O
35	I/O
36	I/O
37	I/O
38	I/O
39	I/O
40	I/O
41	I/O
42	I/O
43	I/O
44	–

Pin Number	XC3090A
45	M1-$\overline{\text{RDATA}}$
46	GND
47	M0-RTRIG
48	VCC
49	M2-I/O
50	HDC-I/O
51	I/O
52	I/O
53	I/O
54	$\overline{\text{LDC}}$-I/O
55	–
56	I/O
57	I/O
58	I/O
59	I/O
60	I/O
61	I/O
62	I/O
63	I/O
64	I/O
65	$\overline{\text{INIT}}$-I/O
66	VCC
67	GND
68	I/O
69	I/O
70	I/O
71	I/O
72	I/O
73	I/O
74	I/O
75	I/O
76	I/O
77	I/O
78	I/O
79	I/O
80	I/O
81	I/O
82	–
83	–
84	I/O
85	XTAL2(IN)-I/O
86	GND
87	$\overline{\text{RESET}}$
88	VCC

Pin Number	XC3090A
89	DONE-$\overline{\text{PG}}$
90	D7-I/O
91	XTAL1(OUT)-BCLKIN-I/O
92	I/O
93	I/O
94	I/O
95	I/O
96	D6-I/O
97	I/O
98	I/O
99	I/O
100	I/O
101	I/O
102	D5-I/O
103	$\overline{\text{CS0}}$-I/O
104	I/O
105	I/O
106	I/O
107	I/O
108	D4-I/O
109	I/O
110	VCC
111	GND
112	D3-I/O
113	$\overline{\text{CS1}}$-I/O
114	I/O
115	I/O
116	I/O
117	I/O
118	D2-I/O
119	I/O
120	I/O
121	I/O
122	I/O
123	I/O
124	D1-I/O
125	RDY/$\overline{\text{BUSY}}$-$\overline{\text{RCLK}}$-I/O
126	I/O
127	I/O
128	I/O
129	I/O
130	D0-DIN-I/O
131	DOUT-I/O
132	CCLK

Pin Number	XC3090A
133	VCC
134	GND
135	A0-$\overline{\text{WS}}$-I/O
136	A1-CS2-I/O
137	–
138	I/O
139	I/O
140	A2-I/O
141	A3-I/O
142	–
143	–
144	I/O
145	I/O
146	A15-I/O
147	A4-I/O
148	I/O
149	I/O
150	A14-I/O
151	A5-I/O
152	I/O
153	I/O
154	GND
155	VCC
156	A13-I/O
157	A6-I/O
158	I/O
159	I/O
160	–
161	–
162	I/O
163	I/O
164	A12-I/O
165	A7-I/O
166	I/O
167	I/O
168	–
169	A11-I/O
170	A8-I/O
171	I/O
172	I/O
173	A10-I/O
174	A9-I/O
175	VCC
176	GND

Unprogrammed IOBs have a default pull-up. This prevents an undefined pad level for unbonded or unused IOBs. Programmed outputs are default slew-rate limited.