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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Obsolete
Number of LABs/CLBs	224
Number of Logic Elements/Cells	-
Total RAM Bits	46064
Number of I/O	70
Number of Gates	4500
Voltage - Supply	4.25V ~ 5.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	84-LCC (J-Lead)
Supplier Device Package	84-PLCC (29.31x29.31)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc3164a-3pc84c

Introduction

XC3000-Series Field Programmable Gate Arrays (FPGAs) provide a group of high-performance, high-density, digital integrated circuits. Their regular, extendable, flexible, user-programmable array architecture is composed of a configuration program store plus three types of configurable elements: a perimeter of I/O Blocks (IOBs), a core array of Configurable Logic Bocks (CLBs) and resources for interconnection. The general structure of an FPGA is shown in Figure 2. The development system provides schematic capture and auto place-and-route for design entry. Logic and timing simulation, and in-circuit emulation are available as design verification alternatives. The design editor is used for interactive design optimization, and to compile the data pattern that represents the configuration program.

The FPGA user logic functions and interconnections are determined by the configuration program data stored in internal static memory cells. The program can be loaded in any of several modes to accommodate various system requirements. The program data resides externally in an EEPROM, EPROM or ROM on the application circuit board, or on a floppy disk or hard disk. On-chip initialization logic provides for optional automatic loading of program data at power-up. The companion XC17XX Serial Configuration PROMs provide a very simple serial configuration program storage in a one-time programmable package.

The XC3000 Field Programmable Gate Array families provide a variety of logic capacities, package styles, temperature ranges and speed grades.

XC3000 Series Overview

There are now four distinct family groupings within the XC3000 Series of FPGA devices:

- XC3000A Family
- XC3000L Family
- XC3100A Family
- XC3100L Family

All four families share a common architecture, development software, design and programming methodology, and also common package pin-outs. An extensive Product Description covers these common aspects.

Detailed parametric information for the XC3000A, XC3000L, XC3100A, and XC3100L product families is then provided. (The XC3000 and XC3100 families are not recommended for new designs.)

Here is a simple overview of those XC3000 products currently emphasized:

- **XC3000A Family** — The XC3000A is an enhanced version of the basic XC3000 family, featuring additional interconnect resources and other user-friendly enhancements.
- **XC3000L Family** — The XC3000L is identical in architecture and features to the XC3000A family, but operates at a nominal supply voltage of 3.3 V. The XC3000L is the right solution for battery-operated and low-power applications.
- **XC3100A Family** — The XC3100A is a performance-optimized relative of the XC3000A family. While both families are bitstream and footprint compatible, the XC3100A family extends toggle rates to 370 MHz and in-system performance to over 80 MHz. The XC3100A family also offers one additional array size, the XC3195A.
- **XC3100L Family** — The XC3100L is identical in architectures and features to the XC3100A family, but operates at a nominal supply voltage of 3.3V.

Figure 1 illustrates the relationships between the families. Compared to the original XC3000 family, XC3000A offers additional functionality and increased speed. The XC3000L family offers the same additional functionality, but reduced speed due to its lower supply voltage of 3.3 V. The XC3100A family offers substantially higher speed and higher density with the XC3195A.

New XC3000 Series Compared to Original XC3000 Family

For readers already familiar with the original XC3000 family of FPGAs, the major new features in the XC3000A, XC3000L, XC3100A, and XC3100L families are listed in this section.

All of these new families are upward-compatible extensions of the original XC3000 FPGA architecture. Any bitstream used to configure an XC3000 device will configure the corresponding XC3000A, XC3000L, XC3100A, or XC3100L device exactly the same way.

The XC3100A and XC3100L FPGA architectures are upward-compatible extensions of the XC3000A and XC3000L architectures. Any bitstream used to configure an XC3000A or XC3000L device will configure the corresponding XC3100A or XC3100L device exactly the same way.

Improvements in the XC3000A and XC3000L Families

The XC3000A and XC3000L families offer the following enhancements over the popular XC3000 family:

The XC3000A and XC3000L families have additional interconnect resources to drive the I-inputs of TBUFs driving horizontal Longlines. The CLB Clock Enable input can be driven from a second vertical Longline. These two additions result in more efficient and faster designs when horizontal Longlines are used for data bussing.

During configuration, the XC3000A and XC3000L devices check the bit-stream format for stop bits in the appropriate positions. Any error terminates the configuration and pulls INIT Low.

When the configuration process is finished and the device starts up in user mode, the first activation of the outputs is automatically slew-rate limited. This feature, called Soft Startup, avoids the potential ground bounce when all out-puts are turned on simultaneously. After start-up, the slew rate of the individual outputs is, as in the XC3000 family, determined by the individual configuration option.

Improvements in the XC3100A and XC3100L Families

Based on a more advanced CMOS process, the XC3100A and XC3100L families are architecturally-identical, performance-optimized relatives of the XC3000A and XC3000L families. While all families are footprint compatible, the XC3100A family extends achievable system performance beyond 85 MHz.

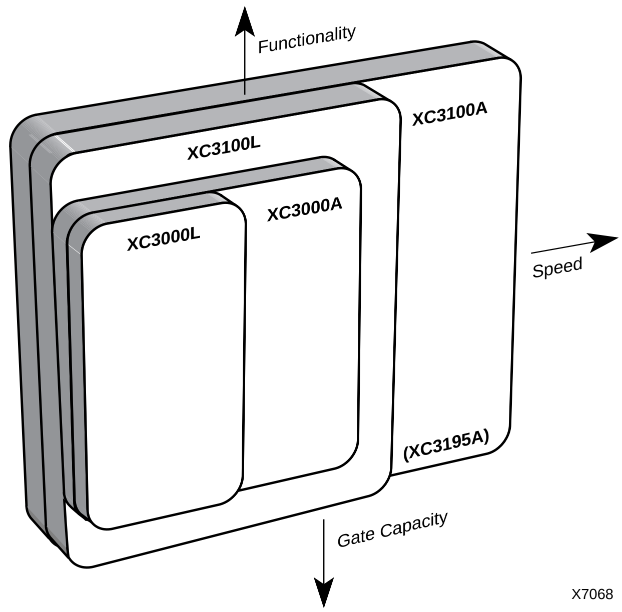

Figure 1: XC3000 FPGA Families

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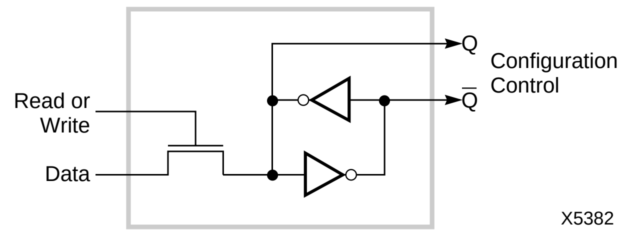

Figure 3: Static Configuration Memory Cell.
It is loaded with one bit of configuration program and controls one program selection in the Field Programmable Gate Array.

The memory cell outputs Q and Q̄ use ground and V_{CC} levels and provide continuous, direct control. The additional capacitive load together with the absence of address decoding and sense amplifiers provide high stability to the cell. Due to the structure of the configuration memory cells, they are not affected by extreme power-supply excursions or very high levels of alpha particle radiation. In reliability testing, no soft errors have been observed even in the presence of very high doses of alpha radiation.

The method of loading the configuration data is selectable. Two methods use serial data, while three use byte-wide data. The internal configuration logic utilizes framing information, embedded in the program data by the development system, to direct memory-cell loading. The serial-data framing and length-count preamble provide programming compatibility for mixes of various FPGA device devices in a synchronous, serial, daisy-chain fashion.

I/O Block

Each user-configurable IOB shown in Figure 4, provides an interface between the external package pin of the device and the internal user logic. Each IOB includes both registered and direct input paths. Each IOB provides a programmable 3-state output buffer, which may be driven by a registered or direct output signal. Configuration options allow each IOB an inversion, a controlled slew rate and a high impedance pull-up. Each input circuit also provides input clamping diodes to provide electrostatic protection, and circuits to inhibit latch-up produced by input currents.

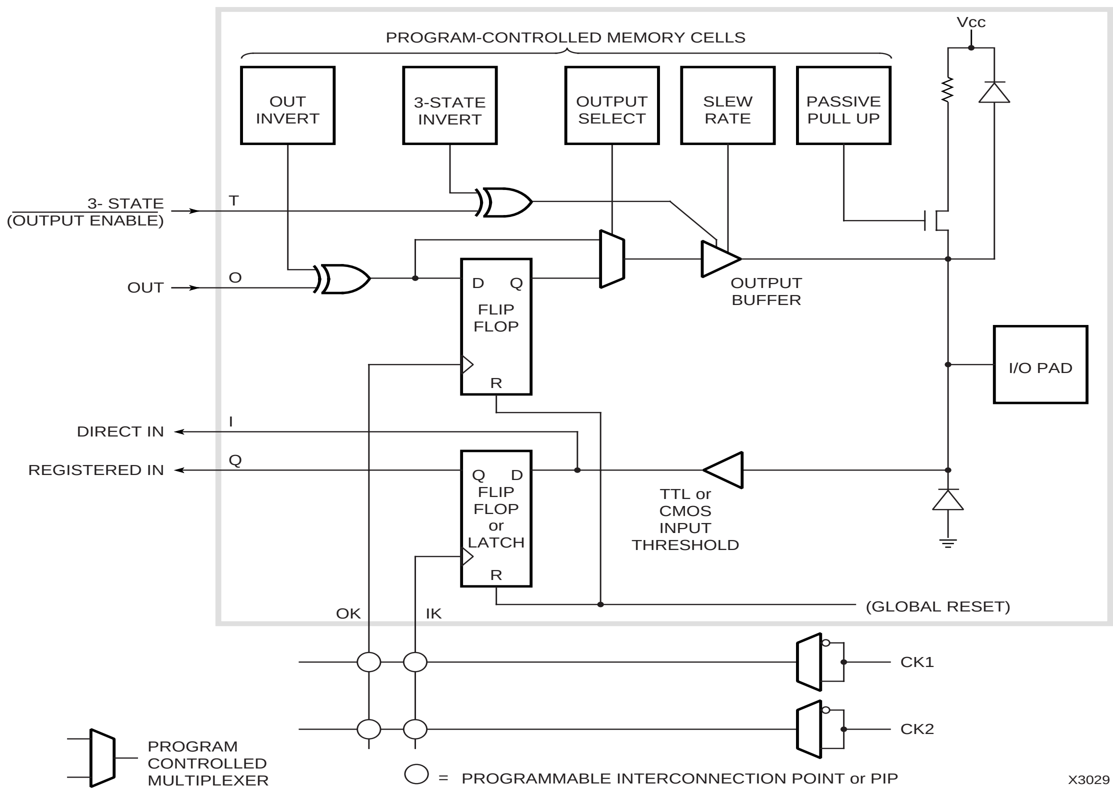

Figure 4: Input/Output Block.
Each IOB includes input and output storage elements and I/O options selected by configuration memory cells. A choice of two clocks is available on each die edge. The polarity of each clock line (not each flip-flop or latch) is programmable. A clock line that triggers the flip-flop on the rising edge is an active Low Latch Enable (Latch transparent) signal and vice versa. Passive pull-up can only be enabled on inputs, not on outputs. All user inputs are programmed for TTL or CMOS thresholds.

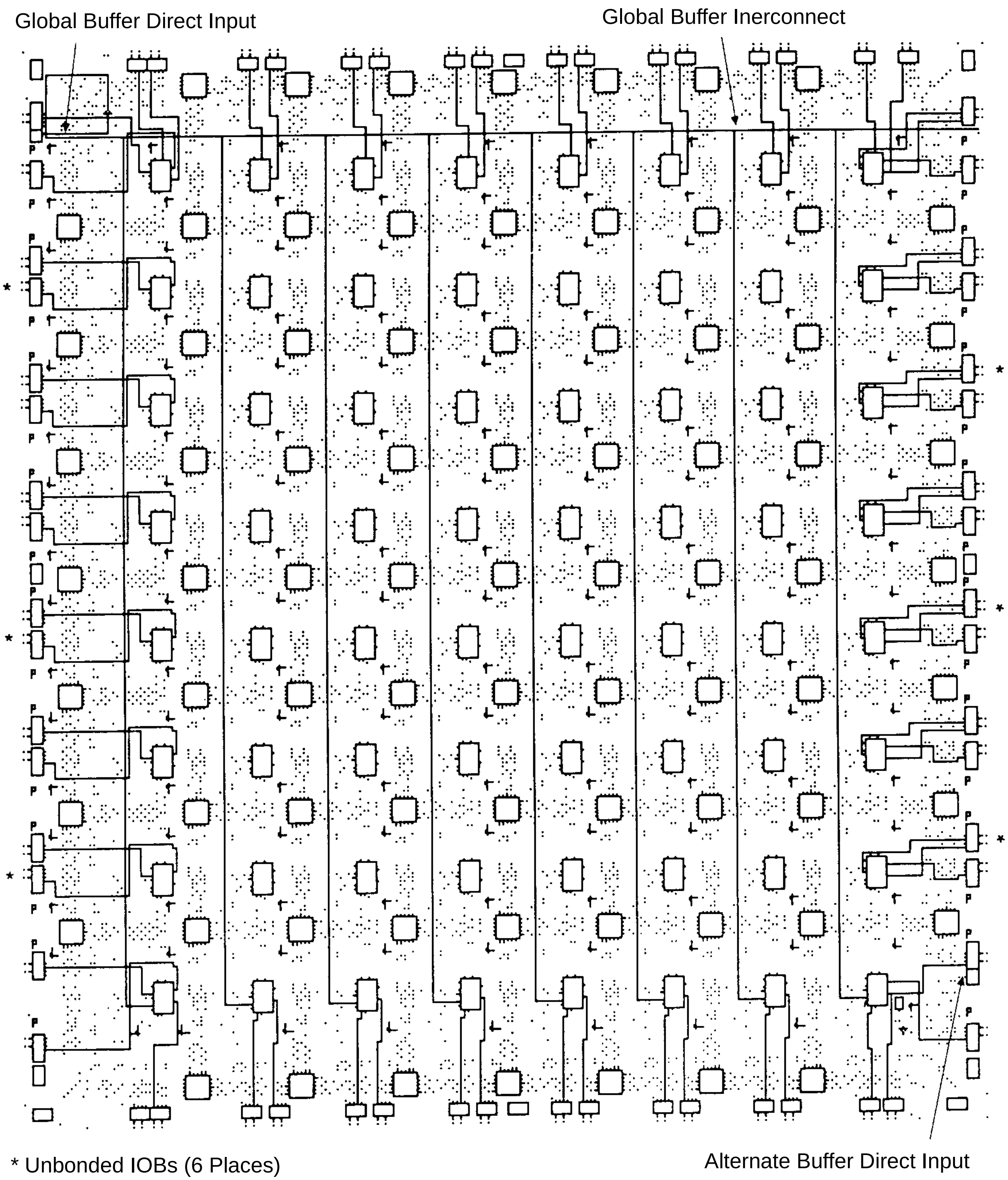

Figure 13: XC3020A Die-Edge IOBs. The XC3020A die-edge IOBs are provided with direct access to adjacent CLBs.

Longlines

The Longlines bypass the switch matrices and are intended primarily for signals that must travel a long distance, or must have minimum skew among multiple destinations. Longlines, shown in Figure 14, run vertically and horizontally the height or width of the interconnect area. Each interconnection column has three vertical Longlines, and each interconnection row has two horizontal Longlines. Two additional Longlines are located adjacent to the outer sets of switching matrices. In devices larger than the XC3020A and XC3120A FPGAs, two vertical Longlines in each column are connectable half-length lines. On the XC3020A and XC3120A FPGAs, only the outer Longlines are connectable half-length lines.

Longlines can be driven by a logic block or IOB output on a column-by-column basis. This capability provides a common low skew control or clock line within each column of logic blocks. Interconnections of these Longlines are shown in Figure 15. Isolation buffers are provided at each input to a Longline and are enabled automatically by the development system when a connection is made.

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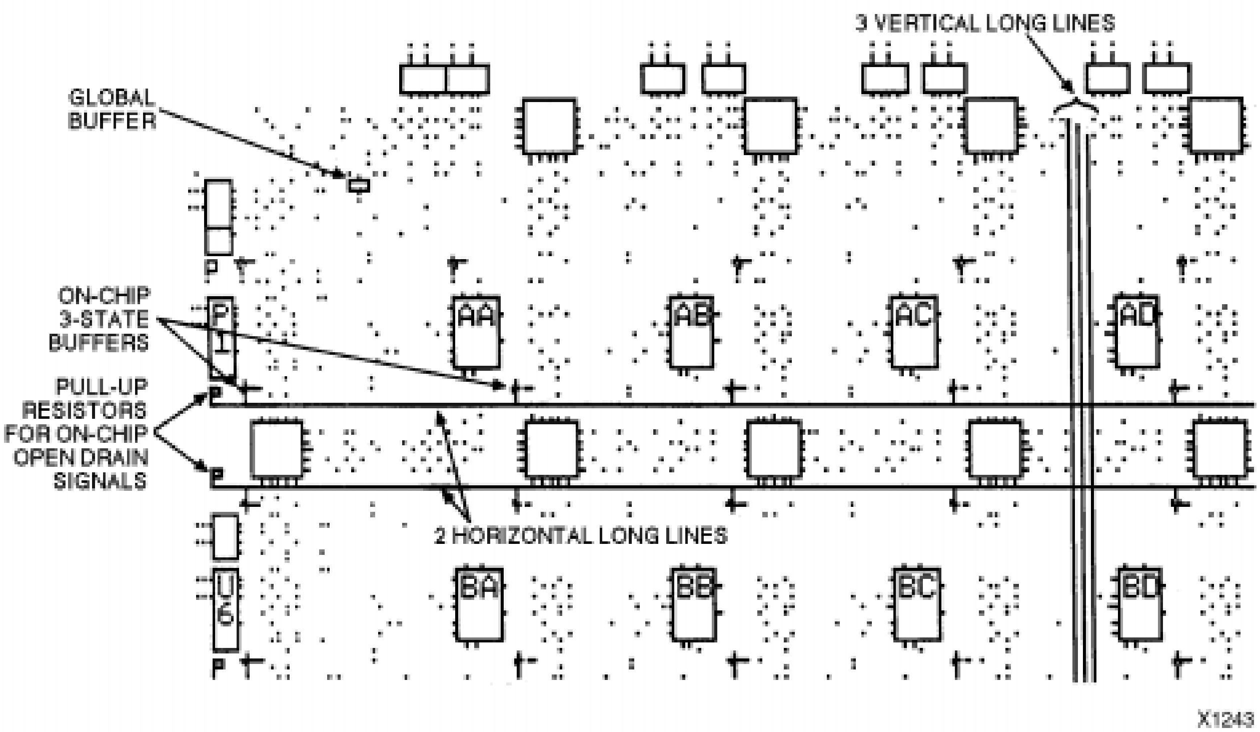


Figure 14: Horizontal and Vertical Longlines. These Longlines provide high fan-out, low-skew signal distribution in each row and column. The global buffer in the upper left die corner drives a common line throughout the FPGA.

Configuration

Initialization Phase

An internal power-on-reset circuit is triggered when power is applied. When V_{CC} reaches the voltage at which portions of the FPGA device begin to operate (nominally 2.5 to 3 V), the programmable I/O output buffers are 3-stated and a high-impedance pull-up resistor is provided for the user I/O pins. A time-out delay is initiated to allow the power supply voltage to stabilize. During this time the power-down mode is inhibited. The Initialization state time-out (about 11 to 33 ms) is determined by a 14-bit counter driven by a self-generated internal timer. This nominal 1-MHz timer is subject to variations with process, temperature and power supply. As shown in Table 1, five configuration mode choices are available as determined by the input levels of three mode pins; M0, M1 and M2.

Table 1: Configuration Mode Choices

M0	M1	M2	CCLK	Mode	Data
0	0	0	output	Master	Bit Serial
0	0	1	output	Master	Byte Wide Addr. = 0000 up
0	1	0	—	reserved	—
0	1	1	output	Master	Byte Wide Addr. = FFFF down
1	0	0	—	reserved	—
1	0	1	output	Peripheral	Byte Wide
1	1	0	—	reserved	—
1	1	1	input	Slave	Bit Serial

In Master configuration modes, the device becomes the source of the Configuration Clock (CCLK). The beginning of configuration of devices using Peripheral or Slave modes must be delayed long enough for their initialization to be completed. An FPGA with mode lines selecting a Master configuration mode extends its initialization state using four times the delay (43 to 130 ms) to assure that all daisy-chained slave devices, which it may be driving, will be ready even if the master is very fast, and the slave(s) very slow. Figure 20 shows the state sequences. At the end of Initialization, the device enters the Clear state where it clears the configuration memory. The active Low, open-drain initialization signal $\overline{\text{INIT}}$ indicates when the Initialization and Clear states are complete. The FPGA tests for the absence of an external active Low $\overline{\text{RESET}}$ before it makes a final sample of the mode lines and enters the Configuration state. An external wired-AND of one or more $\overline{\text{INIT}}$ pins can be used to control configuration by the assertion of the active-Low $\overline{\text{RESET}}$ of a master mode device or to signal a processor that the FPGAs are not yet initialized.

If a configuration has begun, a re-assertion of $\overline{\text{RESET}}$ for a minimum of three internal timer cycles will be recognized and the FPGA will initiate an abort, returning to the Clear state to clear the partially loaded configuration memory words. The FPGA will then resample $\overline{\text{RESET}}$ and the mode lines before re-entering the Configuration state.

During configuration, the XC3000A, XC3000L, XC3100A, and XC3100L devices check the bit-stream format for stop bits in the appropriate positions. Any error terminates the configuration and pulls INIT Low.

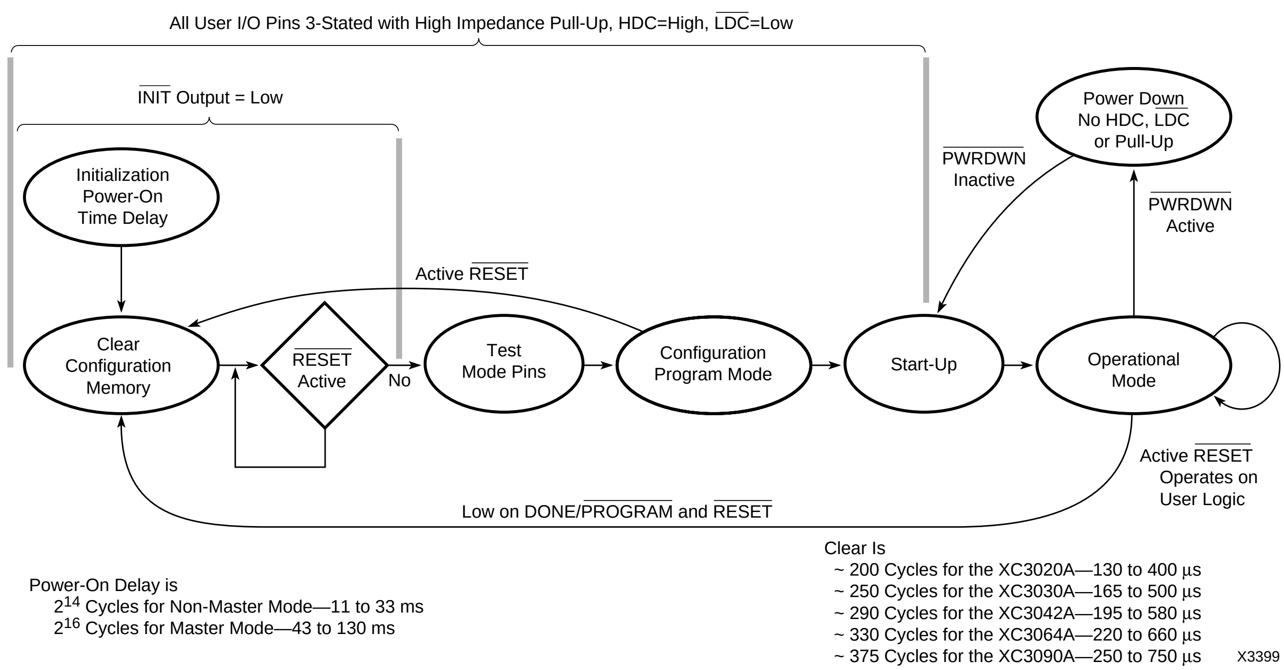
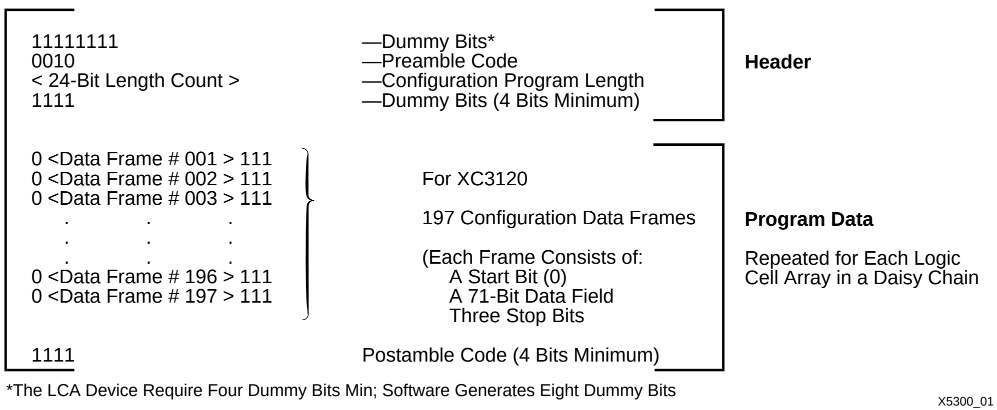


Figure 20: A State Diagram of the Configuration Process for Power-up and Reprogram.

A re-program is initiated.when a configured XC3000 series device senses a High-to-Low transition and subsequent >6 µs Low level on the DONE/PROG package pin, or, if this pin is externally held permanently Low, a High-to-Low transition and subsequent >6 µs Low time on the RESET package pin.

The device returns to the Clear state where the configuration memory is cleared and mode lines re-sampled, as for an aborted configuration. The complete configuration program is cleared and loaded during each configuration program cycle.

Length count control allows a system of multiple Field Programmable Gate Arrays, of assorted sizes, to begin operation in a synchronized fashion. The configuration program generated by the development system begins with a preamble of 111111110010 followed by a 24-bit length count representing the total number of configuration clocks needed to complete loading of the configuration program(s). The data framing is shown in Figure 21. All FPGAs connected in series read and shift preamble and length count in on positive and out on negative configuration clock edges. A device which has received the preamble and length count then presents a High Data Out until it has intercepted the appropriate number of data frames. When the configuration program memory of an FPGA is full and the length count does not yet compare, the device shifts any additional data through, as it did for preamble and length count. When the FPGA configuration memory is full and the length count compares, the device will execute



Device	XC3020A XC3020L XC3120A	XC3030A XC3030L XC3130A	XC3042A XC3042L XC3142A XC3142L	XC3064A XC3064L XC3164A	XC3090A XC3090L XC3190A XC3190L	XC3195A
Gates	1,000 to 1,500	1,500 to 2,000	2,000 to 3,000	3,500 to 4,500	5,000 to 6,000	6,500 to 7,500
CLBs	64	100	144	224	320	484
Row x Col	(8 x 8)	(10 x 10)	(12 x 12)	(16 x 14)	(20 x 16)	(22 x 22)
IOBs	64	80	96	120	144	176
Flip-flops	256	360	480	688	928	1,320
Horizontal Longlines	16	20	24	32	40	44
TBUFs/Horizontal LL	9	11	13	15	17	23
Bits per Frame (including1 start and 3 stop bits)	75	92	108	140	172	188
Frames	197	241	285	329	373	505
Program Data = Bits x Frames + 4 bits (excludes header)	14,779	22,176	30,784	46,064	64,160	94,944
PROM size (bits) = Program Data + 40-bit Header	14,819	22,216	30,824	46,104	64,200	94,984

Figure 21: Internal Configuration Data Structure for an FPGA. This shows the preamble, length count and data frames generated by the Development System.

The Length Count produced by the program = [(40-bit preamble + sum of program data + 1 per daisy chain device) rounded up to multiple of 8] – (2 ≤ K ≤ 4) where K is a function of DONE and RESET timing selected. An additional 8 is added if roundup increment is less than K. K additional clocks are needed to complete start-up after length count is reached.

be used to drive the remaining unused routing, as that might affect timing of user nets. Tie can be omitted for quick breadboard iterations where a few additional milliamps of Icc are acceptable.

The configuration bitstream begins with eight High preamble bits, a 4-bit preamble code and a 24-bit length count. When configuration is initiated, a counter in the FPGA is set to zero and begins to count the total number of configuration clock cycles applied to the device. As each configuration data frame is supplied to the device, it is internally assembled into a data word, which is then loaded in parallel into one word of the internal configuration memory array. The configuration loading process is complete when the current length count equals the loaded length count and the required configuration program data frames have been written. Internal user flip-flops are held Reset during configuration.

Two user-programmable pins are defined in the unconfigured Field Programmable Gate Array. High During Configuration (HDC) and Low During Configuration ($\overline{LDC}$) as well as DONE/$\overline{PROG}$ may be used as external control signals during configuration. In Master mode configurations it is convenient to use $\overline{LDC}$ as an active-Low EPROM Chip Enable. After the last configuration data bit is loaded and the length count compares, the user I/O pins become active. Options allow timing choices of one clock earlier or later for the timing of the end of the internal logic RESET and the assertion of the DONE signal. The open-drain DONE/$\overline{PROG}$ output can be AND-tied with multiple devices and used as an active-High READY, an active-Low PROM enable or a RESET to other portions of the system. The state diagram of Figure 20 illustrates the configuration process.

Configuration Modes

Master Mode

In Master mode, the FPGA automatically loads configuration data from an external memory device. There are three Master modes that use the internal timing source to supply the configuration clock (CCLK) to time the incoming data. Master Serial mode uses serial configuration data supplied to Data-in (DIN) from a synchronous serial source such as the Xilinx Serial Configuration PROM shown in Figure 23. Master Parallel Low and High modes automatically use parallel data supplied to the D0–D7 pins in response to the 16-bit address generated by the FPGA. Figure 25 shows an example of the parallel Master mode connections required. The HEX starting address is 0000 and increments for Master Low mode and it is FFFF and decrements for Master High mode. These two modes provide address compatibility with microprocessors which begin execution from opposite ends of memory.

Peripheral Mode

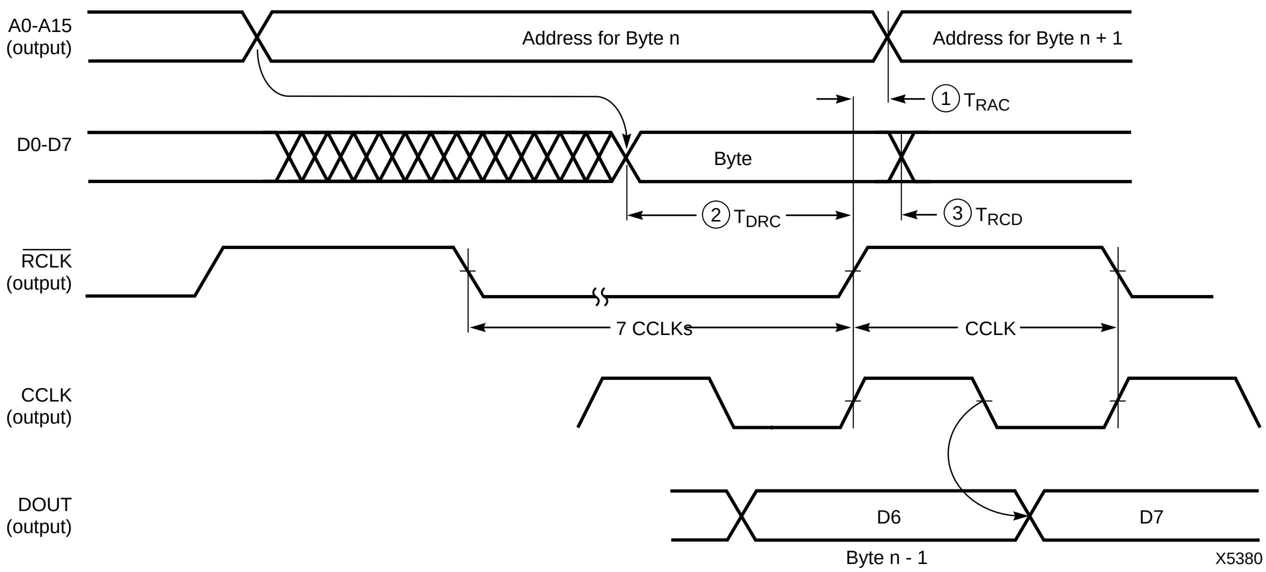
Peripheral mode provides a simplified interface through which the device may be loaded byte-wide, as a processor peripheral. Figure 27 shows the peripheral mode connections. Processor write cycles are decoded from the common assertion of the active low Write Strobe ($\overline{WS}$), and two active low and one active high Chip Selects ($\overline{CS0}$, $\overline{CS1}$, CS2). The FPGA generates a configuration clock from the internal timing generator and serializes the parallel input data for internal framing or for succeeding slaves on Data Out (DOUT). A output High on READY/$\overline{BUSY}$ pin indicates the completion of loading for each byte when the input register is ready for a new byte. As with Master modes, Peripheral mode may also be used as a lead device for a daisy-chain of slave devices.

Slave Serial Mode

Slave Serial mode provides a simple interface for loading the Field Programmable Gate Array configuration as shown in Figure 29. Serial data is supplied in conjunction with a synchronizing input clock. Most Slave mode applications are in daisy-chain configurations in which the data input is driven from the previous FPGA's data out, while the clock is supplied by a lead device in Master or Peripheral mode. Data may also be supplied by a processor or other special circuits.

Daisy Chain

The development system is used to create a composite configuration for selected FPGAs including: a preamble, a length count for the total bitstream, multiple concatenated data programs and a postamble plus an additional fill bit per device in the serial chain. After loading and passing-on the preamble and length count to a possible daisy-chain, a lead device will load its configuration data frames while providing a High DOUT to possible down-stream devices as shown in Figure 25. Loading continues while the lead device has received its configuration program and the current length count has not reached the full value. The additional data is passed through the lead device and appears on the Data Out (DOUT) pin in serial form. The lead device also generates the Configuration Clock (CCLK) to synchronize the serial output data and data in of down-stream FPGAs. Data is read in on DIN of slave devices by the positive edge of CCLK and shifted out the DOUT on the negative edge of CCLK. A parallel Master mode device uses its internal timing generator to produce an internal CCLK of 8 times its EPROM address rate, while a Peripheral mode device produces a burst of 8 CCLKs for each chip select and write-strobe cycle. The internal timing generator continues to operate for general timing and synchronization of inputs in all modes.



	Description	Symbol		Min	Max	Units
RCLK	To address valid	1	T_{RAC}	0	200	ns
	To data setup	2	T_{DRC}	60		ns
	To data hold	3	T_{RCD}	0		ns
	RCLK High		T_{RCH}	600		ns
	RCLK Low		T_{RCL}	4.0		µs

Notes: 1. At power-up, V_{CC} must rise from 2.0 V to V_{CC} min in less than 25 ms. If this is not possible, configuration can be delayed by holding RESET Low until VCC has reached 4.0 V (2.5 V for the XC3000L). A very long V_{CC} rise time of >100 ms, or a non-monotonically rising V_{CC} may require a >6-µs High level on RESET, followed by a >6-µs Low level on RESET and D/P after V_{CC} has reached 4.0 V (2.5 V for the XC3000L).
2. Configuration can be controlled by holding RESET Low with or until after the INIT of all daisy-chain slave-mode devices is High.

This timing diagram shows that the EPROM requirements are extremely relaxed:
EPROM access time can be longer than 4000 ns. EPROM data output has no hold time requirements.

Figure 26: Master Parallel Mode Programming Switching Characteristics

Slave Serial Mode

In Slave Serial mode, an external signal drives the CCLK input(s) of the FPGA(s). The serial configuration bitstream must be available at the DIN input of the lead FPGA a short set-up time before each rising CCLK edge. The lead device then presents the preamble data (and all data that overflows the lead device) on its DOUT pin. There is an internal delay of 0.5 CCLK periods, which means that DOUT changes on the falling CCLK edge, and the next device in the daisy-chain accepts data on the subsequent rising CCLK edge.

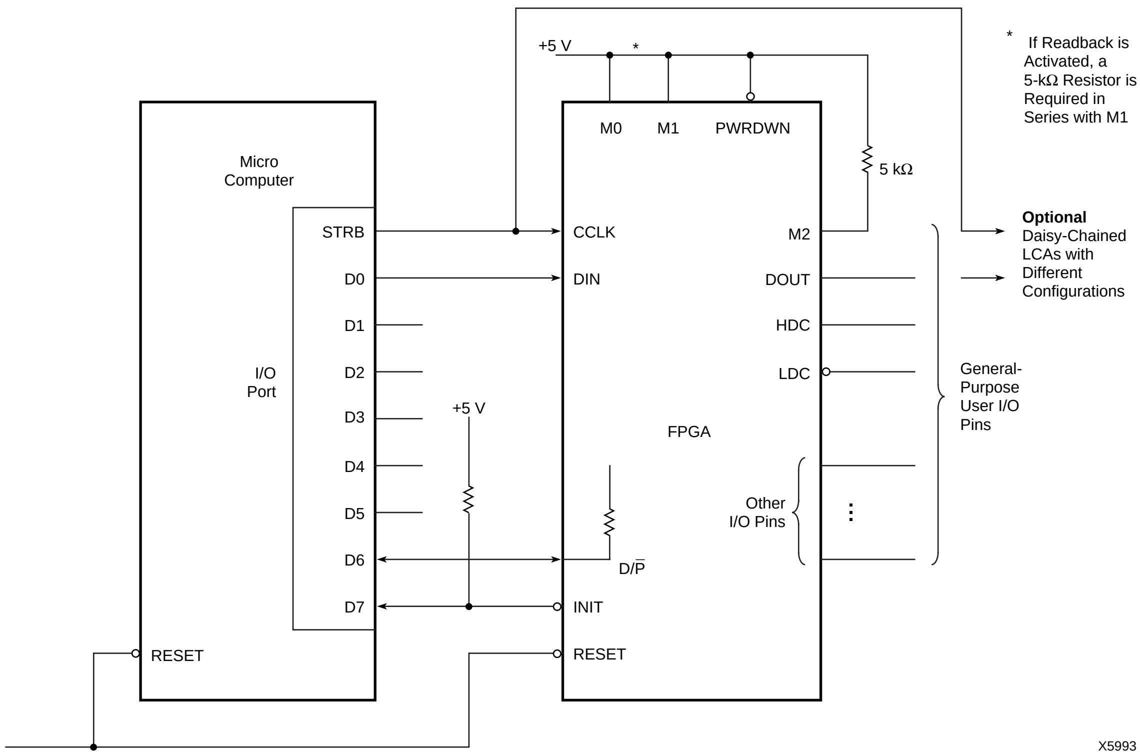


Figure 29: Slave Serial Mode Circuit Diagram

Dynamic Power Consumption

	XC3042A	XC3042L	XC3142A	
One CLB driving three local interconnects	0.25	0.17	0.25	mW per MHz
One global clock buffer and clock line	2.25	1.40	1.70	mW per MHz
One device output with a 50 pF load	1.25	1.25	1.25	mW per MHz

Power Consumption

The Field Programmable Gate Array exhibits the low power consumption characteristic of CMOS ICs. For any design, the configuration option of TTL chip input threshold requires power for the threshold reference. The power required by the static memory cells that hold the configuration data is very low and may be maintained in a power-down mode.

Typically, most of power dissipation is produced by external capacitive loads on the output buffers. This load and frequency dependent power is 25 µW/pF/MHz per output. Another component of I/O power is the external dc loading on all output pins.

Internal power dissipation is a function of the number and size of the nodes, and the frequency at which they change. In an FPGA, the fraction of nodes changing on a given clock is typically low (10-20%). For example, in a long binary counter, the total activity of all counter flip-flops is equivalent to that of only two CLB outputs toggling at the clock frequency. Typical global clock-buffer power is between 2.0 mW/MHz for the XC3020A and 3.5 mW/MHz for the XC3090A. The internal capacitive load is more a function of interconnect than fan-out. With a typical load of three general interconnect segments, each CLB output requires about 0.25 mW per MHz of its output frequency.

Because the control storage of the FPGA is CMOS static memory, its cells require a very low standby current for data retention. In some systems, this low data retention current characteristic can be used as a method of preserving configurations in the event of a primary power loss. The FPGA has built in powerdown logic which, when activated, will disable normal operation of the device and retain only the configuration data. All internal operation is suspended and output buffers are placed in their high-impedance state with no pull-ups. Different from the XC3000 family which can be powered down to a current consumption of a few microamps, the XC3100A draws 5 mA, even in power-down. This makes power-down operation less meaningful. In contrast, I_{CCPD} for the XC3000L is only 10 µA.

To force the FPGA into the Powerdown state, the user must pull the $\overline{PWRDWN}$ pin Low and continue to supply a retention voltage to the V_{CC} pins. When normal power is restored, V_{CC} is elevated to its normal operating voltage and $\overline{PWRDWN}$ is returned to a High. The FPGA resumes operation with the same internal sequence that occurs at the conclusion of configuration. Internal-I/O and logic-block storage elements will be reset, the outputs will become enabled and the DONE/$\overline{PROG}$ pin will be released.

When V_{CC} is shut down or disconnected, some power might unintentionally be supplied from an incoming signal driving an I/O pin. The conventional electrostatic input protection is implemented with diodes to the supply and ground. A positive voltage applied to an input (or output) will cause the positive protection diode to conduct and drive the V_{CC} connection. This condition can produce invalid power conditions and should be avoided. A large series resistor might be used to limit the current or a bipolar buffer may be used to isolate the input signal.

XC3000L IOB Switching Characteristics Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Since many internal timing parameters cannot be measured directly, they are derived from benchmark timing patterns. The following guidelines reflect worst-case values over the recommended operating conditions. For more detailed, more precise, and more up-to-date timing information, use the values provided by the timing calculator and used in the simulator.

Description			Speed Grade	-8		
Description		Symbol		Min	Max	Units
Propagation Delays (Input)						
Pad to Direct In (I)		3	T_{PID}		5.0	ns
Pad to Registered In (Q) with latch transparent			T_{PTG}		24.0	ns
Clock (IK) to Registered In (Q)		4	T_{IKRI}		6.0	ns
Set-up Time (Input)						
Pad to Clock (IK) set-up time		1	T_{PICK}	22.0		ns
Propagation Delays (Output)						
Clock (OK) to Pad	(fast)	7	T_{OKPO}		12.0	ns
same	(slew rate limited)	7	T_{OKPO}		28.0	ns
Output (O) to Pad	(fast)	10	T_{OPF}		9.0	ns
same	(slew-rate limited)	10	T_{OPS}		25.0	ns
3-state to Pad begin hi-Z	(fast)	9	T_{TSHZ}		12.0	ns
same	(slew-rate limited)	9	T_{TSHZ}		28.0	ns
3-state to Pad active and valid	(fast)	8	T_{TSON}		16.0	ns
same	(slew -rate limited)	8	T_{TSON}		32.0	ns
Set-up and Hold Times (Output)						
Output (O) to clock (OK) set-up time		5	T_{OOK}	12.0		ns
Output (O) to clock (OK) hold time		6	T_{OKO}	0		ns
Clock						
Clock High time		11	T_{IOH}	5.0		ns
Clock Low time		12	T_{IOL}	5.0		ns
Max. flip-flop toggle rate			F_{CLK}	80.0		MHz
Global Reset Delays (based on XC3042L)						
$\overline{\text{RESET}}$ Pad to Registered In	(Q)	13	T_{RRI}		25.0	ns
$\overline{\text{RESET}}$ Pad to output pad	(fast)	15	T_{RPO}		35.0	ns
	(slew-rate limited)	15	T_{RPO}		51.0	ns

Notes:
1. Timing is measured at pin threshold, with 50 pF external capacitive loads (incl. test fixture). Typical slew rate limited output rise/fall times are approximately four times longer.
2. Voltage levels of unused (bonded and unbonded) pads must be valid logic levels. Each can be configured with the internal pull-up resistor or alternatively configured as a driven output or driven from an external source.
3. Input pad set-up time is specified with respect to the internal clock (ik). In order to calculate system set-up time, subtract clock delay (pad to ik) from the input pad set-up time value. Input pad holdtime with respect to the internal clock (ik) is negative. This means that pad level changes immediately before the internal clock edge (ik) will not be recognized.
4. T_{PID}, T_{PTG}, and T_{PICK} are 3 ns higher for XTL2 when the pin is configured as a user input.

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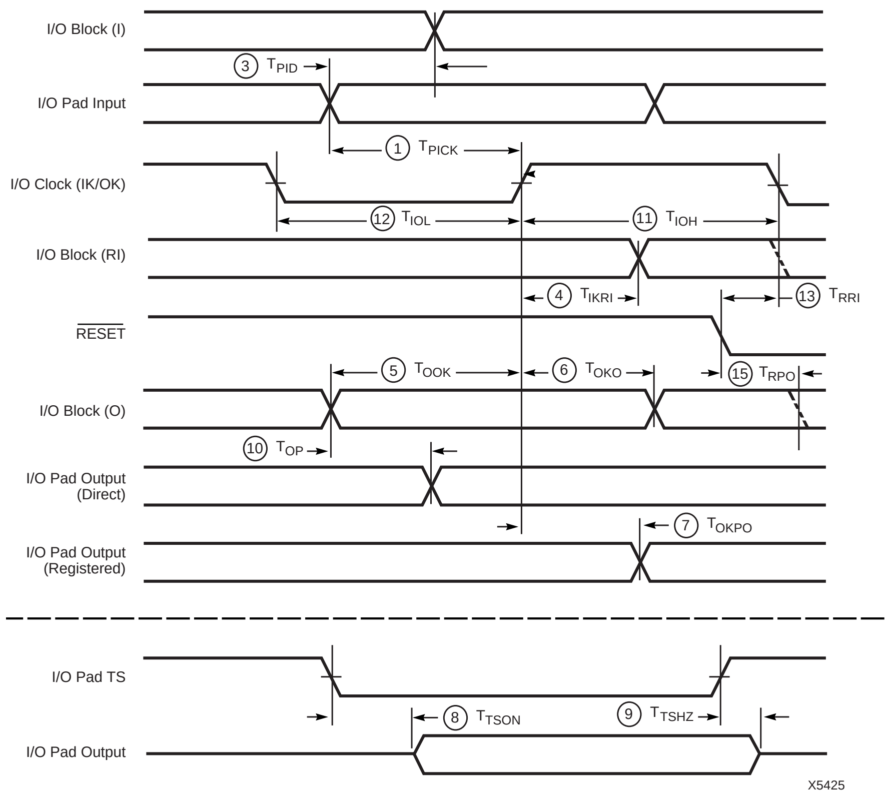
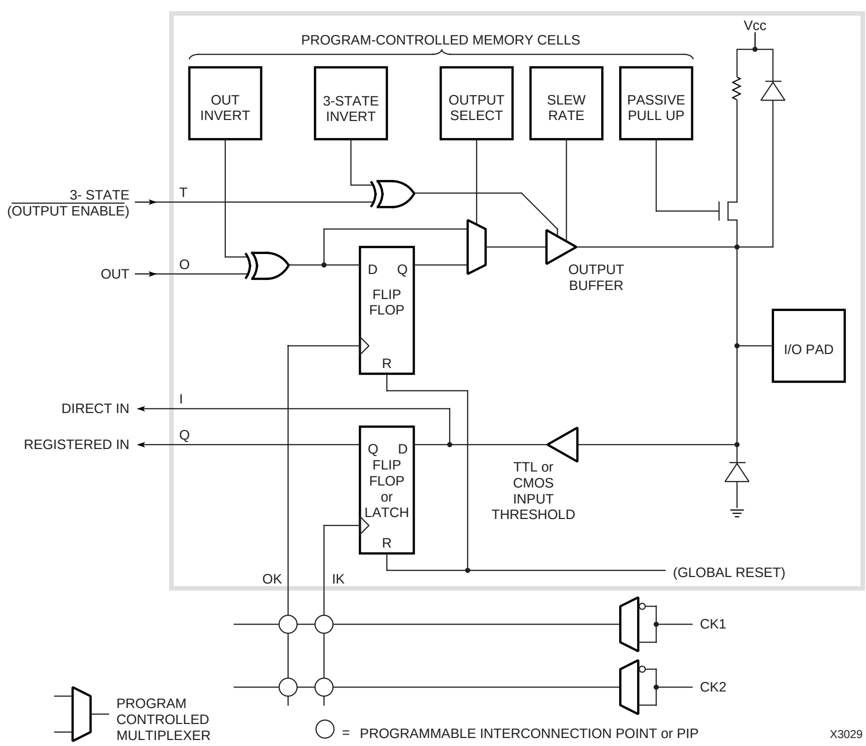
XC3000L IOB Switching Characteristics Guidelines (continued)





XC3100A CLB Switching Characteristics Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Since many internal timing parameters cannot be measured directly, they are derived from benchmark timing patterns. The following guidelines reflect worst-case values over the recommended operating conditions. For more detailed, more precise, and more up-to-date timing information, use the values provided by the timing calculator and used in the simulator.

		Speed Grade	-4		-3		-2		-1		-09		
Description		Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Units
Combinatorial Delay													
Logic Variables A, B, C, D, E, to outputs X or Y	1	T_{ILO}		3.3		2.7		2.2		1.75		1.5	ns
Sequential delay													
Clock k to outputs X or Y	8	T_{CKO}		2.5		2.1		1.7		1.4		1.25	ns
Clock k to outputs X or Y when Q is returned through function generators F or G to drive X or Y		T_{QLO}		5.2		4.3		3.5		3.1		2.7	ns
Set-up time before clock K													
Logic Variables A, B, C, D, E	2	T_{ICK}	2.5		2.1		1.8		1.7		1.5		ns
Data In DI	4	T_{DICK}	1.6		1.4		1.3		1.2		1.0		ns
Enable Clock EC	6	T_{ECCK}	3.2		2.7		2.5		2.3		2.05		ns
Reset Direct inactive RD			1.0		1.0		1.0		1.0		1.0		ns
Hold Time after clock K													
Logic Variables A, B, C, D, E	3	T_{CKI}	0		0		0		0		0		ns
Data In DI	5	T_{CKDI}	1.0		0.9		0.9		0.8		0.7		ns
Enable Clock EC	7	T_{CKEC}	0.8		0.7		0.7		0.6		0.55		ns
Clock													
Clock High time	11	T_{CH}	2.0		1.6		1.3		1.3		1.3		ns
Clock Low time	12	T_{CL}	2.0		1.6		1.3		1.3		1.3		ns
Max. flip-flop toggle rate		F_{CLK}	227		270		323		323		370		MHz
Reset Direct (RD)													
RD width	13	T_{RPW}	3.2		2.7		2.3		2.3		2.05		ns
delay from RD to outputs X or Y	9	T_{RIO}		3.7		3.1		2.7		2.4		2.15	ns
Global Reset ($\overline{\text{RESET}}$ Pad)[1]													
$\overline{\text{RESET}}$ width (Low) (XC3142A)		T_{MRW}	14.0		12.0		12.0		12.0		12.0		ns
delay from $\overline{\text{RESET}}$ pad to outputs X or Y		T_{MRQ}		14.0		12.0		12.0		12.0		12.0	ns
											Prelim		

Notes: 1. The CLB K to Q output delay (T_{CKO}, #8) of any CLB, plus the shortest possible interconnect delay, is always longer than the Data In hold time requirement (T_{CKDI}, #5) of any CLB on the same die.

2. T_{ILO}, T_{QLO} and T_{ICK} are specified for 4-input functions. For 5-input functions or base FGM functions, each of these specifications for the XC3100A family increases by 0.50 ns (-5), 0.42 ns (-4) and 0.35 ns (-3), 0.35 ns (-2), 0.30 ns (-1), and 0.30 ns (-09).

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XC3100L Absolute Maximum Ratings

Symbol	Description		Units
V_{CC}	Supply voltage relative to GND	–0.5 to +7.0	V
V_{IN}	Input voltage with respect to GND	–0.5 to V_{CC} +0.5	V
V_{TS}	Voltage applied to 3-state output	–0.5 to V_{CC} +0.5	V
T_{STG}	Storage temperature (ambient)	–65 to +150	°C
T_{SOL}	Maximum soldering temperature (10 s @ 1/16 in.)	+260	°C
T_J	Junction temperature plastic	+125	°C
	Junction temperature ceramic	+150	°C

Note: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

XC3100L Global Buffer Switching Characteristics Guidelines

	Speed Grade	-3	-2	
Description	**Symbol**	**Max**	**Max**	**Units**
Global and Alternate Clock Distribution[1]				
Either: **Normal** IOB input pad through clock buffer to any CLB or IOB clock input	T_{PID}	5.6	4.7	ns
Or: **Fast** (CMOS only) input pad through clock buffer to any CLB or IOB clock input	T_{PIDC}	4.3	3.7	ns
TBUF driving a Horizontal Longline (L.L.)[1]				
I to L.L. while T is Low (buffer active)	T_{IO}	3.1	3.1	ns
T↓ to L.L. active and valid with single pull-up resistor	T_{ON}	4.2	4.2	ns
T↑ to L.L. High with single pull-up resistor	T_{PUS}	11.4	11.4	ns
BIDI				
Bidirectional buffer delay	T_{BIDI}	1.0	0.9	ns
		Advance		

Notes: 1. Timing is based on the XC3142L, for other devices see timing calculator.
2. The use of two pull-up resistors per longline, available on other XC3000 devices, is not a valid option for XC3100L devices.

XC3100L CLB Switching Characteristics Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Since many internal timing parameters cannot be measured directly, they are derived from benchmark timing patterns. The following guidelines reflect worst-case values over the recommended operating conditions. For more detailed, more precise, and more up-to-date timing information, use the values provided by the timing calculator and used in the simulator.

		Speed Grade	-3		-2		
Description	**Symbol**		**Min**	**Max**	**Min**	**Max**	**Units**
Combinatorial Delay							
Logic Variables A, B, C, D, E, to outputs X or Y	1	T_{ILO}		2.7		2.2	ns
Sequential delay							
Clock k to outputs X or Y	8	T_{CKO}		2.1		1.7	ns
Clock k to outputs X or Y when Q is returned through function generators F or G to drive X or Y		T_{QLO}		4.3		3.5	ns
Set-up time before clock K							
Logic Variables A, B, C, D, E	2	T_{ICK}	2.1		1.8		ns
Data In DI	4	T_{DICK}	1.4		1.3		ns
Enable Clock EC	6	T_{ECCK}	2.7		2.5		ns
Reset Direct Inactive RD			1.0		1.0		ns
Hold Time after clock K							
Logic Variables A, B, C, D, E	3	T_{CKI}	0		0		ns
Data In DI	5	T_{CKDI}	0.9		0.9		ns
Enable Clock EC	7	T_{CKEC}	0.7		0.7		ns
Clock							
Clock High time	11	T_{CH}	1.6		1.3		ns
Clock Low time	12	T_{CL}	1.6		1.3		ns
Max. flip-flop toggle rate		F_{CLK}	270		325		MHz
Reset Direct (RD)							
RD width	13	T_{RPW}	2.7		2.3		ns
delay from RD to outputs X or Y	9	T_{RIO}		3.1		2.7	ns
Global Reset (RESET Pad)							
$\overline{\text{RESET}}$ width (Low)							ns
(XC3142L)		T_{MRW}	12.0		12.0		ns
delay from $\overline{\text{RESET}}$ pad to outputs X or Y		T_{MRQ}		12.0		12.0	
			Advance				

Notes: 1. The CLB K to Q delay (T_{CKO}, #8) of any CLB, plus the shortest possible interconnect delay, is always longer than the Data In hold time requirement (T_{CKDI}, #5) of any CLB on the same die.
2. T_{ILO}, T_{QLO} and T_{ICK} are specified for 4-input functions. For 5-input functions or base FGM functions, each of these specifications for the XC3100L family increase by 0.35 ns (-3) and 0.29 ns (-2).

XC3000 Series 68-Pin PLCC, 84-Pin PLCC and PGA Pinouts

XC3000A, XC3000L, XC3100A, and XC3100L families have identical pinouts

68 PLCC		XC3020A, XC3030A, XC3042A	84 PLCC
XC3030A	XC3020A		
10	10	PWRDN	12
11	11	TCLKIN-I/O	13
12	—	I/O*	14
13	12	I/O	15
14	13	I/O	16
—	—	I/O	17
15	14	I/O	18
16	15	I/O	19
—	16	I/O	20
17	17	I/O	21
18	18	VCC	22
19	19	I/O	23
—	—	I/O	24
20	20	I/O	25
—	21	I/O	26
21	22	I/O	27
22	—	I/O	28
23	23	I/O	29
24	24	I/O	30
25	25	M1-RDATA	31
26	26	M0-RTRIG	32
27	27	M2-I/O	33
28	28	HDC-I/O	34
29	29	I/O	35
30	30	LDC-I/O	36
—	31	I/O	37
—		I/O*	38
31	32	I/O	39
32	33	I/O	40
33	—	I/O*	41
34	34	INIT-I/O	42
35	35	GND	43
36	36	I/O	44
37	37	I/O	45
38	38	I/O	46
39	39	I/O	47
—	40	I/O	48
—	41	I/O	49
40		I/O*	50
41		I/O*	51
42	42	I/O	52
43	43	XTL2(IN)-I/O	53

68 PLCC		XC3020A, XC3030A, XC3042A	84 PLCC
XC3030A	XC3020A		
44	44	RESET	54
45	45	DONE-PG	55
46	46	D7-I/O	56
47	47	XTL1(OUT)-BCLKIN-I/O	57
48	48	D6-I/O	58
—	—	I/O	59
49	49	D5-I/O	60
50	50	CS0-I/O	61
51	51	D4-I/O	62
—	—	I/O	63
52	52	VCC	64
53	53	D3-I/O	65
54	54	CS1-I/O	66
55	55	D2-I/O	67
—	—	I/O	68
—	—	I/O*	69
56	56	D1-I/O	70
57	57	RDY/BUSY-RCLK-I/O	71
58	58	D0-DIN-I/O	72
59	59	DOUT-I/O	73
60	60	CCLK	74
61	61	A0-WS-I/O	75
62	62	A1-CS2-I/O	76
63	63	A2-I/O	77
64	64	A3-I/O	78
—	—	I/O*	79
—	—	I/O*	80
65	65	A15-I/O	81
66	66	A4-I/O	82
67	67	A14-I/O	83
68	68	A5-I/O	84
1	1	GND	1
2	2	A13-I/O	2
3	3	A6-I/O	3
4	4	A12-I/O	4
5	5	A7-I/O	5
—	—	I/O*	6
—	—	I/O*	7
6	6	A11-I/O	8
7	7	A8-I/O	9
8	8	A10-I/O	10
9	9	A9-I/O	11

Unprogrammed IOBs have a default pull-up. This prevents an undefined pad level for unbonded or unused IOBs. Programmed outputs are default slew-rate limited.

This table describes the pinouts of three different chips in three different packages. The pin-description column lists 84 of the 118 pads on the XC3042A (and 84 of the 98 pads on the XC3030A) that are connected to the 84 package pins. Ten pads, indicated by an asterisk, do not exist on the XC3020A, which has 74 pads; therefore the corresponding pins on the 84-pin packages have no connections to an XC3020A. Six pads on the XC3020A and 16 pads on the XC3030A, indicated by a dash (—) in the 68 PLCC column, have no connection to the 68 PLCC, but are connected to the 84-pin packages.

XC3000 Series 176-Pin TQFP Pinouts

XC3000A, XC3000L, XC3100A, and XC3100L families have identical pinouts

Pin Number	XC3090A	Pin Number	XC3090A	Pin Number	XC3090A	Pin Number	XC3090A
1	$\overline{\text{PWRDWN}}$	45	M1-$\overline{\text{RDATA}}$	89	DONE-$\overline{\text{PG}}$	133	VCC
2	TCLKIN-I/O	46	GND	90	D7-I/O	134	GND
3	I/O	47	M0-RTRIG	91	XTAL1(OUT)-BCLKIN-I/O	135	A0-$\overline{\text{WS}}$-I/O
4	I/O	48	VCC	92	I/O	136	A1-CS2-I/O
5	I/O	49	M2-I/O	93	I/O	137	–
6	I/O	50	HDC-I/O	94	I/O	138	I/O
7	I/O	51	I/O	95	I/O	139	I/O
8	I/O	52	I/O	96	D6-I/O	140	A2-I/O
9	I/O	53	I/O	97	I/O	141	A3-I/O
10	I/O	54	$\overline{\text{LDC}}$-I/O	98	I/O	142	–
11	I/O	55	–	99	I/O	143	–
12	I/O	56	I/O	100	I/O	144	I/O
13	I/O	57	I/O	101	I/O	145	I/O
14	I/O	58	I/O	102	D5-I/O	146	A15-I/O
15	I/O	59	I/O	103	$\overline{\text{CS0}}$-I/O	147	A4-I/O
16	I/O	60	I/O	104	I/O	148	I/O
17	I/O	61	I/O	105	I/O	149	I/O
18	I/O	62	I/O	106	I/O	150	A14-I/O
19	I/O	63	I/O	107	I/O	151	A5-I/O
20	I/O	64	I/O	108	D4-I/O	152	I/O
21	I/O	65	$\overline{\text{INIT}}$-I/O	109	I/O	153	I/O
22	GND	66	VCC	110	VCC	154	GND
23	VCC	67	GND	111	GND	155	VCC
24	I/O	68	I/O	112	D3-I/O	156	A13-I/O
25	I/O	69	I/O	113	$\overline{\text{CS1}}$-I/O	157	A6-I/O
26	I/O	70	I/O	114	I/O	158	I/O
27	I/O	71	I/O	115	I/O	159	I/O
28	I/O	72	I/O	116	I/O	160	–
29	I/O	73	I/O	117	I/O	161	–
30	I/O	74	I/O	118	D2-I/O	162	I/O
31	I/O	75	I/O	119	I/O	163	I/O
32	I/O	76	I/O	120	I/O	164	A12-I/O
33	I/O	77	I/O	121	I/O	165	A7-I/O
34	I/O	78	I/O	122	I/O	166	I/O
35	I/O	79	I/O	123	I/O	167	I/O
36	I/O	80	I/O	124	D1-I/O	168	–
37	I/O	81	I/O	125	RDY/$\overline{\text{BUSY}}$-$\overline{\text{RCLK}}$-I/O	169	A11-I/O
38	I/O	82	–	126	I/O	170	A8-I/O
39	I/O	83	–	127	I/O	171	I/O
40	I/O	84	I/O	128	I/O	172	I/O
41	I/O	85	XTAL2(IN)-I/O	129	I/O	173	A10-I/O
42	I/O	86	GND	130	D0-DIN-I/O	174	A9-I/O
43	I/O	87	$\overline{\text{RESET}}$	131	DOUT-I/O	175	VCC
44	–	88	VCC	132	CCLK	176	GND

Unprogrammed IOBs have a default pull-up. This prevents an undefined pad level for unbonded or unused IOBs. Programmed outputs are default slew-rate limited.

XC3000 Series 208-Pin PQFP Pinouts

XC3000A, and XC3000L families have identical pinouts

Pin Number	XC3090A	Pin Number	XC3090A	Pin Number	XC3090A	Pin Number	XC3090A
1	–	53	–	105	–	157	–
2	GND	54	–	106	VCC	158	–
3	PWRDWN	55	VCC	107	D/P	159	–
4	TCLKIN-I/O	56	M2-I/O	108	–	160	GND
5	I/O	57	HDC-I/O	109	D7-I/O	161	WS-A0-I/O
6	I/O	58	I/O	110	XTL1-BCLKIN-I/O	162	CS2-A1-I/O
7	I/O	59	I/O	111	I/O	163	I/O
8	I/O	60	I/O	112	I/O	164	I/O
9	I/O	61	LDC-I/O	113	I/O	165	A2-I/O
10	I/O	62	I/O	114	I/O	166	A3-I/O
11	I/O	63	I/O	115	D6-I/O	167	I/O
12	I/O	64	–	116	I/O	168	I/O
13	I/O	65	–	117	I/O	169	–
14	I/O	66	–	118	I/O	170	–
15	–	67	–	119	–	171	–
16	I/O	68	I/O	120	I/O	172	A15-I/O
17	I/O	69	I/O	121	I/O	173	A4-I/O
18	I/O	70	I/O	122	D5-I/O	174	I/O
19	I/O	71	I/O	123	CS0-I/O	175	I/O
20	I/O	72	–	124	I/O	176	–
21	I/O	73	–	125	I/O	177	–
22	I/O	74	I/O	126	I/O	178	A14-I/O
23	I/O	75	I/O	127	I/O	179	A5-I/O
24	I/O	76	I/O	128	D4-I/O	180	I/O
25	GND	77	INIT-I/O	129	I/O	181	I/O
26	VCC	78	VCC	130	VCC	182	GND
27	I/O	79	GND	131	GND	183	VCC
28	I/O	80	I/O	132	D3-I/O	184	A13-I/O
29	I/O	81	I/O	133	CS1-I/O	185	A6-I/O
30	I/O	82	I/O	134	I/O	186	I/O
31	I/O	83	–	135	I/O	187	I/O
32	I/O	84	–	136	I/O	188	–
33	I/O	85	I/O	137	I/O	189	–
34	I/O	86	I/O	138	D2-I/O	190	I/O
35	I/O	87	I/O	139	I/O	191	I/O
36	I/O	88	I/O	140	I/O	192	A12-I/O
37	–	89	I/O	141	I/O	193	A7-I/O
38	I/O	90	–	142	–	194	–
39	I/O	91	–	143	I/O	195	–
40	I/O	92	–	144	I/O	196	–
41	I/O	93	I/O	145	D1-I/O	197	I/O
42	I/O	94	I/O	146	RDY/BUSY-RCLK-I/O	198	I/O
43	I/O	95	I/O	147	I/O	199	A11-I/O
44	I/O	96	I/O	148	I/O	200	A8-I/O
45	I/O	97	I/O	149	I/O	201	I/O
46	I/O	98	I/O	150	I/O	202	I/O
47	I/O	99	I/O	151	DIN-D0-I/O	203	A10-I/O
48	M1-RDATA	100	XTL2-I/O	152	DOUT-I/O	204	A9-I/O
49	GND	101	GND	153	CCLK	205	VCC
50	M0-RTRIG	102	RESET	154	VCC	206	–
51	–	103	–	155	–	207	–
52	–	104	–	156	–	208	–

Unprogrammed IOBs have a default pull-up. This prevents an undefined pad level for unbonded or unused IOBs. Programmed outputs are default slew-rate limited.

* In PQ208, XC3090A and XC3195A have different pinouts.

Product Availability

Pins		44	64	68	84		100			132		144	160	175		176	208
Type		Plast. PLCC	Plast. VQFP	Plast. PLCC	Plast. PLCC	Cer. PGA	Plast. PQFP	Plast. TQFP	Plast. VQFP	Plast. PGA	Cer. PGA	Plast. TQFP	Plast. PQFP	Plast. PGA	Cer. PGA	Plast. TQFP	Plast. PQFP
Code		PC44	VQ64	PC68	PC84	PG84	PQ100	TQ100	VQ100	PP132	PG132	TQ144	PQ160	PP175	PG175	TQ176	PQ208
XC3020A	-7			CI	CI		CI										
	-6			C	C		C										
XC3030A	-7	CI	CI	CI	CI		CI		CI								
	-6	C	C	C	C		C		C								
XC3042A	-7				CI	CI	CI		CI		CI	CI					
	-6				C	C	C		C		C	C					
XC3064A	-7				CI					CI	CI	CI	CI				
	-6				C					C	C	C	C				
XC3090A	-7				CI							CI	CI	CI	CI	CI	CI
	-6				C							C	C	C	C	C	C
XC3020L	-8				CI												
XC3030L	-8		CI		CI				CI								
XC3042L	-8				CI				CI			CI					
XC3064L	-8				CI							CI					
XC3090L	-8				CI							CI				CI	
XC3120A	-4			CI	CI		CI										
	-3			CI	CI		CI										
	-2			CI	CI		CI										
	-1			C	C		C										
	-09			C	C		C										
XC3130A	-4	CI	CI	CI	CI		CI		CI								
	-3	CI	CI	CI	CI		CI		CI								
	-2	CI	CI	CI	CI		CI		CI								
	-1	C	C	C	C		C		C								
	-09	C	C	C	C		C		C								
XC3142A	-4				CI		CI		C			CI					
	-3				CI		CI		CI			CI					
	-2				CI		CI		CI			CI					
	-1				C		C		C			C					
	-09				C		C		C			C					
XC3164A	-4				CI							CI	CI				
	-3				CI							CI	CI				
	-2				CI							CI	CI				
	-1				C							C	C				
	-09				C							C	C				
XC3190A	-4				CI							CI	CI	CI	CI	CI	CI
	-3				CI							CI	CI	CI	CI	CI	CI
	-2				CI							CI	CI	CI	CI	CI	CI
	-1				C							C	C	C	C	C	C
	-09				C							C	C	C	C	C	C
XC3195A	-4				CI								CI	CI	CI		CI
	-3				CI								CI	CI	CI		CI
	-2				CI								CI	CI	CI		CI
	-1				C								C	C	C		C
	-09				C								C	C	C		C