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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	224
Number of Logic Elements/Cells	-
Total RAM Bits	46064
Number of I/O	120
Number of Gates	4500
Voltage - Supply	4.25V ~ 5.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	144-LQFP
Supplier Device Package	144-TQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc3164a-3tq144c

Detailed Functional Description

The perimeter of configurable Input/Output Blocks (IOBs) provides a programmable interface between the internal logic array and the device package pins. The array of Configurable Logic Blocks (CLBs) performs user-specified logic functions. The interconnect resources are programmed to form networks, carrying logic signals among blocks, analogous to printed circuit board traces connecting MSI/SSI packages.

The block logic functions are implemented by programmed look-up tables. Functional options are implemented by program-controlled multiplexers. Interconnecting networks between blocks are implemented with metal segments joined by program-controlled pass transistors.

These FPGA functions are established by a configuration program which is loaded into an internal, distributed array of configuration memory cells. The configuration program is loaded into the device at power-up and may be reloaded on command. The FPGA includes logic and control signals to implement automatic or passive configuration. Program data may be either bit serial or byte parallel. The development system generates the configuration program bitstream used to configure the device. The memory loading process is independent of the user logic functions.

Configuration Memory

The static memory cell used for the configuration memory in the Field Programmable Gate Array has been designed specifically for high reliability and noise immunity. Integrity of the device configuration memory based on this design is assured even under adverse conditions. As shown in Figure 3, the basic memory cell consists of two CMOS inverters plus a pass transistor used for writing and reading cell data. The cell is only written during configuration and only read during readback. During normal operation, the cell provides continuous control and the pass transistor is off and does not affect cell stability. This is quite different from the operation of conventional memory devices, in which the cells are frequently read and rewritten.

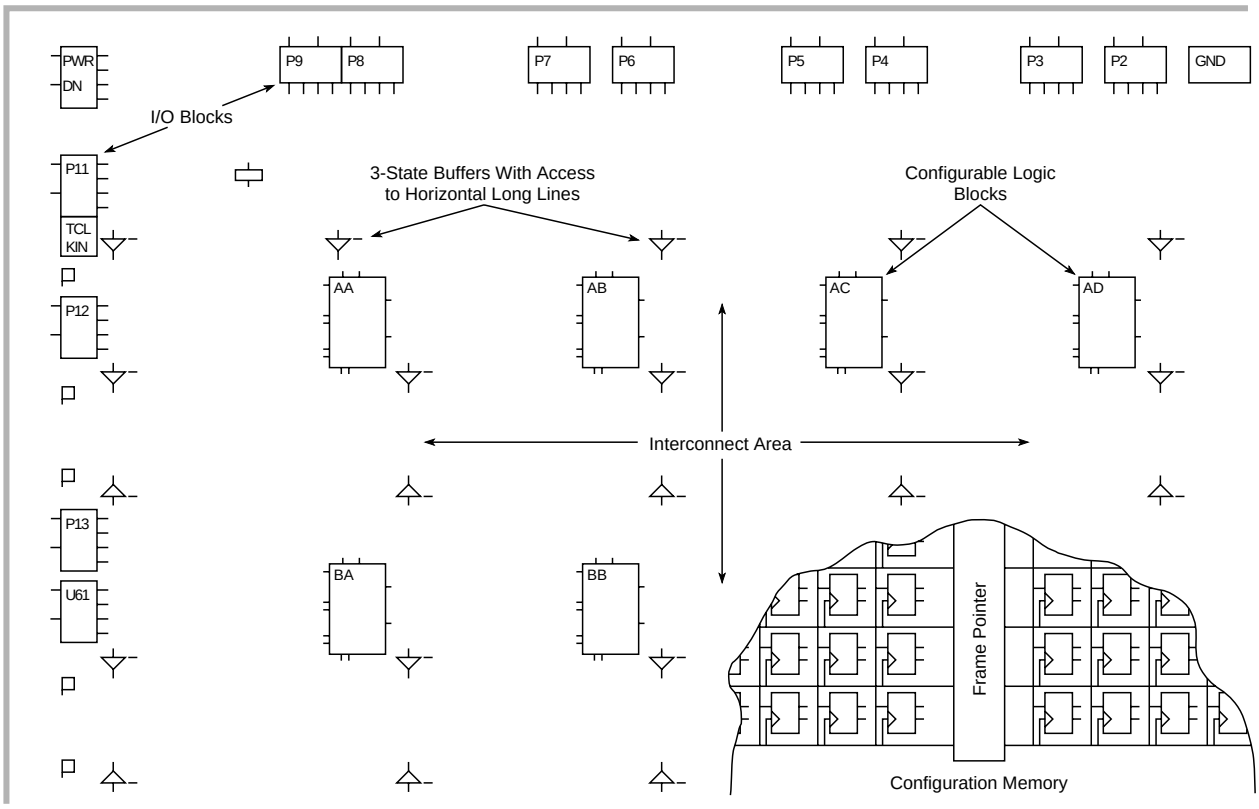

Figure 2: Field Programmable Gate Array Structure.
It consists of a perimeter of programmable I/O blocks, a core of configurable logic blocks and their interconnect resources. These are all controlled by the distributed array of configuration program memory cells.

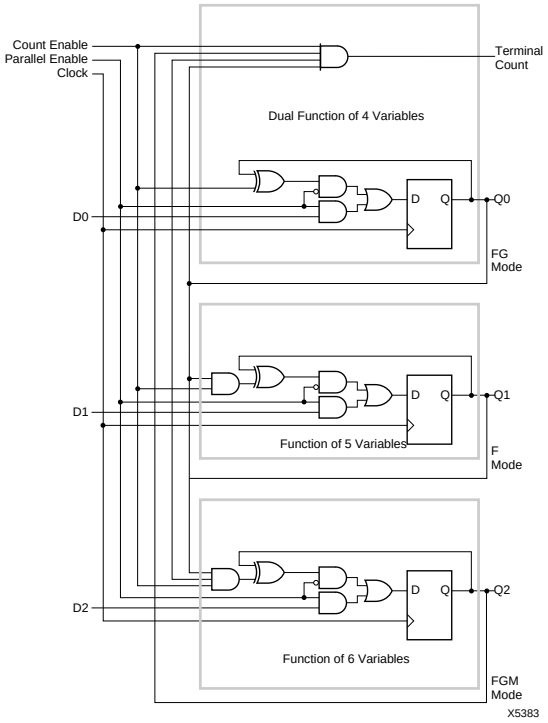

Figure 7: Counter.
The modulo-8 binary counter with parallel enable and clock enable uses one combinatorial logic block of each option.

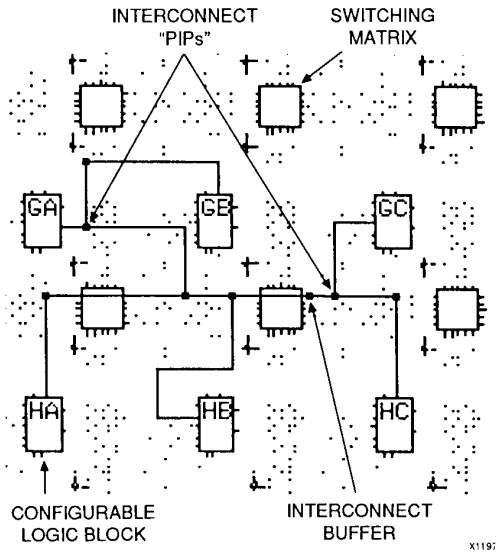

Figure 8: A Design Editor view of routing resources used to form a typical interconnection network from CLB GA.

General Purpose Interconnect

General purpose interconnect, as shown in Figure 10, consists of a grid of five horizontal and five vertical metal segments located between the rows and columns of logic and IOBs. Each segment is the height or width of a logic block. Switching matrices join the ends of these segments and allow programmed interconnections between the metal grid segments of adjoining rows and columns. The switches of an unprogrammed device are all non-conducting. The connections through the switch matrix may be established by the automatic routing or by selecting the desired pairs of matrix pins to be connected or disconnected. The legitimate switching matrix combinations for each pin are indicated in Figure 11.

Special buffers within the general interconnect areas provide periodic signal isolation and restoration for improved performance of lengthy nets. The interconnect buffers are available to propagate signals in either direction on a given general interconnect segment. These bidirectional (bidi) buffers are found adjacent to the switching matrices, above and to the right. The other PIPs adjacent to the matrices are accessed to or from Longlines. The development system automatically defines the buffer direction based on the location of the interconnection network source. The delay calculator of the development system automatically calculates and displays the block, interconnect and buffer delays for any paths selected. Generation of the simulation netlist with a worst-case delay model is provided.

Direct Interconnect

Direct interconnect, shown in Figure 12, provides the most efficient implementation of networks between adjacent CLBs or I/O Blocks. Signals routed from block to block using the direct interconnect exhibit minimum interconnect propagation and use no general interconnect resources. For each CLB, the X output may be connected directly to the B input of the CLB immediately to its right and to the C input of the CLB to its left. The Y output can use direct interconnect to drive the D input of the block immediately above and the A input of the block below. Direct interconnect should be used to maximize the speed of high-performance portions of logic. Where logic blocks are adjacent to IOBs, direct connect is provided alternately to the IOB inputs (I) and outputs (O) on all four edges of the die. The right edge provides additional direct connects from CLB outputs to adjacent IOBs. Direct interconnections of IOBs with CLBs are shown in Figure 13.

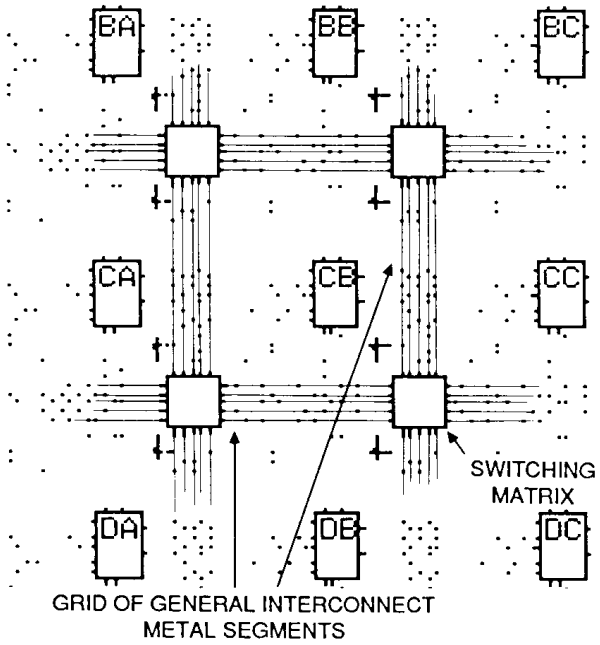

Figure 10: FPGA General-Purpose Interconnect.
Composed of a grid of metal segments that may be interconnected through switch matrices to form networks for CLB and IOB inputs and outputs.

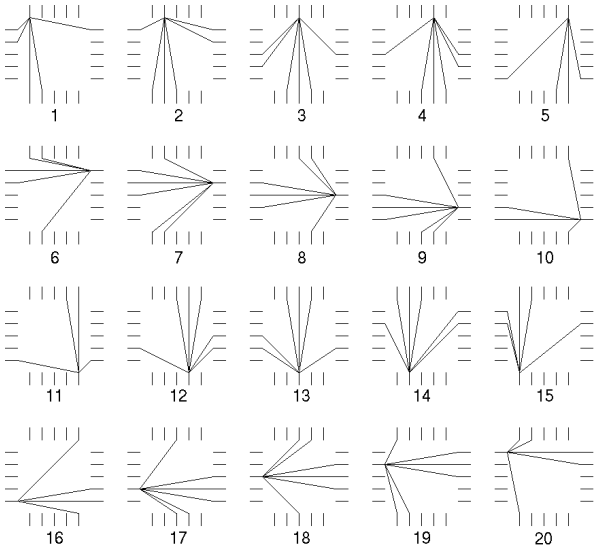

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Figure 11: Switch Matrix Interconnection Options for Each Pin.
Switch matrices on the edges are different.

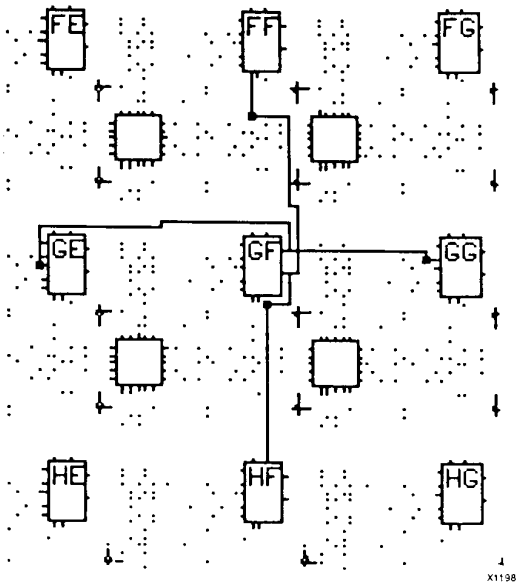

Figure 12: CLB X and Y Outputs.
The X and Y outputs of each CLB have single contact, direct access to inputs of adjacent CLBs

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Configuration Timing

This section describes the configuration modes in detail.

Master Serial Mode

In Master Serial mode, the CCLK output of the lead FPGA drives a Xilinx Serial PROM that feeds the DIN input. Each rising edge of the CCLK output increments the Serial PROM internal address counter. This puts the next data bit on the SPROM data output, connected to the DIN pin. The lead FPGA accepts this data on the subsequent rising CCLK edge.

The lead FPGA then presents the preamble data (and all data that overflows the lead device) on its DOUT pin. There is an internal delay of 1.5 CCLK periods, which means that DOUT changes on the falling CCLK edge, and the next device in the daisy-chain accepts data on the subsequent rising CCLK edge.

The SPROM $\overline{CE}$ input can be driven from either $\overline{LDC}$ or DONE. Using $\overline{LDC}$ avoids potential contention on the DIN pin, if this pin is configured as user-I/O, but $\overline{LDC}$ is then restricted to be a permanently High user output. Using DONE also avoids contention on DIN, provided the early DONE option is invoked.

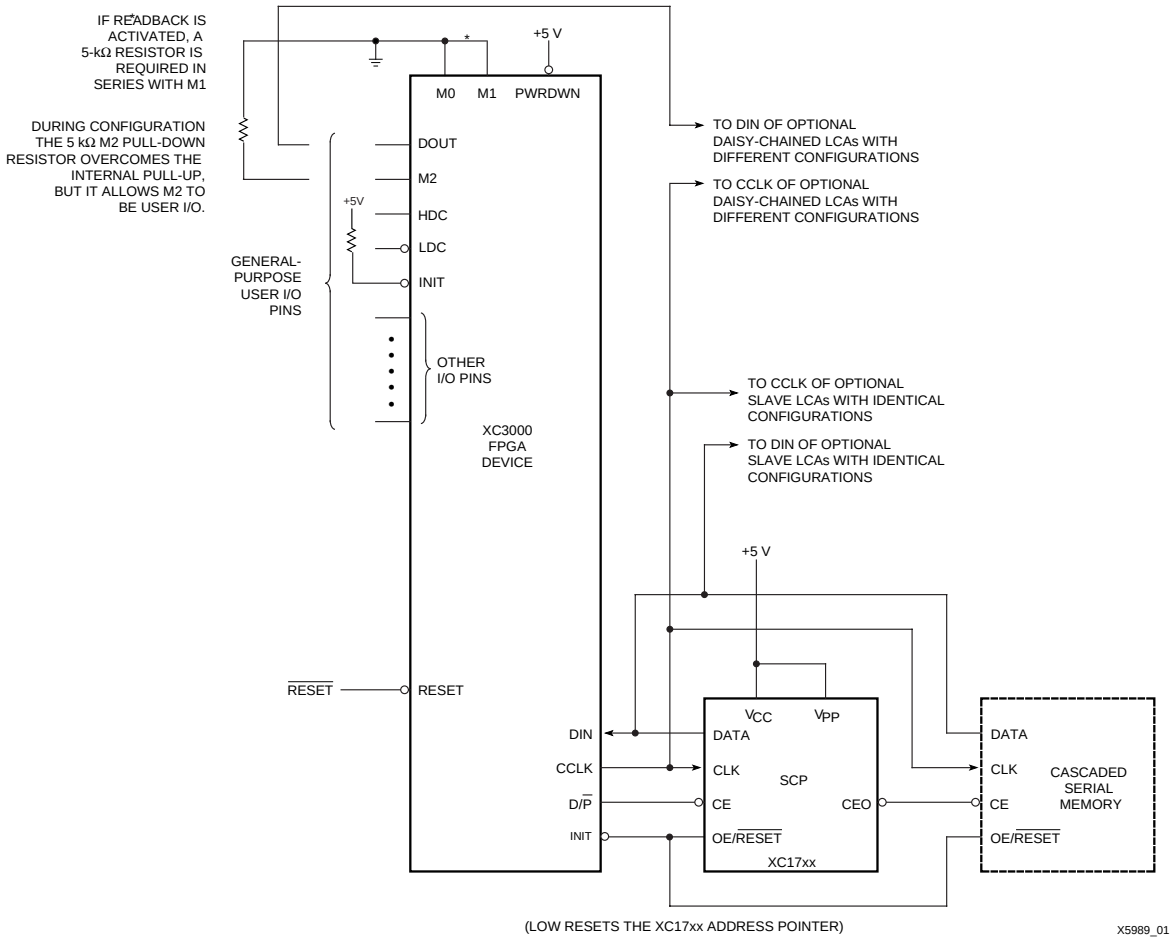
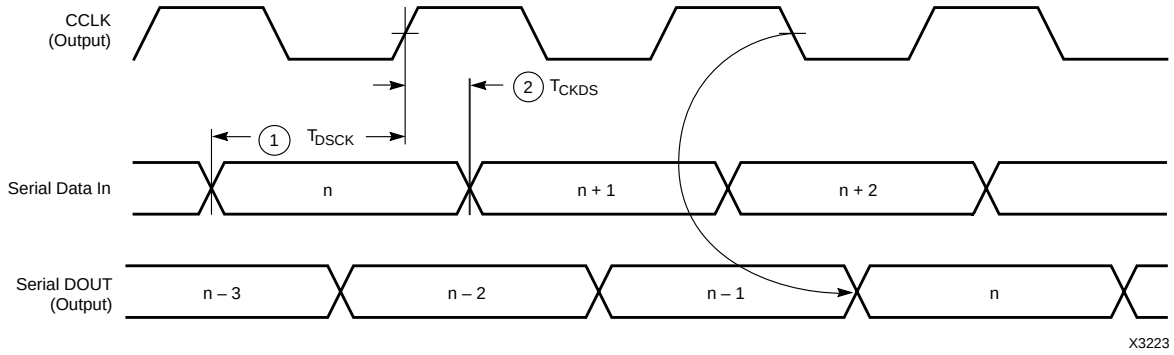


Figure 23: Master Serial Mode Circuit Diagram



	Description	Symbol		Min	Max	Units
CCLK	Data In setup	1	T_{DSCK}	60		ns
	Data In hold	2	C_{KDS}	0		ns

Notes:
1. At power-up, V_{CC} must rise from 2.0 V to V_{CC} min in less than 25 ms. If this is not possible, configuration can be delayed by holding RESET Low until V_{CC} has reached 4.0 V (2.5 V for the XC3000L). A very long V_{CC} rise time of >100 ms, or a non-monotonically rising V_{CC} may require >6-µs High level on RESET, followed by a >6-µs Low level on $\overline{\text{RESET}}$ and $D/\overline{P}$ after VCC has reached 4.0 V (2.5 V for the XC3000L).
2. Configuration can be controlled by holding $\overline{\text{RESET}}$ Low with or until after the $\overline{\text{INIT}}$ of all daisy-chain slave-mode devices is High.
3. Master-serial-mode timing is based on slave-mode testing.

Figure 24: Master Serial Mode Programming Switching Characteristics

Slave Serial Mode

In Slave Serial mode, an external signal drives the CCLK input(s) of the FPGA(s). The serial configuration bitstream must be available at the DIN input of the lead FPGA a short set-up time before each rising CCLK edge. The lead device then presents the preamble data (and all data that overflows the lead device) on its DOUT pin. There is an internal delay of 0.5 CCLK periods, which means that DOUT changes on the falling CCLK edge, and the next device in the daisy-chain accepts data on the subsequent rising CCLK edge.

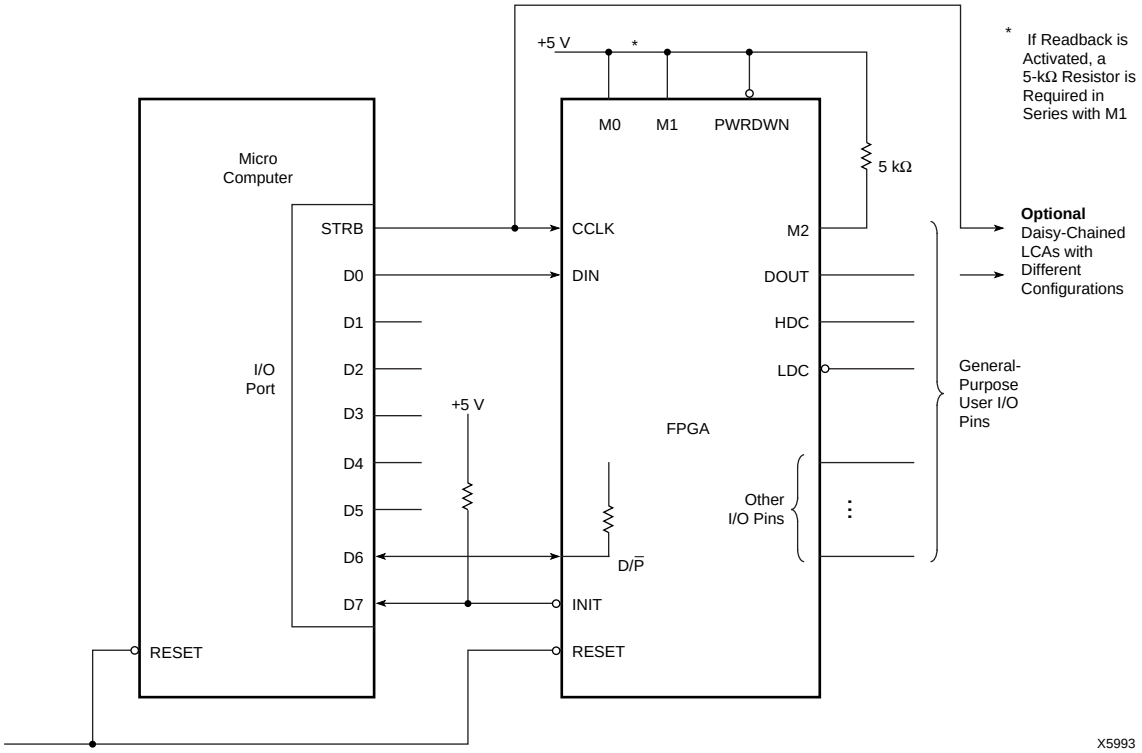
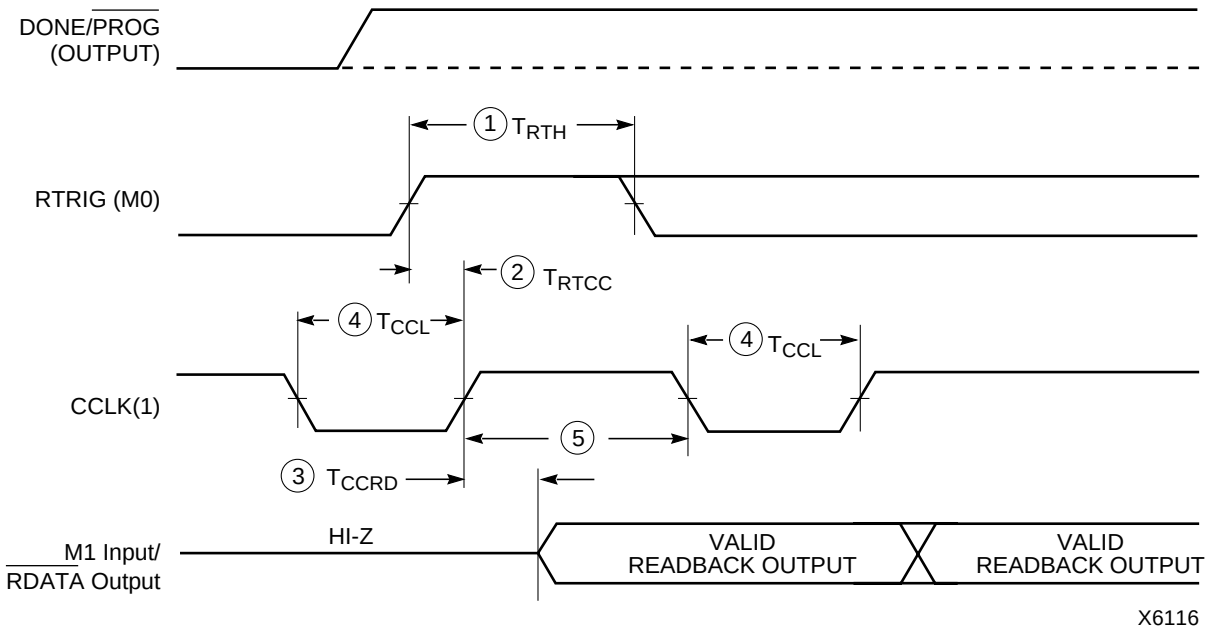


Figure 29: Slave Serial Mode Circuit Diagram

Program Readback Switching Characteristics



	Description	Symbol		Min	Max	Units
RTRIG	RTRIG High	1	T_{RTH}	250		ns
CCLK	RTRIG setup	2	T_{RTCC}	200		ns
	RDATA delay	3	T_{CCRD}		100	ns
	High time	4	T_{CCHR}	0.5		µs
	Low time	5	T_{CCLR}	0.5	5	µs

Notes: 1. During Readback, CCLK frequency may not exceed 1 MHz.
2. RETRIG (M0 positive transition) shall not be done until after one clock following active I/O pins.
3. Readback should not be initiated until configuration is complete.
4. T_{CCLR} is 5 µs min to 15 µs max for XC3000L.

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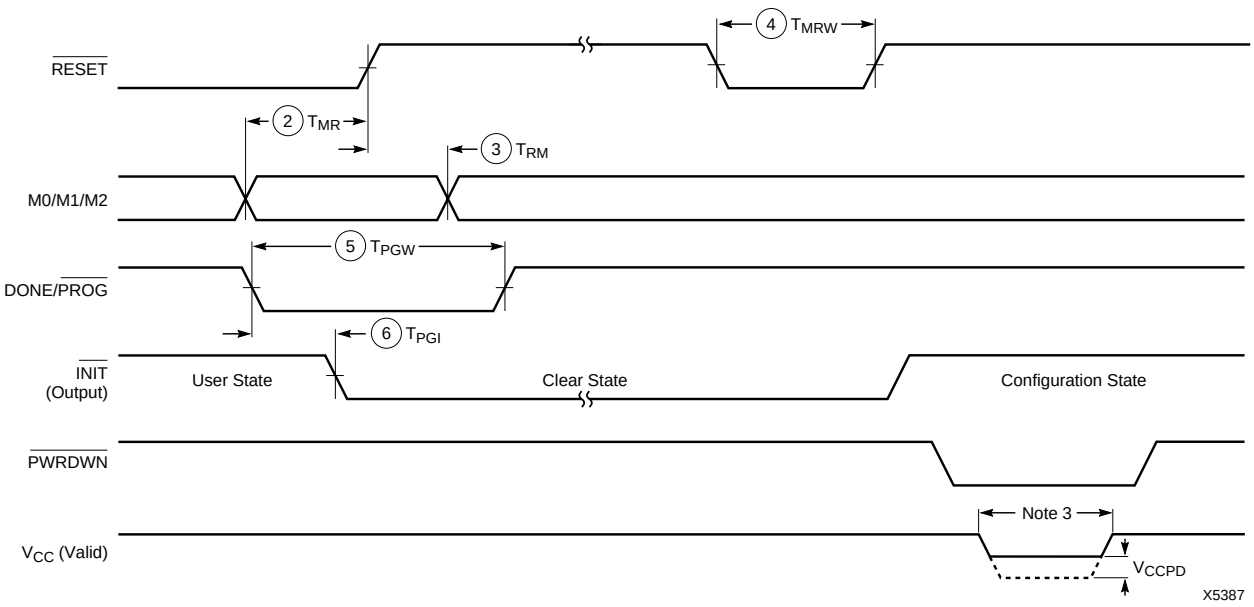
General XC3000 Series Switching Characteristics



	Description		Symbol	Min	Max	Units
RESET (2)	M0, M1, M2 setup time required	2	T_{MR}	1		µs
	M0, M1, M2 hold time required	3	T_{RM}	4.5		µs
	RESET Width (Low) req. for Abort	4	T_{MRW}	6		µs
DONE/PROG	Width (Low) required for Re-config.	5	T_{PGW}	6		µs
	INIT response after D/P is pulled Low	6	T_{PGI}		7	µs
PWRDWN (3)	Power Down V_{CC}		V_{CCPD}	2.3		V

Notes:
1. At power-up, V_{CC} must rise from 2.0 V to V_{CC} min in less than 25 ms. If this is not possible, configuration can be delayed by holding RESET Low until Vcc has reached 4.0 V (2.5 V for XC3000L). A very long Vcc rise time of >100 ms, or a non-monotonically rising V_{CC} may require a >1-µs High level on RESET, followed by a >6-µs Low level on RESET and D/P after Vcc has reached 4.0 V (2.5 V for XC3000L).
2. RESET timing relative to valid mode lines (M0, M1, M2) is relevant when RESET is used to delay configuration. The specified hold time is caused by a shift-register filter slowing down the response to RESET during configuration.
3. PWRDWN transitions must occur while V_{CC} >4.0 V(2.5 V for XC3000L).

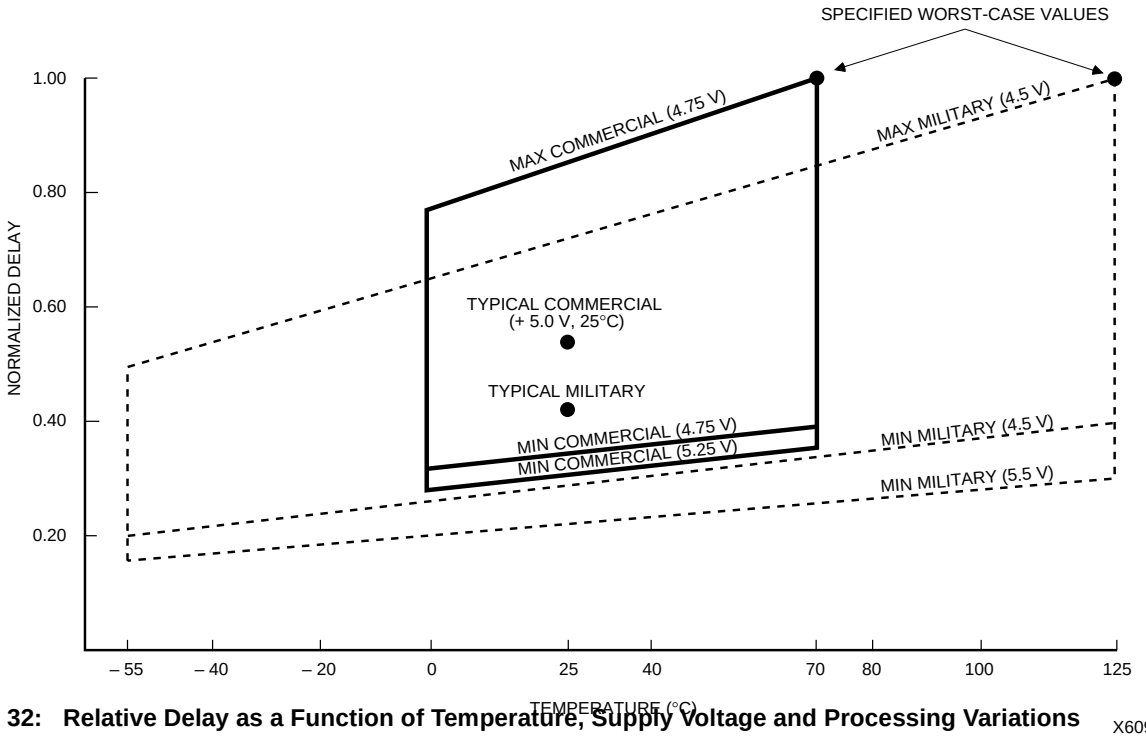


Figure 32: Relative Delay as a Function of Temperature, Supply Voltage and Processing Variations

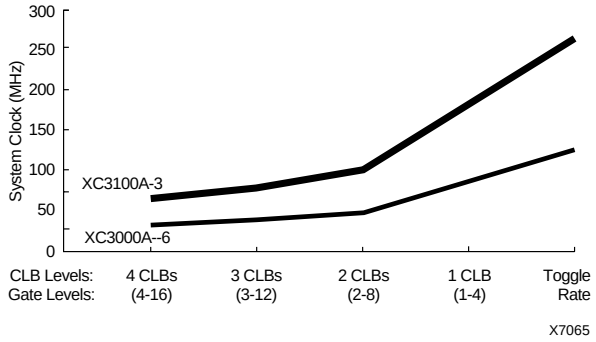


Figure 33: Clock Rate as a Function of Logic Complexity (Number of Combinational Levels between Flip-Flops)

Power

Power Distribution

Power for the FPGA is distributed through a grid to achieve high noise immunity and isolation between logic and I/O. Inside the FPGA, a dedicated V_{CC} and ground ring surrounding the logic array provides power to the I/O drivers. An independent matrix of V_{CC} and groundlines supplies the interior logic of the device. This power distribution grid provides a stable supply and ground for all internal logic, providing the external package power pins are all connected and appropriately decoupled. Typically a 0.1-µF capacitor connected near the V_{CC} and ground pins will provide adequate decoupling.

Output buffers capable of driving the specified 4- or 8-mA loads under worst-case conditions may be capable of driving as much as 25 to 30 times that current in a best case. Noise can be reduced by minimizing external load capacitance and reducing simultaneous output transitions in the same direction. It may also be beneficial to locate heavily loaded output buffers near the ground pads. The I/O Block output buffers have a slew-limited mode which should be used where output rise and fall times are not speed critical. Slew-limited outputs maintain their dc drive capability, but generate less external reflections and internal noise.

Dynamic Power Consumption

	XC3042A	XC3042L	XC3142A	
One CLB driving three local interconnects	0.25	0.17	0.25	mW per MHz
One global clock buffer and clock line	2.25	1.40	1.70	mW per MHz
One device output with a 50 pF load	1.25	1.25	1.25	mW per MHz

Power Consumption

The Field Programmable Gate Array exhibits the low power consumption characteristic of CMOS ICs. For any design, the configuration option of TTL chip input threshold requires power for the threshold reference. The power required by the static memory cells that hold the configuration data is very low and may be maintained in a power-down mode.

Typically, most of power dissipation is produced by external capacitive loads on the output buffers. This load and frequency dependent power is 25 µW/pF/MHz per output. Another component of I/O power is the external dc loading on all output pins.

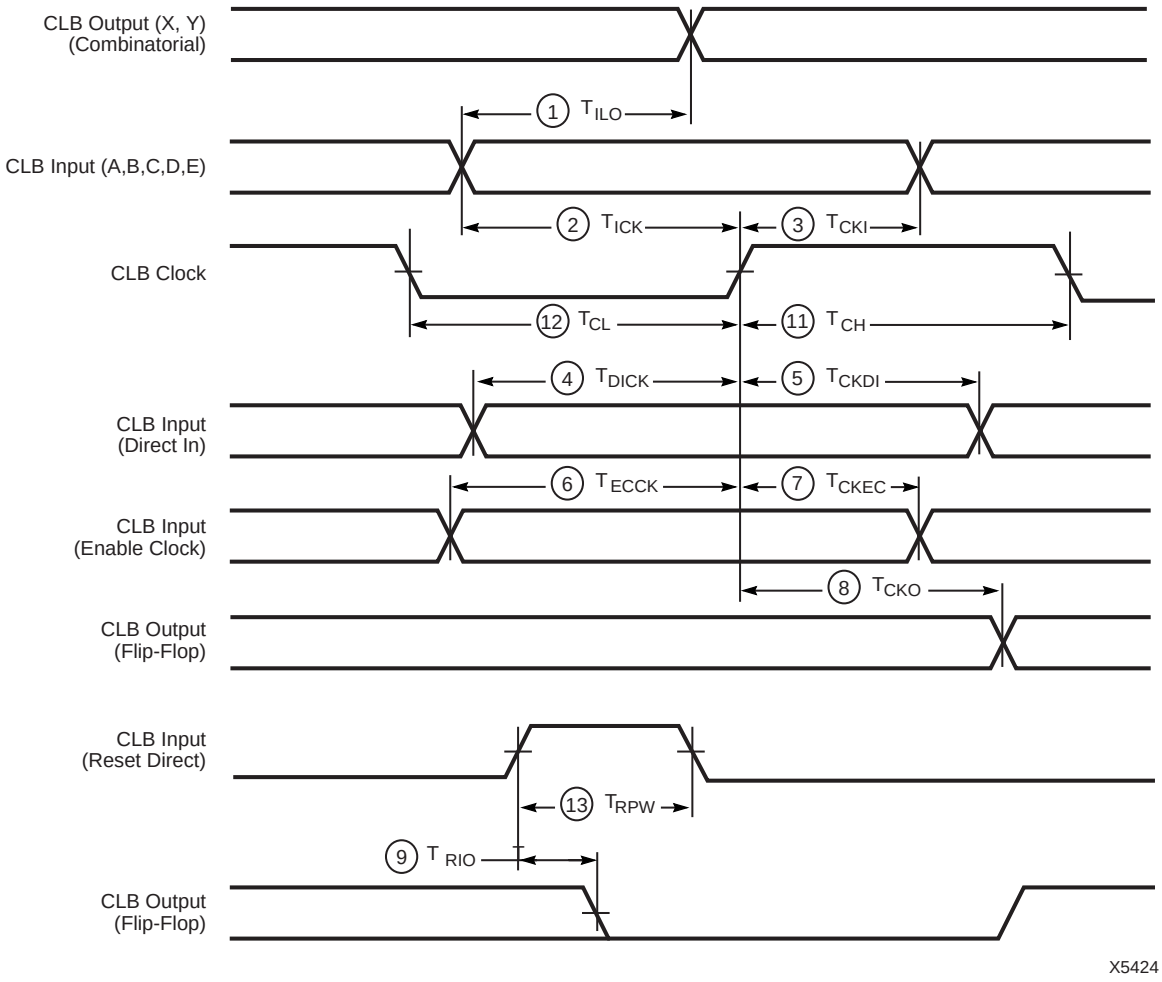
Internal power dissipation is a function of the number and size of the nodes, and the frequency at which they change. In an FPGA, the fraction of nodes changing on a given clock is typically low (10-20%). For example, in a long binary counter, the total activity of all counter flip-flops is equivalent to that of only two CLB outputs toggling at the clock frequency. Typical global clock-buffer power is between 2.0 mW/MHz for the XC3020A and 3.5 mW/MHz for the XC3090A. The internal capacitive load is more a function of interconnect than fan-out. With a typical load of three general interconnect segments, each CLB output requires about 0.25 mW per MHz of its output frequency.

Because the control storage of the FPGA is CMOS static memory, its cells require a very low standby current for data retention. In some systems, this low data retention current characteristic can be used as a method of preserving configurations in the event of a primary power loss. The FPGA has built in powerdown logic which, when activated, will disable normal operation of the device and retain only the configuration data. All internal operation is suspended and output buffers are placed in their high-impedance state with no pull-ups. Different from the XC3000 family which can be powered down to a current consumption of a few microamps, the XC3100A draws 5 mA, even in power-down. This makes power-down operation less meaningful. In contrast, I_{CCPD} for the XC3000L is only 10 µA.

To force the FPGA into the Powerdown state, the user must pull the $\overline{\text{PWRDWN}}$ pin Low and continue to supply a retention voltage to the V_{CC} pins. When normal power is restored, V_{CC} is elevated to its normal operating voltage and $\overline{\text{PWRDWN}}$ is returned to a High. The FPGA resumes operation with the same internal sequence that occurs at the conclusion of configuration. Internal-I/O and logic-block storage elements will be reset, the outputs will become enabled and the DONE/$\overline{\text{PROG}}$ pin will be released.

When V_{CC} is shut down or disconnected, some power might unintentionally be supplied from an incoming signal driving an I/O pin. The conventional electrostatic input protection is implemented with diodes to the supply and ground. A positive voltage applied to an input (or output) will cause the positive protection diode to conduct and drive the V_{CC} connection. This condition can produce invalid power conditions and should be avoided. A large series resistor might be used to limit the current or a bipolar buffer may be used to isolate the input signal.

XC3000A CLB Switching Characteristics Guidelines (continued)



XC3000A IOB Switching Characteristics Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Since many internal timing parameters cannot be measured directly, they are derived from benchmark timing patterns. The following guidelines reflect worst-case values over the recommended operating conditions. For more detailed, more precise, and more up-to-date timing information, use the values provided by the timing calculator and used in the simulator.

		Speed Grade		-7		-6		
Description		**Symbol**		**Min**	**Max**	**Min**	**Max**	**Units**
Propagation Delays (Input)								
Pad to Direct In (I)		3	T_{PID}		4.0		3.0	ns
Pad to Registered In (Q) with latch transparent			T_{PTG}		15.0		14.0	ns
Clock (IK) to Registered In (Q)		4	T_{IKRI}		3.0		2.5	ns
Set-up Time (Input)								
Pad to Clock (IK) set-up time		1	T_{PICK}	14.0		12.0		ns
Propagation Delays (Output)								
Clock (OK) to Pad	(fast)	7	T_{OKPO}		8.0		7.0	ns
same	(slew rate limited)	7	T_{OKPO}		18.0		15.0	ns
Output (O) to Pad	(fast)	10	T_{OPF}		6.0		5.0	ns
same	(slew-rate limited)	10	T_{OPS}		16.0		13.0	ns
3-state to Pad begin hi-Z	(fast)	9	T_{TSHZ}		10.0		9.0	ns
same	(slew-rate limited)	9	T_{TSHZ}		20.0		12.0	ns
3-state to Pad active and valid	(fast)	8	T_{TSON}		11.0		10.0	ns
same	(slew -rate limited)	8	T_{TSON}		21.0		18.0	ns
Set-up and Hold Times (Output)								
Output (O) to clock (OK) set-up time		5	T_{OOK}	8.0		7.0		ns
Output (O) to clock (OK) hold time		6	T_{OKO}	0		0		ns
Clock								
Clock High time		11	T_{IOH}	4.0		3.5		ns
Clock Low time		12	T_{IOL}	4.0		3.5		ns
Max. flip-flop toggle rate			F_{CLK}	113.0		135.0		MHz
Global Reset Delays (based on XC3042A)								
$\overline{\text{RESET}}$ Pad to Registered In	(Q)	13	T_{RRI}		24.0		23.0	ns
$\overline{\text{RESET}}$ Pad to output pad	(fast)	15	T_{RPO}		33.0		29.0	ns
	(slew-rate limited)	15	T_{RPO}		43.0		37.0	ns

Notes:
1. Timing is measured at pin threshold, with 50 pF external capacitive loads (incl. test fixture). Typical slew rate limited output rise/fall times are approximately four times longer.
2. Voltage levels of unused (bonded and unbonded) pads must be valid logic levels. Each can be configured with the internal pull-up resistor or alternatively configured as a driven output or driven from an external source.
3. Input pad set-up time is specified with respect to the internal clock (ik). In order to calculate system set-up time, subtract clock delay (pad to ik) from the input pad set-up time value. Input pad holdtime with respect to the internal clock (ik) is negative. This means that pad level changes immediately before the internal clock edge (ik) will not be recognized.
4. T_{PID}, T_{PTG}, and T_{PICK} are 3 ns higher for XTL2 when the pin is configured as a user input.

XC3000L Absolute Maximum Ratings

Symbol	Description		Units
V_{CC}	Supply voltage relative to GND	–0.5 to +7.0	V
V_{IN}	Input voltage with respect to GND	–0.5 to V_{CC} +0.5	V
V_{TS}	Voltage applied to 3-state output	–0.5 to V_{CC} +0.5	V
T_{STG}	Storage temperature (ambient)	–65 to +150	°C
T_{SOL}	Maximum soldering temperature (10 s @ 1/16 in.)	+260	°C
T_J	Junction temperature plastic	+125	°C
	Junction temperature ceramic	+150	°C

Note: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

XC3000L Global Buffer Switching Characteristics Guidelines

	Speed Grade	-8	
Description	**Symbol**	**Max**	**Units**
Global and Alternate Clock Distribution[1]			
Either: **Normal** IOB input pad through clock buffer to any CLB or IOB clock input	T_{PID}	9.0	ns
Or: **Fast** (CMOS only) input pad through clock buffer to any CLB or IOB clock input	T_{PIDC}	7.0	ns
TBUF driving a Horizontal Longline (L.L.)[1]			
I to L.L. while T is Low (buffer active)	T_{IO}	5.0	ns
T↓ to L.L. active and valid with single pull-up resistor	T_{ON}	12.0	ns
T↑ to L.L. High with single pull-up resistor	T_{PUS}	24.0	ns
BIDI			
Bidirectional buffer delay	T_{BIDI}	2.0	ns

Notes: 1. Timing is based on the XC3042A, for other devices see timing calculator.
2. The use of two pull-up resistors per Longline, available on other XC3000 devices, is not a valid option for XC3000L devices.

XC3000L IOB Switching Characteristics Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Since many internal timing parameters cannot be measured directly, they are derived from benchmark timing patterns. The following guidelines reflect worst-case values over the recommended operating conditions. For more detailed, more precise, and more up-to-date timing information, use the values provided by the timing calculator and used in the simulator.

		Speed Grade	-8		
Description		**Symbol**		**Min**	**Max**	**Units**
Propagation Delays (Input)						
Pad to Direct In (I)		3	T_{PID}		5.0	ns
Pad to Registered In (Q) with latch transparent			T_{PTG}		24.0	ns
Clock (IK) to Registered In (Q)		4	T_{IKRI}		6.0	ns
Set-up Time (Input)						
Pad to Clock (IK) set-up time		1	T_{PICK}	22.0		ns
Propagation Delays (Output)						
Clock (OK) to Pad	(fast)	7	T_{OKPO}		12.0	ns
same	(slew rate limited)	7	T_{OKPO}		28.0	ns
Output (O) to Pad	(fast)	10	T_{OPF}		9.0	ns
same	(slew-rate limited)	10	T_{OPS}		25.0	ns
3-state to Pad begin hi-Z	(fast)	9	T_{TSHZ}		12.0	ns
same	(slew-rate limited)	9	T_{TSHZ}		28.0	ns
3-state to Pad active and valid	(fast)	8	T_{TSON}		16.0	ns
same	(slew -rate limited)	8	T_{TSON}		32.0	ns
Set-up and Hold Times (Output)						
Output (O) to clock (OK) set-up time		5	T_{OOK}	12.0		ns
Output (O) to clock (OK) hold time		6	T_{OKO}	0		ns
Clock						
Clock High time		11	T_{IOH}	5.0		ns
Clock Low time		12	T_{IOL}	5.0		ns
Max. flip-flop toggle rate			F_{CLK}	80.0		MHz
Global Reset Delays (based on XC3042L)						
$\overline{\text{RESET}}$ Pad to Registered In	(Q)	13	T_{RRI}		25.0	ns
$\overline{\text{RESET}}$ Pad to output pad	(fast)	15	T_{RPO}		35.0	ns
	(slew-rate limited)	15	T_{RPO}		51.0	ns

Notes: 1. Timing is measured at pin threshold, with 50 pF external capacitive loads (incl. test fixture). Typical slew rate limited output rise/fall times are approximately four times longer.
2. Voltage levels of unused (bonded and unbonded) pads must be valid logic levels. Each can be configured with the internal pull-up resistor or alternatively configured as a driven output or driven from an external source.
3. Input pad set-up time is specified with respect to the internal clock (ik). In order to calculate system set-up time, subtract clock delay (pad to ik) from the input pad set-up time value. Input pad holdtime with respect to the internal clock (ik) is negative. This means that pad level changes immediately before the internal clock edge (ik) will not be recognized.
4. T_{PID}, T_{PTG}, and T_{PICK} are 3 ns higher for XTL2 when the pin is configured as a user input.

XC3100A CLB Switching Characteristics Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Since many internal timing parameters cannot be measured directly, they are derived from benchmark timing patterns. The following guidelines reflect worst-case values over the recommended operating conditions. For more detailed, more precise, and more up-to-date timing information, use the values provided by the timing calculator and used in the simulator.

	Speed Grade		-4		-3		-2		-1		-09		
Description	**Symbol**		**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**
Combinatorial Delay													
Logic Variables A, B, C, D, E, to outputs X or Y	1	T_{ILO}		3.3		2.7		2.2		1.75		1.5	ns
Sequential delay													
Clock k to outputs X or Y	8	T_{CKO}		2.5		2.1		1.7		1.4		1.25	ns
Clock k to outputs X or Y when Q is returned through function generators F or G to drive X or Y		T_{QLO}		5.2		4.3		3.5		3.1		2.7	ns
Set-up time before clock K													
Logic Variables A, B, C, D, E	2	T_{ICK}	2.5		2.1		1.8		1.7		1.5		ns
Data In DI	4	T_{DICK}	1.6		1.4		1.3		1.2		1.0		ns
Enable Clock EC	6	T_{ECCK}	3.2		2.7		2.5		2.3		2.05		ns
Reset Direct inactive RD			1.0		1.0		1.0		1.0		1.0		ns
Hold Time after clock K													
Logic Variables A, B, C, D, E	3	T_{CKI}	0		0		0		0		0		ns
Data In DI	5	T_{CKDI}	1.0		0.9		0.9		0.8		0.7		ns
Enable Clock EC	7	T_{CKEC}	0.8		0.7		0.7		0.6		0.55		ns
Clock													
Clock High time	11	T_{CH}	2.0		1.6		1.3		1.3		1.3		ns
Clock Low time	12	T_{CL}	2.0		1.6		1.3		1.3		1.3		ns
Max. flip-flop toggle rate		F_{CLK}	227		270		323		323		370		MHz
Reset Direct (RD)													
RD width	13	T_{RPW}	3.2		2.7		2.3		2.3		2.05		ns
delay from RD to outputs X or Y	9	T_{RIO}		3.7		3.1		2.7		2.4		2.15	ns
Global Reset ($\overline{\text{RESET}}$ Pad)[1]													
$\overline{\text{RESET}}$ width (Low) (XC3142A)		T_{MRW}	14.0		12.0		12.0		12.0		12.0		ns
delay from $\overline{\text{RESET}}$ pad to outputs X or Y		T_{MRQ}		14.0		12.0		12.0		12.0		12.0	ns
											Prelim		

Notes: 1. The CLB K to Q output delay (T_{CKO}, #8) of any CLB, plus the shortest possible interconnect delay, is always longer than the Data In hold time requirement (T_{CKDI}, #5) of any CLB on the same die.

2. T_{ILO}, T_{QLO} and T_{ICK} are specified for 4-input functions. For 5-input functions or base FGM functions, each of these specifications for the XC3100A family increases by 0.50 ns (-5), 0.42 ns (-4) and 0.35 ns (-3), 0.35 ns (-2), 0.30 ns (-1), and 0.30 ns (-09).

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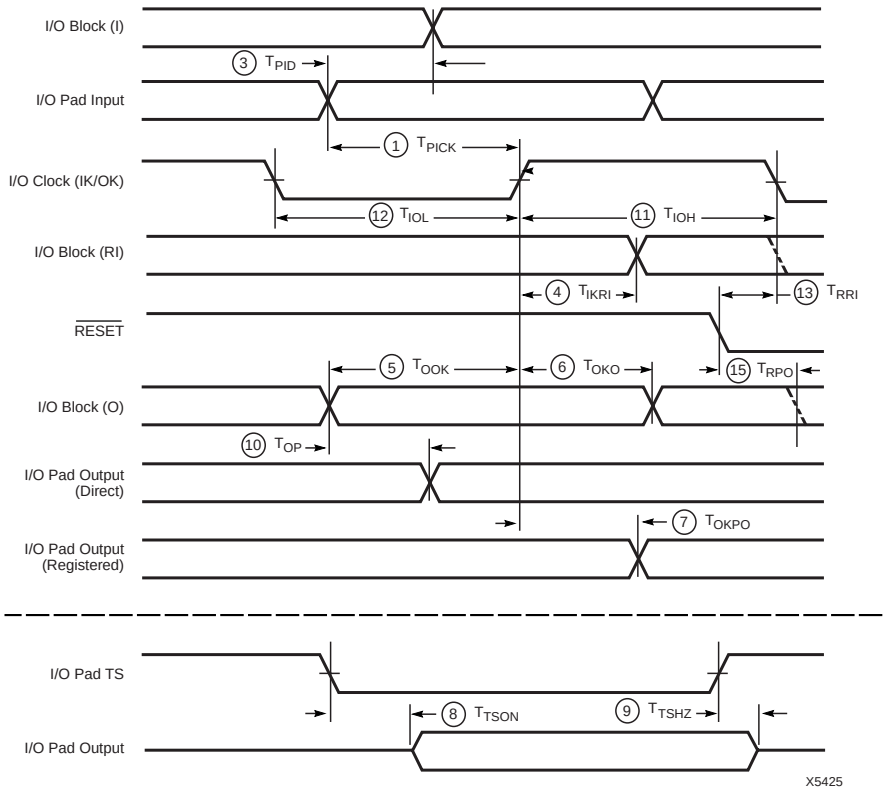
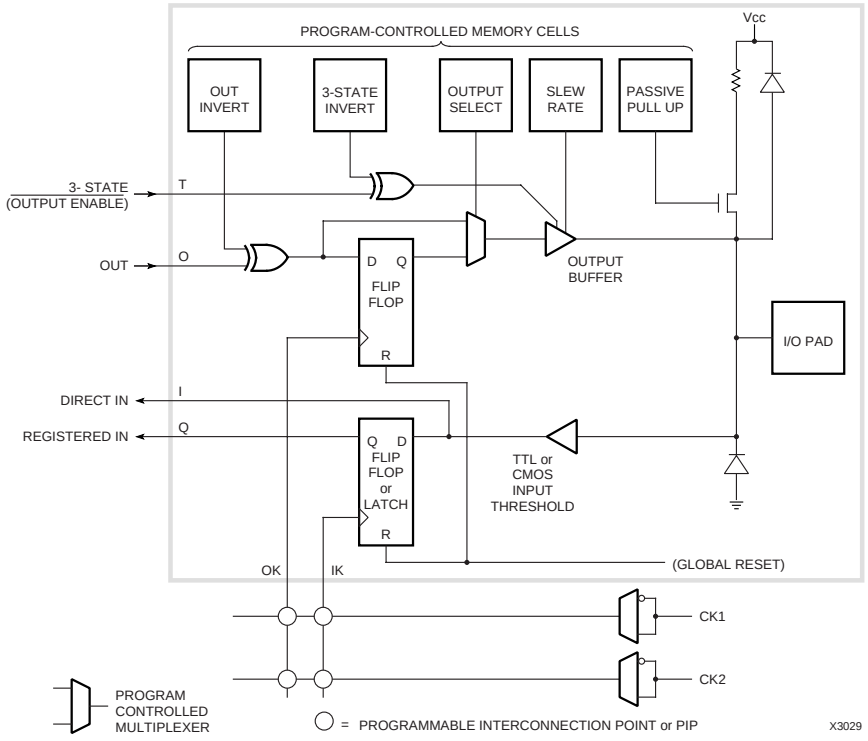
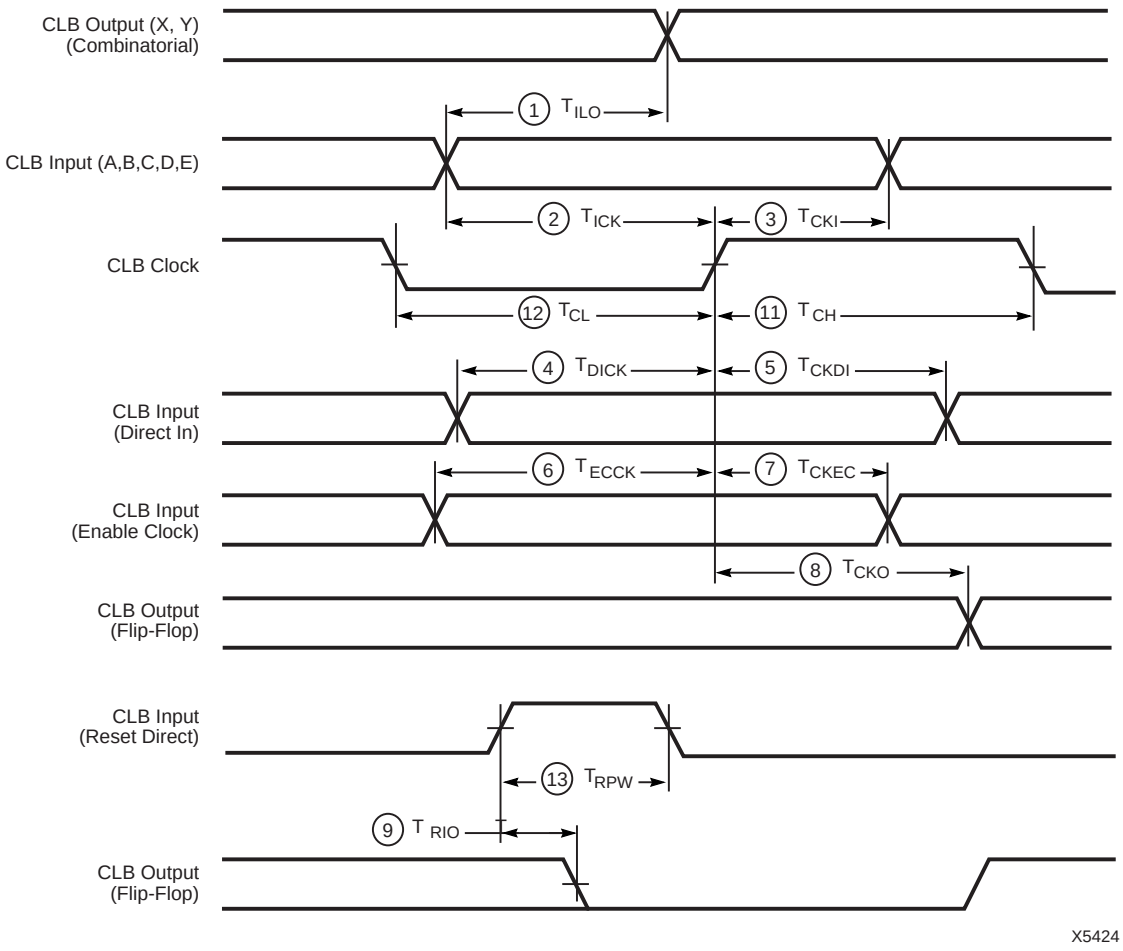
XC3100A IOB Switching Characteristics Guidelines (continued)





XC3100L CLB Switching Characteristics Guidelines (continued)



XC3000 Series 175-Pin Ceramic and Plastic PGA Pinouts

XC3000A, XC3000L, XC3100A, and XC3100L families have identical pinouts

PGA Pin Number	XC3090A, XC3195A
B2	$\overline{\text{PWRDN}}$
D4	TCLKIN-I/O
B3	I/O
C4	I/O
B4	I/O
A4	I/O
D5	I/O
C5	I/O
B5	I/O
A5	I/O
C6	I/O
D6	I/O
B6	I/O
A6	I/O
B7	I/O
C7	I/O
D7	I/O
A7	I/O
A8	I/O
B8	I/O
C8	I/O
D8	GND
D9	VCC
C9	I/O
B9	I/O
A9	I/O
A10	I/O
D10	I/O
C10	I/O
B10	I/O
A11	I/O
B11	I/O
D11	I/O
C11	I/O
A12	I/O
B12	I/O
C12	I/O
D12	I/O
A13	I/O
B13	I/O
C13	I/O
A14	I/O

PGA Pin Number	XC3090A, XC3195A
D13	I/O
B14	M1-$\overline{\text{RDATA}}$
C14	GND
B15	M0-RTRIG
D14	VCC
C15	M2-I/O
E14	HDC-I/O
B16	I/O
D15	I/O
C16	I/O
D16	$\overline{\text{LDC}}$-I/O
F14	I/O
E15	I/O
E16	I/O
F15	I/O
F16	I/O
G14	I/O
G15	I/O
G16	I/O
H16	I/O
H15	$\overline{\text{INIT}}$-I/O
H14	VCC
J14	GND
J15	I/O
J16	I/O
K16	I/O
K15	I/O
K14	I/O
L16	I/O
L15	I/O
M16	I/O
M15	I/O
L14	I/O
N16	I/O
P16	I/O
N15	I/O
R16	I/O
M14	I/O
P15	XTL2(IN)-I/O
N14	GND
R15	$\overline{\text{RESET}}$
P14	VCC

PGA Pin Number	XC3090A, XC3195A
R14	DONE-$\overline{\text{PG}}$
N13	D7-I/O
T14	XTL1(OUT)-BCLKIN-I/O
P13	I/O
R13	I/O
T13	I/O
N12	I/O
P12	D6-I/O
R12	I/O
T12	I/O
P11	I/O
N11	I/O
R11	I/O
T11	D5-I/O
R10	$\overline{\text{CS0}}$-I/O
P10	I/O
N10	I/O
T10	I/O
T9	I/O
R9	D4-I/O
P9	I/O
N9	VCC
N8	GND
P8	D3-I/O
R8	$\overline{\text{CS1}}$-I/O
T8	I/O
T7	I/O
N7	I/O
P7	I/O
R7	D2-I/O
T6	I/O
R6	I/O
N6	I/O
P6	I/O
T5	I/O
R5	D1-I/O
P5	RDY/$\overline{\text{BUSY}}$-$\overline{\text{RCLK}}$-I/O
N5	I/O
T4	I/O
R4	I/O
P4	I/O
R3	D0-DIN-I/O

PGA Pin Number	XC3090A, XC3195A
N4	DOUT-I/O
R2	CCLK
P3	VCC
N3	GND
P2	A0-$\overline{\text{WS}}$-I/O
M3	A1-CS2-I/O
R1	I/O
N2	I/O
P1	A2-I/O
N1	A3-I/O
L3	I/O
M2	I/O
M1	A15-I/O
L2	A4-I/O
L1	I/O
K3	I/O
K2	A14-I/O
K1	A5-I/O
J1	I/O
J2	I/O
J3	GND
H3	VCC
H2	A13-I/O
H1	A6-I/O
G1	I/O
G2	I/O
G3	I/O
F1	I/O
F2	A12-I/O
E1	A7-I/O
E2	I/O
F3	I/O
D1	A11-I/O
C1	A8-I/O
D2	I/O
B1	I/O
E3	A10-I/O
C2	A9-I/O
D3	VCC
C3	GND

Unprogrammed IOBs have a default pull-up. This prevents an undefined pad level for unbonded or unused IOBs. Programmed outputs are default slew-rate limited.

Pins A2, A3, A15, A16, T1, T2, T3, T15 and T16 are not connected. Pin A1 does not exist.

XC3000 Series 208-Pin PQFP Pinouts

XC3000A, and XC3000L families have identical pinouts

Pin Number	XC3090A
1	–
2	GND
3	$\overline{\text{PWRDWN}}$
4	TCLKIN-I/O
5	I/O
6	I/O
7	I/O
8	I/O
9	I/O
10	I/O
11	I/O
12	I/O
13	I/O
14	I/O
15	–
16	I/O
17	I/O
18	I/O
19	I/O
20	I/O
21	I/O
22	I/O
23	I/O
24	I/O
25	GND
26	VCC
27	I/O
28	I/O
29	I/O
30	I/O
31	I/O
32	I/O
33	I/O
34	I/O
35	I/O
36	I/O
37	–
38	I/O
39	I/O
40	I/O
41	I/O
42	I/O
43	I/O
44	I/O
45	I/O
46	I/O
47	I/O
48	M1-$\overline{\text{RDATA}}$
49	GND
50	M0-RTRIG
51	–
52	–

Pin Number	XC3090A
53	–
54	–
55	VCC
56	M2-I/O
57	HDC-I/O
58	I/O
59	I/O
60	I/O
61	$\overline{\text{LDC}}$-I/O
62	I/O
63	I/O
64	–
65	–
66	–
67	–
68	I/O
69	I/O
70	I/O
71	I/O
72	–
73	–
74	I/O
75	I/O
76	I/O
77	$\overline{\text{INIT}}$-I/O
78	VCC
79	GND
80	I/O
81	I/O
82	I/O
83	–
84	–
85	I/O
86	I/O
87	I/O
88	I/O
89	I/O
90	–
91	–
92	–
93	I/O
94	I/O
95	I/O
96	I/O
97	I/O
98	I/O
99	I/O
100	XTL2-I/O
101	GND
102	$\overline{\text{RESET}}$
103	–
104	–

Pin Number	XC3090A
105	–
106	VCC
107	D/$\overline{\text{P}}$
108	–
109	D7-I/O
110	XTL1-BCLKIN-I/O
111	I/O
112	I/O
113	I/O
114	I/O
115	D6-I/O
116	I/O
117	I/O
118	I/O
119	–
120	I/O
121	I/O
122	D5-I/O
123	$\overline{\text{CS0}}$-I/O
124	I/O
125	I/O
126	I/O
127	I/O
128	D4-I/O
129	I/O
130	VCC
131	GND
132	D3-I/O
133	$\overline{\text{CS1}}$-I/O
134	I/O
135	I/O
136	I/O
137	I/O
138	D2-I/O
139	I/O
140	I/O
141	I/O
142	–
143	I/O
144	I/O
145	D1-I/O
146	RDY/$\overline{\text{BUSY}}$-$\overline{\text{RCLK}}$-I/O
147	I/O
148	I/O
149	I/O
150	I/O
151	DIN-D0-I/O
152	DOUT-I/O
153	CCLK
154	VCC
155	–
156	–

Pin Number	XC3090A
157	–
158	–
159	–
160	GND
161	$\overline{\text{WS}}$-A0-I/O
162	CS2-A1-I/O
163	I/O
164	I/O
165	A2-I/O
166	A3-I/O
167	I/O
168	I/O
169	–
170	–
171	–
172	A15-I/O
173	A4-I/O
174	I/O
175	I/O
176	–
177	–
178	A14-I/O
179	A5-I/O
180	I/O
181	I/O
182	GND
183	VCC
184	A13-I/O
185	A6-I/O
186	I/O
187	I/O
188	–
189	–
190	I/O
191	I/O
192	A12-I/O
193	A7-I/O
194	–
195	–
196	–
197	I/O
198	I/O
199	A11-I/O
200	A8-I/O
201	I/O
202	I/O
203	A10-I/O
204	A9-I/O
205	VCC
206	–
207	–
208	–

Unprogrammed IOBs have a default pull-up. This prevents an undefined pad level for unbonded or unused IOBs. Programmed outputs are default slew-rate limited.

* In PQ208, XC3090A and XC3195A have different pinouts.

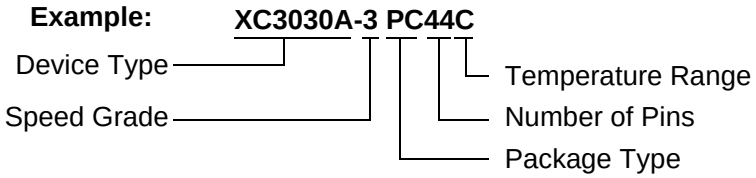
Pins		44	64	68	84		100			132		144	160	175		176	208
Type		Plast. PLCC	Plast. VQFP	Plast. PLCC	Plast. PLCC	Cer. PGA	Plast. PQFP	Plast. TQFP	Plast. VQFP	Plast. PGA	Cer. PGA	Plast. TQFP	Plast. PQFP	Plast. PGA	Cer. PGA	Plast. TQFP	Plast. PQFP
Code		PC44	VQ64	PC68	PC84	PG84	PQ100	TQ100	VQ100	PP132	PG132	TQ144	PQ160	PP175	PG175	TQ176	PQ208
XC3142L					C				C			C					
					C				C			C					
XC3190L					C							C				C	
					C							C				C	

Notes: C = Commercial, T_J= 0° to +85°C I = Industrial, T_J = -40° to +100°C

Number of Available I/O Pins

		Number of Package Pins										
	Max I/O	44	64	68	84	100	132	144	160	175	176	208
XC3020A/XC3120A	64			58	64	64						
XC3030A/XC3130A	80	34	54	58	74	80						
XC3042A/3142A	96				74	82	96	96				
XC2064A/XC3164A	120				70		110	120	120			
XC3090A/XC3190A	144				70			122	138	144	144	144
XC3195A	176				70				138	144		176

Ordering Information



Revision History

Date	Revision
11/98	Revised version number to 3.1, removed XC3100A-5 obsolete packages.