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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	320
Number of Logic Elements/Cells	-
Total RAM Bits	64160
Number of I/O	138
Number of Gates	6000
Voltage - Supply	4.25V ~ 5.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	160-BQFP
Supplier Device Package	160-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc3190a-3pq160c

Improvements in the XC3000A and XC3000L Families

The XC3000A and XC3000L families offer the following enhancements over the popular XC3000 family:

The XC3000A and XC3000L families have additional interconnect resources to drive the I-inputs of TBUFs driving horizontal Longlines. The CLB Clock Enable input can be driven from a second vertical Longline. These two additions result in more efficient and faster designs when horizontal Longlines are used for data bussing.

During configuration, the XC3000A and XC3000L devices check the bit-stream format for stop bits in the appropriate positions. Any error terminates the configuration and pulls INIT Low.

When the configuration process is finished and the device starts up in user mode, the first activation of the outputs is automatically slew-rate limited. This feature, called Soft Startup, avoids the potential ground bounce when all out-puts are turned on simultaneously. After start-up, the slew rate of the individual outputs is, as in the XC3000 family, determined by the individual configuration option.

Improvements in the XC3100A and XC3100L Families

Based on a more advanced CMOS process, the XC3100A and XC3100L families are architecturally-identical, performance-optimized relatives of the XC3000A and XC3000L families. While all families are footprint compatible, the XC3100A family extends achievable system performance beyond 85 MHz.

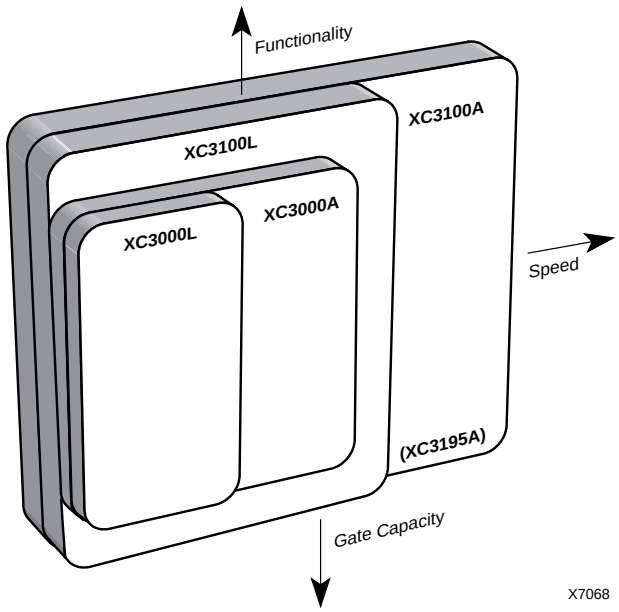

Figure 1: XC3000 FPGA Families

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Detailed Functional Description

The perimeter of configurable Input/Output Blocks (IOBs) provides a programmable interface between the internal logic array and the device package pins. The array of Configurable Logic Blocks (CLBs) performs user-specified logic functions. The interconnect resources are programmed to form networks, carrying logic signals among blocks, analogous to printed circuit board traces connecting MSI/SSI packages.

The block logic functions are implemented by programmed look-up tables. Functional options are implemented by program-controlled multiplexers. Interconnecting networks between blocks are implemented with metal segments joined by program-controlled pass transistors.

These FPGA functions are established by a configuration program which is loaded into an internal, distributed array of configuration memory cells. The configuration program is loaded into the device at power-up and may be reloaded on command. The FPGA includes logic and control signals to implement automatic or passive configuration. Program data may be either bit serial or byte parallel. The development system generates the configuration program bitstream used to configure the device. The memory loading process is independent of the user logic functions.

Configuration Memory

The static memory cell used for the configuration memory in the Field Programmable Gate Array has been designed specifically for high reliability and noise immunity. Integrity of the device configuration memory based on this design is assured even under adverse conditions. As shown in Figure 3, the basic memory cell consists of two CMOS inverters plus a pass transistor used for writing and reading cell data. The cell is only written during configuration and only read during readback. During normal operation, the cell provides continuous control and the pass transistor is off and does not affect cell stability. This is quite different from the operation of conventional memory devices, in which the cells are frequently read and rewritten.

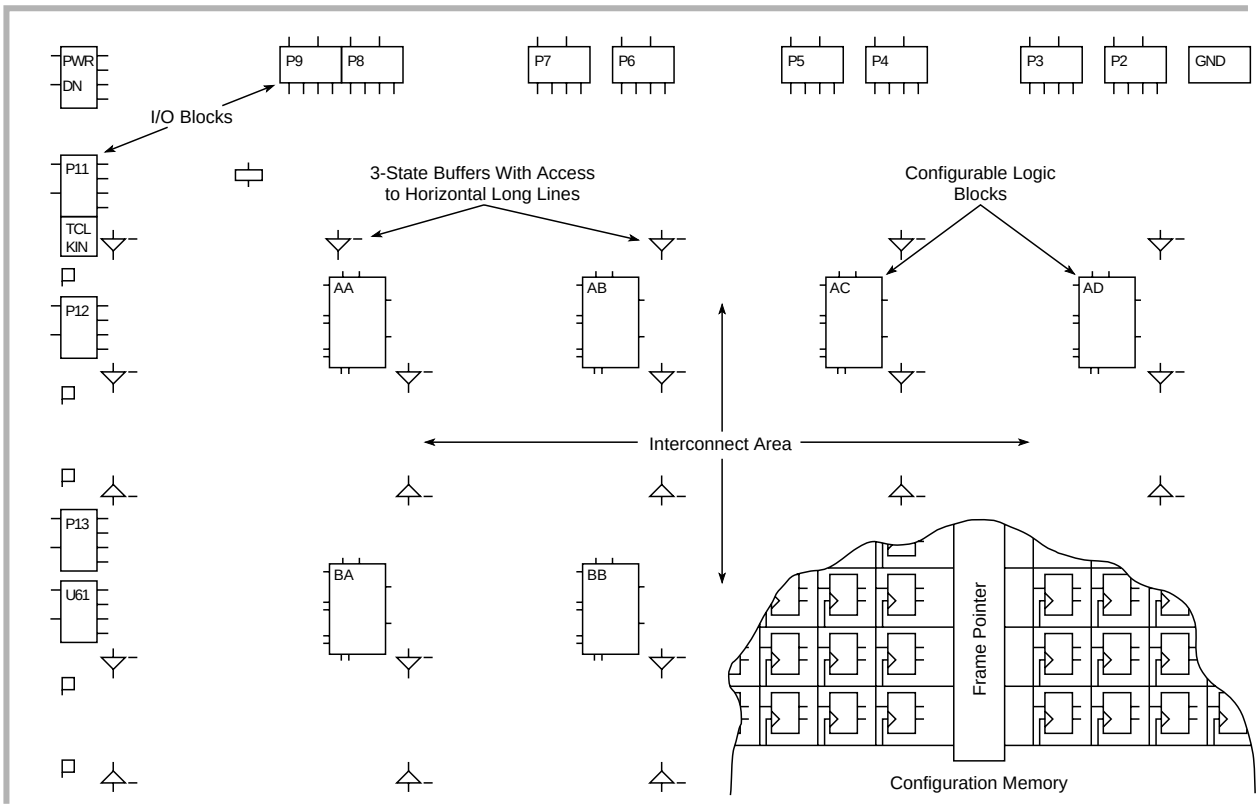


Figure 2: Field Programmable Gate Array Structure.
It consists of a perimeter of programmable I/O blocks, a core of configurable logic blocks and their interconnect resources. These are all controlled by the distributed array of configuration program memory cells.

The input-buffer portion of each IOB provides threshold detection to translate external signals applied to the package pin to internal logic levels. The global input-buffer threshold of the IOBs can be programmed to be compatible with either TTL or CMOS levels. The buffered input signal drives the data input of a storage element, which may be configured as either a flip-flop or a latch. The clocking polarity (rising/falling edge-triggered flip-flop, High/Low transparent latch) is programmable for each of the two clock lines on each of the four die edges. Note that a clock line driving a *rising* edge-triggered flip-flop makes any latch driven by the same line on the same edge Low-level transparent and vice versa (*falling* edge, *High* transparent). All Xilinx primitives in the supported schematic-entry packages, however, are positive edge-triggered flip-flops or High transparent latches. When one clock line must drive flip-flops as well as latches, it is necessary to compensate for the difference in clocking polarities with an additional inverter either in the flip-flop clock input or the latch-enable input. I/O storage elements are reset during configuration or by the active-Low chip $\overline{\text{RESET}}$ input. Both direct input (from IOB pin I) and registered input (from IOB pin Q) signals are available for interconnect.

For reliable operation, inputs should have transition times of less than 100 ns and should not be left floating. Floating CMOS input-pin circuits might be at threshold and produce oscillations. This can produce additional power dissipation and system noise. A typical hysteresis of about 300 mV reduces sensitivity to input noise. Each user IOB includes a programmable high-impedance pull-up resistor, which may be selected by the program to provide a constant High for otherwise undriven package pins. Although the Field Programmable Gate Array provides circuitry to provide input protection for electrostatic discharge, normal CMOS handling precautions should be observed.

Flip-flop loop delays for the IOB and logic-block flip-flops are short, providing good performance under asynchronous clock and data conditions. Short loop delays minimize the probability of a metastable condition that can result from assertion of the clock during data transitions. Because of the short-loop-delay characteristic in the Field Programmable Gate Array, the IOB flip-flops can be used to synchronize external signals applied to the device. Once synchronized in the IOB, the signals can be used internally without further consideration of their clock relative timing, except as it applies to the internal logic and routing-path delays.

IOB output buffers provide CMOS-compatible 4-mA source-or-sink drive for high fan-out CMOS or TTL- compatible signal levels (8 mA in the XC3100A family). The network driving IOB pin O becomes the registered or direct data source for the output buffer. The 3-state control signal (IOB) pin T can control output activity. An open-drain output may be obtained by using the same signal for driving the output and 3-state signal nets so that the buffer output is enabled only for a Low.

Configuration program bits for each IOB control features such as optional output register, logic signal inversion, and 3-state and slew-rate control of the output.

The program-controlled memory cells of Figure 4 control the following options.

- Logic inversion of the output is controlled by one configuration program bit per IOB.
- Logic 3-state control of each IOB output buffer is determined by the states of configuration program bits that turn the buffer on, or off, or select the output buffer 3-state control interconnection (IOB pin T). When this IOB output control signal is High, a logic one, the buffer is disabled and the package pin is high impedance. When this IOB output control signal is Low, a logic zero, the buffer is enabled and the package pin is active. Inversion of the buffer 3-state control-logic sense (output enable) is controlled by an additional configuration program bit.
- Direct or registered output is selectable for each IOB. The register uses a positive-edge, clocked flip-flop. The clock source may be supplied (IOB pin OK) by either of two metal lines available along each die edge. Each of these lines is driven by an invertible buffer.
- Increased output transition speed can be selected to improve critical timing. Slower transitions reduce capacitive-load peak currents of non-critical outputs and minimize system noise.
- An internal high-impedance pull-up resistor (active by default) prevents unconnected inputs from floating.

Unlike the original XC3000 series, the XC3000A, XC3000L, XC3100A, and XC3100L families include the Soft Startup feature. When the configuration process is finished and the device starts up in user mode, the first activation of the outputs is automatically slew-rate limited. This feature avoids potential ground bounce when all outputs are turned on simultaneously. After start-up, the slew rate of the individual outputs is determined by the individual configuration option.

Summary of I/O Options

- Inputs
  - Direct
  - Flip-flop/latch
  - CMOS/TTL threshold (chip inputs)
  - Pull-up resistor/open circuit
- Outputs
  - Direct/registered
  - Inverted/not
  - 3-state/on/off
  - Full speed/slew limited
  - 3-state/output enable (inverse)

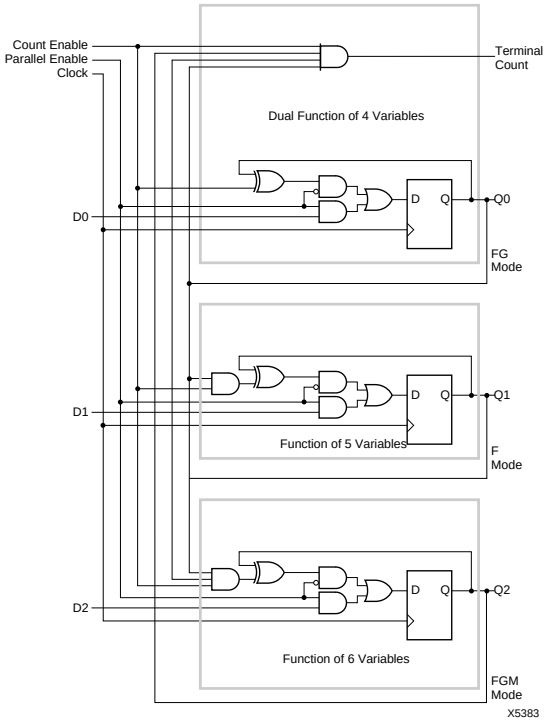


Figure 7: Counter.
The modulo-8 binary counter with parallel enable and clock enable uses one combinatorial logic block of each option.

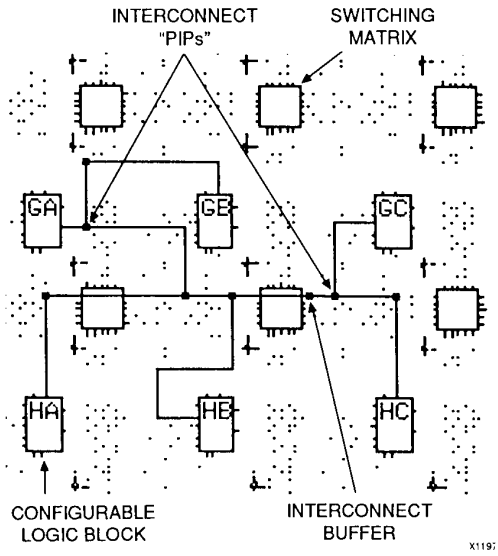


Figure 8: A Design Editor view of routing resources used to form a typical interconnection network from CLB GA.

General Purpose Interconnect

General purpose interconnect, as shown in Figure 10, consists of a grid of five horizontal and five vertical metal segments located between the rows and columns of logic and IOBs. Each segment is the height or width of a logic block. Switching matrices join the ends of these segments and allow programmed interconnections between the metal grid segments of adjoining rows and columns. The switches of an unprogrammed device are all non-conducting. The connections through the switch matrix may be established by the automatic routing or by selecting the desired pairs of matrix pins to be connected or disconnected. The legitimate switching matrix combinations for each pin are indicated in Figure 11.

Special buffers within the general interconnect areas provide periodic signal isolation and restoration for improved performance of lengthy nets. The interconnect buffers are available to propagate signals in either direction on a given general interconnect segment. These bidirectional (bidi) buffers are found adjacent to the switching matrices, above and to the right. The other PIPs adjacent to the matrices are accessed to or from Longlines. The development system automatically defines the buffer direction based on the location of the interconnection network source. The delay calculator of the development system automatically calculates and displays the block, interconnect and buffer delays for any paths selected. Generation of the simulation netlist with a worst-case delay model is provided.

Direct Interconnect

Direct interconnect, shown in Figure 12, provides the most efficient implementation of networks between adjacent CLBs or I/O Blocks. Signals routed from block to block using the direct interconnect exhibit minimum interconnect propagation and use no general interconnect resources. For each CLB, the X output may be connected directly to the B input of the CLB immediately to its right and to the C input of the CLB to its left. The Y output can use direct interconnect to drive the D input of the block immediately above and the A input of the block below. Direct interconnect should be used to maximize the speed of high-performance portions of logic. Where logic blocks are adjacent to IOBs, direct connect is provided alternately to the IOB inputs (I) and outputs (O) on all four edges of the die. The right edge provides additional direct connects from CLB outputs to adjacent IOBs. Direct interconnections of IOBs with CLBs are shown in Figure 13.

Longlines

The Longlines bypass the switch matrices and are intended primarily for signals that must travel a long distance, or must have minimum skew among multiple destinations. Longlines, shown in Figure 14, run vertically and horizontally the height or width of the interconnect area. Each interconnection column has three vertical Longlines, and each interconnection row has two horizontal Longlines. Two additional Longlines are located adjacent to the outer sets of switching matrices. In devices larger than the XC3020A and XC3120A FPGAs, two vertical Longlines in each column are connectable half-length lines. On the XC3020A and XC3120A FPGAs, only the outer Longlines are connectable half-length lines.

Longlines can be driven by a logic block or IOB output on a column-by-column basis. This capability provides a common low skew control or clock line within each column of logic blocks. Interconnections of these Longlines are shown in Figure 15. Isolation buffers are provided at each input to a Longline and are enabled automatically by the development system when a connection is made.

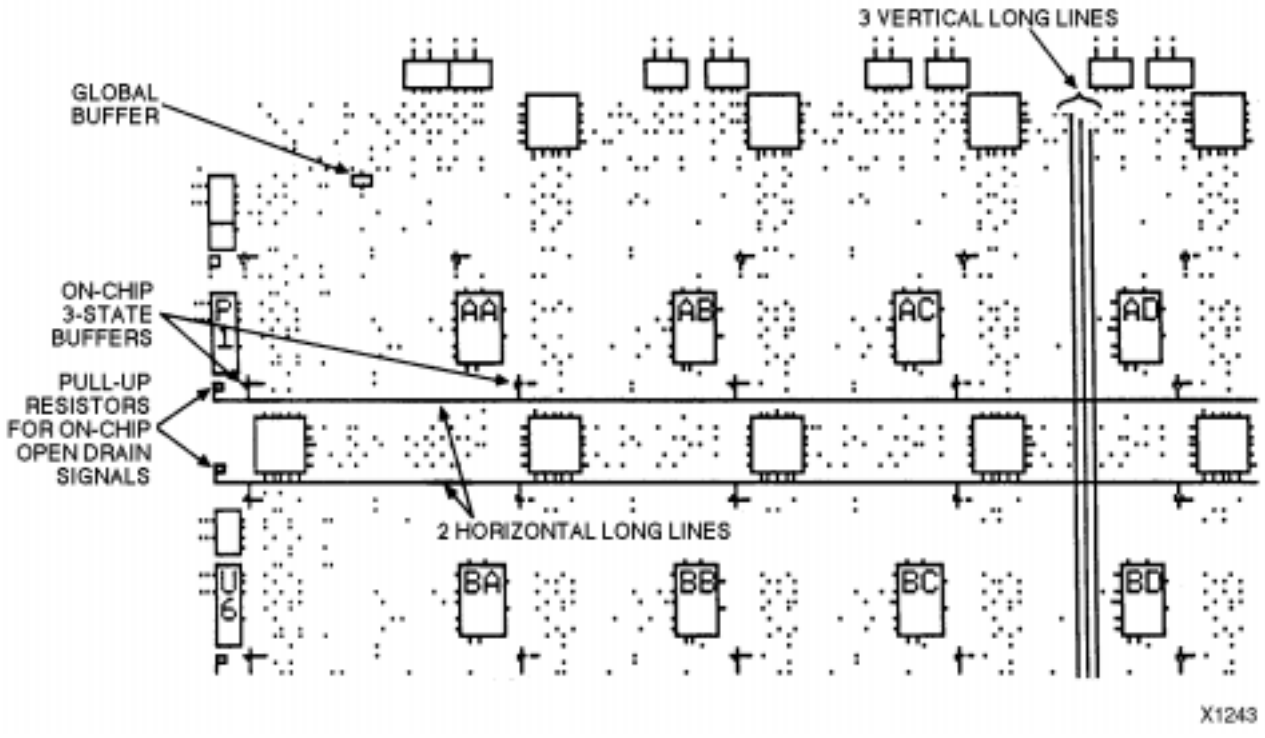


Figure 14: Horizontal and Vertical Longlines. These Longlines provide high fan-out, low-skew signal distribution in each row and column. The global buffer in the upper left die corner drives a common line throughout the FPGA.

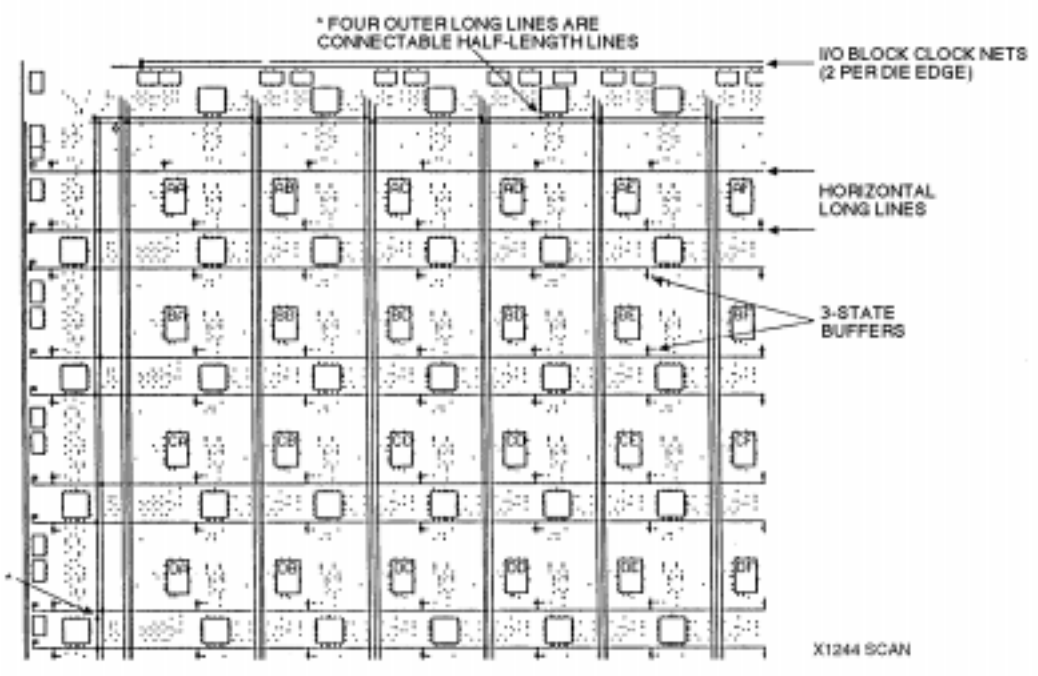


Figure 15: Programmable Interconnection of Longlines. This is provided at the edges of the routing area. Three-state buffers allow the use of horizontal Longlines to form on-chip wired AND and multiplexed buses. The left two non-clock vertical Longlines per column (except XC3020A) and the outer perimeter Longlines may be programmed as connectable half-length lines.

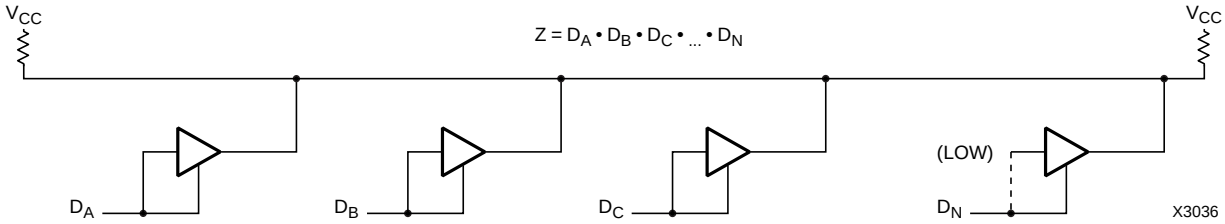


Figure 16: 3-State Buffers Implement a Wired-AND Function. When all the buffer 3-state lines are High, (high impedance), the pull-up resistor(s) provide the High output. The buffer inputs are driven by the control signals or a Low.

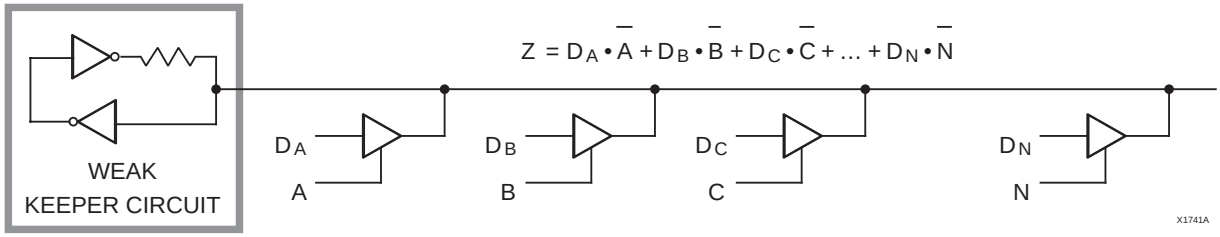


Figure 17: 3-State Buffers Implement a Multiplexer. The selection is accomplished by the buffer 3-state signal.

A buffer in the upper left corner of the FPGA chip drives a global net which is available to all K inputs of logic blocks. Using the global buffer for a clock signal provides a skew-free, high fan-out, synchronized clock for use at any or all of the IOBs and CLBs. Configuration bits for the K input to each logic block can select this global line or another routing resource as the clock source for its flip-flops. This net may also be programmed to drive the die edge clock lines for IOB use. An enhanced speed, CMOS threshold, direct access to this buffer is available at the second pad from the top of the left die edge.

A buffer in the lower right corner of the array drives a horizontal Longline that can drive programmed connections to a vertical Longline in each interconnection column. This alternate buffer also has low skew and high fan-out. The network formed by this alternate buffer's Longlines can be selected to drive the K inputs of the CLBs. CMOS threshold, high speed access to this buffer is available from the third pad from the bottom of the right die edge.

Internal Busses

A pair of 3-state buffers, located adjacent to each CLB, permits logic to drive the horizontal Longlines. Logic operation of the 3-state buffer controls allows them to implement wide multiplexing functions. Any 3-state buffer input can be selected as drive for the horizontal long-line bus by applying a Low logic level on its 3-state control line. See Figure 16. The user is required to avoid contention which can result from multiple drivers with opposing logic levels. Control of the 3-state input by the same signal that drives the buffer input, creates an open-drain wired-AND function. A logic High on both buffer inputs creates a high impedance, which represents no contention. A logic Low enables the buffer to drive the Longline Low. See Figure 17. Pull-up resistors are available at each end of the Longline to provide a High output when all connected buffers are non-conducting. This forms fast, wide gating functions. When data drives the inputs, and separate signals drive the 3-state control lines, these buffers form multiplexers (3-state busses). In this case, care must be used to prevent contention through multiple active buffers of conflicting levels on a common line. Each horizontal Longline is also driven by a weak keeper circuit that prevents undefined floating levels by maintaining the previous logic level when the line is not driven by an active buffer or a pull-up resistor. Figure 18 shows 3-state buffers, Longlines and pull-up resistors.

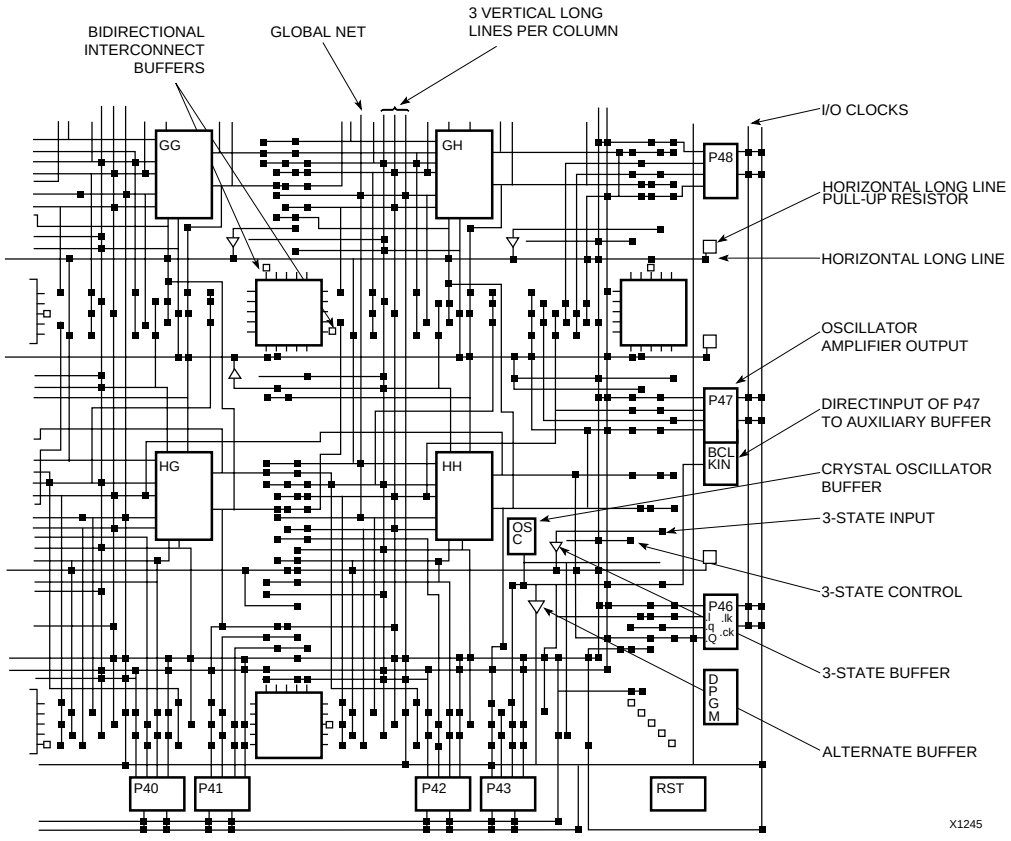
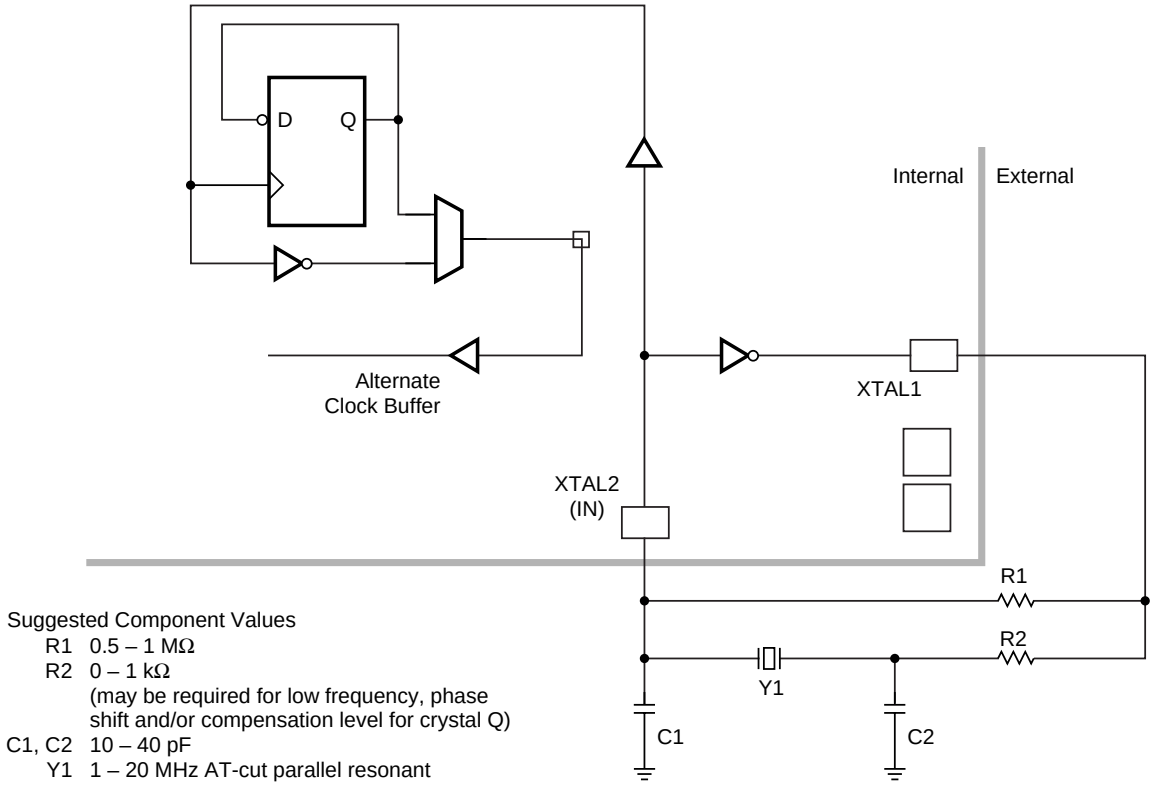


Figure 18: Design Editor.
An extra large view of possible interconnections in the lower right corner of the XC3020A.

Crystal Oscillator

Figure 18 also shows the location of an internal high speed inverting amplifier that may be used to implement an on-chip crystal oscillator. It is associated with the auxiliary buffer in the lower right corner of the die. When the oscillator is configured and connected as a signal source, two special user IOBs are also configured to connect the oscillator amplifier with external crystal oscillator components as shown in Figure 19. A divide by two option is available to assure symmetry. The oscillator circuit becomes active early in the configuration process to allow the oscillator to stabilize. Actual internal connection is delayed until completion of configuration. In Figure 19 the feedback resistor R1, between the output and input, biases the amplifier at threshold. The inversion of the amplifier, together with the R-C networks and an AT-cut series resonant crystal, produce the 360-degree phase shift of the Pierce oscillator. A series resistor R2 may be included to add to the amplifier output impedance when needed for phase-shift control, crystal resistance matching, or to limit the amplifier input swing to control clipping at large amplitudes. Excess feedback voltage may be corrected by the ratio of C2/C1. The amplifier is designed to be used from 1 MHz to about one-half the specified CLB toggle frequency. Use at frequencies below 1 MHz may require individual characterization with respect to a series resistance. Crystal oscillators above 20 MHz generally require a crystal which operates in a third overtone mode, where the fundamental frequency must be suppressed by an inductor across C2, turning this parallel resonant circuit to double the fundamental crystal frequency, i.e., 2/3 of the desired third harmonic frequency network. When the oscillator inverter is not used, these IOBs and their package pins are available for general user I/O.



	44 PIN	68 PIN	84 PIN		100 PIN		132 PIN	160 PIN	164 PIN	175 PIN	176 PIN	208 PIN
	PLCC	PLCC	PLCC	PGA	CQFP	PQFP	PGA	PQFP	CQFP	PGA	TQFP	PQFP
XTAL 1 (OUT)	30	47	57	J11	67	82	P13	82	105	T14	91	110
XTAL 2 (IN)	26	43	53	L11	61	76	M13	76	99	P15	85	100

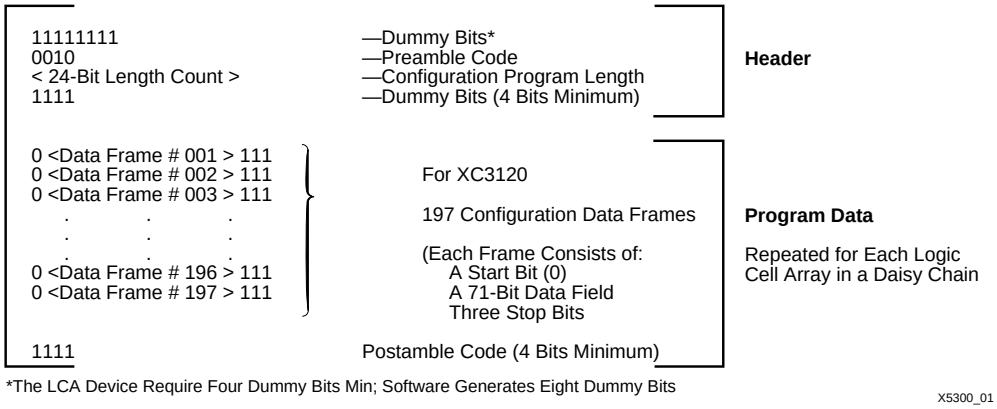
X7064

Figure 19: Crystal Oscillator Inverter. When activated, and by selecting an output network for its buffer, the crystal oscillator inverter uses two unconfigured package pins and external components to implement an oscillator. An optional divide-by-two mode is available to assure symmetry.

A re-program is initiated.when a configured XC3000 series device senses a High-to-Low transition and subsequent >6 µs Low level on the DONE/PROG package pin, or, if this pin is externally held permanently Low, a High-to-Low transition and subsequent >6 µs Low time on the RESET package pin.

The device returns to the Clear state where the configuration memory is cleared and mode lines re-sampled, as for an aborted configuration. The complete configuration program is cleared and loaded during each configuration program cycle.

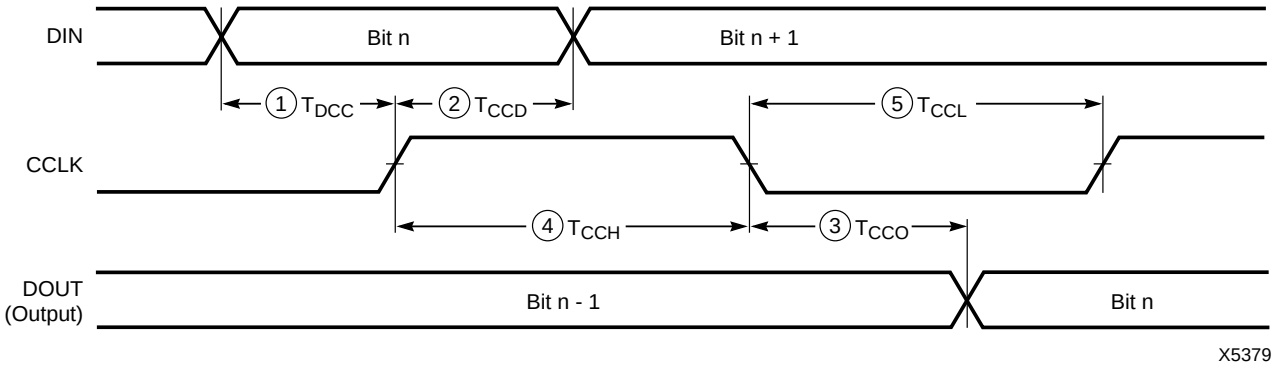
Length count control allows a system of multiple Field Programmable Gate Arrays, of assorted sizes, to begin operation in a synchronized fashion. The configuration program generated by the development system begins with a preamble of 111111110010 followed by a 24-bit length count representing the total number of configuration clocks needed to complete loading of the configuration program(s). The data framing is shown in Figure 21. All FPGAs connected in series read and shift preamble and length count in on positive and out on negative configuration clock edges. A device which has received the preamble and length count then presents a High Data Out until it has intercepted the appropriate number of data frames. When the configuration program memory of an FPGA is full and the length count does not yet compare, the device shifts any additional data through, as it did for preamble and length count. When the FPGA configuration memory is full and the length count compares, the device will execute



Device	XC3020A XC3020L XC3120A	XC3030A XC3030L XC3130A	XC3042A XC3042L XC3142A XC3142L	XC3064A XC3064L XC3164A	XC3090A XC3090L XC3190A XC3190L	XC3195A
Gates	1,000 to 1,500	1,500 to 2,000	2,000 to 3,000	3,500 to 4,500	5,000 to 6,000	6,500 to 7,500
CLBs	64	100	144	224	320	484
Row x Col	(8 x 8)	(10 x 10)	(12 x 12)	(16 x 14)	(20 x 16)	(22 x 22)
IOBs	64	80	96	120	144	176
Flip-flops	256	360	480	688	928	1,320
Horizontal Longlines	16	20	24	32	40	44
TBUFs/Horizontal LL	9	11	13	15	17	23
Bits per Frame (including1 start and 3 stop bits)	75	92	108	140	172	188
Frames	197	241	285	329	373	505
Program Data = Bits x Frames + 4 bits (excludes header)	14,779	22,176	30,784	46,064	64,160	94,944
PROM size (bits) = Program Data + 40-bit Header	14,819	22,216	30,824	46,104	64,200	94,984

Figure 21: Internal Configuration Data Structure for an FPGA. This shows the preamble, length count and data frames generated by the Development System.

The Length Count produced by the program = [(40-bit preamble + sum of program data + 1 per daisy chain device) rounded up to multiple of 8] – ($2 \le K \le 4$) where K is a function of DONE and RESET timing selected. An additional 8 is added if roundup increment is less than K. K additional clocks are needed to complete start-up after length count is reached.

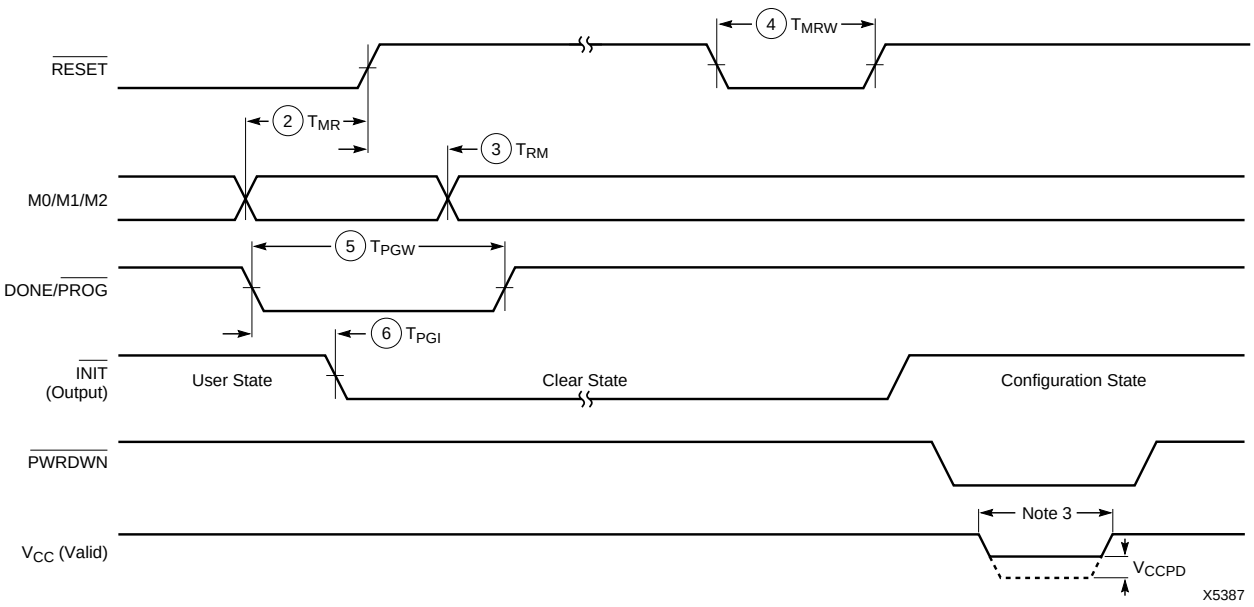


	Description	Symbol		Min	Max	Units
CCLK	To DOUT	3	T_{CCO}		100	ns
	DIN setup	1	T_{DCC}	60		ns
	DIN hold	2	T_{CCD}	0		ns
	High time	4	T_{CCH}	0.05		µs
	Low time (Note 1)	5	T_{CCL}	0.05	5.0	µs
	Frequency		F_{CC}		10	MHz

Notes: 1. The max limit of CCLK Low time is caused by dynamic circuitry inside the FPGA.
2. Configuration must be delayed until the INIT of all FPGAs is High.
3. At power-up, V_{CC} must rise from 2.0 V to V_{CC} min in less than 25 ms. If this is not possible, configuration can be delayed by holding RESET Low until VCC has reached 4.0 V (2.5 V for the XC3000L). A very long V_{CC} rise time of >100 ms, or a non-monotonically rising V_{CC} may require a >6-µs High level on RESET, followed by a >6-µs Low level on RESET and D/P after V_{CC} has reached 4.0 V (2.5 V for the XC3000L).

Figure 30: Slave Serial Mode Programming Switching Characteristics

General XC3000 Series Switching Characteristics



	Description		Symbol	Min	Max	Units
RESET (2)	M0, M1, M2 setup time required	2	T_{MR}	1		µs
	M0, M1, M2 hold time required	3	T_{RM}	4.5		µs
	RESET Width (Low) req. for Abort	4	T_{MRW}	6		µs
DONE/PROG	Width (Low) required for Re-config.	5	T_{PGW}	6		µs
	INIT response after D/P is pulled Low	6	T_{PGI}		7	µs
PWRDWN (3)	Power Down V_{CC}		V_{CCPD}	2.3		V

Notes:
1. At power-up, V_{CC} must rise from 2.0 V to V_{CC} min in less than 25 ms. If this is not possible, configuration can be delayed by holding RESET Low until Vcc has reached 4.0 V (2.5 V for XC3000L). A very long Vcc rise time of >100 ms, or a non-monotonically rising V_{CC} may require a >1-µs High level on RESET, followed by a >6-µs Low level on RESET and D/P after Vcc has reached 4.0 V (2.5 V for XC3000L).
2. RESET timing relative to valid mode lines (M0, M1, M2) is relevant when RESET is used to delay configuration. The specified hold time is caused by a shift-register filter slowing down the response to RESET during configuration.
3. PWRDWN transitions must occur while V_{CC} >4.0 V(2.5 V for XC3000L).

Pin Descriptions

Permanently Dedicated Pins

V_{CC}

Two to eight (depending on package type) connections to the positive V supply voltage. All must be connected.

GND

Two to eight (depending on package type) connections to ground. All must be connected.

$\overline{\text{PWRDWN}}$

A Low on this CMOS-compatible input stops all internal activity, but retains configuration. All flip-flops and latches are reset, all outputs are 3-stated, and all inputs are interpreted as High, independent of their actual level. When $\overline{\text{PWDWN}}$ returns High, the FPGA becomes operational with DONE Low for two cycles of the internal 1-MHz clock. Before and during configuration, $\overline{\text{PWRDWN}}$ must be High. If not used, $\overline{\text{PWRDWN}}$ must be tied to V_{CC}.

$\overline{\text{RESET}}$

This is an active Low input which has three functions.

Prior to the start of configuration, a Low input will delay the start of the configuration process. An internal circuit senses the application of power and begins a minimal time-out cycle. When the time-out and $\overline{\text{RESET}}$ are complete, the levels of the M lines are sampled and configuration begins.

If $\overline{\text{RESET}}$ is asserted during a configuration, the FPGA is re-initialized and restarts the configuration at the termination of $\overline{\text{RESET}}$.

If $\overline{\text{RESET}}$ is asserted after configuration is complete, it provides a global asynchronous $\overline{\text{RESET}}$ of all IOB and CLB storage elements of the FPGA.

CCLK

During configuration, Configuration Clock is an output of an FPGA in Master mode or Peripheral mode, but an input in Slave mode. During Readback, CCLK is a clock input for shifting configuration data out of the FPGA.

CCLK drives dynamic circuitry inside the FPGA. The Low time may, therefore, not exceed a few microseconds. When used as an input, CCLK must be “parked High”. An internal pull-up resistor maintains High when the pin is not being driven.

DONE/$\overline{\text{PROG}}$ (D/$\overline{\text{P}}$)

DONE is an open-drain output, configurable with or without an internal pull-up resistor of 2 to 8 k Ω. At the completion of configuration, the FPGA circuitry becomes active in a synchronous order; DONE is programmed to go active High one cycle either before or after the outputs go active.

Once configuration is done, a High-to-Low transition of this pin will cause an initialization of the FPGA and start a reconfiguration.

M0/RTRIG

As Mode 0, this input is sampled on power-on to determine the power-on delay (2^{14} cycles if M0 is High, 2^{16} cycles if M0 is Low). Before the start of configuration, this input is again sampled together with M1, M2 to determine the configuration mode to be used.

A Low-to-High input transition, after configuration is complete, acts as a Read Trigger and initiates a Readback of configuration and storage-element data clocked by CCLK. By selecting the appropriate Readback option when generating the bitstream, this operation may be limited to a single Readback, or be inhibited altogether.

M1/$\overline{\text{RDATA}}$

As Mode 1, this input and M0, M2 are sampled before the start of configuration to establish the configuration mode to be used. If Readback is never used, M1 can be tied directly to ground or V_{CC}. If Readback is ever used, M1 must use a 5-kΩ resistor to ground or V_{CC}, to accommodate the RDATA output.

As an active-Low Read Data, after configuration is complete, this pin is the output of the Readback data.

User I/O Pins That Can Have Special Functions

M2

During configuration, this input has a weak pull-up resistor. Together with M0 and M1, it is sampled before the start of configuration to establish the configuration mode to be used. After configuration, this pin is a user-programmable I/O pin.

HDC

During configuration, this output is held at a High level to indicate that configuration is not yet complete. After configuration, this pin is a user-programmable I/O pin.

$\overline{\text{LDC}}$

During Configuration, this output is held at a Low level to indicate that the configuration is not yet complete. After configuration, this pin is a user-programmable I/O pin. $\overline{\text{LDC}}$ is particularly useful in Master mode as a Low enable for an EPROM, but it must then be programmed as a High after configuration.

$\overline{\text{INIT}}$

This is an active Low open-drain output with a weak pull-up and is held Low during the power stabilization and internal clearing of the configuration memory. It can be used to indicate status to a configuring microprocessor or, as a wired

XC3000A Switching Characteristics

Xilinx maintains test specifications for each product as controlled documents. To insure the use of the most recently released device performance parameters, please request a copy of the current test-specification revision.

XC3000A Operating Conditions

Symbol	Description	Min	Max	Units
V_{CC}	Supply voltage relative to GND Commercial 0°C to +85°C junction	4.75	5.25	V
	Supply voltage relative to GND Industrial -40°C to +100°C junction	4.5	5.5	V
V_{IHT}	High-level input voltage — TTL configuration	2.0	V_{CC}	V
V_{ILT}	Low-level input voltage — TTL configuration	0	0.8	V
V_{IHC}	High-level input voltage — CMOS configuration	70%	100%	V_{CC}
V_{ILC}	Low-level input voltage — CMOS configuration	0	20%	V_{CC}
T_{IN}	Input signal transition time		250	ns

Note: At junction temperatures above those listed as Operating Conditions, all delay parameters increase by 0.3% per °C.

XC3000A DC Characteristics Over Operating Conditions

Symbol	Description		Min	Max	Units
V_{OH}	High-level output voltage (@ I_{OH} = –4.0 mA, V_{CC} min)	Commercial	3.86		V
V_{OL}	Low-level output voltage (@ I_{OL} = 4.0 mA, V_{CC} min)	Commercial		0.40	V
V_{OH}	High-level output voltage (@ I_{OH} = –4.0 mA, V_{CC} min)	Industrial	3.76		V
V_{OL}	Low-level output voltage (@ I_{OL} = 4.0 mA, V_{CC} min)	Industrial		0.40	V
V_{CCPD}	Power-down supply voltage (PWRDWN must be Low)		2.30		V
I_{CCPD}	Power-down supply current ($V_{CC(MAX)}$ @ T_{MAX})				
		3020A		100	µA
		3030A		160	µA
		3042A		240	µA
		3064A		340	µA
		3090A		500	µA
I_{CCO}	Quiescent FPGA supply current in addition to I_{CCPD}				
	Chip thresholds programmed as CMOS levels			500	µA
	Chip thresholds programmed as TTL levels			10	µA
I_{IL}	Input Leakage Current		–10	+10	µA
C_{IN}	Input capacitance, all packages except PGA175 (sample tested)				
	All Pins except XTL1 and XTL2			10	pF
	XTL1 and XTL2			15	pF
	Input capacitance, PGA 175 (sample tested)				
	All Pins except XTL1 and XTL2			16	pF
	XTL1 and XTL2			20	pF
I_{RIN}	Pad pull-up (when selected) @ V_{IN} = 0 V[3]		0.02	0.17	mA
I_{RLL}	Horizontal Longline pull-up (when selected) @ logic Low			3.4	mA

Notes: 1. With no output current loads, no active input or Longline pull-up resistors, all package pins at V_{CC} or GND, and the FPGA device configured with a tie option.
2. Total continuous output sink current may not exceed 100 mA per ground pin. Total continuous output source may not exceed 100 mA per V_{CC} pin. The number of ground pins varies from the XC3020A to the XC3090A.
3. Not tested. Allow an undriven pin to float High. For any other purposes use an external pull-up.

XC3000A Absolute Maximum Ratings

Symbol	Description		Units
V_{CC}	Supply voltage relative to GND	–0.5 to +7.0	V
V_{IN}	Input voltage with respect to GND	–0.5 to V_{CC} +0.5	V
V_{TS}	Voltage applied to 3-state output	–0.5 to V_{CC} +0.5	V
T_{STG}	Storage temperature (ambient)	–65 to +150	°C
T_{SOL}	Maximum soldering temperature (10 s @ 1/16 in.)	+260	°C
T_J	Junction temperature plastic	+125	°C
	Junction temperature ceramic	+150	°C

Note: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

XC3000A Global Buffer Switching Characteristics Guidelines

	Speed Grade	-7	-6	
Description	**Symbol**	**Max**	**Max**	**Units**
Global and Alternate Clock Distribution[1]				
Either: **Normal** IOB input pad through clock buffer to any CLB or IOB clock input	T_{PID}	7.5	7.0	ns
Or: **Fast** (CMOS only) input pad through clock buffer to any CLB or IOB clock input	T_{PIDC}	6.0	5.7	ns
TBUF driving a Horizontal Longline (L.L.)[1]				
I to L.L. while T is Low (buffer active)	T_{IO}	4.5	4.0	ns
T↓ to L.L. active and valid with single pull-up resistor	T_{ON}	9.0	8.0	ns
T↓ to L.L. active and valid with pair of pull-up resistors	T_{ON}	11.0	10.0	ns
T↑ to L.L. High with single pull-up resistor	T_{PUS}	16.0	14.0	ns
T↑ to L.L. High with pair of pull-up resistors	T_{PUF}	10.0	8.0	ns
BIDI Bidirectional buffer delay	T_{BIDI}	1.7	1.5	ns

Note: 1. Timing is based on the XC3042A, for other devices see timing calculator.

XC3000L Switching Characteristics

Xilinx maintains test specifications for each product as controlled documents. To insure the use of the most recently released device performance parameters, please request a copy of the current test-specification revision.

XC3000L Operating Conditions

Symbol	Description	Min	Max	Units
V_{CC}	Supply voltage relative to GND Commercial 0°C to +85°C junction	3.0	3.6	V
V_{IH}	High-level input voltage — TTL configuration	2.0	V_{CC}+0.3	V
V_{IL}	Low-level input voltage — TTL configuration	-0.3	0.8	V
T_{IN}	Input signal transition time		250	ns

Notes: 1. At junction temperatures above those listed as Operating Conditions, all delay parameters increase by 0.3% per °C.
2. Although the present (1996) devices operate over the full supply voltage range from 3.0 to 5.25 V, Xilinx reserves the right to restrict operation to the 3.0 to 3.6 V range later, when smaller device geometries might preclude operation at 5V. Operating conditions are guaranteed in the 3.0 – 3.6 V V_{CC} range.

XC3000L DC Characteristics Over Operating Conditions

Symbol	Description	Min	Max	Units
V_{OH}	High-level output voltage (@ I_{OH} = –4.0 mA, V_{CC} min)	2.40		V
V_{OL}	Low-level output voltage (@ I_{OL} = 4.0 mA, V_{CC} min)		0.40	V
V_{OH}	High-level output voltage (@ I_{OH} = –4.0 mA, V_{CC} min)	V_{CC} -0.2		V
V_{OL}	Low-level output voltage (@ I_{OL} = 4.0 mA, V_{CC} min)		0.2	V
V_{CCPD}	Power-down supply voltage (PWRDWN must be Low)	2.30		V
I_{CCPD}	Power-down supply current ($V_{CC(MAX)}$ @ T_{MAX})		10	µA
I_{CCO}	Quiescent FPGA supply current in addition to I_{CCPD}[1] Chip thresholds programmed as CMOS levels		 20	 µA
I_{IL}	Input Leakage Current	–10	+10	µA
C_{IN}	Input capacitance, all packages except PGA175 (sample tested) All Pins except XTL1 and XTL2 XTL1 and XTL2		 10 15	 pF pF
	Input capacitance, PGA 175 (sample tested) All Pins except XTL1 and XTL2 XTL1 and XTL2		 15 20	 pF pF
I_{RIN}	Pad pull-up (when selected) @ V_{IN} = 0 V[3]	0.01	0.17	mA
I_{RLL}	Horizontal Longline pull-up (when selected) @ logic Low		2.50	mA

Notes: 1. With no output current loads, no active input or Longline pull-up resistors, all package pins at V_{CC} or GND, and the FPGA device configured with a tie option. I_{CCO} is in addition to I_{CCPD}.
2. Total continuous output sink current may not exceed 100 mA per ground pin. Total continuous output source may not exceed 100 mA per V_{CC} pin. The number of ground pins varies from the XC3020L to the XC3090L.
3. Not tested. Allows an undriven pin to float High. For any other purpose, use an external pull-up.

XC3000L CLB Switching Characteristics Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Since many internal timing parameters cannot be measured directly, they are derived from benchmark timing patterns. The following guidelines reflect worst-case values over the recommended operating conditions. For more detailed, more precise, and more up-to-date timing information, use the values provided by the timing calculator and used in the simulator.

		Speed Grade		-8		
Description		**Symbol**		**Min**	**Max**	**Units**
Combinatorial Delay						
Logic Variables	A, B, C, D, E, to outputs X or Y					
	FG Mode	1	T_{ILO}		6.7	ns
	F and FGM Mode				7.5	ns
Sequential delay						
Clock k to outputs X or Y		8	T_{CKO}		7.5	ns
Clock k to outputs X or Y when Q is returned through function generators F or G to drive X or Y			T_{QLO}			
	FG Mode				14.0	ns
	F and FGM Mode				14.8	ns
Set-up time before clock K						
Logic Variables	A, B, C, D, E					
	FG Mode	2	T_{ICK}	5.0		ns
	F and FGM Mode			5.8		ns
Data In	DI	4	T_{DICK}	5.0		ns
Enable Clock	EC	6	T_{ECCK}	6.0		ns
Hold Time after clock K						
Logic Variables	A, B, C, D, E	3	T_{CKI}	0		ns
Data In	DI[2]	5	T_{CKDI}	2.0		ns
Enable Clock	EC	7	T_{CKEC}	2.0		ns
Clock						
Clock High time		11	T_{CH}	5.0		ns
Clock Low time		12	T_{CL}	5.0		ns
Max. flip-flop toggle rate			F_{CLK}	80.0		MHz
Reset Direct (RD)						
RD width		13	T_{RPW}	7.0		ns
delay from RD to outputs X or Y		9	T_{RIO}	7.0		ns
Global Reset ($\overline{\text{RESET}}$ Pad)[1]						
$\overline{\text{RESET}}$ width (Low)			T_{MRW}	16.0		ns
delay from $\overline{\text{RESET}}$ pad to outputs X or Y			T_{MRQ}		23.0	ns

Notes: 1. Timing is based on the XC3042L, for other devices see timing calculator.
2. The CLB K to Q output delay (T_{CKO}, #8) of any CLB, plus the shortest possible interconnect delay, is always longer than the Data In hold time requirement (T_{CKDI}, #5) of any CLB on the same die.

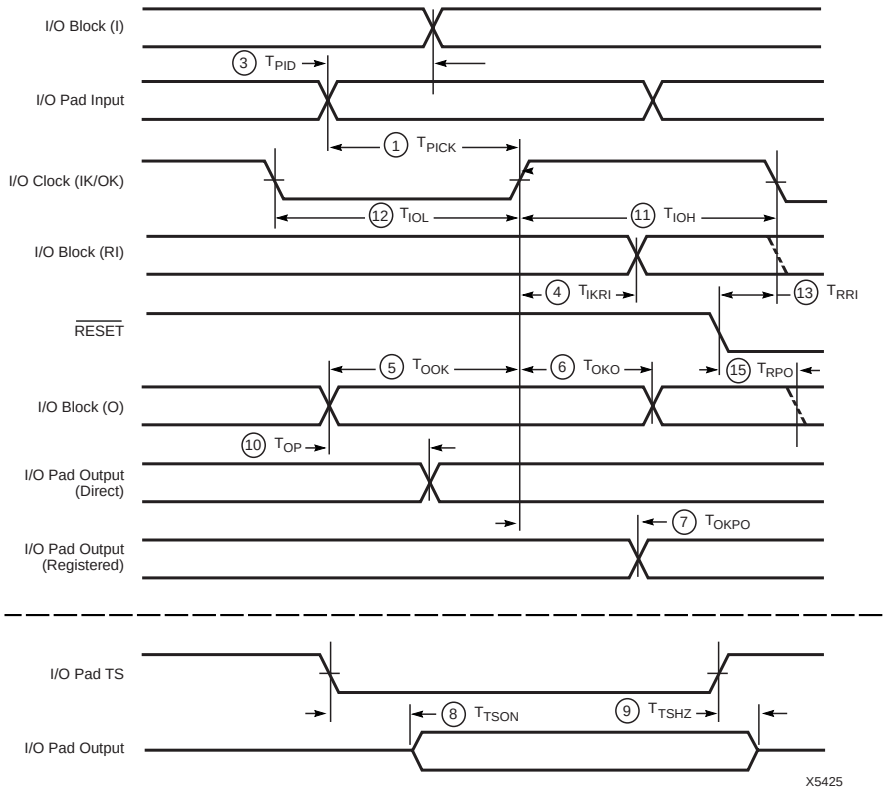
XC3000L IOB Switching Characteristics Guidelines

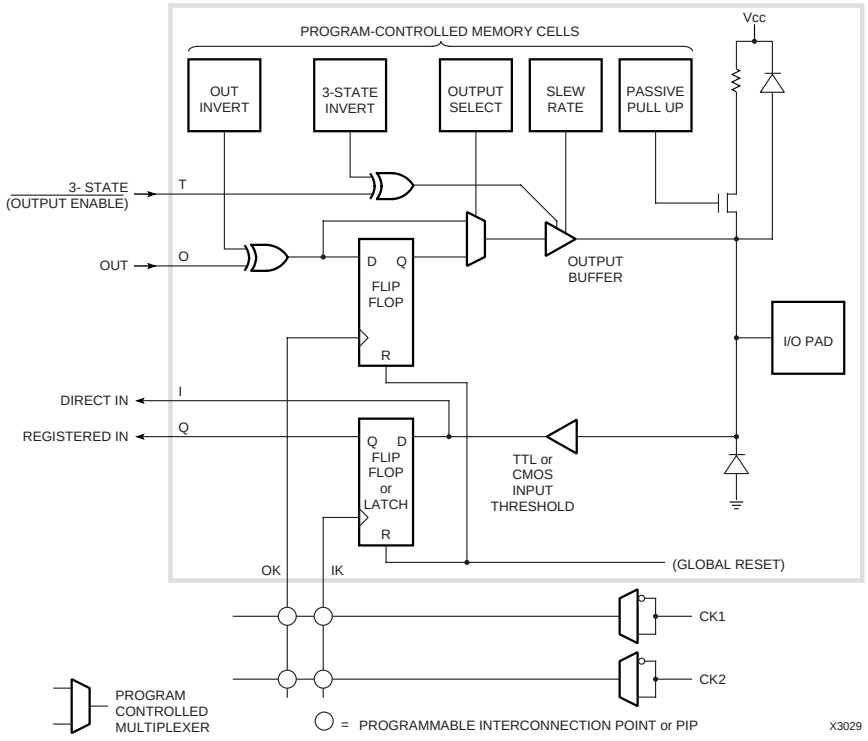
Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Since many internal timing parameters cannot be measured directly, they are derived from benchmark timing patterns. The following guidelines reflect worst-case values over the recommended operating conditions. For more detailed, more precise, and more up-to-date timing information, use the values provided by the timing calculator and used in the simulator.

		Speed Grade	-8		
Description		**Symbol**		**Min**	**Max**	**Units**
Propagation Delays (Input)						
Pad to Direct In (I)		3	T_{PID}		5.0	ns
Pad to Registered In (Q) with latch transparent			T_{PTG}		24.0	ns
Clock (IK) to Registered In (Q)		4	T_{IKRI}		6.0	ns
Set-up Time (Input)						
Pad to Clock (IK) set-up time		1	T_{PICK}	22.0		ns
Propagation Delays (Output)						
Clock (OK) to Pad	(fast)	7	T_{OKPO}		12.0	ns
same	(slew rate limited)	7	T_{OKPO}		28.0	ns
Output (O) to Pad	(fast)	10	T_{OPF}		9.0	ns
same	(slew-rate limited)	10	T_{OPS}		25.0	ns
3-state to Pad begin hi-Z	(fast)	9	T_{TSHZ}		12.0	ns
same	(slew-rate limited)	9	T_{TSHZ}		28.0	ns
3-state to Pad active and valid	(fast)	8	T_{TSON}		16.0	ns
same	(slew -rate limited)	8	T_{TSON}		32.0	ns
Set-up and Hold Times (Output)						
Output (O) to clock (OK) set-up time		5	T_{OOK}	12.0		ns
Output (O) to clock (OK) hold time		6	T_{OKO}	0		ns
Clock						
Clock High time		11	T_{IOH}	5.0		ns
Clock Low time		12	T_{IOL}	5.0		ns
Max. flip-flop toggle rate			F_{CLK}	80.0		MHz
Global Reset Delays (based on XC3042L)						
$\overline{\text{RESET}}$ Pad to Registered In	(Q)	13	T_{RRI}		25.0	ns
$\overline{\text{RESET}}$ Pad to output pad	(fast)	15	T_{RPO}		35.0	ns
	(slew-rate limited)	15	T_{RPO}		51.0	ns

Notes: 1. Timing is measured at pin threshold, with 50 pF external capacitive loads (incl. test fixture). Typical slew rate limited output rise/fall times are approximately four times longer.
2. Voltage levels of unused (bonded and unbonded) pads must be valid logic levels. Each can be configured with the internal pull-up resistor or alternatively configured as a driven output or driven from an external source.
3. Input pad set-up time is specified with respect to the internal clock (ik). In order to calculate system set-up time, subtract clock delay (pad to ik) from the input pad set-up time value. Input pad holdtime with respect to the internal clock (ik) is negative. This means that pad level changes immediately before the internal clock edge (ik) will not be recognized.
4. T_{PID}, T_{PTG}, and T_{PICK} are 3 ns higher for XTL2 when the pin is configured as a user input.

XC3000L IOB Switching Characteristics Guidelines (continued)





XC3064A/XC3090A/XC3195A 84-Pin PLCC Pinouts

XC3000A, XC3000L, XC3100A, and XC3100L families have identical pinouts

PLCC Pin Number	XC3064A, XC3090A, XC3195A
12	PWRDN
13	TCLKIN-I/O
14	I/O
15	I/O
16	I/O
17	I/O
18	I/O
19	I/O
20	I/O
21	GND*
22	VCC
23	I/O
24	I/O
25	I/O
26	I/O
27	I/O
28	I/O
29	I/O
30	I/O
31	M1-RDATA
32	M0-RTRIG
33	M2-I/O
34	HDC-I/O
35	I/O
36	LDC-I/O
37	I/O
38	I/O
39	I/O
40	I/O
41	INIT/I/O*
42	VCC*
43	GND
44	I/O
45	I/O
46	I/O
47	I/O
48	I/O
49	I/O
50	I/O
51	I/O
52	I/O
53	XTL2(IN)-I/O

PLCC Pin Number	XC3064A, XC3090A, XC3195A
54	RESET
55	DONE-PG
56	D7-I/O
57	XTL1(OUT)-BCLKIN-I/O
58	D6-I/O
59	I/O
60	D5-I/O
61	CS0-I/O
62	D4-I/O
63	I/O
64	VCC
65	GND*
66	D3-I/O*
67	CS1-I/O*
68	D2-I/O*
69	I/O
70	D1-I/O
71	RDY/BUSY-RCLK-I/O
72	D0-DIN-I/O
73	DOUT-I/O
74	CCLK
75	A0-WS-I/O
76	A1-CS2-I/O
77	A2-I/O
78	A3-I/O
79	I/O
80	I/O
81	A15-I/O
82	A4-I/O
83	A14-I/O
84	A5-I/O
1	GND
2	VCC*
3	A13-I/O*
4	A6-I/O*
5	A12-I/O*
6	A7-I/O*
7	I/O
8	A11-I/O
9	A8-I/O
10	A10-I/O
11	A9-I/O

Unprogrammed IOBs have a default pull-up. This prevents an undefined pad level for unbonded or unused IOBs. Programmed outputs are default slew-rate limited.

* In the PC84 package, XC3064A, XC3090A and XC3195A have additional VCC and GND pins and thus a different pin definition than XC3020A/XC3030A/XC3042A.

XC3000 Series 208-Pin PQFP Pinouts

XC3000A, and XC3000L families have identical pinouts

Pin Number	XC3090A
1	–
2	GND
3	$\overline{\text{PWRDWN}}$
4	TCLKIN-I/O
5	I/O
6	I/O
7	I/O
8	I/O
9	I/O
10	I/O
11	I/O
12	I/O
13	I/O
14	I/O
15	–
16	I/O
17	I/O
18	I/O
19	I/O
20	I/O
21	I/O
22	I/O
23	I/O
24	I/O
25	GND
26	VCC
27	I/O
28	I/O
29	I/O
30	I/O
31	I/O
32	I/O
33	I/O
34	I/O
35	I/O
36	I/O
37	–
38	I/O
39	I/O
40	I/O
41	I/O
42	I/O
43	I/O
44	I/O
45	I/O
46	I/O
47	I/O
48	M1-$\overline{\text{RDATA}}$
49	GND
50	M0-RTRIG
51	–
52	–

Pin Number	XC3090A
53	–
54	–
55	VCC
56	M2-I/O
57	HDC-I/O
58	I/O
59	I/O
60	I/O
61	$\overline{\text{LDC}}$-I/O
62	I/O
63	I/O
64	–
65	–
66	–
67	–
68	I/O
69	I/O
70	I/O
71	I/O
72	–
73	–
74	I/O
75	I/O
76	I/O
77	$\overline{\text{INIT}}$-I/O
78	VCC
79	GND
80	I/O
81	I/O
82	I/O
83	–
84	–
85	I/O
86	I/O
87	I/O
88	I/O
89	I/O
90	–
91	–
92	–
93	I/O
94	I/O
95	I/O
96	I/O
97	I/O
98	I/O
99	I/O
100	XTL2-I/O
101	GND
102	$\overline{\text{RESET}}$
103	–
104	–

Pin Number	XC3090A
105	–
106	VCC
107	D/$\overline{\text{P}}$
108	–
109	D7-I/O
110	XTL1-BCLKIN-I/O
111	I/O
112	I/O
113	I/O
114	I/O
115	D6-I/O
116	I/O
117	I/O
118	I/O
119	–
120	I/O
121	I/O
122	D5-I/O
123	$\overline{\text{CS0}}$-I/O
124	I/O
125	I/O
126	I/O
127	I/O
128	D4-I/O
129	I/O
130	VCC
131	GND
132	D3-I/O
133	$\overline{\text{CS1}}$-I/O
134	I/O
135	I/O
136	I/O
137	I/O
138	D2-I/O
139	I/O
140	I/O
141	I/O
142	–
143	I/O
144	I/O
145	D1-I/O
146	RDY/$\overline{\text{BUSY}}$-$\overline{\text{RCLK}}$-I/O
147	I/O
148	I/O
149	I/O
150	I/O
151	DIN-D0-I/O
152	DOUT-I/O
153	CCLK
154	VCC
155	–
156	–

Pin Number	XC3090A
157	–
158	–
159	–
160	GND
161	$\overline{\text{WS}}$-A0-I/O
162	CS2-A1-I/O
163	I/O
164	I/O
165	A2-I/O
166	A3-I/O
167	I/O
168	I/O
169	–
170	–
171	–
172	A15-I/O
173	A4-I/O
174	I/O
175	I/O
176	–
177	–
178	A14-I/O
179	A5-I/O
180	I/O
181	I/O
182	GND
183	VCC
184	A13-I/O
185	A6-I/O
186	I/O
187	I/O
188	–
189	–
190	I/O
191	I/O
192	A12-I/O
193	A7-I/O
194	–
195	–
196	–
197	I/O
198	I/O
199	A11-I/O
200	A8-I/O
201	I/O
202	I/O
203	A10-I/O
204	A9-I/O
205	VCC
206	–
207	–
208	–

Unprogrammed IOBs have a default pull-up. This prevents an undefined pad level for unbonded or unused IOBs. Programmed outputs are default slew-rate limited.

* In PQ208, XC3090A and XC3195A have different pinouts.