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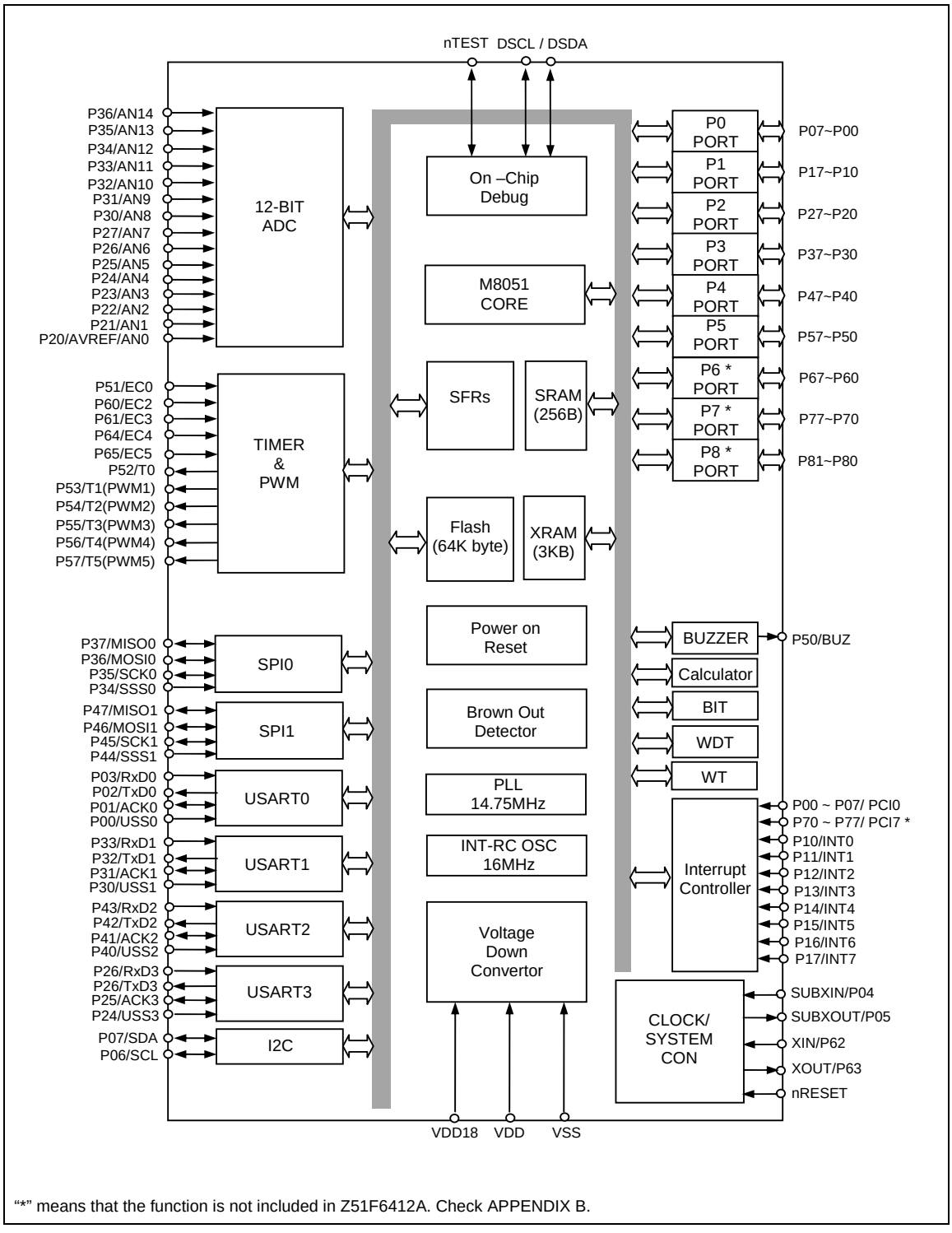
What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	16MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	66
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	3.25K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	A/D 15x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z51f6412atx

2. Block Diagram



"*" means that the function is not included in Z51F6412A. Check APPENDIX B.

Figure 2-1 Z51F6412 block diagram

7.10 DC Characteristics

Table 7-10 DC Characteristics (VDD =2.7~5.5V, VSS =0V, fXIN=10.0MHz, TA=-40~+85℃)

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
Input Low Voltage	VIL1	nTEST, nRESET, DSCL, DSDA	-0.5	-	0.2VDD	V
	VIL2	P0,P1,P2,P4,P5,P6,P7,P8	-0.5	-	0.2VDD	V
	VIL3	P3 (VDD=4.0~5.5V)	-0.5	-	0.1VDD+0.4	V
	VIL4	P3 (VDD=2.7~4.0V)	-0.5	-	0.2VDD	V
Input High Voltage	VIH1	nTEST, nRESET, DSCL, DSDA	0.8VDD	-	VDD	V
	VIH2	P0,P1,P2,P4,P5,P6,P7,P8	0.7VDD	-	VDD	V
	VIH3	P3	0.3VDD+0.7	-	VDD	V
Output Low Voltage	VOL1	ALL I/O (IOL=20mA, VDD=4.5V)	-	-	1	V
Output High Voltage	VOH1	ALL I/O (IOH=-8.57mA, VDD=4.5V)	3.5	-	-	V
Input High Leakage Current	IIH	ALL PAD	-	-	1	uA
Input Low Leakage Current	IIL	ALL PAD	-1	-	-	uA
Pull-Up Resister	RPU	ALL PAD (except DSCL, DSDA)	20	-	50	kΩ
Power Supply Current	IDD1	Run Mode, fXIN=10MHz @5V	-	*2.7	15	mA
	IDD2	Idle Mode, fXIN=10MHz @5V	-	*1.8	10	mA
	IDD3	Sub Active Mode, fSUBXIN=32.768KHz @5V (PLL enable)	-	*0.3	1	mA
	IDD4	Sub Active Mode, fSUBXIN=32.768KHz @5V (PLL disable)	-	*112	500	uA
	IDD5	STOP1 Mode, WDT Active @5V (BOD enable)	-	*60	150	uA
	IDD6	STOP1 Mode, WDT Active @5V (BOD disable)	-	*30	50	uA
	IDD7	STOP2 Mode, WDT Disable @5V (BOD enable), Room Temp(25℃)	-	*32	110	uA
	IDD8	STOP2 Mode, WDT Disable @5V (BOD disable), Room Temp(25℃)	-	*1	10	uA

Note) - STOP1: WDT running, STOP2: WDT disable.
- (*) typical test condition : VDD=5V, Internal RC-OSC=8MHz, ROOM TEMP, all PORT output LOW, Timer0 Active, 1PORT toggling.

7.12 SPI Characteristics

Table 7-12 SPI Characteristics (VDD=5.0V±10%, VSS=0V, TA=-40~+85℃)

Parameter	Symbol	PIN	MIN	TYP	MAX	Unit
Output Clock Pulse Period	tSCK	SCK	-	SPI clock mode	-	ns
Input Clock Pulse Period	tSCK	SCK	2• tSYS	-	-	ns
Input Clock “H” or “L” Pulse Width	tSCKL, tSCKH	SCK		50% duty	-	ns
Input Clock Pulse Transition Time	tFSCK,tRSCK	SCK	-	-	30	ns
Output Clock “H” or “L” Pulse Width	tSCKL, tSCKH	SCK	tSYS-30	-	-	ns
Output Clock Pulse Transition Time	tFSCK,tRSCK	SCK	-	-	30	ns
First Output Clock Delays Time	tFOD	OUTPUT				
Output Clock Delay Time	tDS	OUTPUT	-	-	100	ns
Input Pulse Transition Time	tFSIN,tRSIN	INPUT	-	-	30	ns
Input Setup Time	tDIS	INPUT	100		-	ns
Input Hold Time	tDIH	INPUT	tSYS+70	-	-	ns

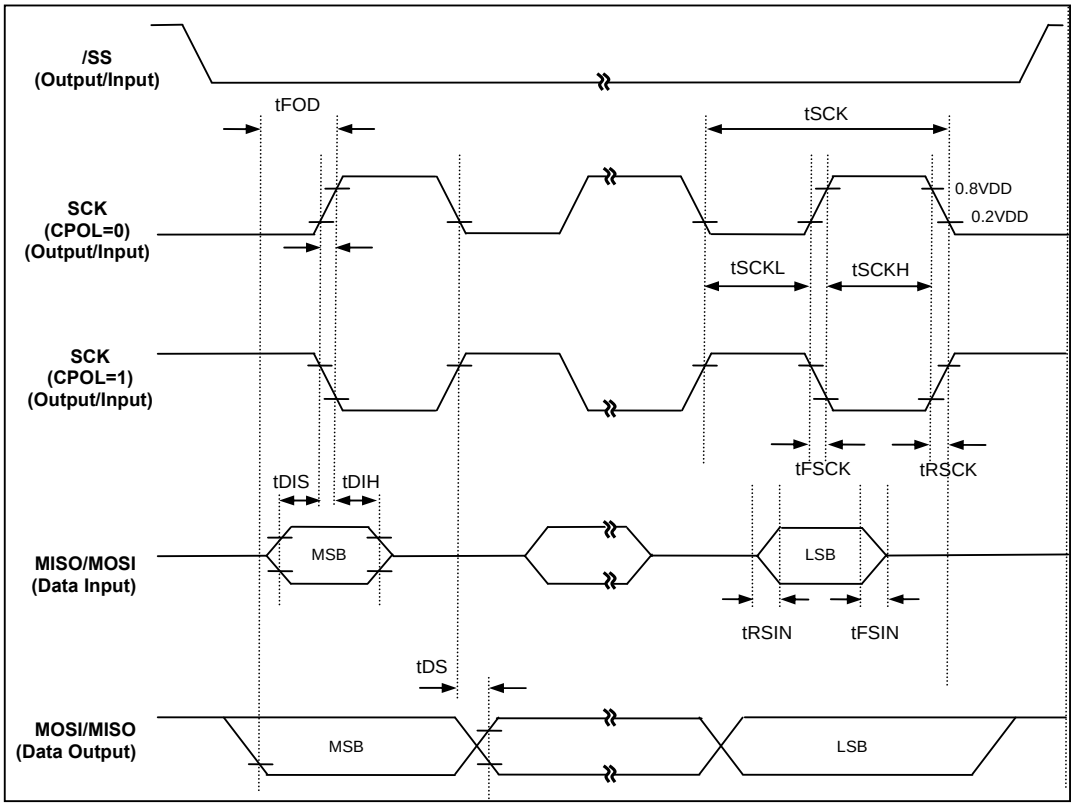


Figure 7-2 SPI Timing

7.13 Typical Characteristics

These graphs and tables provided in this section are for design guidance only and are not tested or guaranteed. In some graphs or tables the data presented are outside specified operating range (e.g. outside specified VDD range). This is for information only and devices are guaranteed to operate properly only within the specified range.

The data presented in this section is a statistical summary of data collected on units from different lots over a period of time. “Typical” represents the mean of the distribution while “max” or “min” represents (mean + 3σ) and (mean - 3σ) respectively where σ is standard deviation.

8.2 Data Memory

Figure 8-2 shows the internal Data memory space available.

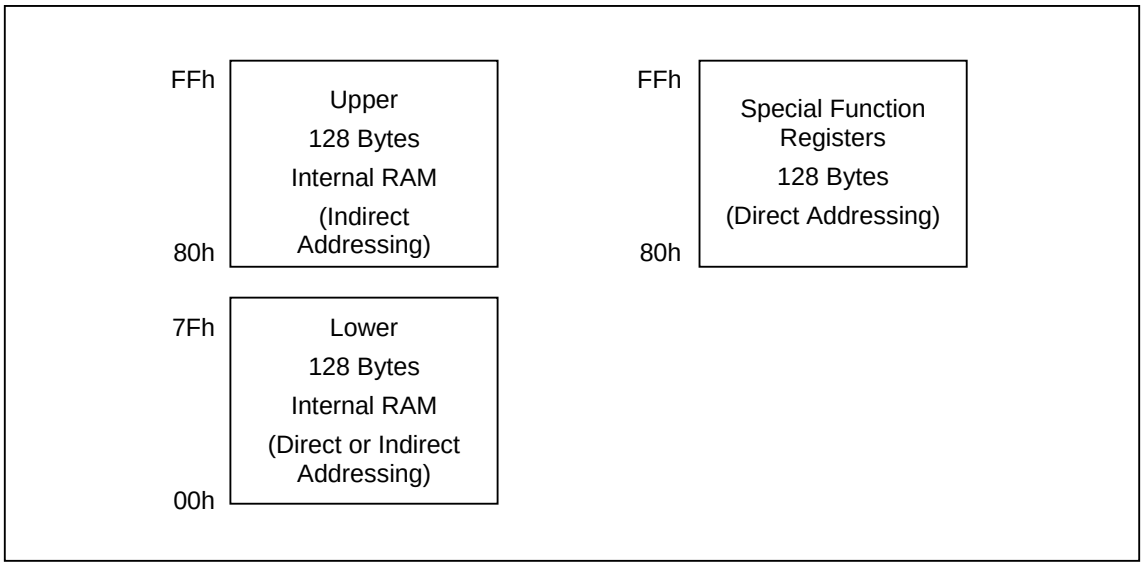


Figure 8-2 Data memory map

The internal memory space is divided into three blocks, which are generally referred to as the lower 128, upper 128, and SFR space.

Internal Data memory addresses are always one byte wide, which implies an address space of only 256 bytes. However, the addressing modes for internal RAM can in fact accommodate 384 bytes, using a simple trick. Direct addresses higher than 7FH access one memory space and indirect addresses higher than 7FH access a different memory space. Thus Fig 8-2 shows the upper 128 and SFR space occupying the same block of addresses, 80H through FFH, although they are physically separate entities.

The lower 128 bytes of RAM are present in all 8051 devices as mapped in Figure 8-3. The lowest 32 bytes are grouped into 4 banks of 8 registers. Program instructions call out these registers as R0 through R7. Two bits in the Program Status Word select which register bank is in use. This allows more efficient used of code space, since register instructions are shorter than instructions that use direct addressing.

The next 16 bytes above the register banks form a block of bit-addressable memory space. The 8051 instruction set includes a wide selection of single-bit instructions, and the 128 bits in this area can be directly addressed by these instructions. The bit addresses in this area are 00H through 7FH.

All of the bytes in the lower 128 can be accessed by either direct or indirect addressing. The upper 128 bytes RAM can only be accessed by indirect addressing. These spaces are used for user RAM and stack pointer.

INT14E Enable or disable Timer 2 Interrupt
0 Disable
1 Enable

INT13E Enable or disable Timer 1 Interrupt
0 Disable
1 Enable

INT12E Enable or disable Timer 0 Interrupt
0 Disable
1 Enable

IE3 (Interrupt Enable Register 3) : ABH

7	6	5	4	3	2	1	0
-	-	INT23E	INT22E	INT21E	INT20E	INT19E	INT18E
R	R	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 00H

INT23E Enable or disable SPI1 Interrupt
0 Disable
1 Enable

INT22E Enable or disable BIT Interrupt
0 Disable
1 Enable

INT21E Enable or disable WDT Interrupt
0 Disable
1 Enable

INT20E Enable or disable WT Interrupt
0 Disable
1 Enable

INT19E Enable or disable EEPROM Interrupt
0 Disable
1 Enable

INT18E Enable or disable ADC Interrupt
0 Disable
1 Enable

IE4 (Interrupt Enable Register 4) : ACH

7	6	5	4	3	2	1	0
-	-	INT29E	INT28E	INT27E	INT26E	INT25E	INT24E
R	R	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : 00H

INT29E Enable or disable External Interrupt 5
0 Disable
1 Enable

INT28E Enable or disable External Interrupt 4
0 Disable
1 Enable

INT27E Enable or disable USART3 Tx Interrupt
0 Disable

11.3.6 WDT Interrupt Timing Waveform

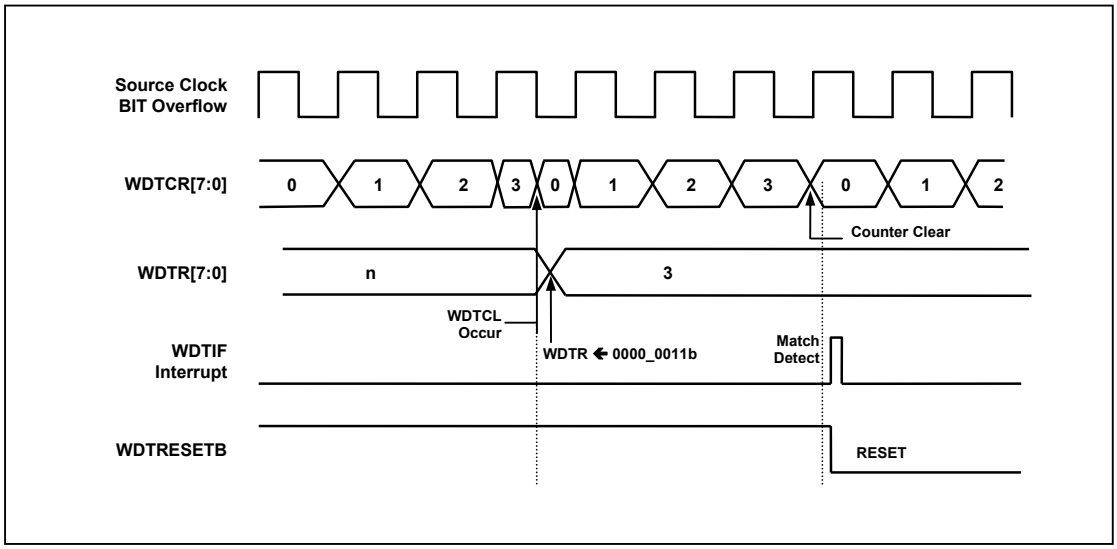


Figure 11-4 WDT Interrupt Timing Waveform

Table 11-7 PWM Frequency vs. Resolution at 8 Mhz

Resolution	Frequency		
	T1CK[1:0]=00 (125ns)	T1CK[1:0]=01 (250ns)	T1CK[1:0]=10 (2us)
10 Bit	7.8KHz	3.9KHz	0.49KHz
9 Bit	15.6KHz	7.8KHz	0.98KHz
8 Bit	31.2KHz	15.6KHz	1.95KHz
7 Bit	62.4KHz	31.2KHz	3.91KHz

The POL bit of T1CR register decides the polarity of duty cycle. If the duty value is set same to the period value, the PWM output is determined by the bit POL (1: High, 0: Low). And if the duty value is set to "00H", the PWM output is determined by the bit POL (1: Low, 0: High).

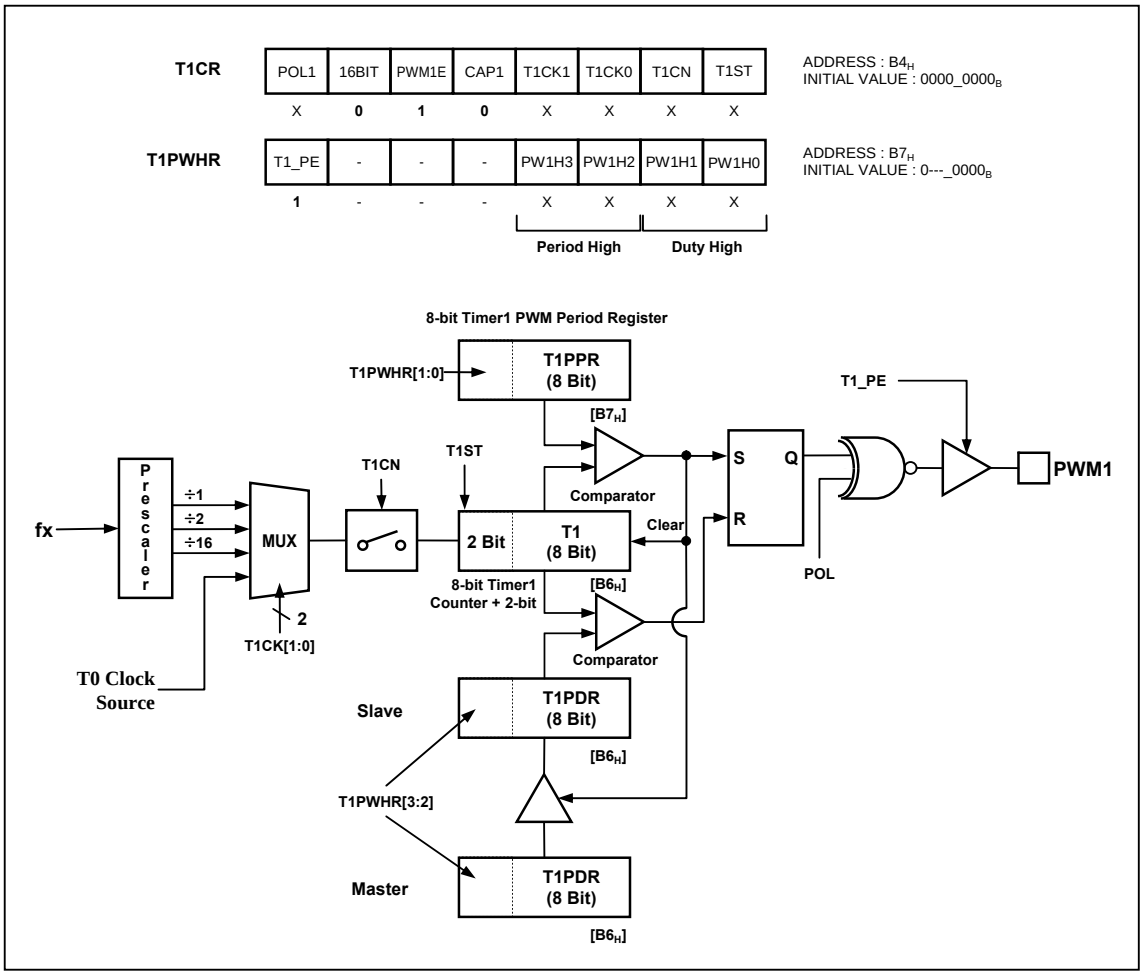


Figure 11-14 PWM Mode

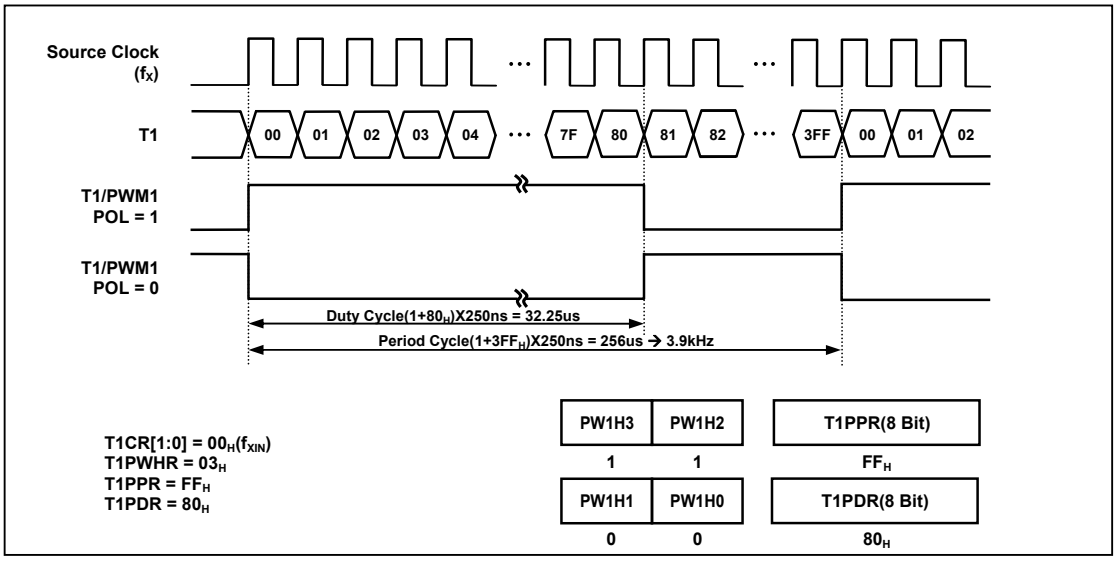


Figure 11-15 Example of PWM at 4MHz

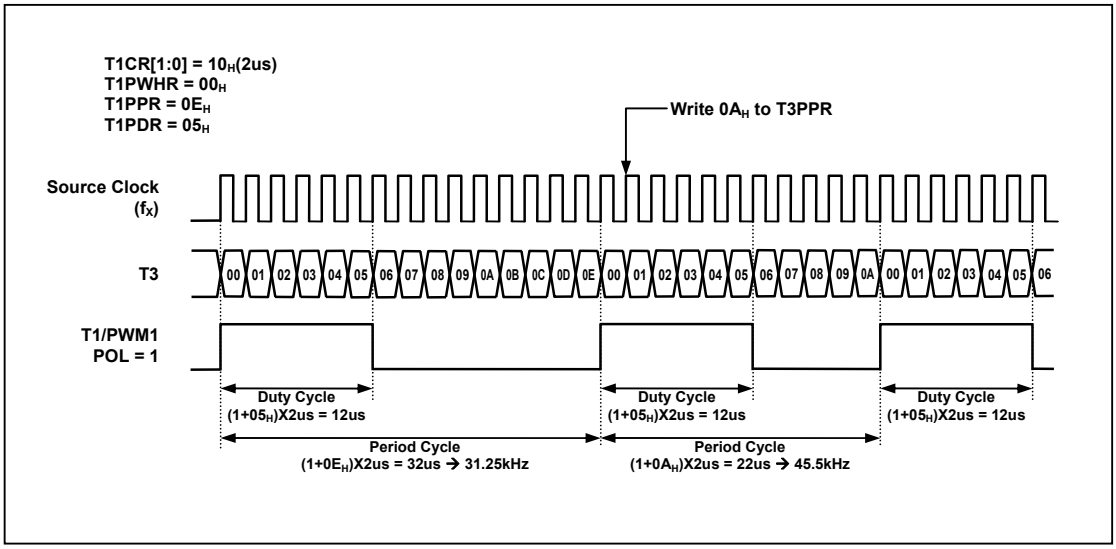


Figure 11-16 Example of Changing the Period in Absolute Duty Cycle at 4Mhz

11.6 Buzzer Driver

11.6.1 Overview

The Buzzer consists of 8 Bit Counter and BUZDR (Buzzer Data Register), BUZCR (Buzzer Control Register). The Square Wave (122.07Hz~250 KHz, @16MHz) gets out of P12/BUZ pin. BUZDR (Buzzer Data Register) controls the Buzzer frequency (look at the following expression). In the BUZCR (Buzzer Control Register), BUCK[1:0] selects source clock divided from prescaler.

$$f_{BUZ}(Hz) = \frac{\text{Oscillator Frequency}}{2 \times \text{Prescaler Ratio} \times (\text{BUZDR} + 1)}$$

Table 11-11 Buzzer Frequency at 16MHz

BUZDR[7:0]	Buzzer Frequency (kHz)			
	BUZCR[2:1]=00	BUZCR[2:1]=01	BUZCR[2:1]=10	BUZCR[2:1]=11
0000_0000	250kHz	125kHz	62.5kHz	31.25kHz
0000_0001	125kHz	62.5kHz	31.25kHz	15.624kHz
…	…	…	…	…
1111_1101	984.252Hz	492.126Hz	246.062Hz	123.03Hz
1111_1110	980.392Hz	490.196Hz	245.098Hz	122.548Hz
1111_1111	976.562Hz	488.282Hz	244.140Hz	122.07Hz

11.6.2 Block Diagram

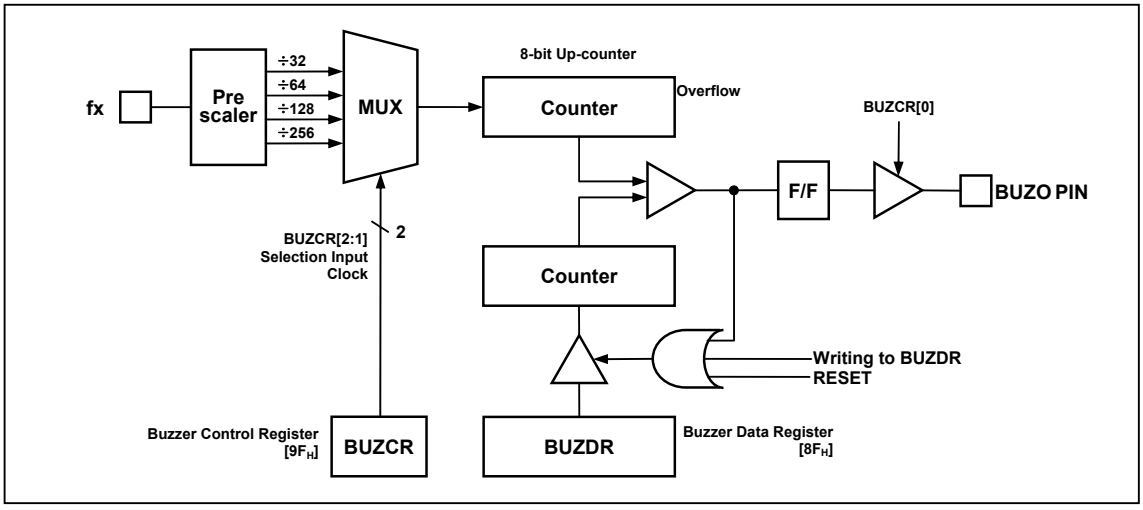


Figure 11-21 Buzzer Driver Block Diagram

11.6.3 Register Map

Table 11-12 Register Map

Name	Address	Dir	Default	Description
BUZDR	8FH	R/W	FFH	Buzzer Data Register
BUZCR	9FH	R/W	00H	Buzzer Control Register

11.6.4 Buzzer Driver Register description

Buzzer Driver consists of Buzzer Data Register (BUZDR), Buzzer Control Register (BUZCR).

11.6.5 Register description for Buzzer Driver

BUZDR (Buzzer Data Register) : 8FH

7	6	5	4	3	2	1	0
BUZDR7	BUZDR6	BUZDR5	BUZDR4	BUZDR3	BUZDR2	BUZDR1	BUZDR0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : FFH

BUZDR[7:0] This bits control the Buzzer frequency
Its resolution is 00H ~ FFH

BUZCR (Buzzer Control Register) : 9FH

7	6	5	4	3	2	1	0
-	-	-	-	-	BUCK1	BUCK0	BUZEN
-	-	-	-	-	R/W	R/W	R/W

Initial value : 00H

BUCK[1:0] Buzzer Driver Source Clock Selection

BUCK1	BUCK0	Source Clock
0	0	fx/32
0	1	fx/64
1	0	fx/128
1	1	fx/256

BUZEN Buzzer Driver Operation Control

0	Buzzer Driver disable
1	Buzzer Driver enable

Note) fx: Main system clock oscillation frequency

11.7.4 External Clock (XCK)

External clocking is used by the synchronous or spi slave modes of operation.

External clock input from the XCK pin is sampled by a synchronization logic to remove meta-stability. The output from the synchronization logic must then pass through an edge detector before it can be used by the Transmitter and Receiver. This process introduces a two CPU clock period delay and therefore the maximum frequency of the external XCK pin is limited by the following equation.

$$fXCK = \frac{fSCLK}{4}$$

where fXCK is the frequency of XCK and fSCLK is the frequency of main system clock (SCLK).

11.7.5 Synchronous mode Operation

When synchronous or spi mode is used, the XCK pin will be used as either clock input (slave) or clock output (master). The dependency between the clock edges and data sampling or data change is the same. The basic principle is that data input on RXD (MISO in spi mode) pin is sampled at the opposite XCK clock edge of the edge in the data output on TXD (MOSI in spi mode) pin is changed.

The UCPOL bit in UCTRLx1 register selects which XCK clock edge is used for data sampling and which is used for data change. As shown in the figure below, when UCPOL is zero the data will be changed at rising XCK edge and sampled at falling XCK edge.

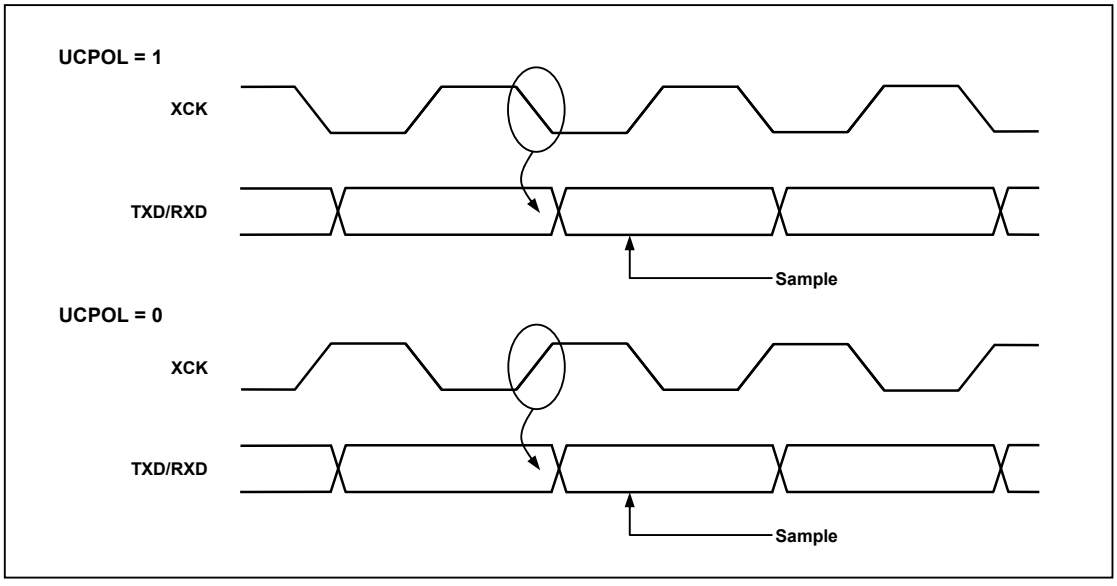


Figure 11-24 Synchronous Mode XCKn Timing

UDRE The UDRE flag indicates if the transmit buffer (UDATA) is ready to receive new data. If UDRE is '1', the buffer is empty and ready to be written. This flag can generate a UDRE interrupt.

0 Transmit buffer is not empty.

1 Transmit buffer is empty.

TXC This flag is set when the entire frame in the transmit shift register has been shifted out and there is no new data currently present in the transmit buffer. This flag is automatically cleared when the interrupt service routine of a TXC interrupt is executed. This flag can generate a TXC interrupt.

0 Transmission is ongoing.

1 Transmit buffer is empty and the data in transmit shift register are shifted out completely.

RXC This flag is set when there are unread data in the receive buffer and cleared when all the data in the receive buffer are read. The RXC flag can be used to generate a RXC interrupt.

0 There is no data unread in the receive buffer

1 There are more than 1 data in the receive buffer

WAKE This flag is set when the RX pin is detected low while the CPU is in stop mode. This flag can be used to generate a WAKE interrupt. This bit is set only when in asynchronous mode of operation.

0 No WAKE interrupt is generated.

1 WAKE interrupt is generated

SOFTRST This is an internal reset and only has effect on USART. Writing '1' to this bit initializes the internal logic of USART and is auto cleared.

0 No operation

1 Reset USART

DOR This bit is set if a Data OverRun occurs. While this bit is set, the incoming data frame is ignored. This flag is valid until the receive buffer is read.

0 No Data OverRun

1 Data OverRun detected

FE This bit is set if the first stop bit of next character in the receive buffer is detected as '0'. This bit is valid until the receive buffer is read.

0 No Frame Error

1 Frame Error detected

PE This bit is set if the next character in the receive buffer has a Parity Error when received while Parity Checking is enabled. This bit is valid until the receive buffer is read.

0 No Parity Error

1 Parity Error detected

UBAUDx(USART Baud-Rate Generation Register) : E6H, FEH, 2F2CH, 2F34H

7	6	5	4	3	2	1	0
UBAUD7	UBAUD6	UBAUD5	UBAUD4	UBAUD3	UBAUD2	UBAUD1	UBAUD0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Initial value : FFH

UBAUD [7:0] The value in this register is used to generate internal baud rate in asynchronous mode or to generate XCK clock in synchronous or spi mode. To prevent malfunction, do not write '0' in asynchronous mode, and do not write '0' or '1' in synchronous or spi mode.

UDATAx (USART Data Register) : E7H, FFH, 2F2DH, 2F35H

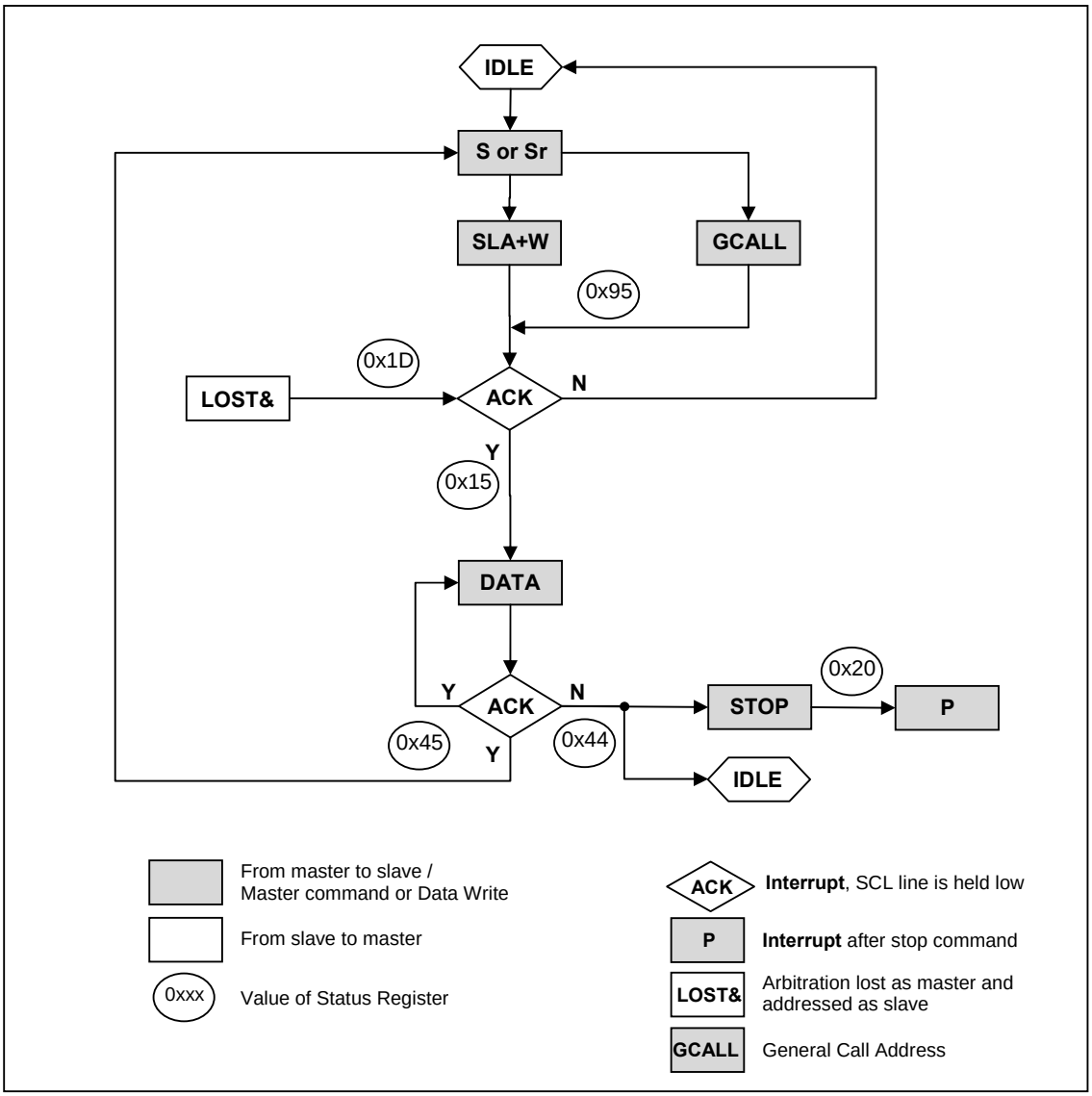


Figure 11-44 Formats and States in the Slave Receiver Mode

11.9.9 Register Map

Name	Address	Dir	Default	Description
I2CMR	DAH	R/W	00H	I^2C Mode Control Register
I2CSR	DBH	R	00H	I^2C Status Register
I2CSCLLR	DCH	R/W	3FH	SCL Low Period Register
I2CSCLHR	DDH	R/W	3FH	SCL High Period Register
I2CSDAHR	DEH	R/W	01H	SDA Hold Time Register
I2CDR	DFH	R/W	FFH	I^2C Data Register
I2CSAR	D7H	R/W	00H	I^2C Slave Address Register
I2CSAR1	D6H	R/W	00H	I^2C Slave Address Register 1

0	1	fx/4	3V~5V
1	0	fx/8	2.7V~3V
1	1	fx/32	2.4V~2.7V

Note) 1. fx : system clock

2. ADC clock have to be used 3MHz under

12. Power Down Operation

12.1 Overview

The Z51F6412 MCU features three power-down modes to minimize the power consumption of the device. In power down mode, power consumption is reduced considerably. The device provides three kinds of power saving functions, IDLE, STOP1 and STOP2 mode. In three modes, program is stopped.

12.2 Peripheral Operation in IDLE/STOP Mode

Table 12-1 Peripheral Operation during Power Down Mode.

Peripheral	IDLE Mode	STOP1 Mode	STOP2 Mode
CPU	ALL CPU Operation are Disable	ALL CPU Operation are Disable	ALL CPU Operation are Disable
RAM	Retain	Retain	Retain
Basic Interval Timer	Operates Continuously	Operates Continuously	Stop
Watch Dog Timer	Operates Continuously	Operates Continuously	Stop
Watch Timer	Operates Continuously	Stop (Only operate in sub clock mode)	Stop (Only operate in sub clock mode)
Timer	Operates Continuously	Halted (Only when the Event Counter Mode is Enable, Timer operates Normally)	Halted (Only when the Event Counter Mode is Enable, Timer operates Normally)
ADC	Operates Continuously	Stop	Stop
BUZ	Operates Continuously	Stop	Stop
SPI/SCI	Operates Continuously	Only operate with external clock	Only operate with external clock
I2C	Operates Continuously	Stop	Stop
Internal OSC (16MHz)	Oscillation	Stop	Stop
Main OSC (1~10MHz)	Oscillation	Stop	Stop
Sub OSC (32.768kHz)	Oscillation	Oscillation	Oscillation
Internal RCOSC (125kHz)	Oscillation	Oscillation	Stop
I/O Port	Retain	Retain	Retain
Control Register	Retain	Retain	Retain
Address Data Bus	Retain	Retain	Retain
Release Method	By RESET, all Interrupts	By RESET,Timer Interrupt (EC0,2,3,4,5), SIO (External clock), External Interrupt, UART by ACK PCI, I2C (slave mode), WT (sub clock), WDT, BIT	By RESET,Timer Interrupt (EC0,2,3,4,5), SIO (External clock), External Interrupt, UART by ACK PCI, I2C (slave mode), WT (sub clock)

12.5 Release Operation of STOP1, 2 Mode

After STOP1, 2 mode is released, the operation begins according to content of related interrupt register just before STOP1, 2 mode start (Figure 12-5). Interrupt Enable Flag of All (EA) of IE should be set to `1`. Released by only interrupt which each interrupt enable flag = `1`, and jump to the relevant interrupt service routine.

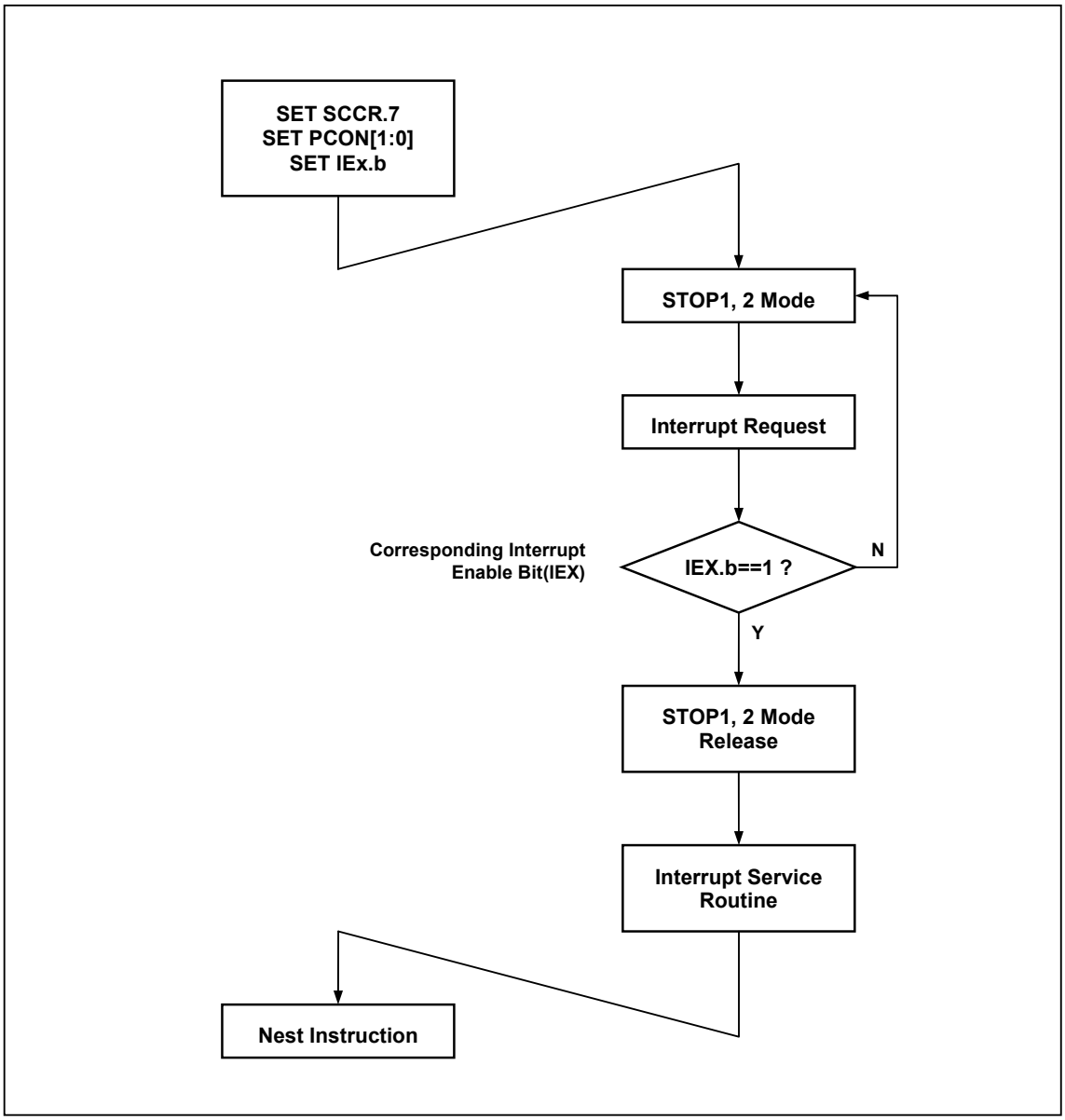


Figure 12-5 STOP1, 2 Mode Release Flow

15.4 Serial In-System Program Mode

Serial in-system program uses the interface of debugger which uses two wires. Refer to chapter 14 in details about debugger

15.4.1 Flash operation

Configuration(This Configuration is just used for follow description)

7	6	5	4	3	2	1	0
-	FEMR[4]&[1]	FEMR[5]&[1]	-	-	FEMR[2]	FECR[6]	FECR[7]
-	ERASE&VFY	PGM&VFY	-	-	OTPE	AEE	AEF

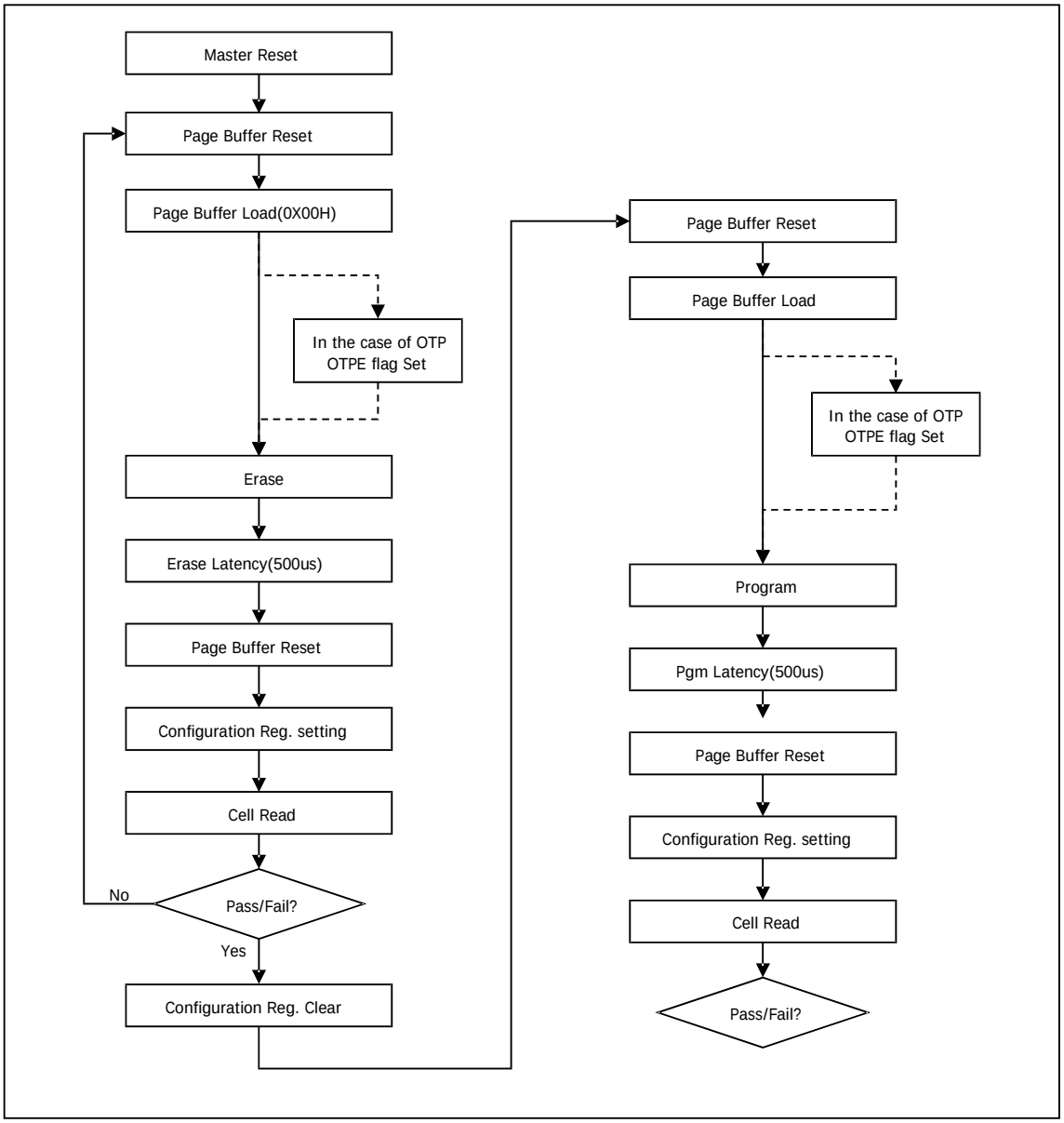


Figure 15-3 The sequence of page program and erase of Flash memory

Step 8. Insert one NOP operation
Step 9. Read FESR until PEVBSY is 1.

15.4.1.6 Flash OTP area read mode

Step 1. Enter OCD(=ISP) mode.
Step 2. Set ENBDM bit of BCR.
Step 3. Enable debug and Request debug mode.
Step 4. Select OTP area. FEMR:1000_0101
Step 5. Read data from Flash.

15.4.1.7 Flash OTP area write mode

Step 1. Enable program mode.
Step 2. Reset page buffer. FEMR: 1000_0001 FECR:0000_0010
Step 3. Select page buffer. FEMR:1000_1001
Step 4. Write data to page buffer.(Address automatically increases by twin.)
Step 5. Set write mode and select OTP area. FEMR:1010_0101
Step 6. Set page address. FEARH:FEARM:FEARL=20'hx_xxxx
Step 7. Set FETCR.
Step 8. Start program. FECR:0000_1011
Step 9. Insert one NOP operation
Step 10. Read FESR until PEVBSY is 1.

15.4.1.8 Flash OTP area erase mode

Step 1. Enable program mode.
Step 2. Reset page buffer. FEMR: 1000_0001 FECR:0000_0010
Step 3. Select page buffer. FEMR:1000_1001
Step 4. Write 'h00 to page buffer. (Data value is not important.)
Step 5. Set erase mode and select OTP area. FEMR:1001_0101
Step 6. Set page address. FEARH:FEARM:FEARL=20'hx_xxxx
Step 7. Set FETCR.
Step 8. Start erase. FECR:0000_1011
Step 9. Insert one NOP operation
Step 10. Read FESR until PEVBSY is 1.

15.4.1.9 Flash program verify mode

Step 1. Enable program mode.
Step 2. Set program verify mode. FEMR:1010_0011
Step 3. Read data from Flash.

16. Configure option

16.1 Configure option Control Register

FUSE_CONF (Pseudo-Configure Data) : 2F5DH

7	6	5	4	3	2	1	0
BSIZE1	BSIZE0	SXINEN	XINENA	-	OCDSEL	LOCKB	LOCKF
R	R	R	R	R	R	R	R

Initial value : 00H

BSIZE Boot Code size option
- 00 768B (1KB – 256B : 0x0FF ~ 0x3FF) (default)
- 01 1792B (2KB – 256B : 0x0FF ~ 0x7FF)
- 10 3840B (4KB – 256B : 0x0FF ~ 0xFFF)
- 11 7936B (8KB – 256B : 0x0FF ~ 0x1FFF)

SXINEN External Sub Oscillator Enable Bit
- 0 Sub OSC disable (default)
- 1 Sub OSC enable

XINENA External Main Oscillator Enable Bit
- 0 Main OSC disable (default)
- 1 Main OSC Enable

OCDSEL Selects noise cancelling scheme of OCD pins.
- 0 OCD lines are outputs of 10ns noise canceller
- 1 OCD lines synchronized by INTRC clock

LOCKE Boot Code LOCK bit
- 0 Boot LOCK Disable
- 1 Boot LOCK Enable (protect boot code from byte/page erase)

LOCKF CODE memory LOCK bit
- 0 LOCK Disable
- 1 LOCK Enable

In OCD debug mode, user can change FUSE_CONF bits value temporarily except LOCKF for debugging job.