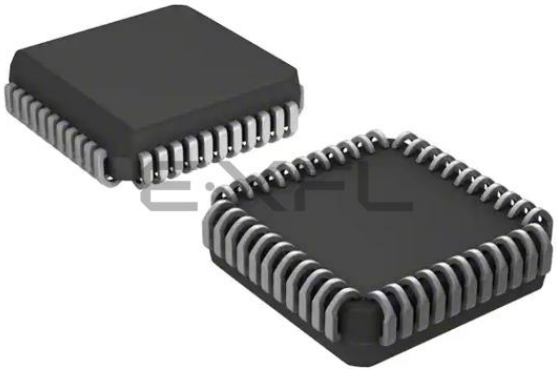

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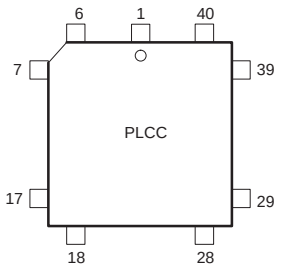
## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | XA |
| Core Size | 16-Bit |
| Speed | 30MHz |
| Connectivity | UART/USART |
| Peripherals | PWM, WDT |
| Number of I/O | 32 |
| Program Memory Size | 32KB (32K x 8) |
| Program Memory Type | OTP |
| EEPROM Size | - |
| RAM Size | 512 x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.7V ~ 5.5V |
| Data Converters | - |
| Oscillator Type | External |
| Operating Temperature | 0°C ~ 70°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 44-LCC (J-Lead) |
| Supplier Device Package | 44-PLCC (16.59x16.59) |
| Purchase URL | https://www.e-xfl.com/product-detail/nxp-semiconductors/pxag37kba-512 |

## PIN CONFIGURATIONS

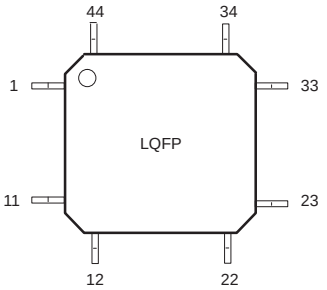
### 44-Pin PLCC Package




| Pin | Function | Pin | Function |
|---|---|---|---|
| 1 | $V_{SS}$ | 23 | $V_{DD}$ |
| 2 | P1.0/A0/$\overline{WRH}$ | 24 | P2.0/A12D8 |
| 3 | P1.1/A1 | 25 | P2.1/A13D9 |
| 4 | P1.2/A2 | 26 | P2.2/A14D10 |
| 5 | P1.3/A3 | 27 | P2.3/A15D11 |
| 6 | P1.4/RxD1 | 28 | P2.4/A16D12 |
| 7 | P1.5/TxD1 | 29 | P2.5/A17D13 |
| 8 | P1.6/T2 | 30 | P2.6/A18D14 |
| 9 | P1.7/T2EX | 31 | P2.7/A19D15 |
| 10 | $\overline{RST}$ | 32 | $\overline{PSEN}$ |
| 11 | P3.0/RxD0 | 33 | ALE/$\overline{PROG}$ |
| 12 | NC | 34 | NC |
| 13 | P3.1/TxD0 | 35 | $\overline{EA}$/$V_{PP}$/WAIT |
| 14 | P3.2/$\overline{INT0}$ | 36 | P0.7/A11D7 |
| 15 | P3.3/$\overline{INT1}$ | 37 | P0.6/A10D6 |
| 16 | P3.4/T0 | 38 | P0.5/A9D5 |
| 17 | P3.5/T1/BUSW | 39 | P0.4/A8D4 |
| 18 | P3.6/$\overline{WRL}$ | 40 | P0.3/A7D3 |
| 19 | P3.7/$\overline{RD}$ | 41 | P0.2/A6D2 |
| 20 | XTAL2 | 42 | P0.1/A5D1 |
| 21 | XTAL1 | 43 | P0.0/A4D0 |
| 22 | $V_{SS}$ | 44 | $V_{DD}$ |

*SU00525*

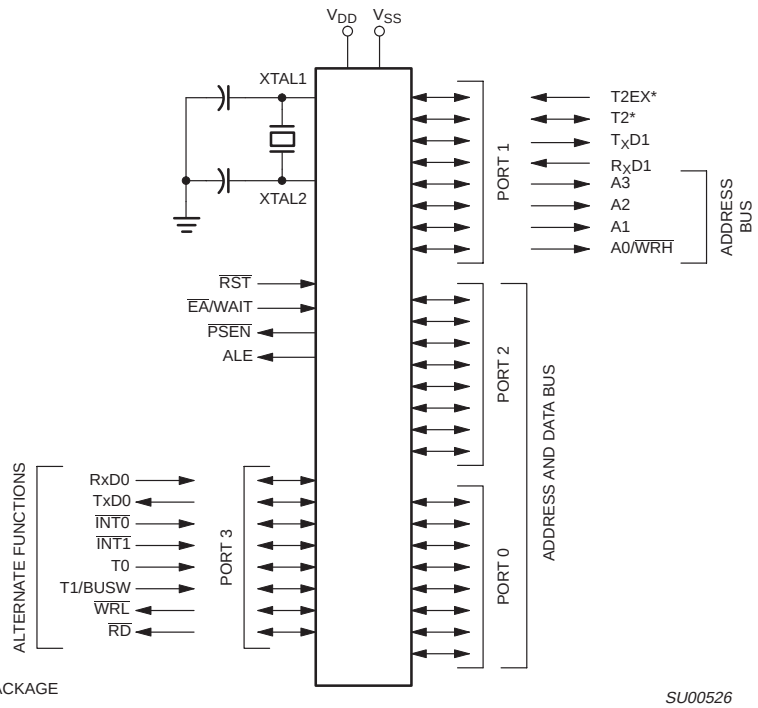
### 44-Pin LQFP Package




| Pin | Function | Pin | Function |
|---|---|---|---|
| 1 | P1.5/TxD1 | 23 | P2.5/A17D13 |
| 2 | P1.6/T2 | 24 | P2.6/A18D14 |
| 3 | P1.7/T2EX | 25 | P2.7/A19D15 |
| 4 | $\overline{RST}$ | 26 | $\overline{PSEN}$ |
| 5 | P3.0/RxD0 | 27 | ALE/$\overline{PROG}$ |
| 6 | NC | 28 | NC |
| 7 | P3.1/TxD0 | 29 | $\overline{EA}$/$V_{PP}$/WAIT |
| 8 | P3.2/$\overline{INT0}$ | 30 | P0.7/A11D7 |
| 9 | P3.3/$\overline{INT1}$ | 31 | P0.6/A10D6 |
| 10 | P3.4/T0 | 32 | P0.5/A9D5 |
| 11 | P3.5/T1/BUSW | 33 | P0.4/A8D4 |
| 12 | P3.6/$\overline{WRL}$ | 34 | P0.3/A7D3 |
| 13 | P3.7/$\overline{RD}$ | 35 | P0.2/A6D2 |
| 14 | XTAL2 | 36 | P0.1/A5D1 |
| 15 | XTAL1 | 37 | P0.0/A4D0 |
| 16 | $V_{SS}$ | 38 | $V_{DD}$ |
| 17 | $V_{DD}$ | 39 | $V_{SS}$ |
| 18 | P2.0/A12D8 | 40 | P1.0/A0/$\overline{WRH}$ |
| 19 | P2.1/A13D9 | 41 | P1.1/A1 |
| 20 | P2.2/A14D10 | 42 | P1.2/A2 |
| 21 | P2.3/A15D11 | 43 | P1.3/A3 |
| 22 | P2.4/A16/D12 | 44 | P1.4/RxD1 |

*SU00580*

## LOGIC SYMBOL




* NOT AVAILABLE ON 40-PIN DIP PACKAGE

*SU00526*

| MNEMONIC | PIN. NO. | | TYPE | NAME AND FUNCTION |
|---|---|---|---|---|
| | PLCC | LQFP | | |
| $\overline{PSEN}$ | 32 | 26 | O | **Program Store Enable:** The read strobe for external program memory. When the microcontroller accesses external program memory, $\overline{PSEN}$ is driven low in order to enable memory devices. $\overline{PSEN}$ is only active when external code accesses are performed. |
| $\overline{EA}$/WAIT/ $V_{PP}$ | 35 | 29 | I | **External Access/Wait:** The $\overline{EA}$ input determines whether the internal program memory of the microcontroller is used for code execution. The value on the $\overline{EA}$ pin is latched as the external reset input is released and applies during later execution. When latched as a 0, external program memory is used exclusively, when latched as a 1, internal program memory will be used up to its limit, and external program memory used above that point. After reset is released, this pin takes on the function of bus Wait input. If Wait is asserted high during any external bus access, that cycle will be extended until Wait is released. During EPROM programming, this pin is also the programming supply voltage input. |
| XTAL1 | 21 | 15 | I | **Crystal 1:** Input to the inverting amplifier used in the oscillator circuit and input to the internal clock generator circuits. |
| XTAL2 | 20 | 14 | O | **Crystal 2:** Output from the oscillator amplifier. |

## SPECIAL FUNCTION REGISTERS

| NAME | DESCRIPTION | SFR ADDRESS | BIT FUNCTIONS AND ADDRESSES MSB | | | | | | | LSB | RESET VALUE |
|---|---|---|---|---|---|---|---|---|---|---|---|
| BCR | Bus configuration register | 46A | — | — | — | WAITD | BUSD | BC2 | BC1 | BC0 | Note 1 |
| BTRH | Bus timing register high byte | 469 | DW1 | DW0 | DWA1 | DWA0 | DR1 | DR0 | DRA1 | DRA0 | FF |
| BTRL | Bus timing register low byte | 468 | WM1 | WM0 | ALEW | — | CR1 | CR0 | CRA1 | CRA0 | EF |
| CS | Code segment | 443 | | | | | | | | | 00 |
| DS | Data segment | 441 | | | | | | | | | 00 |
| ES | Extra segment | 442 | | | | | | | | | 00 |
| | | | 33F | 33E | 33D | 33C | 33B | 33A | 339 | 338 | |
| IEH* | Interrupt enable high byte | 427 | — | — | — | — | ETI1 | ERI1 | ETI0 | ERI0 | 00 |
| | | | 337 | 336 | 335 | 334 | 333 | 332 | 331 | 330 | |
| IEL* | Interrupt enable low byte | 426 | EA | — | — | ET2 | ET1 | EX1 | ET0 | EX0 | 00 |
| IPA0 | Interrupt priority 0 | 4A0 | — | PT0 | | | — | PX0 | | | 00 |
| IPA1 | Interrupt priority 1 | 4A1 | — | PT1 | | | — | PX1 | | | 00 |
| IPA2 | Interrupt priority 2 | 4A2 | — | — | | | — | PT2 | | | 00 |
| IPA4 | Interrupt priority 4 | 4A4 | — | PTI0 | | | — | PRI0 | | | 00 |
| IPA5 | Interrupt priority 5 | 4A5 | — | PTI1 | | | — | PRI1 | | | 00 |
| | | | 387 | 386 | 385 | 384 | 383 | 382 | 381 | 380 | |
| P0* | Port 0 | 430 | AD7 | AD6 | AD5 | AD4 | AD3 | AD2 | AD1 | AD0 | FF |
| | | | 38F | 38E | 38D | 38C | 38B | 38A | 389 | 388 | |
| P1* | Port 1 | 431 | T2EX | T2 | TxD1 | RxD1 | A3 | A2 | A1 | WRH | FF |
| | | | 397 | 396 | 395 | 394 | 393 | 392 | 391 | 390 | |
| P2* | Port 2 | 432 | P2.7 | P2.6 | P2.5 | P2.4 | P2.3 | P2.2 | P2.1 | P2.0 | FF |

| NAME | DESCRIPTION | SFR ADDRESS | BIT FUNCTIONS AND ADDRESSES MSB | | | | | | | LSB | RESET VALUE |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 357 | 356 | 355 | 354 | 353 | 352 | 351 | 350 | |
| SWR* | Software Interrupt Request | 42A | — | SWR7 | SWR6 | SWR5 | SWR4 | SWR3 | SWR2 | SWR1 | 00 |
| | | | 2C7 | 2C6 | 2C5 | 2C4 | 2C3 | 2C2 | 2C1 | 2C0 | |
| T2CON* | Timer 2 control register | 418 | TF2 | EXF2 | RCLK0 | TCLK0 | EXEN2 | TR2 | C/T2 | CP/RL2 | 00 |
| | | | 2CF | 2CE | 2CD | 2CC | 2CB | 2CA | 2C9 | 2C8 | |
| T2MOD* | Timer 2 mode control | 419 | — | — | RCLK1 | TCLK1 | — | — | T2OE | DCEN | 00 |
| TH2 | Timer 2 high byte | 459 | | | | | | | | | 00 |
| TL2 | Timer 2 low byte | 458 | | | | | | | | | 00 |
| T2CAPH | Timer 2 capture register, high byte | 45B | | | | | | | | | 00 |
| T2CAPL | Timer 2 capture register, low byte | 45A | | | | | | | | | 00 |
| | | | 287 | 286 | 285 | 284 | 283 | 282 | 281 | 280 | |
| TCON* | Timer 0 and 1 control register | 410 | TF1 | TR1 | TF0 | TR0 | IE1 | IT1 | IE0 | IT0 | 00 |
| TH0 | Timer 0 high byte | 451 | | | | | | | | | 00 |
| TH1 | Timer 1 high byte | 453 | | | | | | | | | 00 |
| TL0 | Timer 0 low byte | 450 | | | | | | | | | 00 |
| TL1 | Timer 1 low byte | 452 | | | | | | | | | 00 |
| TMOD | Timer 0 and 1 mode control | 45C | GATE | C/T | M1 | M0 | GATE | C/T | M1 | M0 | 00 |
| | | | 28F | 28E | 28D | 28C | 28B | 28A | 289 | 288 | |
| TSTAT* | Timer 0 and 1 extended status | 411 | — | — | — | — | — | T1OE | — | T0OE | 00 |
| | | | 2FF | 2FE | 2FD | 2FC | 2FB | 2FA | 2F9 | 2F8 | |
| WDCON* | Watchdog control register | 41F | PRE2 | PRE1 | PRE0 | — | — | WDRUN | WDTOF | — | Note 6 |
| WDL | Watchdog timer reload | 45F | | | | | | | | | 00 |
| WFEED1 | Watchdog feed 1 | 45D | | | | | | | | | x |
| WFEED2 | Watchdog feed 2 | 45E | | | | | | | | | x |

**NOTES:**

* SFRs are bit addressable.

1. At reset, the BCR register is loaded with the binary value 0000 0a11, where “a” is the value on the BUSW pin. This defaults the address bus size to 20 bits since the XA-G37 has only 20 address lines.
2. SFR is loaded from the reset vector.
3. All bits except F1, F0, and P are loaded from the reset vector. Those bits are all 0.
4. Unimplemented bits in SFRs are X (unknown) at all times. Ones should not be written to these bits since they may be used for other purposes in future XA derivatives. The reset value shown for these bits is 0.
5. Port configurations default to quasi-bidirectional when the XA begins execution from internal code memory after reset, based on the condition found on the EA pin. Thus all PnCFGA registers will contain FF and PnCFGB registers will contain 00. When the XA begins execution using external code memory, the default configuration for pins that are associated with the external bus will be push-pull. The PnCFGA and PnCFGB register contents will reflect this difference.
6. The WDCON reset value is E6 for a Watchdog reset, E4 for all other reset causes.
7. The XA-G37 implements an 8-bit SFR bus, as stated in Chapter 8 of the *XA User Guide*. All SFR accesses must be 8-bit operations. Attempts to write 16 bits to an SFR will actually write only the lower 8 bits. Sixteen bit SFR reads will return undefined data in the upper byte.

T2CON Address:418
Bit Addressable
Reset Value: 00H

| MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|
| TF2 | EXF2 | RCLK0 | TCLK0 | EXEN2 | TR2 | C2 or T2 | CP or RL2 |

| BIT | SYMBOL | FUNCTION |
|---|---|---|
| T2CON.7 | TF2 | Timer 2 overflow flag. Set by hardware on Timer/Counter overflow. Must be cleared by software. TF2 will not be set when RCLK0, RCLK1, TCLK0, TCLK1 or T2OE=1. |
| T2CON.6 | EXF2 | Timer 2 external flag is set when a capture or reload occurs due to a negative transition on T2EX (and EXEN2 is set). This flag will cause a Timer 2 interrupt when this interrupt is enabled. EXF2 is cleared by software. |
| T2CON.5 | RCLK0 | Receive Clock Flag. |
| T2CON.4 | TCLK0 | Transmit Clock Flag. RCLK0 and TCLK0 are used to select Timer 2 overflow rate as a clock source for UART0 instead of Timer T1. |
| T2CON.3 | EXEN2 | Timer 2 external enable bit allows a capture or reload to occur due to a negative transition on T2EX. |
| T2CON.2 | TR2 | Start=1/Stop=0 control for Timer 2. |
| T2CON.1 | C2 or T2 | Timer or counter select.<br>0=Internal timer<br>1=External event counter (falling edge triggered) |
| T2CON.0 | CP or RL2 | Capture/Reload flag.<br>If CP/RL2 & EXEN2=1 captures will occur on negative transitions of T2EX.<br>If CP/RL2=0, EXEN2=1 auto reloads occur with either Timer 2 overflows or negative transitions at T2EX.<br>If RCLK or TCLK=1 the timer is set to auto reload on Timer 2 overflow, this bit has no effect. |

SU00606

**Figure 4. Timer/Counter 2 Control (T2CON) Register**

## New Timer-Overflow Toggle Output

In the XA, the timer module now has two outputs, which toggle on overflow from the individual timers. The same device pins that are used for the T0 and T1 count inputs are also used for the new overflow outputs. An SFR bit (TnOE in the TSTAT register) is associated with each counter and indicates whether Port-SFR data or the overflow signal is output to the pin. These outputs could be used in applications for generating variable duty cycle PWM outputs (changing the auto-reload register values). Also variable frequency (Osc/8 to Osc/8,388,608) outputs could be achieved by adjusting the prescaler along with the auto-reload register values. With a 30.0MHz oscillator, this range would be 3.58Hz to 3.75MHz.

## Timer T2

Timer 2 in the XA is a 16-bit Timer/Counter which can operate as either a timer or as an event counter. This is selected by C/T2 in the special function register T2CON. Upon timer T2 overflow/underflow, the TF2 flag is set, which may be used to generate an interrupt. It can be operated in one of three operating modes: auto-reload (up or down counting), capture, or as the baud rate generator (for either or both UARTs via SFRs T2MOD and T2CON). These modes are shown in Table 1.

### Capture Mode

In the capture mode there are two options which are selected by bit EXEN2 in T2CON. If EXEN2 = 0, then timer 2 is a 16-bit timer or counter, which upon overflowing sets bit TF2, the timer 2 overflow bit. This will cause an interrupt when the timer 2 interrupt is enabled.

If EXEN2 = 1, then Timer 2 still does the above, but with the added feature that a 1-to-0 transition at external input T2EX causes the current value in the Timer 2 registers, TL2 and TH2, to be captured into registers RCAP2L and RCAP2H, respectively. In addition, the transition at T2EX causes bit EXF2 in T2CON to be set. This will cause an interrupt in the same fashion as TF2 when the Timer 2 interrupt is enabled. The capture mode is illustrated in Figure 7.

### Auto-Reload Mode (Up or Down Counter)

In the auto-reload mode, the timer registers are loaded with the 16-bit value in T2CAPH and T2CAPL when the count overflows. T2CAPH and T2CAPL are initialized by software. If the EXEN2 bit in T2CON is set, the timer registers will also be reloaded and the EXF2 flag set when a 1-to-0 transition occurs at input T2EX. The auto-reload mode is shown in Figure 8.

In this mode, Timer 2 can be configured to count up or down. This is done by setting or clearing the bit DCEN (Down Counter Enable) in the T2MOD special function register (see Table 1). The T2EX pin then controls the count direction. When T2EX is high, the count is in the up direction, when T2EX is low, the count is in the down direction.

Figure 8 shows Timer 2, which will count up automatically, since DCEN = 0. In this mode there are two options selected by bit EXEN2 in the T2CON register. If EXEN2 = 0, then Timer 2 counts up to FFFFH and sets the TF2 (Overflow Flag) bit upon overflow. This causes the Timer 2 registers to be reloaded with the 16-bit value in T2CAPL and T2CAPH, whose values are preset by software. If EXEN2 = 1, a 16-bit reload can be triggered either by an overflow or by a 1-to-0 transition at input T2EX. This transition also sets the EXF2 bit. If enabled, either TF2 or EXF2 bit can generate the Timer 2 interrupt.

In Figure 9, the DCEN = 1; this enables the Timer 2 to count up or down. In this mode, the logic level of T2EX pin controls the direction of count. When a logic ‘1’ is applied at pin T2EX, the Timer 2 will count up. The Timer 2 will overflow at FFFFH and set the TF2 flag, which can then generate an interrupt if enabled. This timer overflow, also causes the 16-bit value in T2CAPL and T2CAPH to be reloaded into the timer registers TL2 and TH2, respectively.

A logic ‘0’ at pin T2EX causes Timer 2 to count down. When counting down, the timer value is compared to the 16-bit value contained in T2CAPH and T2CAPL. When the value is equal, the

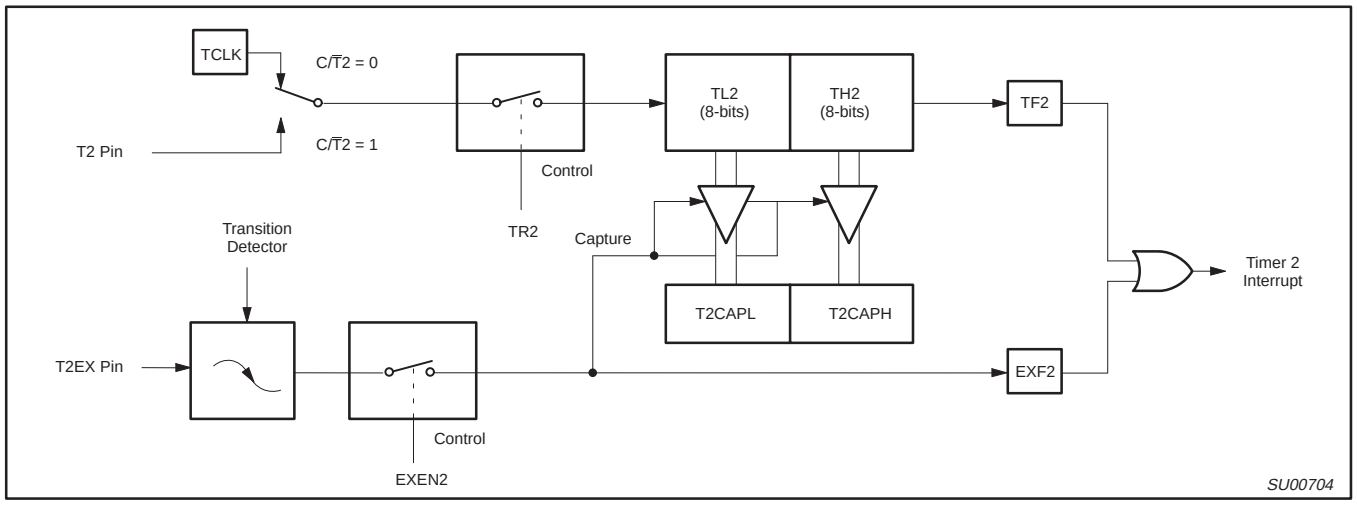



**Figure 7. Timer 2 in Capture Mode**

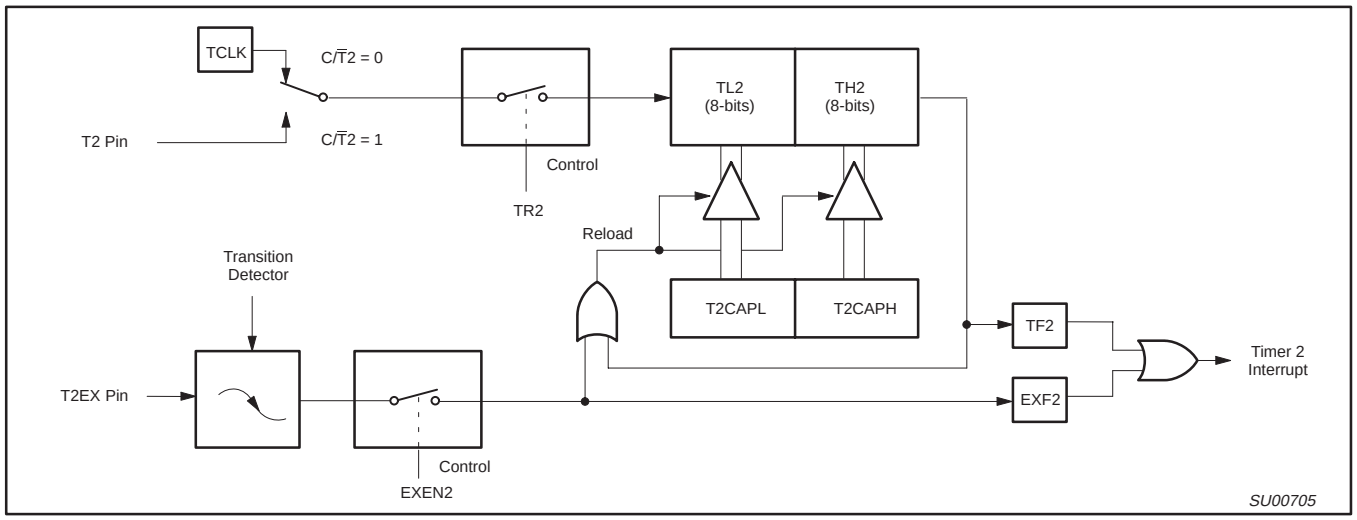



**Figure 8. Timer 2 in Auto-Reload Mode (DCEN = 0)**

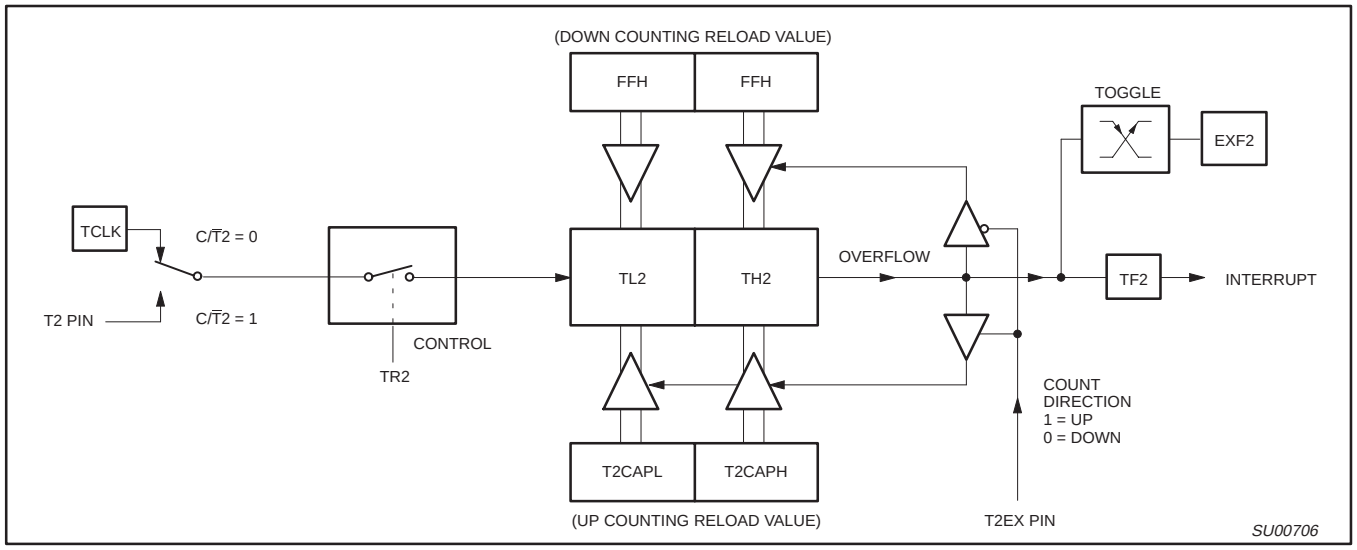



**Figure 9. Timer 2 Auto Reload Mode (DCEN = 1)**

## CLOCKING SCHEME/BAUD RATE GENERATION

The XA UARTS clock rates are determined by either a fixed division (modes 0 and 2) of the oscillator clock or by the Timer 1 or Timer 2 overflow rate (modes 1 and 3).

The clock for the UARTs in XA runs at 16x the Baud rate. If the timers are used as the source for Baud Clock, since maximum speed of timers/Baud Clock is Osc/4, the maximum baud rate is timer overflow divided by 16 i.e. Osc/64.

In Mode 0, it is fixed at Osc/16. In Mode 2, however, the fixed rate is Osc/32.

| | | |
|---|---|---|
| Pre-scaler for all Timers T0,1,2 controlled by PT1, PT0 bits in SCR | 00 | Osc/4 |
| | 01 | Osc/16 |
| | 10 | Osc/64 |
| | 11 | reserved |

**Baud Rate for UART Mode 0:**

Baud_Rate = Osc/16

**Baud Rate calculation for UART Mode 1 and 3:**

Baud_Rate = Timer_Rate/16

Timer_Rate = Osc/(N*(Timer_Range– Timer_Reload_Value))

where N = the TCLK prescaler value: 4, 16, or 64.
and Timer_Range = 256 for timer 1 in mode 2.
65536 for timer 1 in mode 0 and timer 2 in count up mode.

The timer reload value may be calculated as follows:

Timer_Reload_Value = Timer_Range–(Osc/(Baud_Rate*N*16))

**NOTES:**

1. The maximum baud rate for a UART in mode 1 or 3 is Osc/64.
2. The lowest possible baud rate (for a given oscillator frequency and N value) may be found by using a timer reload value of 0.
3. The timer reload value may never be larger than the timer range.
4. If a timer reload value calculation gives a negative or fractional result, the baud rate requested is not possible at the given oscillator frequency and N value.

**Baud Rate for UART Mode 2:**

Baud_Rate = Osc/32

### Using Timer 2 to Generate Baud Rates

Timer T2 is a 16-bit up/down counter in XA. As a baud rate generator, timer 2 is selected as a clock source for either/both UART0 and UART1 transmitters and/or receivers by setting TCLKn and/or RCLKn in T2CON and T2MOD. As the baud rate generator, T2 is incremented as Osc/N where N = 4, 16 or 64 depending on TCLK as programmed in the SCR bits PT1, and PTO. So, if T2 is the source of one UART, the other UART could be clocked by either T1 overflow or fixed clock, and the UARTs could run independently with different baud rates.

| | | | | |
|---|---|---|---|---|
| T2CON 0x418 | | bit5 | bit4 | |
| | | RCLK0 | TCLK0 | |

| | | | | |
|---|---|---|---|---|
| T2MOD 0x419 | | bit5 | bit4 | |
| | | RCLK1 | TCLK1 | |

**Prescaler Select for Timer Clock (TCLK)**

| | | | | |
|---|---|---|---|---|
| SCR 0x440 | | bit3 | bit2 | |
| | | PT1 | PT0 | |

SnSTAT Address: S0STAT 421
S1STAT 425

Bit Addressable
Reset Value: 00H

| MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|
| — | — | — | — | FEn | BRn | OEn | STINTn |

| BIT | SYMBOL | FUNCTION |
|---|---|---|
| SnSTAT.3 | FEn | Framing Error flag is set when the receiver fails to see a valid STOP bit at the end of the frame. Cleared by software. |
| SnSTAT.2 | BRn | Break Detect flag is set if a character is received with all bits (including STOP bit) being logic ‘0’. Thus it gives a “Start of Break Detect” on bit 8 for Mode 1 and bit 9 for Modes 2 and 3. The break detect feature operates independently of the UARTs and provides the START of Break Detect status bit that a user program may poll. Cleared by software. |
| SnSTAT.1 | OEn | Overrun Error flag is set if a new character is received in the receiver buffer while it is still full (before the software has read the previous character from the buffer), i.e., when bit 8 of a new byte is received while RI in SnCON is still set. Cleared by software. |
| SnSTAT.0 | STINTn | This flag must be set to enable any of the above status flags to generate a receive interrupt (RIn). The only way it can be cleared is by a software write to this register. |

SU00607B

**Figure 11. Serial Port Extended Status (SnSTAT) Register (See also Figure 13 regarding Framing Error flag)**

## UART INTERRUPT SCHEME

There are separate interrupt vectors for each UART's transmit and receive functions.

### Table 3. Vector Locations for UARTs in XA

| Vector Address | Interrupt Source | Arbitration |
|---|---|---|
| A0H – A3H | UART 0 Receiver | 7 |
| A4H – A7H | UART 0 Transmitter | 8 |
| A8H – ABH | UART 1 Receiver | 9 |
| ACH – AFH | UART 1 Transmitter | 10 |

**NOTE:**
The transmit and receive vectors could contain the same ISR address to work like a 8051 interrupt scheme

**Error Handling, Status Flags and Break Detect**
The UARTs in XA has the following error flags; see Figure 11.

## Multiprocessor Communications

Modes 2 and 3 have a special provision for multiprocessor communications. In these modes, 9 data bits are received. The 9th one goes into RB8. Then comes a stop bit. The port can be programmed such that when the stop bit is received, the serial port interrupt will be activated only if RB8 = 1. This feature is enabled by setting bit SM2 in SCON. A way to use this feature in multiprocessor systems is as follows:

When the master processor wants to transmit a block of data to one of several slaves, it first sends out an address byte which identifies the target slave. An address byte differs from a data byte in that the 9th bit is 1 in an address byte and 0 in a data byte. With SM2 = 1, no slave will be interrupted by a data byte. An address byte, however, will interrupt all slaves, so that each slave can examine the received byte and see if it is being addressed. The addressed slave will clear its SM2 bit and prepare to receive the data bytes that will be coming. The slaves that weren't being addressed leave their SM2s set and go on about their business, ignoring the coming data bytes.

SM2 has no effect in Mode 0, and in Mode 1 can be used to check the validity of the stop bit although this is better done with the Framing Error (FE) flag. In a Mode 1 reception, if SM2 = 1, the receive interrupt will not be activated unless a valid stop bit is received.

**Automatic Address Recognition**
Automatic Address Recognition is a feature which allows the UART to recognize certain addresses in the serial bit stream by using hardware to make the comparisons. This feature saves a great deal of software overhead by eliminating the need for the software to examine every serial address which passes by the serial port. This feature is enabled by setting the SM2 bit in SCON. In the 9 bit UART modes, mode 2 and mode 3, the Receive Interrupt flag (RI) will be automatically set when the received byte contains either the "Given" address or the "Broadcast" address. The 9 bit mode requires that the 9th information bit is a 1 to indicate that the received information is an address and not data. Automatic address recognition is shown in Figure 14.

Using the Automatic Address Recognition feature allows a master to selectively communicate with one or more slaves by invoking the Given slave address or addresses. All of the slaves may be contacted by using the Broadcast address. Two special Function Registers are used to define the slave's address, SADDR, and the address mask, SADEN. SADEN is used to define which bits in the SADDR are to be used and which bits are "don't care". The SADEN mask can be logically ANDed with the SADDR to create the "Given" address which the master will use for addressing each of the slaves. Use of the Given address allows multiple slaves to be recognized while excluding others. The following examples will help to show the versatility of this scheme:

| | | | |
|---|---|---|---|
| Slave 0 | SADDR | = | 1100 0000 |
| | SADEN | = | 1111 1101 |
| | Given | = | 1100 00X0 |
| Slave 1 | SADDR | = | 1100 0000 |
| | SADEN | = | 1111 1110 |
| | Given | = | 1100 000X |

In the above example SADDR is the same and the SADEN data is used to differentiate between the two slaves. Slave 0 requires a 0 in bit 0 and it ignores bit 1. Slave 1 requires a 0 in bit 1 and bit 0 is ignored. A unique address for Slave 0 would be 1100 0010 since slave 1 requires a 0 in bit 1. A unique address for slave 1 would be 1100 0001 since a 1 in bit 0 will exclude slave 0. Both slaves can be selected at the same time by an address which has bit 0 = 0 (for slave 0) and bit 1 = 0 (for slave 1). Thus, both could be addressed with 1100 0000.

In a more complex system the following could be used to select slaves 1 and 2 while excluding slave 0:

| | | | |
|---|---|---|---|
| Slave 0 | SADDR | = | 1100 0000 |
| | SADEN | = | 1111 1001 |
| | Given | = | 1100 0XX0 |
| Slave 1 | SADDR | = | 1110 0000 |
| | SADEN | = | 1111 1010 |
| | Given | = | 1110 0X0X |
| Slave 2 | SADDR | = | 1110 0000 |
| | SADEN | = | 1111 1100 |
| | Given | = | 1110 00XX |

In the above example the differentiation among the 3 slaves is in the lower 3 address bits. Slave 0 requires that bit 0 = 0 and it can be uniquely addressed by 1110 0110. Slave 1 requires that bit 1 = 0 and it can be uniquely addressed by 1110 and 0101. Slave 2 requires that bit 2 = 0 and its unique address is 1110 0011. To select Slaves 0 and 1 and exclude Slave 2 use address 1110 0100, since it is necessary to make bit 2 = 1 to exclude slave 2.

The Broadcast Address for each slave is created by taking the logical OR of SADDR and SADEN. Zeros in this result are teated as don't-cares. In most cases, interpreting the don't-cares as ones, the broadcast address will be FF hexadecimal.

Upon reset SADDR and SADEN are loaded with 0s. This produces a given address of all "don't cares" as well as a Broadcast address of all "don't cares". This effectively disables the Automatic Addressing mode and allows the microcontroller to use standard UART drivers which do not make use of this feature.

## ABSOLUTE MAXIMUM RATINGS

| PARAMETER | RATING | UNIT |
|---|---|---|
| Operating temperature under bias | –55 to +125 | °C |
| Storage temperature range | –65 to +150 | °C |
| Voltage on $\overline{EA}/V_{PP}$ pin to $V_{SS}$ | 0 to +13.0 | V |
| Voltage on any other pin to $V_{SS}$ | –0.5 to $V_{DD}$+0.5 V | V |
| Maximum $I_{OL}$ per I/O pin | 15 | mA |
| Power dissipation (based on package heat transfer limitations, not device power consumption) | 1.5 | W |

## DC ELECTRICAL CHARACTERISTICS

$V_{DD}$ = 2.7 V to 5.5 V unless otherwise specified; $V_{DD}$ = $T_{amb}$ = 0 to 70 °C for commercial, –40 °C to +85 °C for industrial, unless otherwise specified.

| SYMBOL | PARAMETER | TEST CONDITIONS | LIMITS | | | UNIT |
|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | |
| **Supplies** | | | | | | |
| $I_{DD}$ | Supply current operating[9,10] | $f_{osc}$ = 30 MHz | – | 60 | 80 | mA |
| $I_{ID}$ | Idle mode supply current[9,10] | $f_{osc}$ = 30 MHz | – | 22 | 30 | mA |
| $I_{PD}$ | Power-down current | – | – | 15 | 100 | µA |
| $I_{PDI}$ | Power-down current (–40°C to +85°C) | – | – | | 150 | µA |
| $V_{RAM}$ | RAM-keep-alive voltage | RAM-keep-alive voltage | 1.5 | | – | V |
| $V_{IL}$ | Input low voltage | – | –0.5 | | 0.22 $V_{DD}$ | V |
| $V_{IH}$ | Input high voltage, except XTAL1, RST | At 5.0 V | 2.2 | | – | V |
| | | At 3.3 V | 2 | | – | V |
| $V_{IH1}$ | Input high voltage to XTAL1, RST | For both 3.0 & 5.0 V | 0.7 $V_{DD}$ | | – | V |
| $V_{OL}$ | Output low voltage all ports, ALE, PSEN[3] | $I_{OL}$ = 3.2mA, $V_{DD}$ = 5.0 V | – | | 0.5 | V |
| | | 1.0mA, $V_{DD}$ = 3.0 V | – | | 0.4 | V |
| $V_{OH1}$ | Output high voltage all ports, ALE, PSEN[1] | $I_{OH}$ = –100µA, $V_{DD}$ = 4.5 V | 2.4 | | – | V |
| | | $I_{OH}$ = –15µA, $V_{DD}$ = 2.7 V | 2.0 | | – | V |
| $V_{OH2}$ | Output high voltage, ports P0–3, ALE, PSEN[2] | $I_{OH}$ = 3.2mA, $V_{DD}$ = 4.5 V | 2.4 | | – | V |
| | | $I_{OH}$ = 1mA, $V_{DD}$ = 2.7 V | 2.2 | | – | V |
| $C_{IO}$ | Input/Output pin capacitance | – | – | | 15 | pF |
| $I_{IL}$ | Logical 0 input current, P0–3[6] | $V_{IN}$ = 0.45 V | – | –25 | –75 | µA |
| $I_{LI}$ | Input leakage current, P0–3[5] | $V_{IN}$ = $V_{IL}$ or $V_{IH}$ | – | | ±10 | µA |
| $I_{TL}$ | Logical 1 to 0 transition current all ports[4] | At 5.5 V | – | | –650 | µA |

**NOTES:**
1. Ports in Quasi bi-directional mode with weak pull-up (applies to ALE, $\overline{PSEN}$ only during RESET).
2. Ports in Push-Pull mode, both pull-up and pull-down assumed to be same strength
3. In all output modes
4. Port pins source a transition current when used in quasi-bidirectional mode and externally driven from 1 to 0. This current is highest when $V_{IN}$ is approximately 2 V.
5. Measured with port in high impedance output mode.
6. Measured with port in quasi-bidirectional output mode.
7. Load capacitance for all outputs=80 pF.
8. Under steady state (non-transient) conditions, $I_{OL}$ must be externally limited as follows:
   Maximum $I_{OL}$ per port pin: 15 mA (*NOTE: This is 85°C specification for $V_{DD}$ = 5 V.)
   Maximum $I_{OL}$ per 8-bit port: 26 mA
   Maximum total $I_{OL}$ for all output: 71 mA
   If $I_{OL}$ exceeds the test condition, $V_{OL}$ may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
9. See Figures 25, 26, 29, and 30 for $I_{DD}$ test conditions, and Figures 27 and 28 for $I_{CC}$ vs. Frequency.
   Max. 5 V Active $I_{DD}$ = (fosc * 1.77 mA) + 7 mA
   Max. 5 V Idle $I_{DD}$ = (fosc * 0.87 mA) + 4 mA
   Max. 3 V Active $I_{DD}$ = (fosc * 0.77 mA) + 7 mA
   Max. 3 V Idle $I_{DD}$ = (fosc * 0.54 mA) + 4 mA
10. $V_{DDMIN}$ = 2.85 V for operating at $f_{OSC}$ = 30 MHz and –40 °C to +85 °C

## AC ELECTRICAL CHARACTERISTICS ($V_{DD}$ = 2.7 V TO 4.5 V)

$T_{amb}$ = 0 to +70 °C for commercial, –40 °C to +85 °C for industrial.

| SYMBOL | FIGURE | PARAMETER | VARIABLE CLOCK | | UNIT |
|---|---|---|---|---|---|
| | | | MIN | MAX | |
| **Address Cycle** | | | | | |
| $t_{CRAR}$ | 21 | Delay from clock rising edge to ALE rising edge | 15 | 60 | ns |
| $t_{LHLL}$ | 16 | ALE pulse width (programmable) | (V1 * $t_C$) – 10 | | ns |
| $t_{AVLL}$ | 16 | Address valid to ALE de-asserted (set-up) | (V1 * $t_C$) – 18 | | ns |
| $t_{LLAX}$ | 16 | Address hold after ALE de-asserted | ($t_C$/2) – 12 | | ns |
| **Code Read Cycle** | | | | | |
| $t_{PLPH}$ | 16 | $\overline{PSEN}$ pulse width | (V2 * $t_C$) – 12 | | ns |
| $t_{LLPL}$ | 16 | ALE de-asserted to $\overline{PSEN}$ asserted | ($t_C$/2) – 9 | | ns |
| $t_{AVIVA}$ | 16 | Address valid to instruction valid, ALE cycle (access time) | | (V3 * $t_C$) – 58 | ns |
| $t_{AVIVB}$ | 17 | Address valid to instruction valid, non-ALE cycle (access time) | | (V4 * $t_C$) – 52 | ns |
| $t_{PLIV}$ | 16 | $\overline{PSEN}$ asserted to instruction valid (enable time) | | (V2 * $t_C$) – 52 | ns |
| $t_{PXIX}$ | 16 | Instruction hold after $\overline{PSEN}$ de-asserted | 0 | | ns |
| $t_{PXIZ}$ | 16 | Bus 3-State after $\overline{PSEN}$ de-asserted (disable time) | | $t_C$ – 8 | ns |
| $t_{IXUA}$ | 16 | Hold time of unlatched part of address after instruction latched | 0 | | ns |
| **Data Read Cycle** | | | | | |
| $t_{RLRH}$ | 18 | $\overline{RD}$ pulse width | (V7 * $t_C$) – 12 | | ns |
| $t_{LLRL}$ | 18 | ALE de-asserted to $\overline{RD}$ asserted | ($t_C$/2) – 9 | | ns |
| $t_{AVDVA}$ | 18 | Address valid to data input valid, ALE cycle (access time) | | (V6 * $t_C$) – 58 | ns |
| $t_{AVDVB}$ | 19 | Address valid to data input valid, non-ALE cycle (access time) | | (V5 * $t_C$) – 52 | ns |
| $t_{RLDV}$ | 18 | $\overline{RD}$ low to valid data in, enable time | | (V7 * $t_C$) – 52 | ns |
| $t_{RHDX}$ | 18 | Data hold time after $\overline{RD}$ de-asserted | 0 | | ns |
| $t_{RHDZ}$ | 18 | Bus 3-State after $\overline{RD}$ de-asserted (disable time) | | $t_C$ – 8 | ns |
| $t_{DXUA}$ | 18 | Hold time of unlatched part of address after data latched | 0 | | ns |
| **Data Write Cycle** | | | | | |
| $t_{WLWH}$ | 20 | $\overline{WR}$ pulse width | (V8 * $t_C$) – 12 | | ns |
| $t_{LLWL}$ | 20 | ALE falling edge to $\overline{WR}$ asserted | (V12 * $t_C$) – 10 | | ns |
| $t_{QVWX}$ | 20 | Data valid before $\overline{WR}$ asserted (data setup time) | (V13 * $t_C$) – 28 | | ns |
| $t_{WHQX}$ | 20 | Data hold time after $\overline{WR}$ de-asserted (Note 6) | (V11 * $t_C$) – 8 | | ns |
| $t_{AVWL}$ | 20 | Address valid to $\overline{WR}$ asserted (address setup time) (Note 5) | (V9 * $t_C$) – 28 | | ns |
| $t_{UAWH}$ | 20 | Hold time of unlatched part of address after $\overline{WR}$ is de-asserted | (V11 * $t_C$) – 10 | | ns |
| **Wait Input** | | | | | |
| $t_{WTH}$ | 21 | WAIT stable after bus strobe ($\overline{RD}$, $\overline{WR}$, or $\overline{PSEN}$) asserted | | (V10 * $t_C$) – 40 | ns |
| $t_{WTL}$ | 21 | WAIT hold after bus strobe ($\overline{RD}$, $\overline{WR}$, or $\overline{PSEN}$) assertion | (V10 * $t_C$) – 5 | | ns |

**NOTES:**

1. Load capacitance for all outputs = 80 pF.
2. Variables V1 through V13 reflect programmable bus timing, which is programmed via the Bus Timing registers (BTRH and BTRL). Refer to the *XA User Guide* for details of the bus timing settings.
   - V1) This variable represents the programmed width of the ALE pulse as determined by the ALEW bit in the BTRL register. V1 = 0.5 if the ALEW bit = 0, and 1.5 if the ALEW bit = 1.
   - V2) This variable represents the programmed width of the $\overline{PSEN}$ pulse as determined by the CR1 and CR0 bits or the CRA1, CRA0, and ALEW bits in the BTRL register.
     - For a bus cycle with **no** ALE, V2 = 1 if CR1/0 = 00, 2 if CR1/0 = 01, 3 if CR1/0 = 10, and 4 if CR1/0 = 11. Note that during burst mode code fetches, $\overline{PSEN}$ does not exhibit transitions at the boundaries of bus cycles. V2 still applies for the purpose of determining peripheral timing requirements.
     - For a bus cycle **with** an ALE, V2 = the total bus cycle duration (2 if CRA1/0 = 00, 3 if CRA1/0 = 01, 4 if CRA1/0 = 10, and 5 if CRA1/0 = 11) minus the number of clocks used by ALE (V1 + 0.5).
       Example: If CRA1/0 = 10 and ALEW = 1, the V2 = 4 – (1.5 + 0.5) = 2.

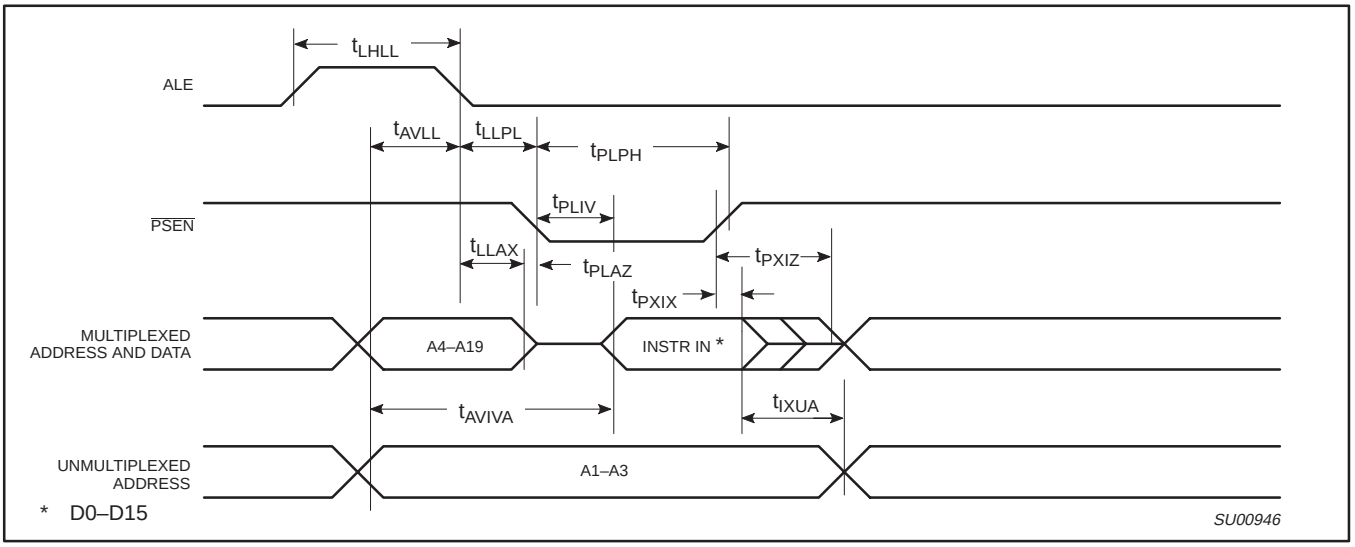



**Figure 16. External Program Memory Read Cycle (ALE Cycle)**

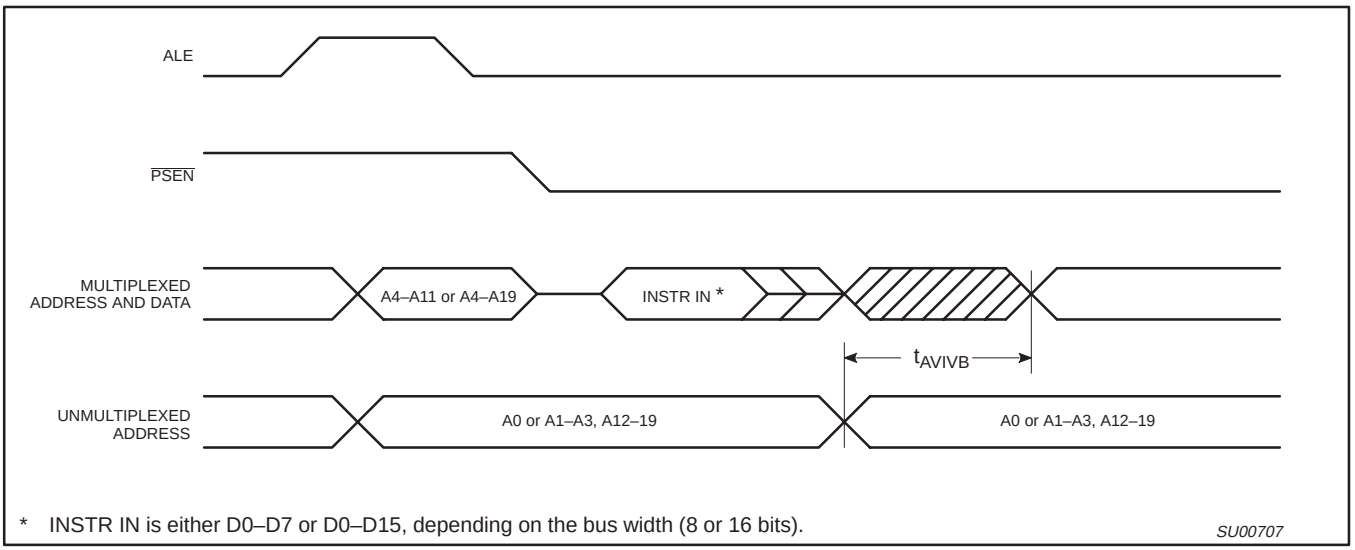



**Figure 17. External Program Memory Read Cycle (Non-ALE Cycle)**

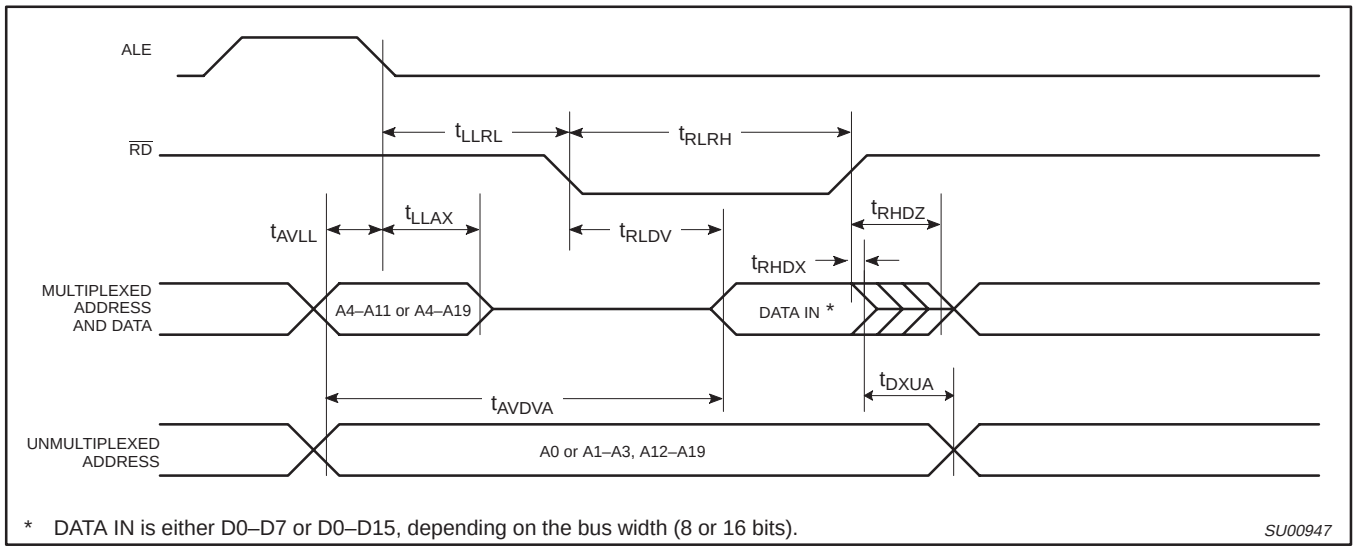



**Figure 18. External Data Memory Read Cycle (ALE Cycle)**

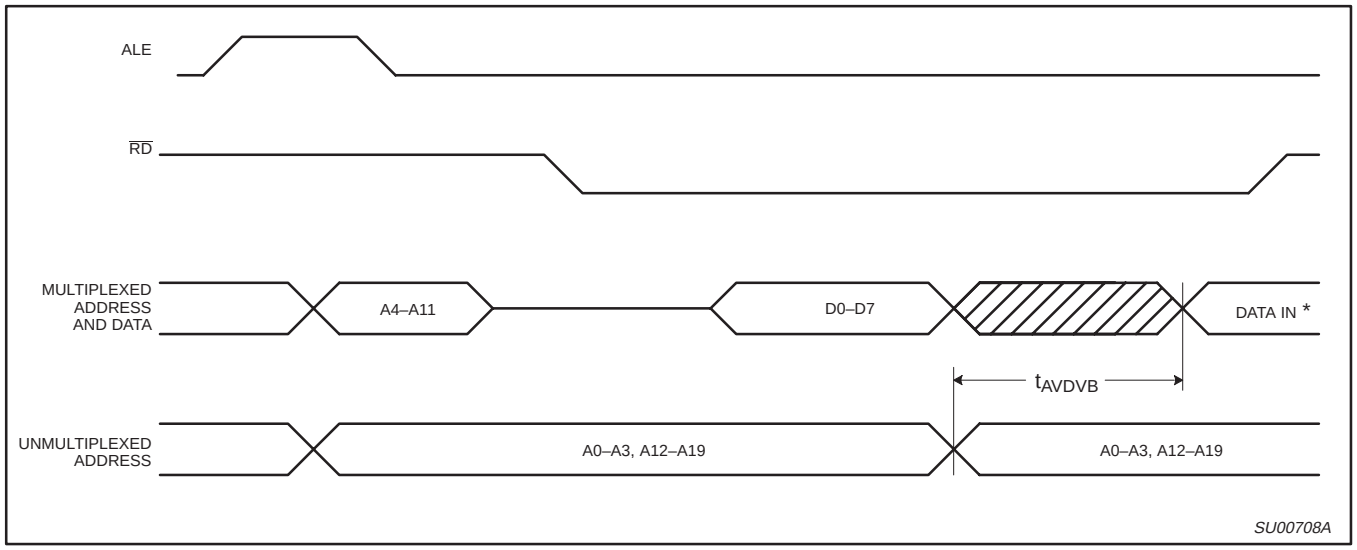



**Figure 19. External Data Memory Read Cycle (Non-ALE Cycle) 8 Bit Bus Only**

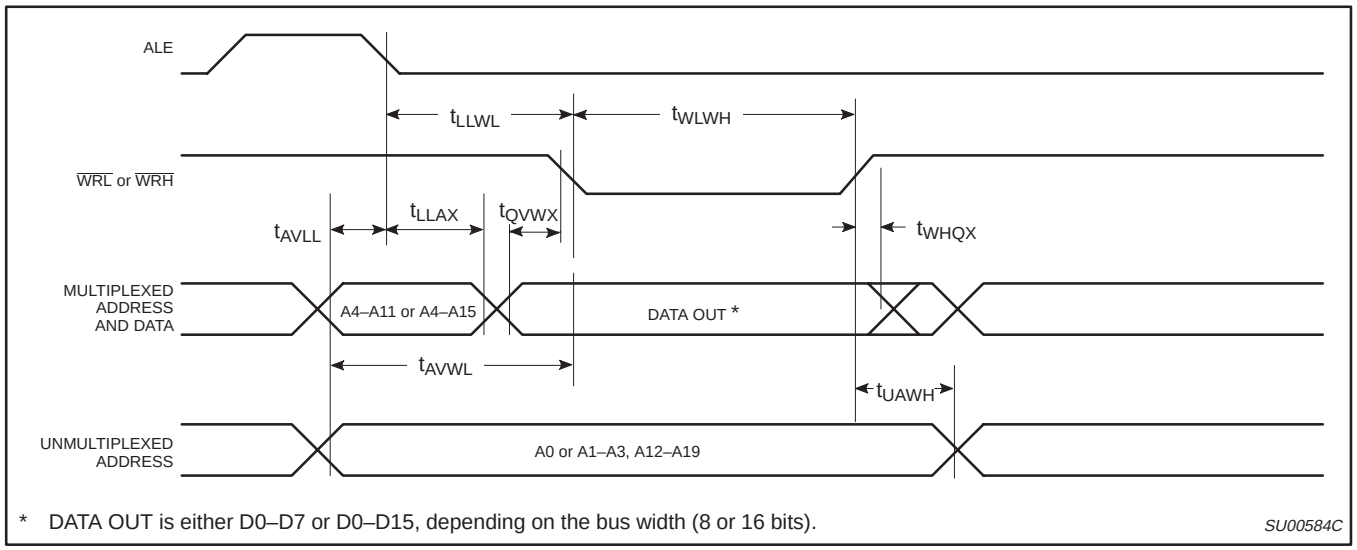



**Figure 20. External Data Memory Write Cycle**

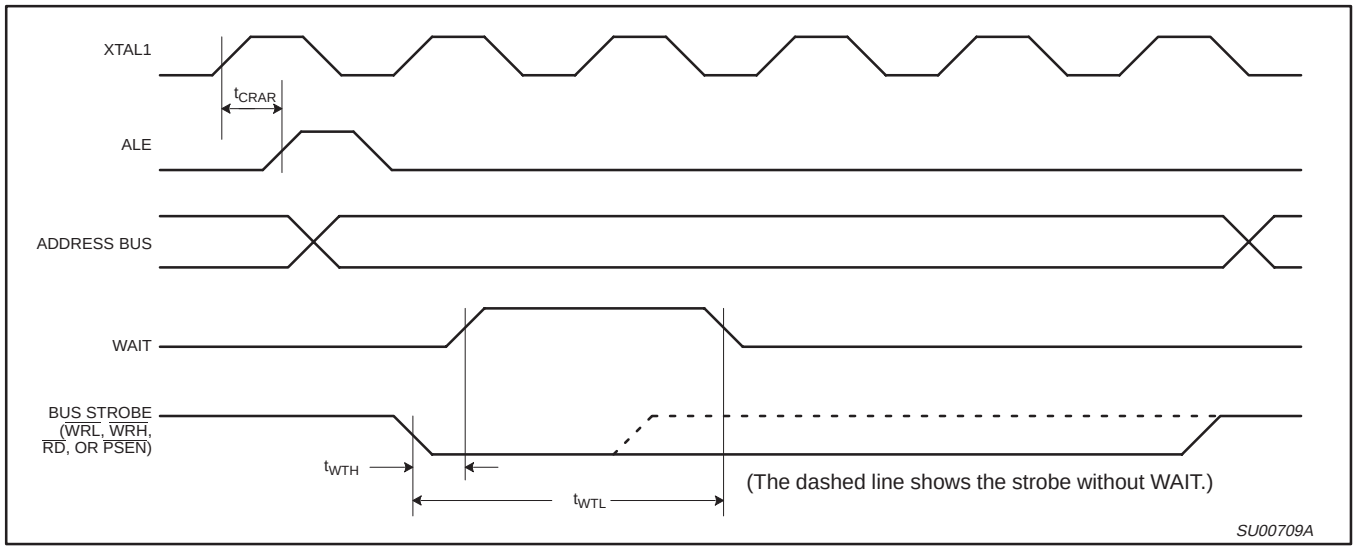



**Figure 21. WAIT Signal Timing**

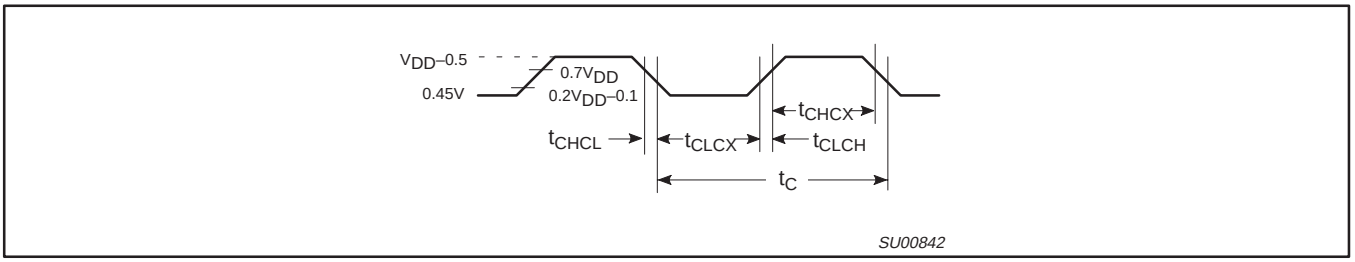



**Figure 22. External Clock Drive**

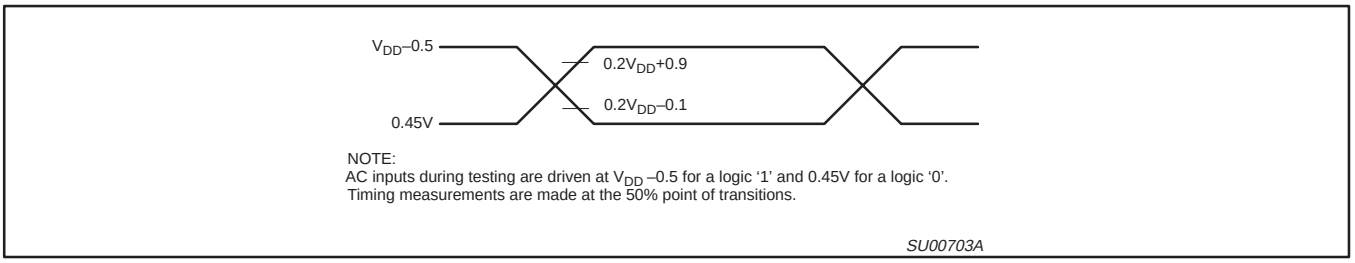



**Figure 23. AC Testing Input/Output**

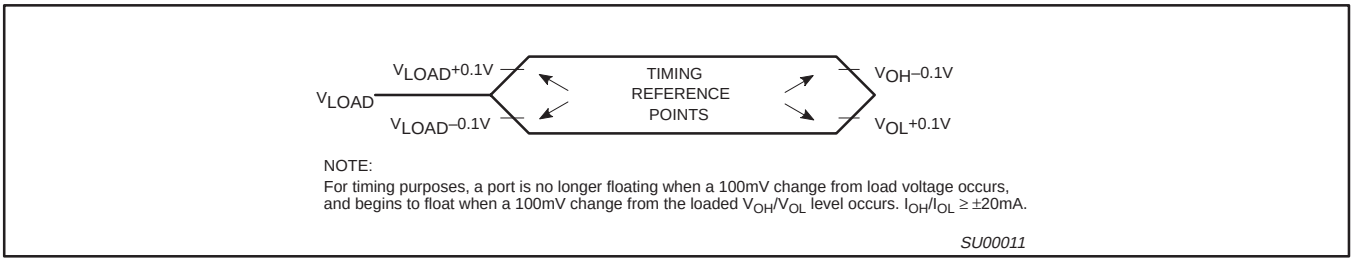



**Figure 24. Float Waveform**

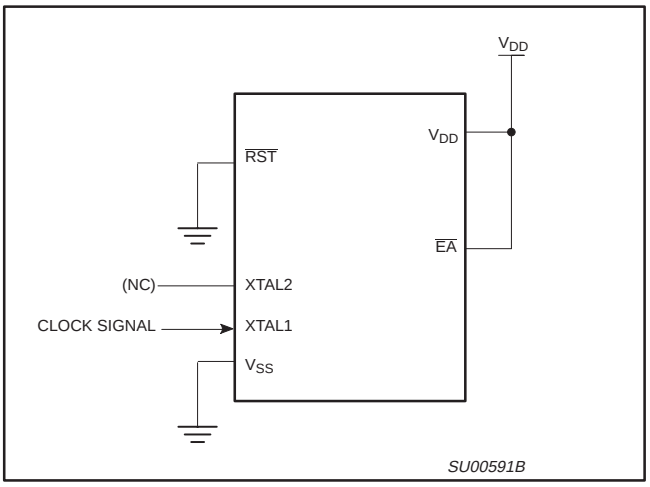



**Figure 25. $I_{DD}$ Test Condition, Active Mode**
**All other pins are disconnected**

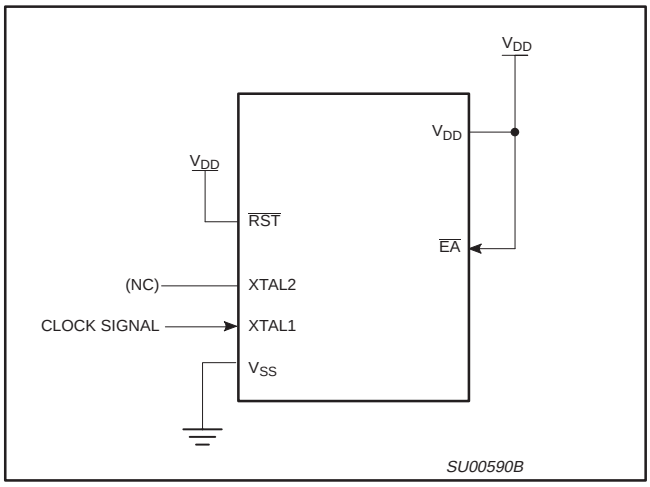



**Figure 26. $I_{DD}$ Test Condition, Idle Mode**
**All other pins are disconnected**

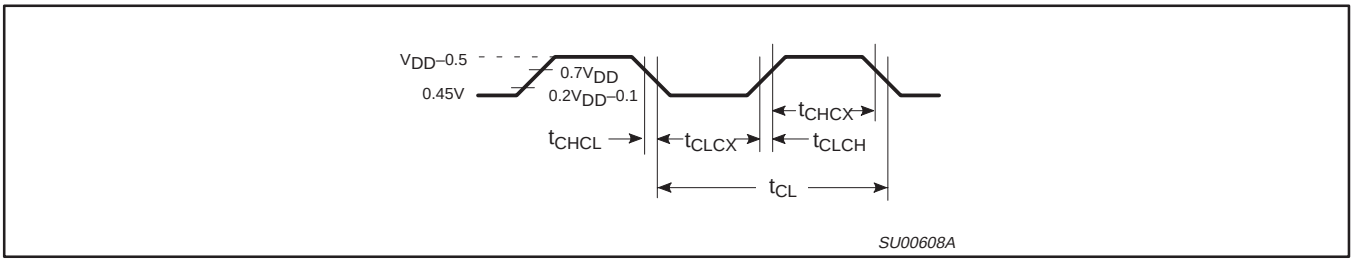



**Figure 29. Clock Signal Waveform for $I_{DD}$ Tests in Active and Idle Modes**
**$t_{CLCH} = t_{CHCL} = 5$ns**

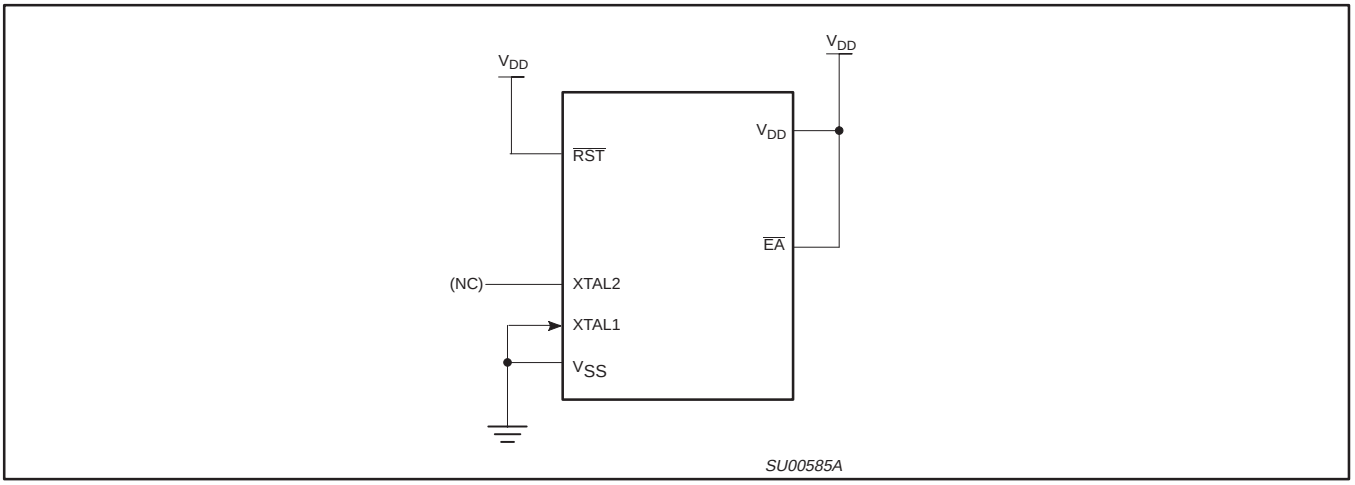



**Figure 30. $I_{DD}$ Test Condition, Power Down Mode**
**All other pins are disconnected. $V_{DD}$=2 V to 5.5 V**

## EPROM CHARACTERISTICS

The XA-G37 is programmed by using a modified Improved Quick-Pulse Programming™ algorithm. This algorithm is essentially the same as that used by the later 80C51 family EPROM parts. However different pins are used for many programming functions.

Detailed EPROM programming information may be obtained from the internet at www.philipsmcu.com/ftp.html.

The XA-G37 contains three signature bytes that can be read and used by an EPROM programming system to identify the device. The signature bytes identify the device as an XA-Gx manufactured by Philips.

### Security Bits

With none of the security bits programmed the code in the program memory can be verified. When only security bit 1 (see Table 6) is programmed, MOVC instructions executed from external program memory are disabled from fetching code bytes from the internal memory. All further programming of the EPROM is disabled. When security bits 1 and 2 are programmed, in addition to the above, verify mode is disabled. When all three security bits are programmed, all of the conditions above apply and all external program memory execution is disabled. (See Table 6)

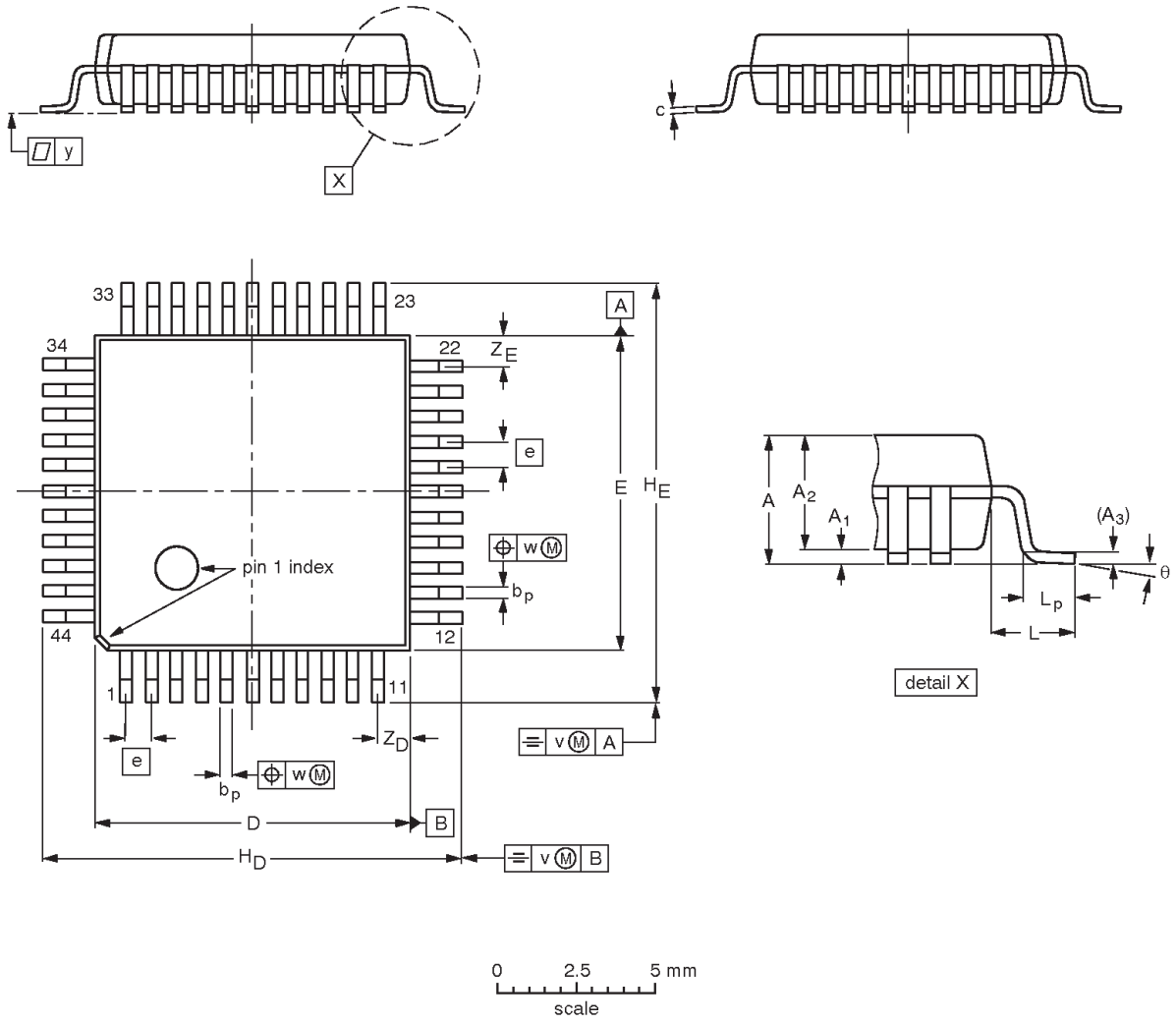
**Table 6. Program Security Bits**

| PROGRAM LOCK BITS | | | | |
|---|---|---|---|---|
| | SB1 | SB2 | SB3 | PROTECTION DESCRIPTION |
| 1 | U | U | U | No Program Security features enabled. |
| 2 | P | U | U | MOVC instructions executed from external program memory are disabled from fetching code bytes from internal memory and further programming of the EPROM is disabled. |
| 3 | P | P | U | Same as 2, also verify is disabled. |
| 4 | P | P | P | Same as 3, external execution is disabled. Internal data RAM is not accessible. |

**NOTES:**
1. P – programmed. U – unprogrammed.
2. Any other combination of the security bits is not defined.

™Trademark phrase of Intel Corporation.

**LQFP44: plastic low profile quad flat package; 44 leads; body 10 x 10 x 1.4 mm** **SOT389-1**




**DIMENSIONS (mm are the original dimensions)**

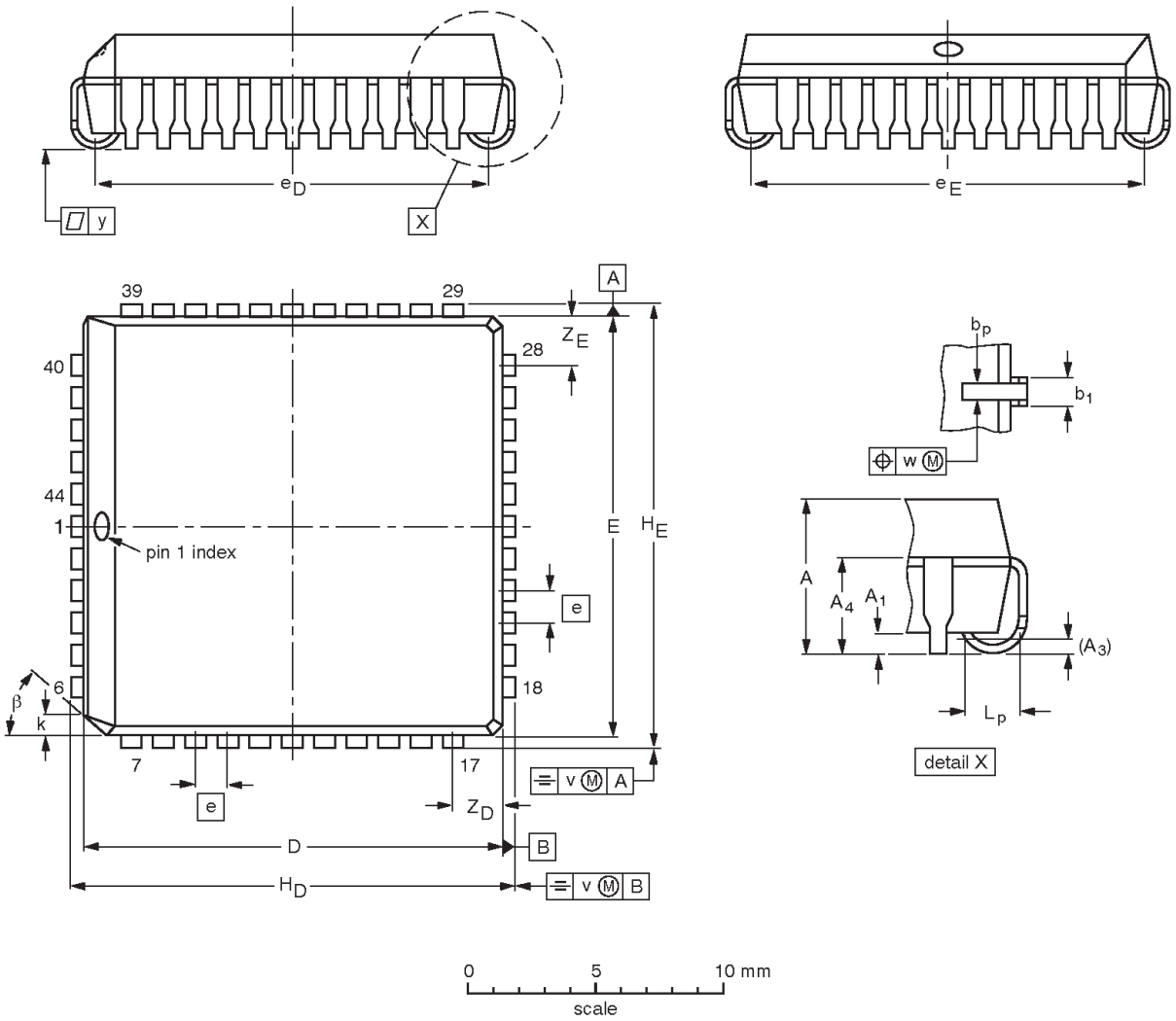
| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | $D^{(1)}$ | $E^{(1)}$ | e | $H_D$ | $H_E$ | L | $L_p$ | v | w | y | $Z_D^{(1)}$ | $Z_E^{(1)}$ | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.60 | 0.15<br>0.05 | 1.45<br>1.35 | 0.25 | 0.45<br>0.30 | 0.20<br>0.12 | 10.10<br>9.90 | 10.10<br>9.90 | 0.80 | 12.15<br>11.85 | 12.15<br>11.85 | 1.0 | 0.75<br>0.45 | 0.20 | 0.20 | 0.10 | 1.14<br>0.85 | 1.14<br>0.85 | $7^o$<br>$0^o$ |

**Note**

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | EIAJ | | | |
| SOT389-1 | 136E08 | MS-026 | | | | ~~99-12-17~~<br>00-01-19 |

**PLCC44: plastic leaded chip carrier; 44 leads** **SOT187-2**




**DIMENSIONS (mm dimensions are derived from the original inch dimensions)**

| UNIT | A | $A_1$ min. | $A_3$ | $A_4$ max. | $b_p$ | $b_1$ | $D^{(1)}$ | $E^{(1)}$ | e | $e_D$ | $e_E$ | $H_D$ | $H_E$ | k | $L_p$ | v | w | y | $Z_D^{(1)}$ max. | $Z_E^{(1)}$ max. | β |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 4.57<br>4.19 | 0.51 | 0.25 | 3.05 | 0.53<br>0.33 | 0.81<br>0.66 | 16.66<br>16.51 | 16.66<br>16.51 | 1.27 | 16.00<br>14.99 | 16.00<br>14.99 | 17.65<br>17.40 | 17.65<br>17.40 | 1.22<br>1.07 | 1.44<br>1.02 | 0.18 | 0.18 | 0.1 | 2.16 | 2.16 | 45° |
| inches | 0.180<br>0.165 | 0.02 | 0.01 | 0.12 | 0.021<br>0.013 | 0.032<br>0.026 | 0.656<br>0.650 | 0.656<br>0.650 | 0.05 | 0.63<br>0.59 | 0.63<br>0.59 | 0.695<br>0.685 | 0.695<br>0.685 | 0.048<br>0.042 | 0.057<br>0.040 | 0.007 | 0.007 | 0.004 | 0.085 | 0.085 | |

**Note**

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT187-2 | 112E10 | MS-018 | EDR-7319 | | | ~~99-12-27~~<br>01-11-14 |

## REVISION HISTORY

| Date | CPCN | Description |
|---|---|---|
| 2002 Mar 25 | 9397 750 09585 | – Deleted information for XA-G33<br>– Spun off XA-G30 into a separate data sheet<br>– Corrected Figure 27 ($I_{DD}$ vs. Frequency)<br>– Corrected typical power down current to 15 μA |
| 2001 Jun 25 | 9397 750 08554 | Previous release |

# XA 16-bit microcontroller family
## 32K OTP, 512 B RAM, watchdog, 2 UARTs

XA-G37

### Data sheet status

| Data sheet status [1] | Product status [2] | Definitions |
|---|---|---|
| Objective data | Development | This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice. |
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[1] Please consult the most recently issued data sheet before initiating or completing a design.

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