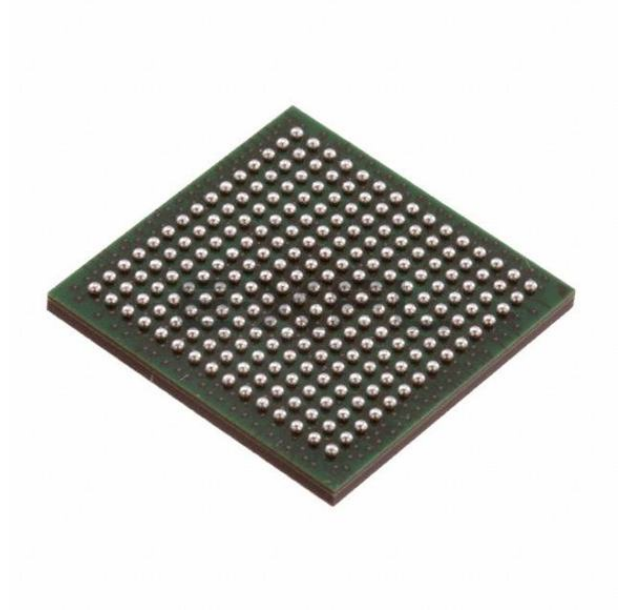

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Obsolete
Type	Floating Point
Interface	Host Interface, Link Port, Serial Port
Clock Rate	100MHz
Non-Volatile Memory	External
On-Chip RAM	128kB
Voltage - I/O	3.30V
Voltage - Core	1.80V
Operating Temperature	-40°C ~ 105°C (TC)
Mounting Type	Surface Mount
Package / Case	255-BGA, CSPBGA
Supplier Device Package	255-CSPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-21161ncca-100

Instruction Cache

The ADSP-21161N includes an on-chip instruction cache that enables three-bus operation for fetching an instruction and four data values. The cache is selective—only the instructions whose fetches conflict with PM bus data accesses are cached. This cache enables full-speed execution of core, looped operations such as digital filter multiply-accumulates, and FFT butterfly processing.

Data Address Generators With Hardware Circular Buffers

The ADSP-21161N's two data address generators (DAGs) are used for indirect addressing and implementing circular data buffers in hardware. Circular buffers allow efficient programming of delay lines and other data structures required in digital signal processing, and are commonly used in digital filters and Fourier transforms. The two DAGs of the ADSP-21161N contain sufficient registers to allow the creation of up to 32 circular buffers (16 primary register sets, 16 secondary). The DAGs automatically handle address pointer wrap-around, reduce overhead, increase performance, and simplify implementation. Circular buffers can start and end at any memory location.

Flexible Instruction Set

The 48-bit instruction word accommodates a variety of parallel operations, for concise programming. For example, the ADSP-21161N can conditionally execute a multiply, an add, and a subtract in both processing elements, while branching, all in a single instruction.

ADSP-21161N MEMORY AND I/O INTERFACE FEATURES

The ADSP-21161N adds the following architectural features to the ADSP-2116x family core.

Dual-Ported On-Chip Memory

The ADSP-21161N contains one megabit of on-chip SRAM, organized as two blocks of 0.5M bits (Figure 3). Each block can be configured for different combinations of code and data storage. Each memory block is dual-ported for single-cycle, independent accesses by the core processor and I/O processor. The dual-ported memory in combination with three separate on-chip buses allow two data transfers from the core and one from the I/O processor, in a single cycle. On the ADSP-21161N, the memory can be configured as a maximum of 32K words of 32-bit data, 64K words of 16-bit data, 21K words of 48-bit instructions (or 40-bit data), or combinations of different word sizes up to one megabit. All of the memory can be accessed as 16-bit, 32-bit, 48-bit, or 64-bit words. A 16-bit floating-point storage format is supported that effectively doubles the amount of data that may be stored on-chip. Conversion between the 32-bit floating-point and 16-bit floating-point formats is done in a single instruction. While each memory block can store combinations of code and data, accesses are most efficient when one block stores data using the DM bus for transfers, and the other block stores instructions and data using the PM bus for transfers. Using the DM bus and PM bus, with one dedicated to each memory block, assures single-cycle execution with two data transfers. In this case, the instruction must be available in the cache.

Off-Chip Memory and Peripherals Interface

The ADSP-21161N's external port provides the processor's interface to off-chip memory and peripherals. The 62.7-M word off-chip address space (254.7-M word if all SDRAM) is included in the ADSP-21161N's unified address space. The separate on-chip buses—for PM addresses, PM data, DM addresses, DM data, I/O addresses, and I/O data—are multiplexed at the external port to create an external system bus with a single 24-bit address bus and a single 32-bit data bus. Every access to external memory is based on an address that fetches a 32-bit word. When fetching an instruction from external memory, two 32-bit data locations are being accessed for packed instructions. Unused link port lines can also be used as additional data lines DATA15–DATA0, allowing single-cycle execution of instructions from external memory, at up to 110 MHz. Figure 4 shows the alignment of various accesses to external memory.

The external port supports asynchronous, synchronous, and synchronous burst accesses. Synchronous burst SRAM can be interfaced gluelessly. The ADSP-21161N also can interface gluelessly to SDRAM. Addressing of external memory devices is facilitated by on-chip decoding of high-order address lines to generate memory bank select signals. The ADSP-21161N provides programmable memory wait states and external memory acknowledge controls to allow interfacing to memory and peripherals with variable access, hold, and disable time requirements.

SDRAM Interface

The SDRAM interface enables the ADSP-21161N to transfer data to and from synchronous DRAM (SDRAM) at the core clock frequency or at one-half the core clock frequency. The synchronous approach, coupled with the core clock frequency, supports data transfer at a high throughput—up to 440M bytes/s for 32-bit transfers and up to 660M bytes/s for 48-bit transfers.

The SDRAM interface provides a glueless interface with standard SDRAMs—16Mb, 64Mb, 128Mb, and 256Mb— and includes options to support additional buffers between the ADSP-21161N and SDRAM. The SDRAM interface is extremely flexible and provides capability for connecting SDRAMs to any one of the ADSP-21161N's four external memory banks, with up to all four banks mapped to SDRAM.

Systems with several SDRAM devices connected in parallel may require buffering to meet overall system timing requirements. The ADSP-21161N supports pipelining of the address and control signals to enable such buffering between itself and multiple SDRAM devices.

Target Board JTAG Emulator Connector

Analog Devices DSP Tools product line of JTAG emulators uses the IEEE 1149.1 JTAG test access port of the ADSP-21161N processor to monitor and control the target board processor during emulation. Analog Devices DSP Tools product line of

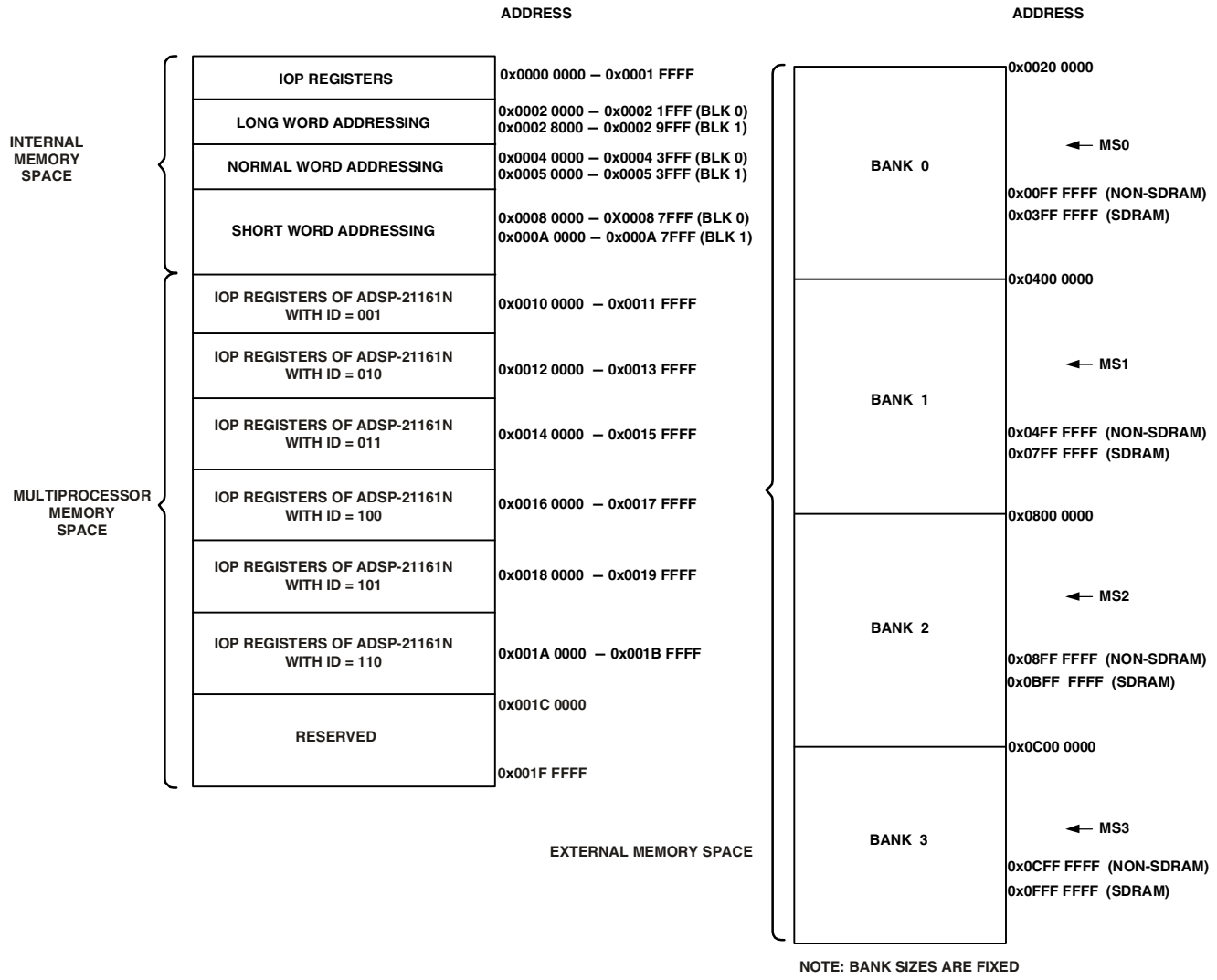

Figure 3. Memory Map

JTAG emulators provides emulation at full processor speed, allowing inspection and modification of memory, registers, and processor stacks. The processor's JTAG interface ensures that the emulator will not affect target system loading or timing.

For complete information on SHARC Analog Devices DSP Tools product line of JTAG emulator operation, see the appropriate Emulator Hardware User's Guide. For detailed information on the interfacing of Analog Devices JTAG emulators with Analog Devices DSP products with JTAG emulation ports, please refer to Engineer to Engineer Note *EE-68: Analog Devices JTAG Emulation Technical Reference*. Both of these documents can be found on the Analog Devices website.

DMA Controller

The ADSP-21161N's on-chip DMA controller enables zero-overhead data transfers without processor intervention. The DMA controller operates independently and invisibly to the processor core, allowing DMA operations to occur while the core is simultaneously executing its program instructions. DMA transfers can occur between the ADSP-21161N's internal memory and external memory, external peripherals, or a host processor. DMA transfers can also occur between the ADSP-21161N's internal memory and its serial ports, link ports, or the SPI-compatible (Serial Peripheral Interface) port. External bus packing and unpacking of 32-, 48-, or 64-bit words in internal memory is performed during DMA transfers from either 8-, 16-, or 32-bit wide external memory. Fourteen channels of DMA are available on the ADSP-21161N—two are shared between the SPI interface and the link ports, eight via the serial ports, and four via the processor's external port (for host processor, other ADSP-21161Ns, memory, or I/O transfers). Programs can be downloaded to the ADSP-21161N using DMA transfers. Asynchronous off-chip peripherals can control two DMA channels using DMA Request/Grant lines ($\overline{\text{DMAR2–1}}$, $\overline{\text{DMAG2–1}}$). Other DMA features include interrupt generation upon completion of DMA transfers, and DMA chaining for automatic linked DMA transfers.

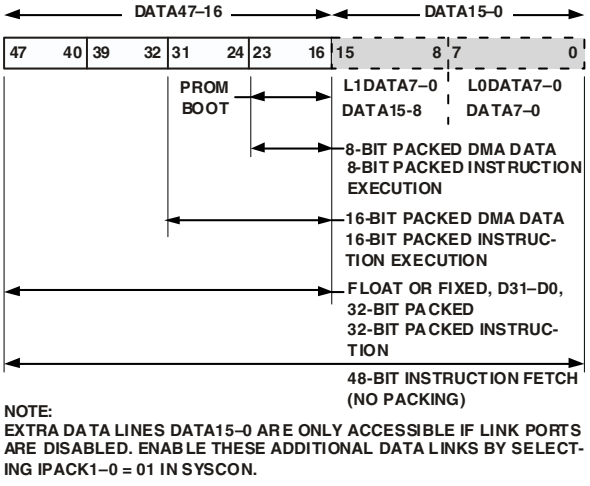

Figure 4. External Data Alignment Options

Multiprocessing

The ADSP-21161N offers powerful features tailored to multiprocessing DSP systems. The external port and link ports provide integrated glueless multiprocessing support.

The external port supports a unified address space (see Figure 3) that enables direct interprocessor accesses of each ADSP-21161N's internal memory-mapped (I/O processor) registers. All other internal memory can be indirectly accessed via DMA transfers initiated via the programming of the IOP DMA parameter and control registers. Distributed bus arbitration logic is included on-chip for simple, glueless connection of systems containing up to six ADSP-21161Ns and a host processor (Figure 5). Master processor change over incurs only one cycle of overhead. Bus arbitration is selectable as either fixed or rotating priority. Bus lock enables indivisible read-modify-write sequences for semaphores. A vector interrupt is provided for interprocessor commands. Using an instruction rate of 110 MHz, maximum throughput for interprocessor data transfer is 440M bytes/s over the external port.

Two link ports provide a second method of multiprocessing communications. Each link port can support communications to another ADSP-21161N. The ADSP-21161N, running at 110 MHz, has a maximum throughput for interprocessor communications over the links of 220M bytes/s. The link ports and cluster multiprocessing can be used concurrently or independently.

Link Ports

The ADSP-21161N features two 8-bit link ports that provide additional I/O capabilities. With the capability of running at 110 MHz, each link port can support 110M bytes/s. Link port I/O is especially useful for point-to-point interprocessor communication in multiprocessing systems. The link ports can operate independently and simultaneously, with a maximum data throughput of 220M bytes/s. Link port data is packed into 48- or 32-bit words and can be directly read by the core processor or DMA-transferred to on-chip memory. Each link port has its own double-buffered input and output registers. Clock/acknowledge handshaking controls link port transfers. Transfers are programmable as either transmit or receive.

Serial Ports

The ADSP-21161N features four synchronous serial ports that provide an inexpensive interface to a wide variety of digital and mixed-signal peripheral devices. Each serial port is made up of two data lines, a clock and frame sync. The data lines can be programmed to either transmit or receive.

The serial ports operate at up to half the clock rate of the core, providing each with a maximum data rate of 55M bit/s. The serial data pins are programmable as either a transmitter or receiver, providing greater flexibility for serial communications. Serial port data can be automatically transferred to and from on-chip memory via a dedicated DMA. Each of the serial ports features a Time Division Multiplex (TDM) multichannel mode, where two serial ports are TDM transmitters and two serial ports are TDM receivers (SPORT0 Rx paired with SPORT2 Tx, SPORT1 Rx paired with SPORT3 Tx). Each of the serial ports also support the I^2S protocol (an industry standard interface commonly used by audio codecs, ADCs and DACs), with two data pins, allowing four I^2S channels (using two I^2S stereo devices) per serial port, with a maximum of up to 16 I^2S channels. The serial ports permit little-endian or big-endian transmission formats and word lengths selectable from 3 bits to 32 bits. For I^2S mode, data-word lengths are selectable between 8 bits and 32 bits. Serial ports offer selectable synchronization and transmit modes as well as optional µ-law or A-law companding. Serial port clocks and frame syncs can be internally or externally generated.

Serial Peripheral (Compatible) Interface

Serial Peripheral Interface (SPI) is an industry standard synchronous serial link, enabling the ADSP-21161N SPI-compatible port to communicate with other SPI-compatible devices. SPI is a 4-wire interface consisting of two data pins, one device select pin, and one clock pin. It is a full-duplex synchronous serial interface, supporting both master and slave modes. The SPI port can operate in a multimaster environment by interfacing with up to four other SPI-compatible devices, either acting as a master or slave device. The ADSP-21161N SPI-compatible peripheral implementation also features programmable baud rate and clock phase/polarities. The ADSP-21161N SPI-compatible port uses open drain drivers to support a multimaster configuration and to avoid data contention.

Host Processor Interface

The ADSP-21161N host interface enables easy connection to standard 8-bit, 16-bit, or 32-bit microprocessor buses with little additional hardware required. The host interface is accessed through the ADSP-21161N's external port. Four channels of DMA are available for the host interface; code and data transfers are accomplished with low software overhead. The host processor requests the ADSP-21161N's external bus with the host bus request ($\overline{\text{HBR}}$), host bus grant ($\overline{\text{HBG}}$), and chip select (CS) signals. The host can directly read and write the internal IOP registers of the ADSP-21161N, and can access the DMA channel

Core Embedded Studio or VisualDSP++ installed (sold separately), engineers can develop software for supported EZ-KITs or any custom system utilizing supported Analog Devices processors.

Software Add-Ins for CrossCore Embedded Studio

Analog Devices offers software add-ins which seamlessly integrate with CrossCore Embedded Studio to extend its capabilities and reduce development time. Add-ins include board support packages for evaluation hardware, various middleware packages, and algorithmic modules. Documentation, help, configuration dialogs, and coding examples present in these add-ins are viewable through the CrossCore Embedded Studio IDE once the add-in is installed.

Board Support Packages for Evaluation Hardware

Software support for the EZ-KIT Lite evaluation boards and EZ-Extender daughter cards is provided by software add-ins called Board Support Packages (BSPs). The BSPs contain the required drivers, pertinent release notes, and select example code for the given evaluation hardware. A download link for a specific BSP is located on the web page for the associated EZ-KIT or EZ-Extender product. The link is found in the *Product Download* area of the product web page.

Middleware Packages

Analog Devices separately offers middleware add-ins such as real time operating systems, file systems, USB stacks, and TCP/IP stacks. For more information see the following web pages:

- www.analog.com/ucos3
- www.analog.com/ucfs
- www.analog.com/ucusbd
- www.analog.com/lwip

Algorithmic Modules

To speed development, Analog Devices offers add-ins that perform popular audio and video processing algorithms. These are available for use with both CrossCore Embedded Studio and VisualDSP++. For more information visit www.analog.com and search on “Blackfin software modules” or “SHARC software modules”.

Designing an Emulator-Compatible DSP Board (Target)

For embedded system test and debug, Analog Devices provides a family of emulators. On each JTAG DSP, Analog Devices supplies an IEEE 1149.1 JTAG Test Access Port (TAP). In-circuit emulation is facilitated by use of this JTAG interface. The emulator accesses the processor’s internal features via the processor’s TAP, allowing the developer to load code, set breakpoints, and view variables, memory, and registers. The processor must be halted to send data and commands, but once an operation is completed by the emulator, the DSP system is set to run at full speed with no impact on system timing. The emulators require the target board to include a header that supports connection of the DSP’s JTAG port to the emulator.

For details on target board design issues including mechanical layout, single processor connections, signal buffering, signal termination, and emulator pod logic, see the *EE-68: Analog Devices JTAG Emulation Technical Reference* on the Analog Devices website (www.analog.com)—use site search on “EE-68.” This document is updated regularly to keep pace with improvements to emulator support.

ADDITIONAL INFORMATION

This data sheet provides a general overview of the ADSP-21161N architecture and functionality. For detailed information on the ADSP-2116x Family core architecture and instruction set, refer to the *ADSP-21161 SHARC DSP Hardware Reference* and the *ADSP-21160 SHARC DSP Instruction Set Reference*.

RELATED SIGNAL CHAINS

A *signal chain* is a series of signal-conditioning electronic components that receive input (data acquired from sampling either real-time phenomena or from stored data) in tandem, with the output of one portion of the chain supplying input to the next. Signal chains are often used in signal processing applications to gather and process data or to apply system controls based on analysis of real-time phenomena. For more information about this term and related topics, see the “signal chain” entry in Wikipedia or the Glossary of EE Terms on the Analog Devices website.

Analog Devices eases signal processing system development by providing signal processing components that are designed to work together well. A tool for viewing relationships between specific applications and related components is available on the www.analog.com website.

The Application Signal Chains page in the Circuits from the Lab™ site (http://www.analog.com/signal chains) provides:

- Graphical circuit block diagram presentation of signal chains for a variety of circuit types and applications
- Drill down links for components in each chain to selection guides and application information
- Reference designs applying best practice design techniques

Table 2. Pin Function Descriptions (Continued)

Pin	Type	Function
REDY	O (O/D)	**Host Bus Acknowledge**. The ADSP-21161N deasserts REDY (low) to add wait states to a host access of its IOP registers when $\overline{CS}$ and $\overline{HBR}$ inputs are asserted.
$\overline{DMAR1}$	I/A	**DMA Request 1** (DMA Channel 11). Asserted by external port devices to request DMA services. $\overline{DMAR1}$ has a 20 kΩ internal pull-up resistor that is enabled for DSPs with ID2–0=00x.
$\overline{DMAR2}$	I/A	**DMA Request 2** (DMA Channel 12). Asserted by external port devices to request DMA services. $\overline{DMAR2}$ has a 20 kΩ internal pull-up resistor that is enabled for DSPs with ID2–0=00x.
$\overline{DMAG1}$	O/T	**DMA Grant 1** (DMA Channel 11). Asserted by ADSP-21161N to indicate that the requested DMA starts on the next cycle. Driven by bus master only. $\overline{DMAG1}$ has a 20 kΩ internal pull-up resistor that is enabled for DSPs with ID2–0=00x.
$\overline{DMAG2}$	O/T	**DMA Grant 2** (DMA Channel 12). Asserted by ADSP-21161N to indicate that the requested DMA starts on the next cycle. Driven by bus master only. $\overline{DMAG2}$ has a 20 kΩ internal pull-up resistor that is enabled for DSPs with ID2–0=00x.
$\overline{BR6–1}$	I/O/S	**Multiprocessing Bus Requests**. Used by multiprocessing ADSP-21161Ns to arbitrate for bus mastership. An ADSP-21161N only drives its own $\overline{BRx}$ line (corresponding to the value of its ID2–0 inputs) and monitors all others. In a multiprocessor system with less than six ADSP-21161Ns, the unused $\overline{BRx}$ pins should be pulled high; the processor's own $\overline{BRx}$ line must not be pulled high or low because it is an output.
BMSTR	O	**Bus Master Output**. In a multiprocessor system, indicates whether the ADSP-21161N is current bus master of the shared external bus. The ADSP-21161N drives BMSTR high only while it is the bus master. In a single-processor system (ID=000), the processor drives this pin high. This pin is used for debugging purposes.
ID2–0	I	**Multiprocessing ID**. Determines which multiprocessing bus request ($\overline{BR6}$–$\overline{BR1}$) is used by ADSP-21161N. ID=001 corresponds to $\overline{BR1}$, ID=010 corresponds to $\overline{BR2}$, and so on. Use ID=000 or ID=001 in single-processor systems. These lines are a system configuration selection that should be hardwired or only changed at reset.
RPBA	I/S	**Rotating Priority Bus Arbitration Select**. When RPBA is high, rotating priority for multiprocessor bus arbitration is selected. When RPBA is low, fixed priority is selected. This signal is a system configuration selection that must be set to the same value on every ADSP-21161N. If the value of RPBA is changed during system operation, it must be changed in the same CLKIN cycle on every ADSP-21161N.
$\overline{PA}$	I/O/T	**Priority Access**. Asserting its $\overline{PA}$ pin enables an ADSP-21161N bus slave to interrupt background DMA transfers and gain access to the external bus. $\overline{PA}$ is connected to all ADSP-21161Ns in the system. If access priority is not required in a system, the $\overline{PA}$ pin should be left unconnected. $\overline{PA}$ has a 20 kΩ internal pull-up resistor that is enabled for DSPs with ID2–0=00x.
DxA	I/O	**Data Transmit or Receive Channel A** (Serial Ports 0, 1, 2, 3). Each DxA pin has an internal pull-up resistor. Bidirectional data pin. This signal can be configured as an output to transmit serial data, or as an input to receive serial data.
DxB	I/O	**Data Transmit or Receive Channel B** (Serial Ports 0, 1, 2, 3). Each DxB pin has an internal pull-up resistor. Bidirectional data pin. This signal can be configured as an output to transmit serial data, or as an input to receive serial data.
SCLKx	I/O	**Transmit/Receive Serial Clock** (Serial Ports 0, 1, 2, 3). Each SCLK pin has an internal pull-up resistor. This signal can be either internally or externally generated.
FSx	I/O	**Transmit or Receive Frame Sync** (Serial Ports 0, 1, 2, 3). The frame sync pulse initiates shifting of serial data. This signal is either generated internally or externally. It can be active high or low or an early or a late frame sync, in reference to the shifting of serial data.
SPICLK	I/O	**Serial Peripheral Interface Clock Signal**. Driven by the master, this signal controls the rate at which data is transferred. The master may transmit data at a variety of baud rates. SPICLK cycles once for each bit transmitted. SPICLK is a gated clock that is active during data transfers, only for the length of the transferred word. Slave devices ignore the serial clock if the slave select input is driven inactive (HIGH). SPICLK is used to shift out and shift in the data driven on the MISO and MOSI lines. The data is always shifted out on one clock edge of the clock and sampled on the opposite edge of the clock. Clock polarity and clock phase relative to data are programmable into the SPICTL control register and define the transfer format. SPICLK has a 50 kΩ internal pull-up resistor.

Table 2. Pin Function Descriptions (Continued)

Pin	Type	Function
$\overline{\text{SPIDS}}$	I	**Serial Peripheral Interface Slave Device Select**. An active low signal used to enable slave devices. This input signal behaves like a chip select, and is provided by the master device for the slave devices. In multimaster mode $\overline{\text{SPIDS}}$ signal can be asserted to a master device to signal that an error has occurred, as some other device is also trying to be the master device. If asserted low when the device is in master mode, it is considered a multimaster error. For a single-master, multiple-slave configuration where FLAG3–0 are used, this pin must be tied or pulled high to V_{DDEXT} on the master device. For ADSP-21161N to ADSP-21161N SPI interaction, any of the master ADSP-21161N's FLAG3–0 pins can be used to drive the $\overline{\text{SPIDS}}$ signal on the ADSP-21161N SPI slave device.
MOSI	I/O (o/d)	**SPI Master Out Slave**. If the ADSP-21161N is configured as a master, the MOSI pin becomes a data transmit (output) pin, transmitting output data. If the ADSP-21161N is configured as a slave, the MOSI pin becomes a data receive (input) pin, receiving input data. In an ADSP-21161N SPI interconnection, the data is shifted out from the MOSI output pin of the master and shifted into the MOSI input(s) of the slave(s). MOSI has an internal pull-up resistor.
MISO	I/O (o/d)	**SPI Master In Slave Out**. If the ADSP-21161N is configured as a master, the MISO pin becomes a data receive (input) pin, receiving input data. If the ADSP-21161N is configured as a slave, the MISO pin becomes a data transmit (output) pin, transmitting output data. In an ADSP-21161N SPI interconnection, the data is shifted out from the MISO output pin of the slave and shifted into the MISO input pin of the master. MISO has an internal pull-up resistor. MISO can be configured as o/d by setting the OPD bit in the SPICTL register. **Note:** *Only one slave is allowed to transmit data at any given time.*
LxDAT7–0 [DATA15–0]	I/O [I/O/T]	Link Port Data (Link Ports 0–1). For silicon revisions 1.2 and higher, each LxDAT pin has a keeper latch that is enabled when used as a data pin; or a 20 kΩ internal pull-down resistor that is enabled or disabled by the LxPDRDE bit of the LCTL register. For silicon revisions 0.3, 1.0, and 1.1 each LxDAT pin has a 50 kΩ internal pull-down resistor that is enabled or disabled by the LxPDRDE bit of the LCTL register. **Note:** *L1DAT7–0 are multiplexed with the DATA15–8 pins L0DAT7–0 are multiplexed with the DATA7–0 pins. If link ports are disabled and are not used, these pins can be used as additional data lines for executing instructions at up to the full clock rate from external memory. See DATA47–16 for more information.*
LxCLK	I/O	**Link Port Clock** (Link Ports 0–1). Each LxCLK pin has an internal pull-down 50 kΩ resistor that is enabled or disabled by the LxPDRDE bit of the LCTL register.
LxACK	I/O	**Link Port Acknowledge** (Link Ports 0–1). Each LxACK pin has an internal pull-down 50 kΩ resistor that is enabled or disabled by the LxPDRDE bit of the LCTL register.
EBOOT	I	**EPROM Boot Select**. For a description of how this pin operates, see the table in the $\overline{\text{BMS}}$ pin description. This signal is a system configuration selection that should be hardwired.
LBOOT	I	**Link Boot**. For a description of how this pin operates, see the table in the $\overline{\text{BMS}}$ pin description. This signal is a system configuration selection that should be hardwired.
$\overline{\text{BMS}}$	I/O/T	**Boot Memory Select**. Serves as an output or input as selected with the EBOOT and LBOOT pins (see Table 4). This input is a system configuration selection that should be hardwired. For Host and PROM boot, DMA channel 10 (EPB0) is used. For Link boot and SPI boot, DMA channel 8 is used. Three-state only in EPROM boot mode (when $\overline{\text{BMS}}$ is an output).
CLKIN	I	**Local Clock In**. Used in conjunction with XTAL. CLKIN is the ADSP-21161N clock input. It configures the ADSP-21161N to use either its internal clock generator or an external clock source. Connecting the necessary components to CLKIN and XTAL enables the internal clock generator. Connecting the external clock to CLKIN while leaving XTAL unconnected configures the ADSP-21161N to use the external clock source such as an external clock oscillator.The ADSP-21161N external port cycles at the frequency of CLKIN. The instruction cycle rate is a multiple of the CLKIN frequency; it is programmable at power-up via the CLK_CFG1–0 pins. CLKIN may not be halted, changed, or operated below the specified frequency.
XTAL	O	**Crystal Oscillator Terminal 2**. Used in conjunction with CLKIN to enable the ADSP-21161N's internal clock oscillator or to disable it to use an external clock source. See CLKIN.
CLK_CFG1-0	I	**Core/CLKIN Ratio Control**. ADSP-21161N core clock (instruction cycle) rate is equal to n × PLLICLK where n is user selectable to 2, 3, or 4, using the CLK_CFG1–0 inputs. These pins can also be used in combination with the $\overline{\text{CLKDBL}}$ pin to generate additional core clock rates of 6 × CLKIN and 8 × CLKIN (see the Clock Rate Ratios table in the $\overline{\text{CLKDBL}}$ description).

Table 2. Pin Function Descriptions (Continued)

Pin	Type	Function
$\overline{\text{CLKDBL}}$	I	**Crystal Double Mode Enable**. This pin is used to enable the 2× clock double circuitry, where CLKOUT can be configured as either 1× or 2× the rate of CLKIN. This CLKIN double circuit is primarily intended to be used for an external crystal in conjunction with the internal clock generator and the XTAL pin. The internal clock generator when used in conjunction with the XTAL pin and an external crystal is designed to support up to a maximum of 27.5 MHz external crystal frequency. $\overline{\text{CLKDBL}}$ can be used in XTAL mode to generate a 55 MHz input into the PLL. The 2× clock mode is enabled (during $\overline{\text{RESET}}$ low) by tying $\overline{\text{CLKDBL}}$ to GND, otherwise it is connected to V_{DDEXT} for 1× clock mode. For example, this enables the use of a 27.5 MHz crystal to enable 110 MHz core clock rates and a 55 MHz CLKOUT operation when CLK_CFG0=0, CLK_CFG1=0 and $\overline{\text{CLKDBL}}$=0. This pin can also be used to generate different clock rate ratios for external clock oscillators as well. The possible clock rate ratio options (up to 110 MHz) for either CLKIN (external clock oscillator) or XTAL (crystal input) are shown in Table 3 on Page 16. An 8:1 ratio enables the use of a 12.5 MHz crystal to generate a 100 MHz core (instruction clock) rate and a 25 MHz CLKOUT (external port) clock rate. See also Figure 8 on Page 20. **Note:** *When using an external crystal, the maximum crystal frequency cannot exceed 27.5 MHz. For all other external clock sources, the maximum CLKIN frequency is 55 MHz.*
CLKOUT	O/T	**Local Clock Out**. CLKOUT is 1× or 2× and is driven at either 1× or 2× the frequency of CLKIN frequency by the current bus master. The frequency is determined by the $\overline{\text{CLKDBL}}$ pin. This output is three-stated when the ADSP-21161N is not the bus master or when the host controls the bus ($\overline{\text{HBG}}$ asserted). A keeper latch on the DSP's CLKOUT pin maintains the output at the level it was last driven. This latch is only enabled on the ADSP-21161N with ID2–0=00x. If $\overline{\text{CLKDBL}}$ enabled, CLKOUT=2 × CLKIN If $\overline{\text{CLKDBL}}$ disabled, CLKOUT=1 × CLKIN **Note:** *CLKOUT is only controlled by the* $\overline{\text{CLKDBL}}$ *pin and operates at either 1 × CLKIN or 2 × CLKIN.* Do not use CLKOUT in multiprocessing systems. Use CLKIN instead.
$\overline{\text{RESET}}$	I/A	**Processor Reset**. Resets the ADSP-21161N to a known state and begins execution at the program memory location specified by the hardware reset vector address. The $\overline{\text{RESET}}$ input must be asserted (low) at power-up.
$\overline{\text{RSTOUT}}$[1]	O	**Reset Out**. When $\overline{\text{RSTOUT}}$ is asserted (low), this pin indicates that the core blocks are in reset. It is deasserted 4080 cycles after $\overline{\text{RESET}}$ is deasserted indicating that the PLL is stable and locked.
TCK	I	**Test Clock (JTAG)**. Provides a clock for JTAG boundary scan.
TMS	I/S	**Test Mode Select (JTAG)**. Used to control the test state machine. TMS has a 20 kΩ internal pull-up resistor.
TDI	I/S	**Test Data Input (JTAG)**. Provides serial data for the boundary scan logic. TDI has a 20 kΩ internal pull-up resistor.
TDO	O	**Test Data Output (JTAG)**. Serial scan output of the boundary scan path.
$\overline{\text{TRST}}$	I/A	**Test Reset (JTAG)**. Resets the test state machine. $\overline{\text{TRST}}$ must be asserted (pulsed low) after power-up or held low for proper operation of the ADSP-21161N. $\overline{\text{TRST}}$ has a 20 kΩ internal pull-up resistor.
$\overline{\text{EMU}}$	O (O/D)	**Emulation Status**. Must be connected to the ADSP-21161N Analog Devices DSP Tools product line of JTAG emulators target board connector only. $\overline{\text{EMU}}$ has a 50 kΩ internal pull-up resistor.
V_{DDINT}	P	**Core Power Supply**. Nominally +1.8 V dc and supplies the DSP's core processor (14 pins).
V_{DDEXT}	P	**I/O Power Supply**. Nominally +3.3 V dc. (13 pins).
AVDD	P	**Analog Power Supply**. Nominally +1.8 V dc and supplies the DSP's internal PLL (clock generator). This pin has the same specifications as V_{DDINT}, except that added filtering circuitry is required. For more information, see Power Supplies on Page 9.
AGND	G	**Analog Power Supply Return**.
GND	G	**Power Supply Return**. (26 pins).
NC		**Do Not Connect**. Reserved pins that must be left open and unconnected. (4 pins)

[1] $\overline{\text{RSTOUT}}$ exists only for silicon revisions 1.2 and greater.

PACKAGE INFORMATION

The information presented in Figure 7 provides details about how to read the package brand and relate it to specific product features.

Figure 7. Typical Package Brand

Table 5. Package Brand Information

Brand Key	Field Description
ADSP-21161N	Model Number
t	Temperature Range
pp	Package Type
z	RoHS Compliance Option
vvvvv.x	Assembly Lot Code
n.n	Silicon Revision
#	RoHS Compliance Designation
yyww	Date Code

ABSOLUTE MAXIMUM RATINGS

Stresses greater than those listed in Table 6 may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 6. Absolute Maximum Ratings

Parameter	Rating
Internal (Core) Supply Voltage (V_{DDINT})	–0.3 V to +2.2 V
Analog (PLL) Supply Voltage (A_{VDD})	–0.3 V to +2.2 V
External (I/O) Supply Voltage (V_{DDEXT})	–0.3 V to +4.6 V
Input Voltage	–0.5 V to V_{DDEXT} + 0.5 V
Output Voltage Swing	–0.5 V to V_{DDEXT} + 0.5 V
Load Capacitance	200 pF
Storage Temperature Range	–65°C to +150°C

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

TIMING SPECIFICATIONS

The ADSP-21161N's internal clock switches at higher frequencies than the system input clock (CLKIN). To generate the internal clock, the DSP uses an internal phase-locked loop (PLL). This PLL-based clocking minimizes the skew between the system clock (CLKIN) signal and the DSP's internal clock (the clock source for the external port logic and I/O pads).

The ADSP-21161N's internal clock (a multiple of CLKIN) provides the clock signal for timing internal memory, processor core, link ports, serial ports, and external port (as required for read/write strobes in asynchronous access mode). During reset, program the ratio between the DSP's internal clock frequency and external (CLKIN) clock frequency with the CLK_CFG1–0 and $\overline{\text{CLKDBL}}$ pins. Even though the internal clock is the clock source for the external port, it behaves as described in the Clock Rate Ratio chart in Table 3 on Page 16. To determine switching frequencies for the serial and link ports, divide down the internal clock, using the programmable divider control of each port (DIVx for the serial ports and LxCLKD for the link ports).

Note the following definitions of various clock periods that are a function of CLKIN and the appropriate ratio control (Table 7).

Figure 8 enables Core-to-CLKIN ratios of 2:1, 3:1, 4:1, 6:1, and 8:1 with external oscillator or crystal. It also shows support for CLKOUT-to-CLKIN ratios of 1:1 and 2:1.

Use the exact timing information given. Do not attempt to derive parameters from the addition or subtraction of others. While addition or subtraction would yield meaningful results for an individual device, the values given in this data sheet reflect statistical variations and worst cases. Consequently, it is not meaningful to add parameters to derive longer times.

See Figure 37 on Page 54 under Test Conditions for voltage reference levels.

Switching characteristics specify how the processor changes its signals. Circuitry external to the processor must be designed for compatibility with these signal characteristics. Switching characteristics describe what the processor will do in a given circumstance. Use switching characteristics to ensure that any timing requirement of a device connected to the processor (such as memory) is satisfied.

Timing requirements apply to signals that are controlled by circuitry external to the processor, such as the data input for a read operation. Timing requirements guarantee that the processor operates correctly with other devices.

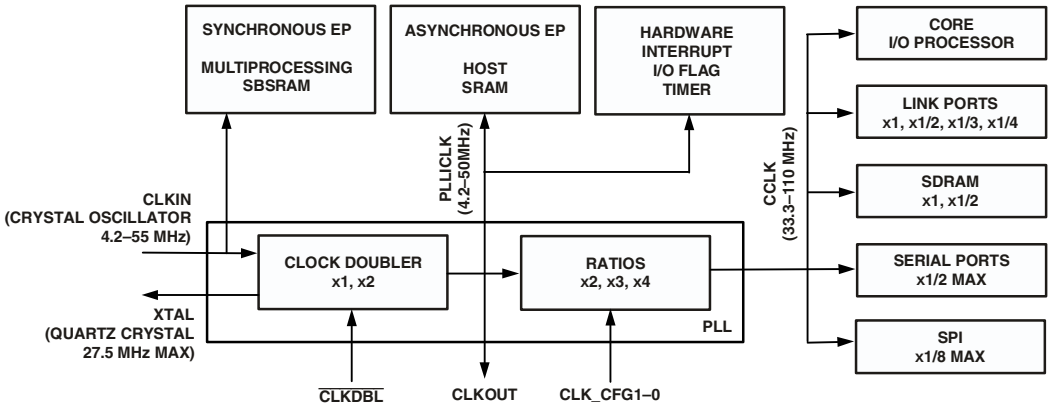

Figure 8. Core Clock and System Clock Relationship to CLKIN

Table 7. CLKOUT and CCLK Clock Generation Operation

Timing Requirements	Description[1]	Calculation
CLKIN	Input Clock	$1/t_{CK}$
CLKOUT	External Port System Clock	$1/t_{CKOP}$
PLLICLK	PLL Input Clock	$1/t_{PLLIN}$
CCLK	Core Clock	$1/t_{CCLK}$
t_{CK}	CLKIN Clock Period	1/CLKIN
t_{CCLK}	(Processor) Core Clock Period	1/CCLK
t_{LCLK}	Link Port Clock Period	$(t_{CCLK}) \times LR$
t_{SCLK}	Serial Port Clock Period	$(t_{CCLK}) \times SR$
t_{SDK}	SDRAM Clock Period	$(t_{CCLK}) \times SDCKR$
t_{SPICLK}	SPI Clock Period	$(t_{CCLK}) \times SPIR$

[1] where:
LR = link port-to-core clock ratio (1, 2, 3, or 1:4, determined by LxCLKD)
SR = serial port-to-core clock ratio (wide range, determined by CLKDIV)
SDCKR = SDRAM-to-Core Clock Ratio (1:1 or 1:2, determined by SDCTL register)
SPIR = SPI-to-Core Clock Ratio (wide range, determined by SPICTL register)
LCLK = Link Port Clock
SCLK = Serial Port Clock
SDK = SDRAM Clock
SPICLK = SPI Clock

POWER DISSIPATION

Total power dissipation has two components: one due to internal circuitry and one due to the switching of external output drivers.

Internal power dissipation depends on the instruction execution sequence and the data operands involved. Using the current specifications ($I_{DDINPEAK}$, $I_{DDINHIGH}$, $I_{DDINLOW}$, I_{DDIDLE}) from the Electrical Characteristics on Page 18 and the current-versus-operation information in Table 8, the programmer can estimate the ADSP-21161N's internal power supply (V_{DDINT}) input current for a specific application, according to the following formula:

$$\begin{aligned} &\%\ \text{Peak} \times I_{DD\text{-}INPEAK} \\ &\%\ \text{High} \times I_{DD\text{-}INHIGH} \\ &\%\ \text{Low} \times I_{DD\text{-}INLOW} \\ +\ &\%\ \text{Peak} \times I_{DD\text{-}IDLE} \\ &= I_{DDINT} \end{aligned}$$

Clock Input

In systems that use multiprocessing or SBSRAM, $\overline{\text{CLKDBL}}$ cannot be enabled nor can the systems use an external crystal as the CLKIN source.

Do not use CLKOUT as the clock source for the SBSRAM device. Using an external crystal in conjunction with $\overline{\text{CLKDBL}}$ to generate a CLKOUT frequency is not supported. Negative hold times can result from the potential skew between CLKIN and CLKOUT.

Table 11. Clock Input

Parameter		100 MHz Min	100 MHz Max	110 MHz Min	110 MHz Max	Unit
Timing Requirements						
t_{CK}	CLKIN Period[1]	20	238	18	238	ns
t_{CKL}	CLKIN Width Low[1]	7.5	119	7	119	ns
t_{CKH}	CLKIN Width High[1]	7.5	119	7	119	ns
t_{CKRF}	CLKIN Rise/Fall (0.4 V–2.0 V)		3		3	ns
t_{CCLK}	CCLK Period	10	30	9	30	ns
Switching Characteristics						
t_{DCKOO}	CLKOUT Delay After CLKIN	0	2	0	2	ns
t_{CKOP}	CLKOUT Period	$t_{CK}-1$	$t_{CK}+1$	$t_{CK}-1$	$t_{CK}+1$	ns
t_{CKWH}	CLKOUT Width High	$t_{CKOP}/2-2$	$t_{CKOP}/2+2$	$t_{CKOP}/2-2$	$t_{CKOP}/2+2$	ns
t_{CKWL}	CLKOUT Width Low	$t_{CKOP}/2-2$	$t_{CKOP}/2+2$	$t_{CKOP}/2-2$	$t_{CKOP}/2+2$	ns

[1] CLKIN is dependent on the configuration of the CLKCFGx and $\overline{\text{CLKDBL}}$ pins to achieve desired t_{CCLK}.

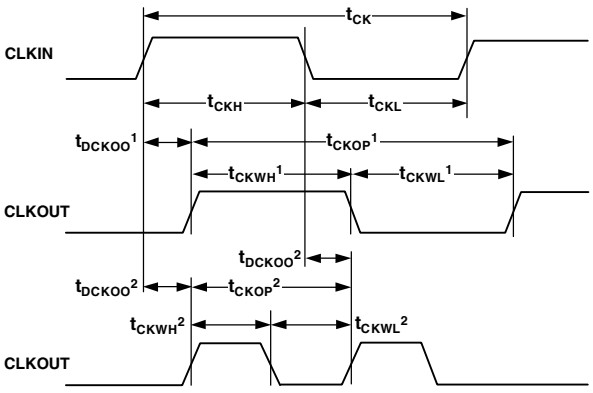

Figure 11. Clock Input

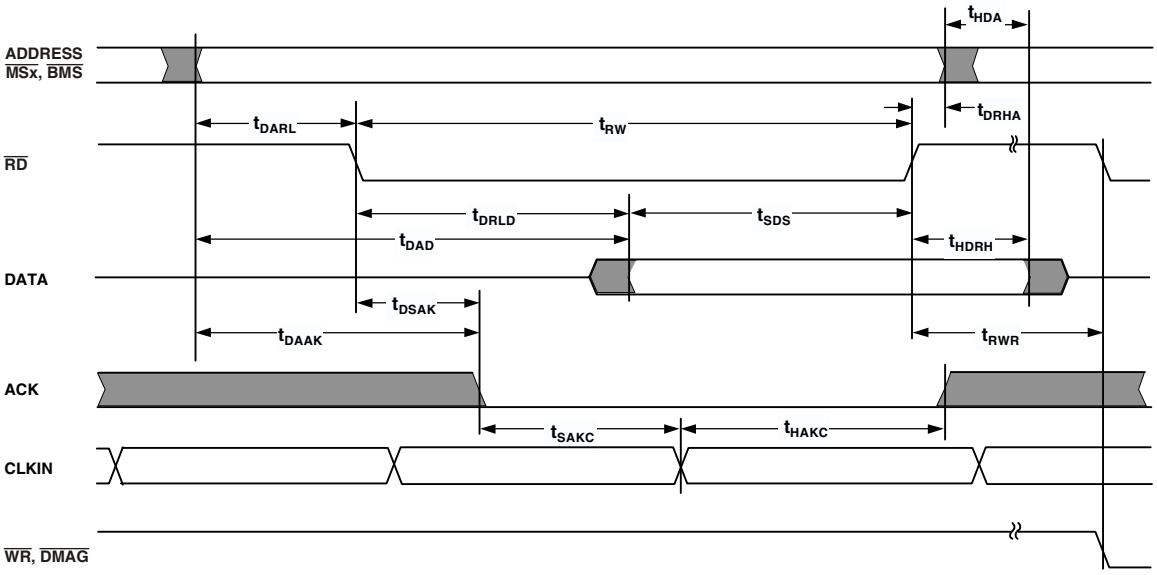

Figure 17. Memory Read — Bus Master

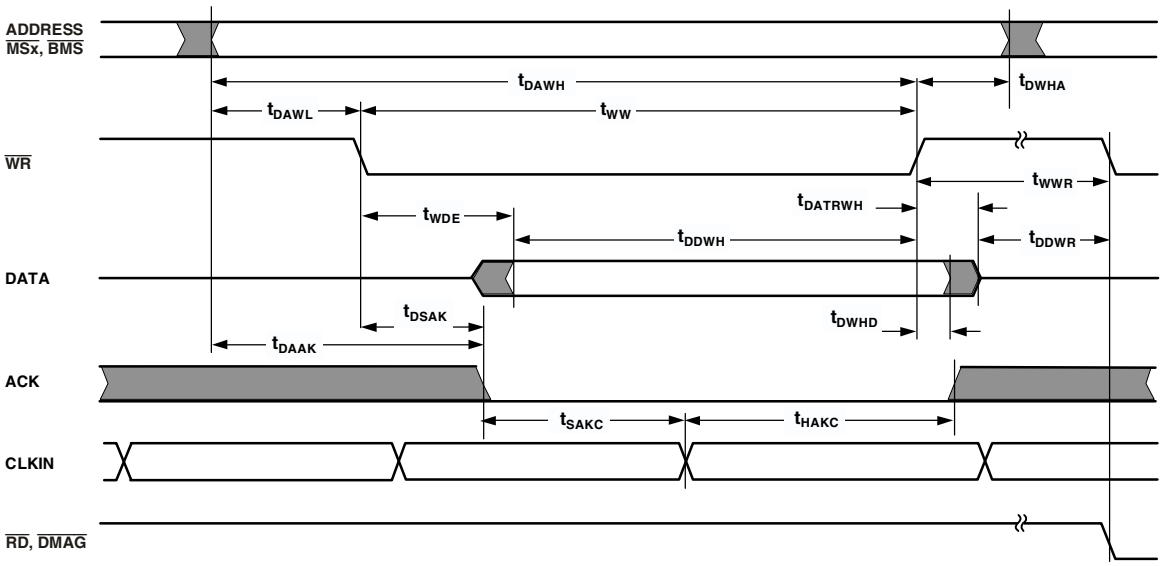

Figure 18. Memory Write — Bus Master

Synchronous Read/Write — Bus Master

Use these specifications for interfacing to external memory systems that require CLKIN, relative to timing or for accessing a slave ADSP-21161N (in multiprocessor memory space). When accessing a slave ADSP-21161N, these switching characteristics must meet the slave's timing requirements for synchronous read/writes (see Synchronous Read/Write — Bus Slave on Page 32). The slave ADSP-21161N must also meet these (bus master) timing requirements for data and acknowledge setup and hold times.

Table 18. Synchronous Read/Write — Bus Master

Parameter		Min	Max	Unit
Timing Requirements				
t_{SSDATI}	Data Setup Before CLKIN	5.5		ns
t_{HSDATI}	Data Hold After CLKIN	1		ns
t_{SACKC}	ACK Setup Before CLKIN	$0.5t_{CCLK}$+3		ns
t_{HACKC}	ACK Hold After CLKIN	1		ns
Switching Characteristics				
t_{DADDO}	Address, $\overline{MSx}$, $\overline{BMS}$, BRST, Delay After CLKIN		10	ns
t_{HADDO}	Address, $\overline{MSx}$, $\overline{BMS}$, BRST, Hold After CLKIN	1.5		ns
t_{DRDO}	$\overline{RD}$ High Delay After CLKIN	$0.25t_{CCLK}$–1	$0.25t_{CCLK}$+9	ns
t_{DWRO}	$\overline{WR}$ High Delay After CLKIN	$0.25t_{CCLK}$–1	$0.25t_{CCLK}$+9	ns
t_{DRWL}	$\overline{RD}$/$\overline{WR}$ Low Delay After CLKIN	$0.25t_{CCLK}$–1	$0.25t_{CCLK}$+9	ns
t_{DDATO}	Data Delay After CLKIN		12.5	ns
t_{HDATO}	Data Hold After CLKIN	1.5		ns

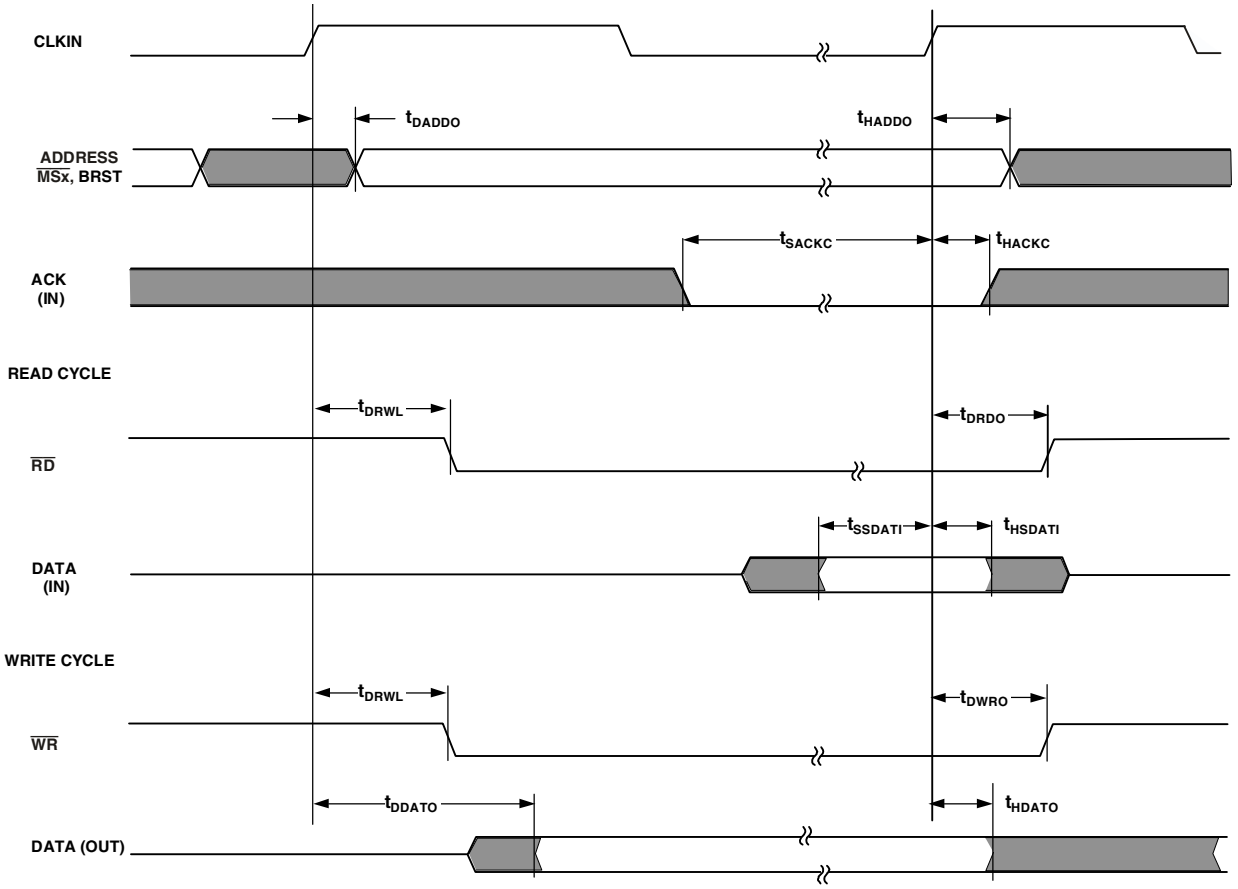

Figure 19. Synchronous Read/Write — Bus Master

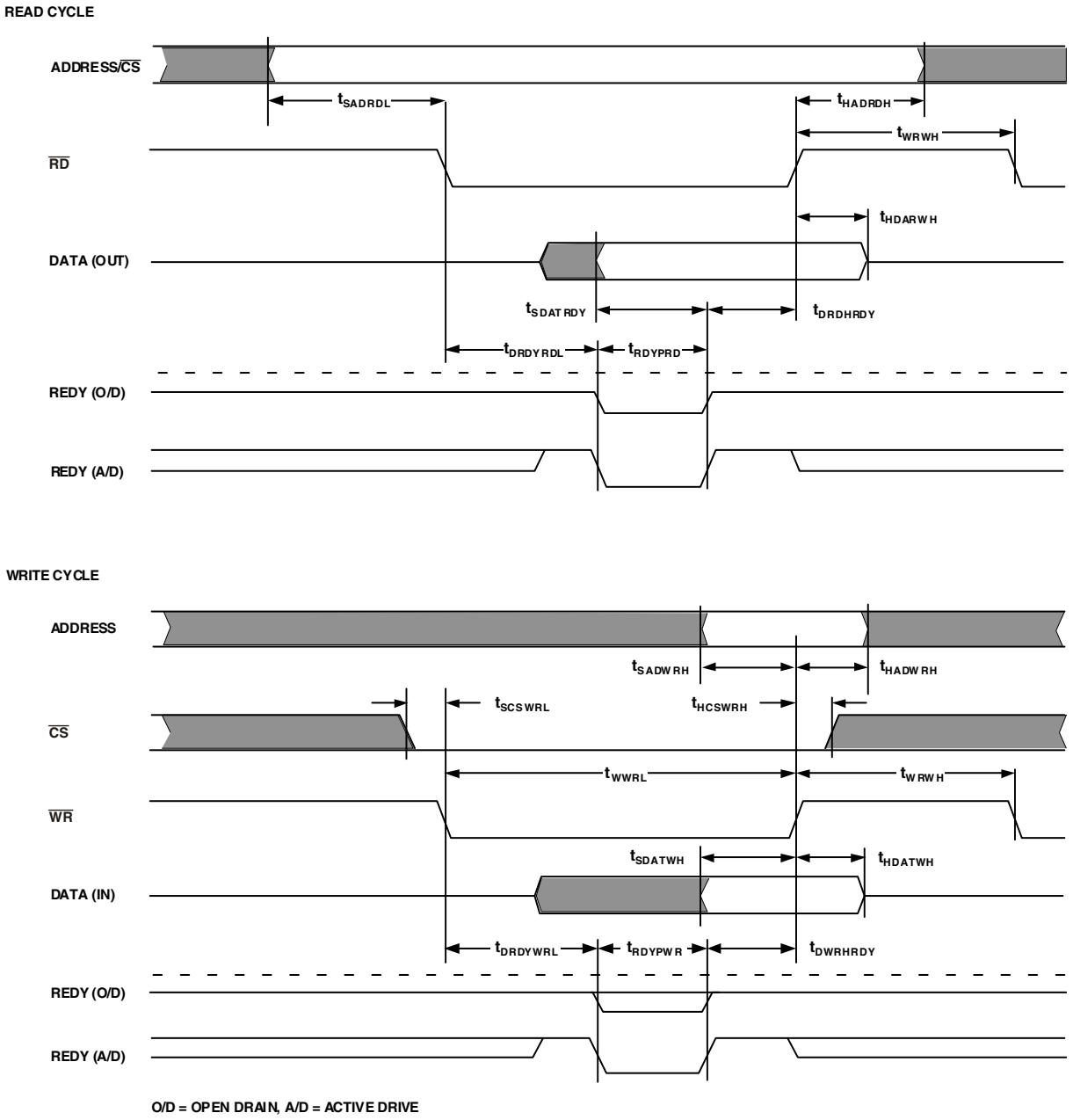

Figure 23. Asynchronous Read/Write — Host to ADSP-21161N

SDRAM Interface — Bus Master

Use these specifications for ADSP-21161N bus master accesses of SDRAM:

Table 26. SDRAM Interface — Bus Master

Parameter		100 MHz		110 MHz		Unit
		Min	Max	Min	Max	
Timing Requirements						
t_{SDSDK}	Data Setup Before SDCLK	2.0		2.0		ns
t_{HDSDK}	Data Hold After SDCLK	2.3		2.3		ns
Switching Characteristics						
t_{DSDK1}	First SDCLK Rise Delay After CLKIN[1, 2]	$0.75t_{CCLK} + 1.5$	$0.75t_{CCLK} + 8.0$	$0.75t_{CCLK} + 1.5$	$0.75t_{CCLK} + 8.0$	ns
t_{SDK}	SDCLK Period	t_{CCLK}	$2 \times t_{CCLK}$	t_{CCLK}	$2 \times t_{CCLK}$	ns
t_{SDKH}	SDCLK Width High	4		3		ns
t_{SDKL}	SDCLK Width Low	4		3		ns
$t_{DCADSDK}$	Command, Address, Data, Delay After SDCLK[3]		$0.25t_{CCLK} + 2.5$		$0.25t_{CCLK} + 2.5$	ns
$t_{HCADSDK}$	Command, Address, Data, Hold After SDCLK[3]	2.0		2.0		ns
$t_{SDTRSDK}$	Data Three-State After SDCLK[4]		$0.5t_{CCLK} + 2.0$		$0.5t_{CCLK} + 2.0$	ns
$t_{SDENSDK}$	Data Enable After SDCLK[5]	$0.75t_{CCLK}$		$0.75t_{CCLK}$		ns
t_{SDCTR}	Command Three-State After CLKIN	$0.5t_{CCLK} - 1.5$	$0.5t_{CCLK} + 6.0$	$0.5t_{CCLK} - 1.5$	$0.5t_{CCLK} + 6.0$	ns
t_{SDCEN}	Command Enable After CLKIN	2	5	2	5	ns
$t_{SDSDKTR}$	SDCLK Three-State After CLKIN	0	3	0	3	ns
$t_{SDSDKEN}$	SDCLK Enable After CLKIN	1	4	1	4	ns
t_{SDATR}	Address Three-State After CLKIN	$-0.25\ t_{CCLK} - 5$	$-0.25t_{CCLK}$	$-0.25\ t_{CCLK} - 5$	$-0.25t_{CCLK}$	ns
t_{SDAEN}	Address Enable After CLKIN	−0.4	+7.2	−0.4	+7.2	ns

[1] For the second, third, and fourth rising edges of SDCLK delay from CLKIN, add appropriate number of SDCLK period to the t_{DSDK1} and t_{SSDKC1} values, depending upon the SDCKR value and the core clock to CLKIN ratio.
[2] Subtract t_{CCLK} from result if value is greater than or equal to t_{CCLK}.
[3] Command = SDCKE, $\overline{MSx}$, DQM, $\overline{RAS}$, $\overline{CAS}$, SDA10, and $\overline{SDWE}$.
[4] SDRAM Controller adds one SDRAM CLK three-stated cycle delay on a read, followed by a write.
[5] Valid when DSP transitions to SDRAM master from SDRAM slave.

SDRAM Interface — Bus Slave

These timing requirements allow a bus slave to sample the bus master's SDRAM command and detect when a refresh occurs:

Table 27. SDRAM Interface — Bus Slave

Parameter		Min	Max	Unit
Timing Requirements				
t_{SSDKC1}	First SDCLK Rise after CLKOUT[1, 2, 3]	$SDCK \times t_{CCLK} - 0.5t_{CCLK} - 0.5$	$SDCKR \times t_{CCLK} - 0.25t_{CCLK} + 2.0$	ns
t_{SCSDK}	Command Setup before SDCLK[4]	2		ns
t_{HCSDK}	Command Hold after SDCLK[4]	1		ns

[1] For the second, third, and fourth rising edges of SDCLK delay from CLKOUT, add appropriate number of SDCLK period to the t_{DSDK1} and t_{SSDKC1} values, depending upon the SDCKR value and the Core clock to CLKOUT ratio.
[2] SDCKR = 1 for SDCLK equal to core clock frequency and SDCKR = 2 for SDCLK equal to half core clock frequency.
[3] Subtract t_{CCLK} from result if value is greater than or equal to t_{CCLK}.
[4] Command = SDCKE, $\overline{RAS}$, $\overline{CAS}$, and $\overline{SDWE}$.

Table 29. Link Ports — Transmit

Parameter		Min	Max	Unit
Timing Requirements				
t_{SLACH}	LACK Setup Before LCLK High	8		ns
t_{HLACH}	LACK Hold After LCLK High	–2		ns
Switching Characteristics				
t_{DLDCH}	Data Delay After LCLK High		3	ns
t_{HLDCH}	Data Hold After LCLK High	0		ns
$t_{LCLKTWL}$	LCLK Width Low	$0.5t_{LCLK}$–1.0	$0.5t_{LCLK}$+1.0	ns
$t_{LCLKTWH}$	LCLK Width High	$0.5t_{LCLK}$–1.0	$0.5t_{LCLK}$+1.0	ns
t_{DLACLK}	LCLK Low Delay After LACK High	$0.5t_{LCLK}$+3	$3t_{LCLK}$+11	ns

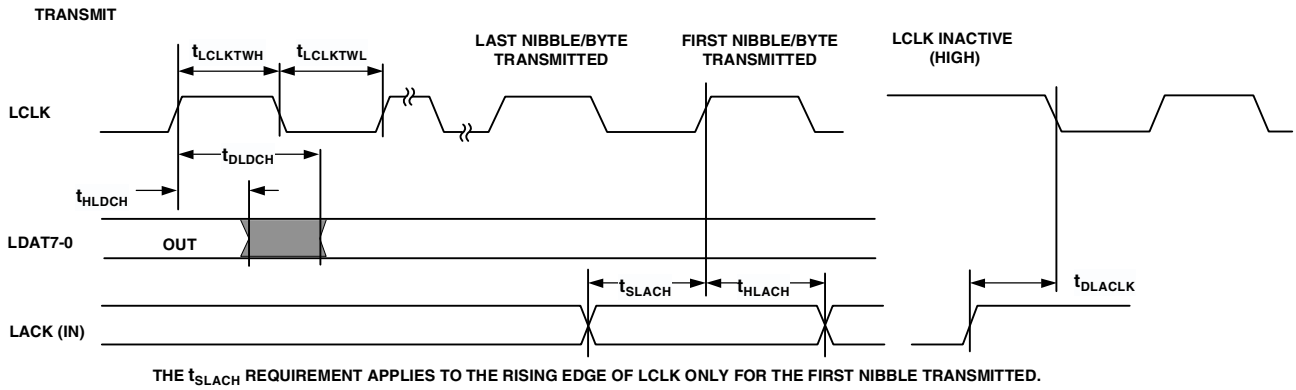

Figure 28. Link Ports—Transmit

Table 34. Serial Ports —– Enable and Three-State

Parameter		Min	Max	Unit
Switching Characteristics				
t_{DDTEN}	Data Enable from External Transmit SCLK[1, 2]	4		ns
t_{DDTTE}	Data Disable from External Transmit SCLK[1]		10	ns
t_{DDTIN}	Data Enable from Internal Transmit SCLK[1]	0		ns
t_{DDTTI}	Data Disable from Internal Transmit SCLK[1]		3	ns

[1] Referenced to drive edge.
[2] SCLK/FS Configured as a transmit clock/frame sync with the DDIR bit = 1 in SPCTLx register.

Table 35. Serial Ports — External Late Frame Sync

Parameter		Min	Max	Unit
Switching Characteristics				
$t_{DDTLFSE}$	Data Delay from Late External Transmit FS or External Receive FS with MCE = 1, MFD = 0[1]		13	ns
$t_{DDTENFS}$	Data Enable from Late FS or MCE = 1, MFD = 0[1]	0.5		ns

[1] MCE = 1, Transmit FS enable and Transmit FS valid follow $t_{DDTLFSE}$ and $t_{DDTENFS}$.

JTAG Test Access Port and Emulation

Table 38. JTAG Test Access Port and Emulation

Parameter		Min	Max	Unit
Timing Requirements				
t_{TCK}	TCK Period	t_{CK}		ns
t_{STAP}	TDI, TMS Setup Before TCK High	5		ns
t_{HTAP}	TDI, TMS Hold After TCK High	6		ns
t_{SSYS}	System Inputs Setup Before TCK Low[1]	2		ns
t_{HSYS}	System Inputs Hold After TCK Low[1]	15		ns
t_{TRSTW}	$\overline{TRST}$ Pulsewidth	$4t_{CK}$		ns
Switching Characteristics				
t_{DTDO}	TDO Delay from TCK Low		13	ns
t_{DSYS}	System Outputs Delay After TCK Low[2]		30	ns

[1] System Inputs = DATA47–16, ADDR23–0, $\overline{RD}$, $\overline{WR}$, ACK, RPBA, $\overline{SPIDS}$, EBOOT, LBOOT, $\overline{DMAR2–1}$, CLK_CFG1–0, $\overline{CLKDBL}$, $\overline{CS}$, $\overline{HBR}$, $\overline{SBTS}$, ID2–0, $\overline{IRQ2–0}$, $\overline{RESET}$, $\overline{BMS}$, MISO, MOSI, SPICLK, DxA, DxB, SCLKx, FSx, LxDAT7–0, LxCLK, LxACK, $\overline{SDWE}$, $\overline{HBG}$, $\overline{RAS}$, $\overline{CAS}$, SDCLK0, SDCKE, BRST, $\overline{BR6–1}$, $\overline{PA}$, $\overline{MS3–0}$, FLAG11–0.
[2] System Outputs = $\overline{BMS}$, MISO, MOSI, SPICLK, DxA, DxB, SCLKx, FSx, LxDAT7–0, LxCLK, LxACK, DATA47–16, $\overline{SDWE}$, ACK, $\overline{HBG}$, $\overline{RAS}$, $\overline{CAS}$, SDCLK1–0, SDCKE, BRST, $\overline{RD}$, $\overline{WR}$, $\overline{BR6–1}$, $\overline{PA}$, $\overline{MS3–0}$, ADDR23–0, FLAG11–0, $\overline{DMAG2–1}$, DQM, REDY, CLKOUT, SDA10, TIMEXP, $\overline{EMU}$, BMSTR, $\overline{RSTOUT}$.

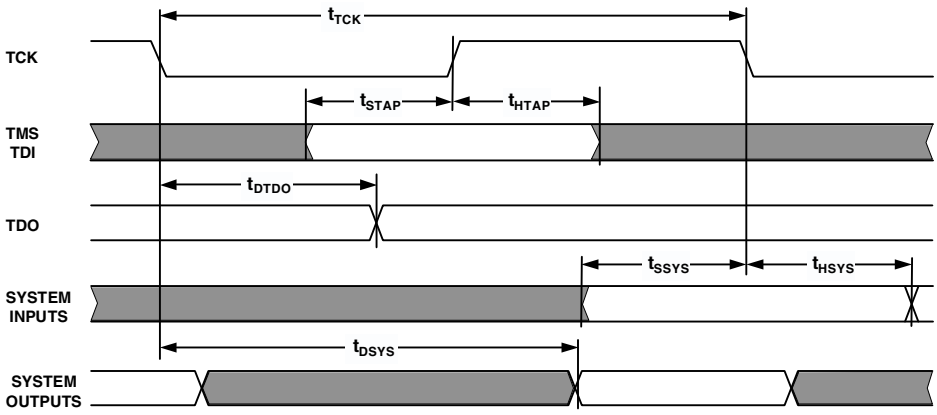

Figure 33. JTAG Test Access Port and Emulation

OUTLINE DIMENSIONS

The ADSP-21161N comes in a 17 mm × 17 mm, 225-ball CSP_BGA package with 15 rows of balls.

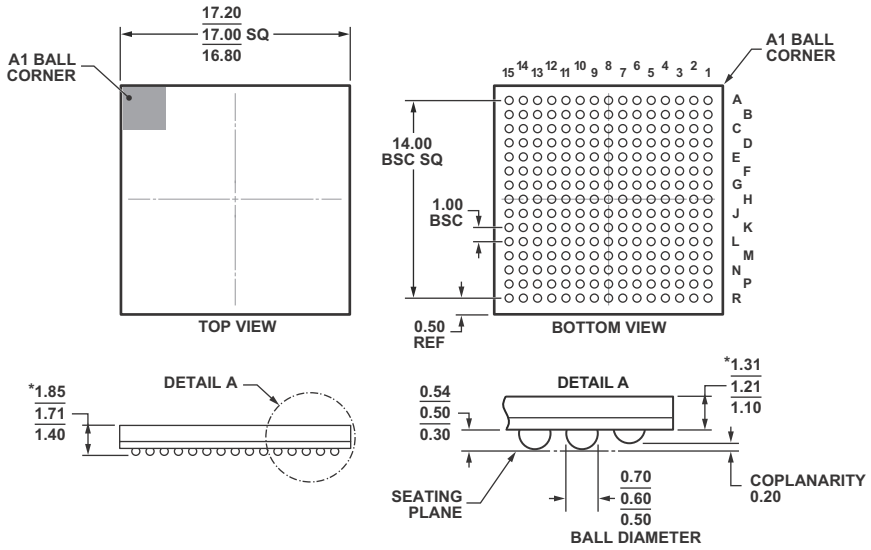

Figure 42. 225-Ball CSP_BGA (BC-225-1)

SURFACE-MOUNT DESIGN

Table 41 is provided as an aid to PCB design. For industry standard design recommendations, refer to IPC-7351, *Generic Requirements for Surface-Mount Design and Land Pattern Standard.*

Table 41. BGA Data for Use with Surface-Mount Design

Package	Ball Attach Type	Solder Mask Opening	Ball Pad Size
225-Ball CSP_BGA (BC-225-1)	Solder Mask Defined	0.40 mm diameter	0.53 mm diameter

ORDERING GUIDE

Model[1]	Temperature Range[2]	Instruction Rate	On-Chip SRAM	Package Description	Package Option
ADSP-21161NKCA-100	0°C to 85°C	100 MHz	1M bit	225-Ball CSP_BGA	BC-225-1
ADSP-21161NCCA-100	–40°C to +105°C	100 MHz	1M bit	225-Ball CSP_BGA	BC-225-1
ADSP-21161NKCAZ100	0°C to 85°C	100 MHz	1M bit	225-Ball CSP_BGA	BC-225-1
ADSP-21161NCCAZ100	–40°C to +105°C	100 MHz	1M bit	225-Ball CSP_BGA	BC-225-1
ADSP-21161NYCAZ110	–40°C to +125°C	110 MHz	1M bit	225-Ball CSP_BGA	BC-225-1

[1] Z = RoHS Compliant Part.
[2] Referenced temperature is case temperature.

D02935-0-1/13 (C)