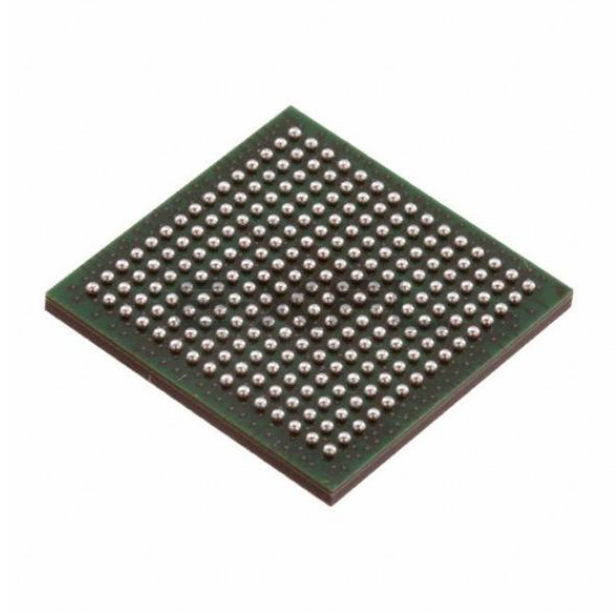

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Active
Type	Floating Point
Interface	Host Interface, Link Port, Serial Port
Clock Rate	100MHz
Non-Volatile Memory	External
On-Chip RAM	128kB
Voltage - I/O	3.30V
Voltage - Core	1.80V
Operating Temperature	-40°C ~ 105°C (TC)
Mounting Type	Surface Mount
Package / Case	255-BGA, CSPBGA
Supplier Device Package	255-CSPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-21161nccaz100

TOOLS AND SIMULATIONS

- ADSP-21161: 225 ball PBGA and MBGA Packages Silicon
- Designing with BGA
- SHARC Processors Software and Tools
- ADSP-21161N R1.1 IBIS Datafile BGA Package
- ADSP-21161N R1.2 IBIS Datafile BGA Package

REFERENCE MATERIALS

Product Selection Guide

- ADI Complementary Parts Guide - Supervisory Devices and DSP Processors

Technical Articles

- An Efficient Asynchronous Sampling-rate Conversion Algorithm for Multi-channel Audio Applications

DESIGN RESOURCES

- ADSP-21161N Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

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GENERAL DESCRIPTION

The ADSP-21161N SHARC® DSP is a low cost derivative of the ADSP-21160 featuring Analog Devices Super Harvard Architecture. Easing portability, the ADSP-21161N is source code compatible with the ADSP-21160 and with first generation ADSP-2106x SHARC processors in SISD (Single-Instruction, Single-Data) mode. Like other SHARC DSPs, the ADSP-21161N is a 32-bit processor that is optimized for high performance DSP applications. The ADSP-21161N includes a 100 MHz or 110 MHz core, a dual-ported on-chip SRAM, an integrated I/O processor with multiprocessing support, and multiple internal buses to eliminate I/O bottlenecks.

As was first offered in the ADSP-21160, the ADSP-21161N offers a single-instruction multiple-data (SIMD) architecture. Using two computational units (ADSP-2106x SHARC processors have one), the ADSP-21161N can double cycle performance versus the ADSP-2106x on a range of DSP algorithms.

Fabricated in a state of the art, high speed, low power CMOS process, the ADSP-21161N has a 10 ns or 9 ns instruction cycle time. With its SIMD computational hardware running at 110 MHz, the ADSP-21161N can perform 660 million floating-point operations per second. Table 1 shows performance benchmarks for the ADSP-21161N.

These benchmarks provide single-channel extrapolations of measured dual-channel processing performance. For more information on benchmarking and optimizing DSP code, for both single and dual-channel processing, see the Analog Devices Inc. website.

Table 1. Benchmarks

Benchmark Algorithm	100 MHz Instruction Rate	110 MHz Instruction Rate
1024 Point Complex FFT (Radix 4, with Reversal)	92 µs	83.6 µs
FIR Filter (Per Tap)	5 ns	4.5 ns
IIR Filter (Per Biquad)	20 ns	18.18 ns
Matrix Multiply (Pipelined)		
[3 × 3] × [3 × 1]	45 ns	40.9 ns
[4 × 4] × [4 × 1]	80 ns	72.72 ns
Divide (y/x)	60 ns	54.54 ns
Inverse Square Root	40 ns	36.36 ns
DMA Transfers	800M bytes/s	880M bytes/s

The ADSP-21161N continues SHARC's industry-leading standards of integration for DSPs, combining a high performance 32-bit DSP core with integrated, on-chip system features. These features include a 1M bit dual ported SRAM memory, host processor interface, I/O processor that supports 14 DMA channels, four serial ports, two link ports, SDRAM controller, SPI interface, external parallel bus, and glueless multiprocessing.

The block diagram of the ADSP-21161N on Page 1 illustrates the following architectural features:

- Two processing elements, each made up of an ALU, multiplier, shifter, and data register file
- Data address generators (DAG1, DAG2)
- Program sequencer with instruction cache
- PM and DM buses capable of supporting four 32-bit data transfers between memory and the core every core processor cycle
- Interval timer
- On-Chip SRAM (1M bit)
- SDRAM controller for glueless interface to SDRAMs
- External port that supports:
  - Interfacing to off-chip memory peripherals
  - Glueless multiprocessing support for six ADSP-21161N SHARCs
  - Host port read/write of IOP registers
- DMA controller
- Four serial ports
- Two link ports
- SPI compatible interface
- JTAG test access port
- 12 general-purpose I/O pins

Figure 2 shows a typical single-processor system. A multiprocessing system appears in Figure 5 on Page 8.

ADSP-21161N FAMILY CORE ARCHITECTURE

The ADSP-21161N includes the following architectural features of the ADSP-2116x family core. The ADSP-21161N is code compatible at the assembly level with the ADSP-21160, ADSP-21060, ADSP-21061, ADSP-21062, and ADSP-21065L.

SIMD Computational Engine

The ADSP-21161N contains two computational processing elements that operate as a single-instruction multiple-data (SIMD) engine. The processing elements are referred to as PEX and PEY, and each contains an ALU, multiplier, shifter, and register file. PEX is always active, and PEY may be enabled by setting the PEYEN mode bit in the MODE1 register. When this mode is enabled, the same instruction is executed in both processing elements, but each processing element operates on different data. This architecture is efficient at executing math intensive DSP algorithms.

Entering SIMD mode also has an effect on the way data is transferred between memory and the processing elements. When in SIMD mode, twice the data bandwidth is required to sustain computational operation in the processing elements. Because of this requirement, entering SIMD mode also doubles the bandwidth between memory and the processing elements.

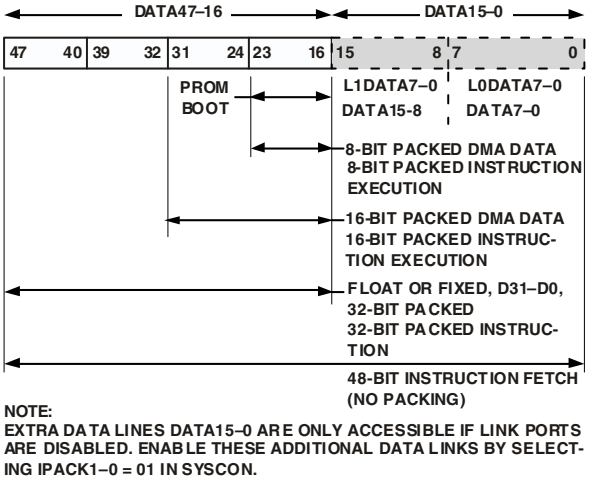

Figure 4. External Data Alignment Options

Multiprocessing

The ADSP-21161N offers powerful features tailored to multiprocessing DSP systems. The external port and link ports provide integrated glueless multiprocessing support.

The external port supports a unified address space (see Figure 3) that enables direct interprocessor accesses of each ADSP-21161N's internal memory-mapped (I/O processor) registers. All other internal memory can be indirectly accessed via DMA transfers initiated via the programming of the IOP DMA parameter and control registers. Distributed bus arbitration logic is included on-chip for simple, glueless connection of systems containing up to six ADSP-21161Ns and a host processor (Figure 5). Master processor change over incurs only one cycle of overhead. Bus arbitration is selectable as either fixed or rotating priority. Bus lock enables indivisible read-modify-write sequences for semaphores. A vector interrupt is provided for interprocessor commands. Using an instruction rate of 110 MHz, maximum throughput for interprocessor data transfer is 440M bytes/s over the external port.

Two link ports provide a second method of multiprocessing communications. Each link port can support communications to another ADSP-21161N. The ADSP-21161N, running at 110 MHz, has a maximum throughput for interprocessor communications over the links of 220M bytes/s. The link ports and cluster multiprocessing can be used concurrently or independently.

Link Ports

The ADSP-21161N features two 8-bit link ports that provide additional I/O capabilities. With the capability of running at 110 MHz, each link port can support 110M bytes/s. Link port I/O is especially useful for point-to-point interprocessor communication in multiprocessing systems. The link ports can operate independently and simultaneously, with a maximum data throughput of 220M bytes/s. Link port data is packed into 48- or 32-bit words and can be directly read by the core processor or DMA-transferred to on-chip memory. Each link port has its own double-buffered input and output registers. Clock/acknowledge handshaking controls link port transfers. Transfers are programmable as either transmit or receive.

Serial Ports

The ADSP-21161N features four synchronous serial ports that provide an inexpensive interface to a wide variety of digital and mixed-signal peripheral devices. Each serial port is made up of two data lines, a clock and frame sync. The data lines can be programmed to either transmit or receive.

The serial ports operate at up to half the clock rate of the core, providing each with a maximum data rate of 55M bit/s. The serial data pins are programmable as either a transmitter or receiver, providing greater flexibility for serial communications. Serial port data can be automatically transferred to and from on-chip memory via a dedicated DMA. Each of the serial ports features a Time Division Multiplex (TDM) multichannel mode, where two serial ports are TDM transmitters and two serial ports are TDM receivers (SPORT0 Rx paired with SPORT2 Tx, SPORT1 Rx paired with SPORT3 Tx). Each of the serial ports also support the I^2S protocol (an industry standard interface commonly used by audio codecs, ADCs and DACs), with two data pins, allowing four I^2S channels (using two I^2S stereo devices) per serial port, with a maximum of up to 16 I^2S channels. The serial ports permit little-endian or big-endian transmission formats and word lengths selectable from 3 bits to 32 bits. For I^2S mode, data-word lengths are selectable between 8 bits and 32 bits. Serial ports offer selectable synchronization and transmit modes as well as optional µ-law or A-law companding. Serial port clocks and frame syncs can be internally or externally generated.

Serial Peripheral (Compatible) Interface

Serial Peripheral Interface (SPI) is an industry standard synchronous serial link, enabling the ADSP-21161N SPI-compatible port to communicate with other SPI-compatible devices. SPI is a 4-wire interface consisting of two data pins, one device select pin, and one clock pin. It is a full-duplex synchronous serial interface, supporting both master and slave modes. The SPI port can operate in a multimaster environment by interfacing with up to four other SPI-compatible devices, either acting as a master or slave device. The ADSP-21161N SPI-compatible peripheral implementation also features programmable baud rate and clock phase/polarities. The ADSP-21161N SPI-compatible port uses open drain drivers to support a multimaster configuration and to avoid data contention.

Host Processor Interface

The ADSP-21161N host interface enables easy connection to standard 8-bit, 16-bit, or 32-bit microprocessor buses with little additional hardware required. The host interface is accessed through the ADSP-21161N's external port. Four channels of DMA are available for the host interface; code and data transfers are accomplished with low software overhead. The host processor requests the ADSP-21161N's external bus with the host bus request ($\overline{\text{HBR}}$), host bus grant ($\overline{\text{HBG}}$), and chip select (CS) signals. The host can directly read and write the internal IOP registers of the ADSP-21161N, and can access the DMA channel

(for example 10k ohm). These pins must be driven low with a strong enough drive strength (10–50 ohms) to overcome the SHARC keeper latches present on these pins. If the drive strength provided is not strong enough, data access failures can occur.

For single processor SHARC systems using this host access feature, address pins ADDR17, ADDR18, ADDR19, and ADDR20 may be tied low (for example through a 10k ohm resistor), driven low by a buffer/driver, or left floating. Any of these options is sufficient.

General-Purpose I/O Ports

The ADSP-21161N also contains 12 programmable, general purpose I/O pins that can function as either input or output. As output, these pins can signal peripheral devices; as input, these pins can provide the test for conditional branching.

Program Booting

The internal memory of the ADSP-21161N can be booted at system power-up from either an 8-bit EPROM, a host processor, the SPI interface, or through one of the link ports. Selection of the boot source is controlled by the Boot Memory Select ($\overline{BMS}$), EBOOT (EPROM Boot), and Link/Host Boot (LBOOT) pins. 8-, 16-, or 32-bit host processors can also be used for booting.

Phase-Locked Loop and Crystal Double Enable

The ADSP-21161N uses an on-chip phase-locked loop (PLL) to generate the internal clock for the core. The CLK_CFG1–0 pins are used to select ratios of 2:1, 3:1, and 4:1. In addition to the PLL ratios, the $\overline{CLKDBL}$ pin can be used for more clock ratio options. The (1×/2× CLKIN) rate set by the $\overline{CLKDBL}$ pin determines the rate of the PLL input clock and the rate at which the external port operates. With the combination of CLK_CFG1–0 and $\overline{CLKDBL}$, ratios of 2:1, 3:1, 4:1, 6:1, and 8:1 between the core and CLKIN are supported. See also Figure 8 on Page 20.

Power Supplies

The ADSP-21161N has separate power supply connections for the analog (AV_{DD}/AGND), internal (V_{DDINT}), and external (V_{DDEXT}) power supplies. The internal and analog supplies must meet the 1.8 V requirement. The external supply must meet the 3.3 V requirement. All external supply pins must be connected to the same supply.

Note that the analog supply (AV_{DD}) powers the ADSP-21161N's clock generator PLL. To produce a stable clock, provide an external circuit to filter the power input to the AV_{DD} pin. Place the filter as close as possible to the pin. The AV_{DD} filter circuit shown in Figure 6 must be added for each ADSP-21161N in the multiprocessor system. To prevent noise coupling, use a wide trace for the analog ground (AGND) signal and install a decoupling capacitor as close as possible to the pin.

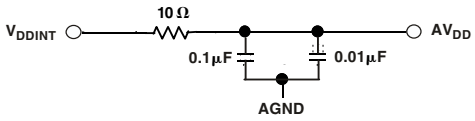

Figure 6. Analog Power (AV_{DD}) Filter Circuit

DEVELOPMENT TOOLS

Analog Devices supports its processors with a complete line of software and hardware development tools, including integrated development environments (which include CrossCore® Embedded Studio and/or VisualDSP++®), evaluation products, emulators, and a wide variety of software add-ins.

Integrated Development Environments (IDEs)

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The newest IDE, CrossCore Embedded Studio, is based on the Eclipse™ framework. Supporting most Analog Devices processor families, it is the IDE of choice for future processors, including multicore devices. CrossCore Embedded Studio seamlessly integrates available software add-ins to support real time operating systems, file systems, TCP/IP stacks, USB stacks, algorithmic software modules, and evaluation hardware board support packages. For more information visit www.analog.com/cces.

The other Analog Devices IDE, VisualDSP++, supports processor families introduced prior to the release of CrossCore Embedded Studio. This IDE includes the Analog Devices VDK real time operating system and an open source TCP/IP stack. For more information visit www.analog.com/visualdsp. Note that VisualDSP++ will not support future Analog Devices processors.

EZ-KIT Lite Evaluation Board

For processor evaluation, Analog Devices provides wide range of EZ-KIT Lite® evaluation boards. Including the processor and key peripherals, the evaluation board also supports on-chip emulation capabilities and other evaluation and development features. Also available are various EZ-Extenders®, which are daughter cards delivering additional specialized functionality, including audio and video processing. For more information visit www.analog.com and search on "ezkit" or "ezextender".

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PIN FUNCTION DESCRIPTIONS

ADSP-21161N pin definitions are listed below. Inputs identified as synchronous (S) must meet timing requirements with respect to CLKIN (or with respect to TCK for TMS, TDI). Inputs identified as asynchronous (A) can be asserted asynchronously to CLKIN (or to TCK for $\overline{\text{TRST}}$). Tie or pull unused inputs to V_{DDEXT} or GND, except for the following:

- ADDR23–0, DATA47–0, BRST, CLKOUT (Note: These pins have a logic-level hold circuit enabled on the ADSP-21161N DSP with ID2–0 = 00x.)
- $\overline{\text{PA}}$, ACK, $\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{DMARx}}$, $\overline{\text{DMAGx}}$, (ID2–0 = 00x) (Note: These pins have a pull-up enabled on the ADSP-21161N DSP with ID2–0 = 00x.)
- LxCLK, LxACK, LxDAT7–0 (LxPDRDE = 0) (Note: See Link Port Buffer Control Register Bit definitions in the ADSP-21161N *SHARC DSP Hardware Reference.*)
- DxA, DxB, SCLKx, SPICLK, MISO, MOSI, $\overline{\text{EMU}}$, TMS,$\overline{\text{TRST}}$, TDI (Note: These pins have a pull-up.)

The following symbols appear in the Type column of Table 2: A = Asynchronous, G = Ground, I = Input, O = Output, P = Power Supply, S = Synchronous, (A/D) = Active Drive, (O/D) = Open Drain, and T = Three-State (when $\overline{\text{SBTS}}$ is asserted or when the ADSP-21161N is a bus slave).

Unlike previous SHARC processors, the ADSP-21161N contains internal series resistance equivalent to 50 Ω on all input/output drivers except the CLKIN and XTAL pins. Therefore, for traces longer than six inches, external series resistors on control, data, clock, or frame sync pins are not required to dampen reflections from transmission line effects for point-to-point connections. However, for more complex networks such as a star configuration, series termination is still recommended.

Table 2. Pin Function Descriptions

Pin	Type	Function
ADDR23–0	I/O/T	**External Bus Address.** The ADSP-21161N outputs addresses for external memory and peripherals on these pins. In a multiprocessor system the bus master outputs addresses for read/writes of the IOP registers of other ADSP-21161Ns while all other internal memory resources can be accessed indirectly via DMA control (that is, accessing IOP DMA parameter registers). The ADSP-21161N inputs addresses when a host processor or multiprocessing bus master is reading or writing its IOP registers. A keeper latch on the DSP's ADDR23-0 pins maintains the input at the level it was last driven. This latch is only enabled on the ADSP-21161N with ID2–0=00x.
DATA47–16	I/O/T	**External Bus Data.** The ADSP-21161N inputs and outputs data and instructions on these pins. Pull-up resistors on unused data pins are not necessary. A keeper latch on the DSP's DATA47–16 pins maintains the input at the level it was last driven. This latch is only enabled on the ADSP-21161N with ID2–0=00x. **Note:** *DATA15–8 pins (multiplexed with L1DAT7–0) can also be used to extend the data bus if the link ports are disabled and will not be used. In addition, DATA7–0 pins (multiplexed with L0DAT7–0) can also be used to extend the data bus if the link ports are not used. This enables execution of 48-bit instructions from external SBSRAM (system clock speed-external port), SRAM (system clock speed-external port) and SDRAM (core clock or one-half the core clock speed). The IPACKx Instruction Packing Mode Bits in SYSCON should be set correctly (IPACK1–0=0x1) to enable this full instruction Width/No-packing Mode of operation.*
$\overline{\text{MS3–0}}$	I/O/T	**Memory Select Lines.** These outputs are asserted (low) as chip selects for the corresponding banks of external memory. Memory bank sizes are fixed to 16 M words for non-SDRAM and 64M words for SDRAM. The $\overline{\text{MS3–0}}$ outputs are decoded memory address lines. In asynchronous access mode, the $\overline{\text{MS3–0}}$ outputs transition with the other address outputs. In synchronous access modes, the $\overline{\text{MS3–0}}$ outputs assert with the other address lines; however, they deassert after the first CLKIN cycle in which ACK is sampled asserted. In a multiprocessor system, the $\overline{\text{MSx}}$ signals are tracked by slave SHARCs.
$\overline{\text{RD}}$	I/O/T	**Memory Read Strobe.** $\overline{\text{RD}}$ is asserted whenever ADSP-21161N reads a word from external memory or from the IOP registers of other ADSP-21161Ns. External devices, including other ADSP-21161Ns, must assert $\overline{\text{RD}}$ for reading from a word of the ADSP-21161N IOP register memory. In a multiprocessing system, $\overline{\text{RD}}$ is driven by the bus master. $\overline{\text{RD}}$ has a 20 kΩ internal pull-up resistor that is enabled for DSPs with ID2–0=00x.
$\overline{\text{WR}}$	I/O/T	**Memory Write Low Strobe.** $\overline{\text{WR}}$ is asserted when ADSP-21161N writes a word to external memory or IOP registers of other ADSP-21161Ns. External devices must assert $\overline{\text{WR}}$ for writing to ADSP-21161N IOP registers. In a multiprocessing system, the bus master drives WR. $\overline{\text{WR}}$ has a 20 kΩ internal pull-up resistor that is enabled for DSPs with ID2–0=00x.

Table 2. Pin Function Descriptions (Continued)

Pin	Type	Function
$\overline{\text{CLKDBL}}$	I	**Crystal Double Mode Enable**. This pin is used to enable the 2× clock double circuitry, where CLKOUT can be configured as either 1× or 2× the rate of CLKIN. This CLKIN double circuit is primarily intended to be used for an external crystal in conjunction with the internal clock generator and the XTAL pin. The internal clock generator when used in conjunction with the XTAL pin and an external crystal is designed to support up to a maximum of 27.5 MHz external crystal frequency. $\overline{\text{CLKDBL}}$ can be used in XTAL mode to generate a 55 MHz input into the PLL. The 2× clock mode is enabled (during $\overline{\text{RESET}}$ low) by tying $\overline{\text{CLKDBL}}$ to GND, otherwise it is connected to V_{DDEXT} for 1× clock mode. For example, this enables the use of a 27.5 MHz crystal to enable 110 MHz core clock rates and a 55 MHz CLKOUT operation when CLK_CFG0=0, CLK_CFG1=0 and $\overline{\text{CLKDBL}}$=0. This pin can also be used to generate different clock rate ratios for external clock oscillators as well. The possible clock rate ratio options (up to 110 MHz) for either CLKIN (external clock oscillator) or XTAL (crystal input) are shown in Table 3 on Page 16. An 8:1 ratio enables the use of a 12.5 MHz crystal to generate a 100 MHz core (instruction clock) rate and a 25 MHz CLKOUT (external port) clock rate. See also Figure 8 on Page 20. **Note:** *When using an external crystal, the maximum crystal frequency cannot exceed 27.5 MHz. For all other external clock sources, the maximum CLKIN frequency is 55 MHz.*
CLKOUT	O/T	**Local Clock Out**. CLKOUT is 1× or 2× and is driven at either 1× or 2× the frequency of CLKIN frequency by the current bus master. The frequency is determined by the $\overline{\text{CLKDBL}}$ pin. This output is three-stated when the ADSP-21161N is not the bus master or when the host controls the bus ($\overline{\text{HBG}}$ asserted). A keeper latch on the DSP's CLKOUT pin maintains the output at the level it was last driven. This latch is only enabled on the ADSP-21161N with ID2–0=00x. If $\overline{\text{CLKDBL}}$ enabled, CLKOUT=2 × CLKIN If $\overline{\text{CLKDBL}}$ disabled, CLKOUT=1 × CLKIN **Note:** *CLKOUT is only controlled by the* $\overline{\text{CLKDBL}}$ *pin and operates at either 1 × CLKIN or 2 × CLKIN.* Do not use CLKOUT in multiprocessing systems. Use CLKIN instead.
$\overline{\text{RESET}}$	I/A	**Processor Reset**. Resets the ADSP-21161N to a known state and begins execution at the program memory location specified by the hardware reset vector address. The $\overline{\text{RESET}}$ input must be asserted (low) at power-up.
$\overline{\text{RSTOUT}}$[1]	O	**Reset Out**. When $\overline{\text{RSTOUT}}$ is asserted (low), this pin indicates that the core blocks are in reset. It is deasserted 4080 cycles after $\overline{\text{RESET}}$ is deasserted indicating that the PLL is stable and locked.
TCK	I	**Test Clock (JTAG)**. Provides a clock for JTAG boundary scan.
TMS	I/S	**Test Mode Select (JTAG)**. Used to control the test state machine. TMS has a 20 kΩ internal pull-up resistor.
TDI	I/S	**Test Data Input (JTAG)**. Provides serial data for the boundary scan logic. TDI has a 20 kΩ internal pull-up resistor.
TDO	O	**Test Data Output (JTAG)**. Serial scan output of the boundary scan path.
$\overline{\text{TRST}}$	I/A	**Test Reset (JTAG)**. Resets the test state machine. $\overline{\text{TRST}}$ must be asserted (pulsed low) after power-up or held low for proper operation of the ADSP-21161N. $\overline{\text{TRST}}$ has a 20 kΩ internal pull-up resistor.
$\overline{\text{EMU}}$	O (O/D)	**Emulation Status**. Must be connected to the ADSP-21161N Analog Devices DSP Tools product line of JTAG emulators target board connector only. $\overline{\text{EMU}}$ has a 50 kΩ internal pull-up resistor.
V_{DDINT}	P	**Core Power Supply**. Nominally +1.8 V dc and supplies the DSP's core processor (14 pins).
V_{DDEXT}	P	**I/O Power Supply**. Nominally +3.3 V dc. (13 pins).
AVDD	P	**Analog Power Supply**. Nominally +1.8 V dc and supplies the DSP's internal PLL (clock generator). This pin has the same specifications as V_{DDINT}, except that added filtering circuitry is required. For more information, see Power Supplies on Page 9.
AGND	G	**Analog Power Supply Return**.
GND	G	**Power Supply Return**. (26 pins).
NC		**Do Not Connect**. Reserved pins that must be left open and unconnected. (4 pins)

[1] $\overline{\text{RSTOUT}}$ exists only for silicon revisions 1.2 and greater.

Table 3. Clock Rate Ratios

$\overline{\text{CLKDBL}}$	CLK_CFG1	CLK_CFG0	Core:CLKIN	CLKIN:CLKOUT
1	0	0	2:1	1:1
1	0	1	3:1	1:1
1	1	0	4:1	1:1
0	0	0	4:1	1:2
0	0	1	6:1	1:2
0	1	0	8:1	1:2

BOOT MODES

Table 4. Boot Mode Selection

EBOOT	LBOOT	$\overline{\text{BMS}}$	Booting Mode
1	0	Output	EPROM (Connect $\overline{\text{BMS}}$ to EPROM chip select.)
0	0	1 (Input)	Host Processor
0	1	0 (Input)	Serial Boot via SPI
0	1	1 (Input)	Link Port
0	0	0 (Input)	No Booting. Processor executes from external memory.
1	1	x (Input)	Reserved

SPECIFICATIONS

OPERATING CONDITIONS

Parameter[1]	Description	Test Conditions	100 MHz		110 MHz		Unit
			Min	Max	Min	Max	
V_{DDINT}	Internal (Core) Supply Voltage		1.71	1.89	1.71	1.89	V
AV_{DD}	Analog (PLL) Supply Voltage		1.71	1.89	1.71	1.89	V
V_{DDEXT}	External (I/O) Supply Voltage		3.13	3.47	3.13	3.47	V
V_{IH}	High Level Input Voltage[2]	@ V_{DDEXT} = Max	2.0	V_{DDEXT}+0.5	2.0	V_{DDEXT}+0.5	V
V_{IL}	Low Level Input Voltage[2]	@ V_{DDEXT} = Min	–0.5	+0.8	–0.5	+0.8	V
T_{CASE}	Case Operating Temperature[3]		–40	+105	–40	+125	°C

[1] Specifications subject to change without notice.

[2] Applies to input and bidirectional pins: DATA47–16, ADDR23–0, $\overline{MS3–0}$, $\overline{RD}$, $\overline{WR}$, ACK, $\overline{SBTS}$, $\overline{IRQ2–0}$, FLAG11–0, $\overline{HBG}$, $\overline{HBR}$, $\overline{CS}$, $\overline{DMAR1}$, $\overline{DMAR2}$, $\overline{BR6–1}$, ID2–0, RPBA, $\overline{PA}$, BRST, FSx, DxA, DxB, SCLKx, $\overline{RAS}$, $\overline{CAS}$, $\overline{SDWE}$, SDCLK0, LxDAT7–0, LxCLK, LxACK, SPICLK, MOSI, MISO, $\overline{SPIDS}$, EBOOT, LBOOT, $\overline{BMS}$, SDCKE, CLK_CFGx, $\overline{CLKDBL}$, CLKIN, $\overline{RESET}$, TRST, TCK, TMS, TDI.

[3] See Thermal Characteristics on Page 55 for information on thermal specifications.

PACKAGE INFORMATION

The information presented in Figure 7 provides details about how to read the package brand and relate it to specific product features.

Figure 7. Typical Package Brand

Table 5. Package Brand Information

Brand Key	Field Description
ADSP-21161N	Model Number
t	Temperature Range
pp	Package Type
z	RoHS Compliance Option
vvvvv.x	Assembly Lot Code
n.n	Silicon Revision
#	RoHS Compliance Designation
yyww	Date Code

ABSOLUTE MAXIMUM RATINGS

Stresses greater than those listed in Table 6 may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 6. Absolute Maximum Ratings

Parameter	Rating
Internal (Core) Supply Voltage (V_{DDINT})	–0.3 V to +2.2 V
Analog (PLL) Supply Voltage (A_{VDD})	–0.3 V to +2.2 V
External (I/O) Supply Voltage (V_{DDEXT})	–0.3 V to +4.6 V
Input Voltage	–0.5 V to V_{DDEXT} + 0.5 V
Output Voltage Swing	–0.5 V to V_{DDEXT} + 0.5 V
Load Capacitance	200 pF
Storage Temperature Range	–65°C to +150°C

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

TIMING SPECIFICATIONS

The ADSP-21161N's internal clock switches at higher frequencies than the system input clock (CLKIN). To generate the internal clock, the DSP uses an internal phase-locked loop (PLL). This PLL-based clocking minimizes the skew between the system clock (CLKIN) signal and the DSP's internal clock (the clock source for the external port logic and I/O pads).

The ADSP-21161N's internal clock (a multiple of CLKIN) provides the clock signal for timing internal memory, processor core, link ports, serial ports, and external port (as required for read/write strobes in asynchronous access mode). During reset, program the ratio between the DSP's internal clock frequency and external (CLKIN) clock frequency with the CLK_CFG1–0 and $\overline{\text{CLKDBL}}$ pins. Even though the internal clock is the clock source for the external port, it behaves as described in the Clock Rate Ratio chart in Table 3 on Page 16. To determine switching frequencies for the serial and link ports, divide down the internal clock, using the programmable divider control of each port (DIVx for the serial ports and LxCLKD for the link ports).

Note the following definitions of various clock periods that are a function of CLKIN and the appropriate ratio control (Table 7).

Figure 8 enables Core-to-CLKIN ratios of 2:1, 3:1, 4:1, 6:1, and 8:1 with external oscillator or crystal. It also shows support for CLKOUT-to-CLKIN ratios of 1:1 and 2:1.

Use the exact timing information given. Do not attempt to derive parameters from the addition or subtraction of others. While addition or subtraction would yield meaningful results for an individual device, the values given in this data sheet reflect statistical variations and worst cases. Consequently, it is not meaningful to add parameters to derive longer times.

See Figure 37 on Page 54 under Test Conditions for voltage reference levels.

Switching characteristics specify how the processor changes its signals. Circuitry external to the processor must be designed for compatibility with these signal characteristics. Switching characteristics describe what the processor will do in a given circumstance. Use switching characteristics to ensure that any timing requirement of a device connected to the processor (such as memory) is satisfied.

Timing requirements apply to signals that are controlled by circuitry external to the processor, such as the data input for a read operation. Timing requirements guarantee that the processor operates correctly with other devices.

Power-Up Sequencing — Silicon Revision 1.2 and Greater

The timing requirements for DSP startup are given in Table 10.

During the power-up sequence of the DSP, differences in the ramp-up rates and activation time between the two supplies can cause current to flow in the I/O ESD protection circuitry. To prevent damage to the ESD diode protection circuitry, Analog Devices recommends including a bootstrap Schottky diode.

The bootstrap Schottky diode is connected between the 1.8 V and 3.3 V power supplies as shown in Figure 9. It protects the ADSP-21161N from partially powering the 3.3 V supply. Including a Schottky diode will shorten the delay between the supply ramps and thus prevent damage to the ESD diode protection circuitry. With this technique, if the 1.8 V rail rises ahead of the 3.3 V rail, the Schottky diode pulls the 3.3 V rail along with the 1.8 V rail.

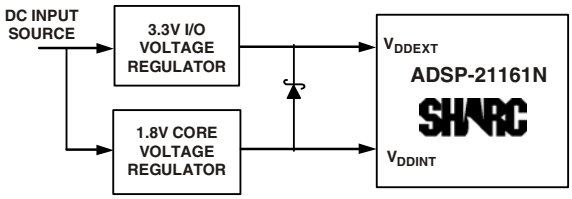


Figure 9. Dual Voltage Schottky Diode

Table 10. Power-Up Sequencing Silicon Revision 1.2 and Greater (DSP Startup)

Parameter		Min	Max	Unit
Timing Requirements				
t_{RSTVDD}	$\overline{\text{RESET}}$ Low Before V_{DDINT}/V_{DDEXT} on	0		ns
$t_{IVDDEVDD}$	V_{DDINT} on Before V_{DDEXT}	–50	+200	ms
t_{CLKVDD}	CLKIN Valid After V_{DDINT}/V_{DDEXT} Valid[1]	0	200	ms
t_{CLKRST}	CLKIN Valid Before $\overline{\text{RESET}}$ Deasserted[2]	10		µs
t_{PLLRST}	PLL Control Setup Before $\overline{\text{RESET}}$ Deasserted[3]	20		µs
t_{WRST}	Subsequent $\overline{\text{RESET}}$ Low Pulsewidth[4]	$4t_{CK}$		ns
Switching Requirements				
$t_{CORERST}$	DSP core reset deasserted after $\overline{\text{RESET}}$ deasserted	$4080t_{CK}$[3, 5]		

[1] Valid V_{DDINT}/V_{DDEXT} assumes that the supplies are fully ramped to their 1.8 and 3.3 volt rails. Voltage ramp rates can vary from microseconds to hundreds of milliseconds depending on the design of the power supply subsystem.

[2] Assumes a stable CLKIN signal, after meeting worst-case start-up timing of crystal oscillators. Refer to the crystal oscillator manufacturer's data sheet for start-up time. Assume a 25 ms maximum oscillator start-up time if using the XTAL pin and internal oscillator circuit in conjunction with an external crystal.

[3] Based on CLKIN cycles.

[4] Applies after the power-up sequence is complete. Subsequent resets require a minimum of 4 CLKIN cycles for $\overline{\text{RESET}}$ to be held low in order to properly initialize and propagate default states at all I/O pins.

[5] The 4080 cycle count depends on t_{SRST} specification in Table 12. If setup time is not met, one additional CLKIN cycle may be added to the core reset time, resulting in 4081 cycles maximum.

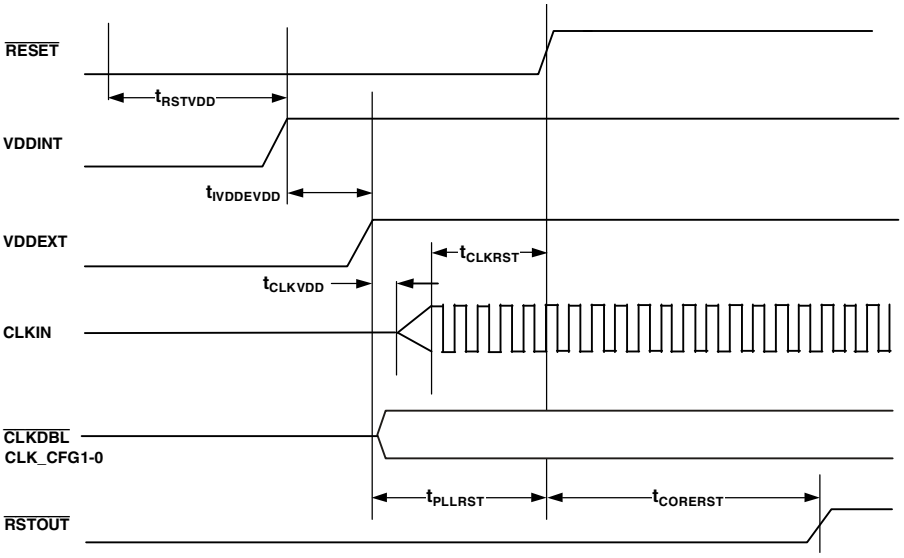


Figure 10. Power-Up Sequencing for Silicon Revision 1.2 and Greater (DSP Startup)

Clock Input

In systems that use multiprocessing or SBSRAM, $\overline{\text{CLKDBL}}$ cannot be enabled nor can the systems use an external crystal as the CLKIN source.

Do not use CLKOUT as the clock source for the SBSRAM device. Using an external crystal in conjunction with $\overline{\text{CLKDBL}}$ to generate a CLKOUT frequency is not supported. Negative hold times can result from the potential skew between CLKIN and CLKOUT.

Table 11. Clock Input

Parameter		100 MHz Min	100 MHz Max	110 MHz Min	110 MHz Max	Unit
Timing Requirements						
t_{CK}	CLKIN Period[1]	20	238	18	238	ns
t_{CKL}	CLKIN Width Low[1]	7.5	119	7	119	ns
t_{CKH}	CLKIN Width High[1]	7.5	119	7	119	ns
t_{CKRF}	CLKIN Rise/Fall (0.4 V–2.0 V)		3		3	ns
t_{CCLK}	CCLK Period	10	30	9	30	ns
Switching Characteristics						
t_{DCKOO}	CLKOUT Delay After CLKIN	0	2	0	2	ns
t_{CKOP}	CLKOUT Period	$t_{CK}-1$	$t_{CK}+1$	$t_{CK}-1$	$t_{CK}+1$	ns
t_{CKWH}	CLKOUT Width High	$t_{CKOP}/2-2$	$t_{CKOP}/2+2$	$t_{CKOP}/2-2$	$t_{CKOP}/2+2$	ns
t_{CKWL}	CLKOUT Width Low	$t_{CKOP}/2-2$	$t_{CKOP}/2+2$	$t_{CKOP}/2-2$	$t_{CKOP}/2+2$	ns

[1] CLKIN is dependent on the configuration of the CLKCFGx and $\overline{\text{CLKDBL}}$ pins to achieve desired t_{CCLK}.

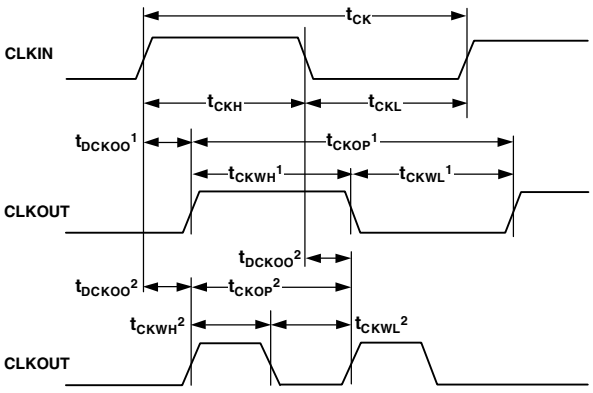


Figure 11. Clock Input

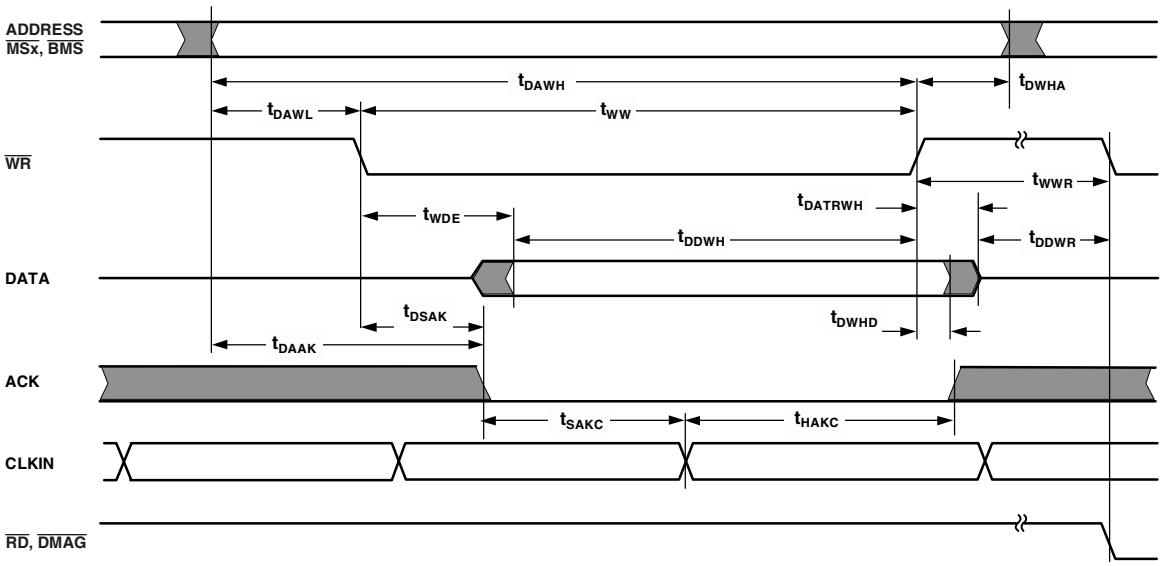


Figure 18. Memory Write — Bus Master

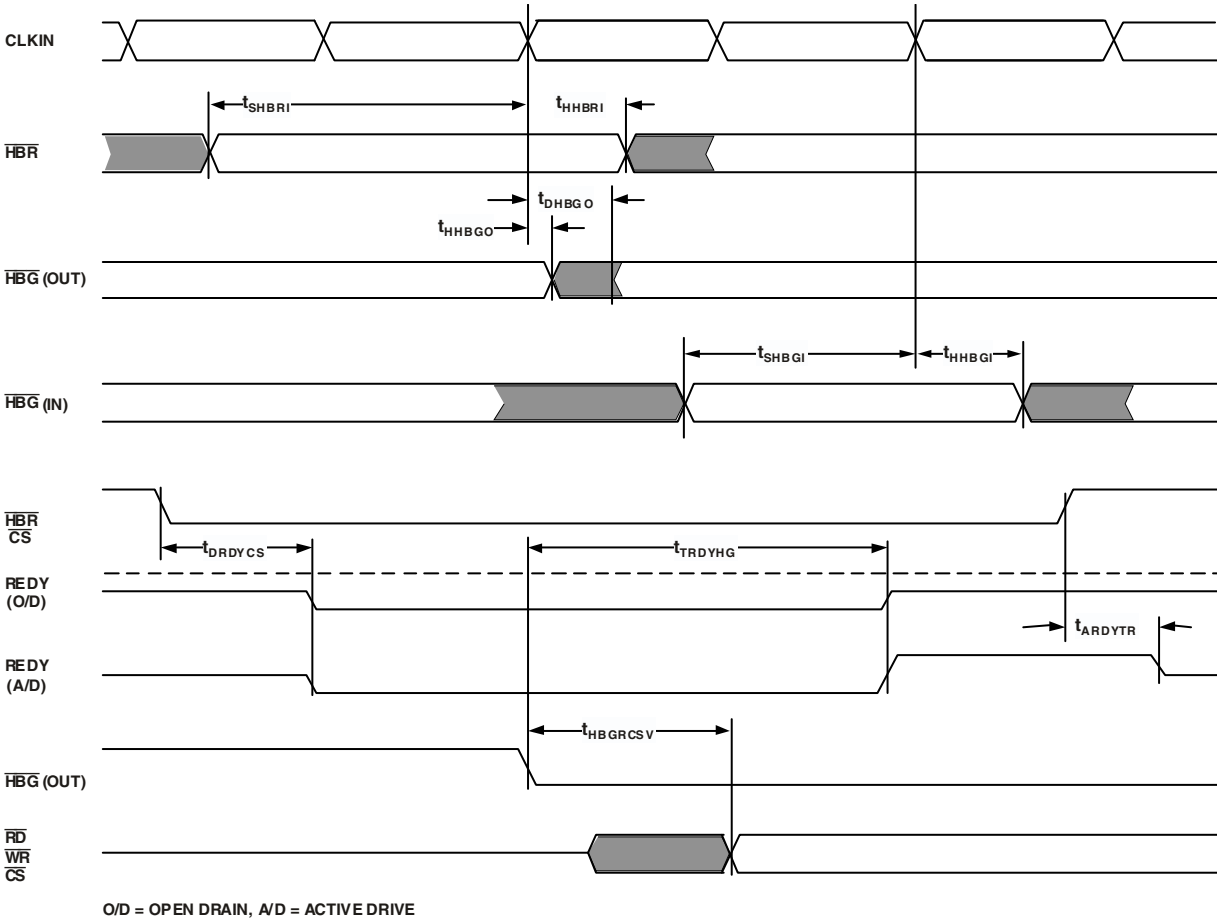


Figure 21. Host Bus Request

Multiprocessor Bus Request

Use these specifications for passing of bus mastership between multiprocessing ADSP-21161Ns ($\overline{BRx}$).

Table 21. Multiprocessor Bus Request

Parameter		Min	Max	Unit
Timing Requirements				
t_{SBRI}	$\overline{BRx}$ Setup Before CLKIN High	9		ns
t_{HBRI}	$\overline{BRx}$ Hold After CLKIN High	0.5		ns
t_{SPAI}	$\overline{PA}$ Setup Before CLKIN High	9		ns
t_{HPAI}	$\overline{PA}$ Hold After CLKIN High	1		ns
t_{SRPBAI}	RPBA Setup Before CLKIN High	6		ns
t_{HRPBAI}	RPBA Hold After CLKIN High	2		ns
Switching Characteristics				
t_{DBRO}	$\overline{BRx}$ Delay After CLKIN High		8	ns
t_{HBRO}	$\overline{BRx}$ Hold After CLKIN High	1.0		ns
t_{DPASO}	$\overline{PA}$ Delay After CLKIN High, Slave		8	ns
t_{TRPAS}	$\overline{PA}$ Disable After CLKIN High, Slave	1.5		ns
t_{DPAMO}	$\overline{PA}$ Delay After CLKIN High, Master		$0.25t_{CCLK}+9$	ns
t_{PATR}	$\overline{PA}$ Disable Before CLKIN High, Master	$0.25t_{CCLK}-5$		ns

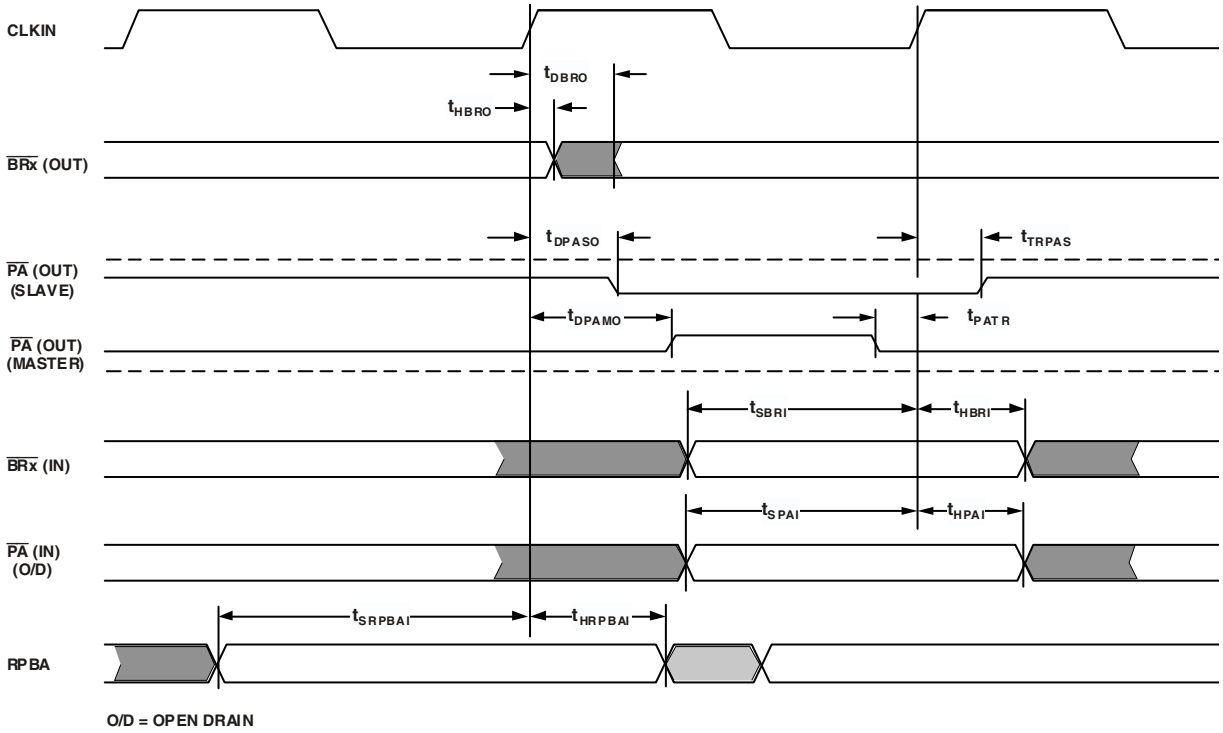


Figure 22. Multiprocessor Bus Request

Asynchronous Read/Write — Host to ADSP-21161N

Use these specifications for asynchronous host processor accesses of an ADSP-21161N, after the host has asserted $\overline{CS}$ and $\overline{HBR}$ (low). After $\overline{HBG}$ is returned by the ADSP-21161N, the host can drive the $\overline{RD}$ and $\overline{WR}$ pins to access the ADSP-21161N's IOP registers. $\overline{HBR}$ and $\overline{HBG}$ are assumed low for this timing. Although the DSP will recognize $\overline{HBR}$ asserted before reset, a $\overline{HBG}$ will not be returned by the DSP until after reset is deasserted and the DSP completes bus synchronization. **Note**: *Host internal memory access is not supported.*

Table 22. Read Cycle

Parameter		Min	Max	Unit
Timing Requirements				
t_{SADRDL}	Address Setup and $\overline{CS}$ Low Before $\overline{RD}$ Low	0		ns
t_{HADRDH}	Address Hold and $\overline{CS}$ Hold Low After $\overline{RD}$	2		ns
t_{WRWH}	$\overline{RD}$/$\overline{WR}$ High Width	3.5		ns
$t_{DRDHRDY}$	$\overline{RD}$ High Delay After REDY (O/D) Disable	0		ns
$t_{DRDHRDY}$	$\overline{RD}$ High Delay After REDY (A/D) Disable	0		ns
Switching Characteristics				
$t_{SDATRDY}$	Data Valid Before REDY Disable from Low	2		ns
$t_{DRDYRDL}$	REDY (O/D) or (A/D) Low Delay After $\overline{RD}$ Low		10	ns
t_{RDYPRD}	REDY (O/D) or (A/D) Low Pulsewidth for Read	$1.5t_{CCLK}$		ns
t_{HDARWH}	Data Disable After $\overline{RD}$ High	2	6	ns

Table 23. Write Cycle

Parameter		Min	Max	Unit
Timing Requirements				
t_{SCSWRL}	$\overline{CS}$ Low Setup Before $\overline{WR}$ Low	0		ns
t_{HCSWRH}	$\overline{CS}$ Low Hold After $\overline{WR}$ High	0		ns
t_{SADWRH}	Address Setup Before $\overline{WR}$ High	6		ns
t_{HADWRH}	Address Hold After $\overline{WR}$ High	2		ns
t_{WWRL}	$\overline{WR}$ Low Width	$t_{CCLK}+1$		ns
t_{WRWH}	$\overline{RD}$/$\overline{WR}$ High Width	3.5		ns
$t_{DWRHRDY}$	$\overline{WR}$ High Delay After REDY (O/D) or (A/D) Disable	0		ns
t_{SDATWH}	Data Setup Before $\overline{WR}$ High	5		ns
t_{HDATWH}	Data Hold After $\overline{WR}$ High	4		ns
Switching Characteristics				
$t_{DRDYWRL}$	REDY (O/D) or (A/D) Low Delay After $\overline{WR}$/$\overline{CS}$ Low[1]		11	ns
t_{RDYPWR}	REDY (O/D) or (A/D) Low Pulsewidth for Write[1]	12		ns

[1] Only when slave write FIFO is full.

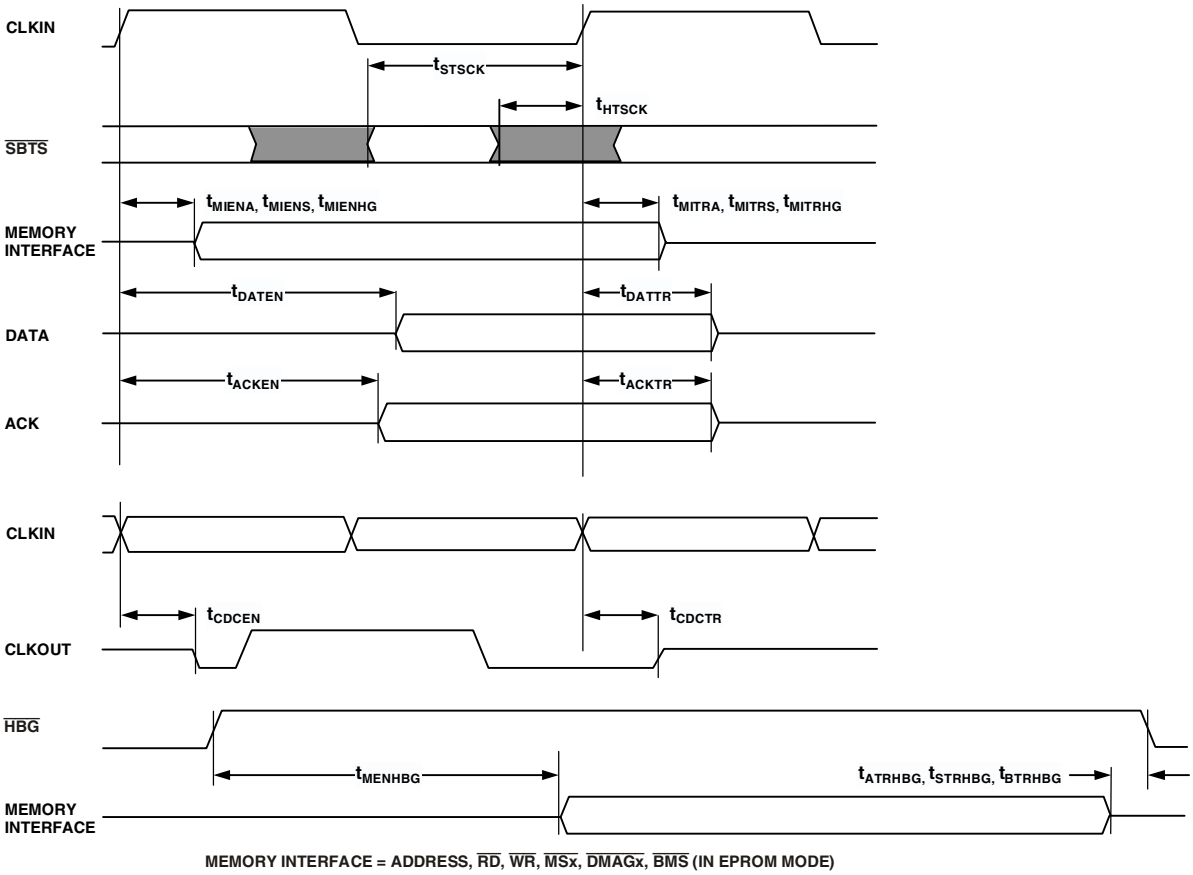


Figure 24. Three-State Timing — Bus Master, Bus Slave

Link Ports

Calculation of link receiver data setup and hold relative to link clock is required to determine the maximum allowable skew that can be introduced in the transmission path between LDATA and LCLK. Setup skew is the maximum delay that can be introduced in LDATA relative to LCLK, (setup skew = $t_{LCLKTWH}$ min – t_{DLDCH} – t_{SLDCL}). Hold skew is the maximum delay that can be introduced in LCLK relative to LDATA, (hold skew = $t_{LCLKTWL}$ min – t_{HLDCH} – t_{HLDCL}). Calculations made directly from speed specifications will result in unrealistically small skew times because they include multiple tester guardbands. The setup and hold skew times shown below are calculated to include only one tester guardband.

ADSP-21161N Setup Skew = 1.5 ns max

ADSP-21161N Hold Skew = 1.5 ns max

Note that there is a two-cycle effect latency between the link port enable instruction and the DSP enabling the link port.

Table 28. Link Ports — Receive

Parameter		Min	Max	Unit
Timing Requirements				
t_{SLDCL}	Data Setup Before LCLK Low	1		ns
t_{HLDCL}	Data Hold After LCLK Low	3.5		ns
t_{LCLKIW}	LCLK Period	t_{LCLK}		ns
$t_{LCLKRWL}$	LCLK Width Low	4.0		ns
$t_{LCLKRWH}$	LCLK Width High	4.0		ns
Switching Characteristics				
t_{DLALC}	LACK Low Delay After LCLK High[1]	8	12	ns

[1] LACK goes low with t_{DLALC} relative to rise of LCLK after first nibble, but does not go low if the receiver's link buffer is not about to fill.

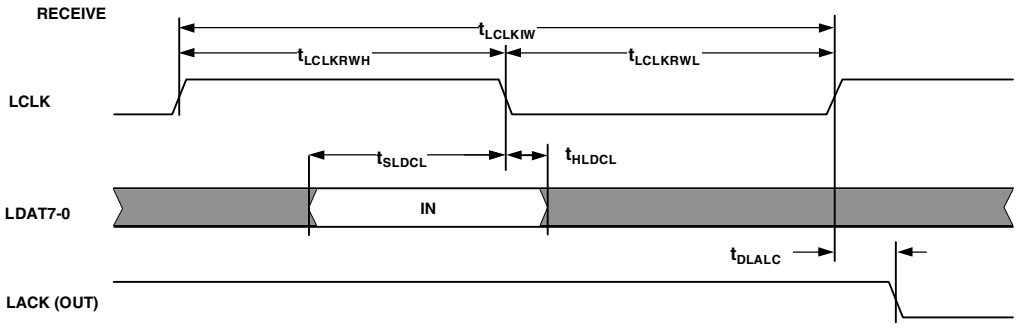


Figure 27. Link Ports—Receive

Table 34. Serial Ports —– Enable and Three-State

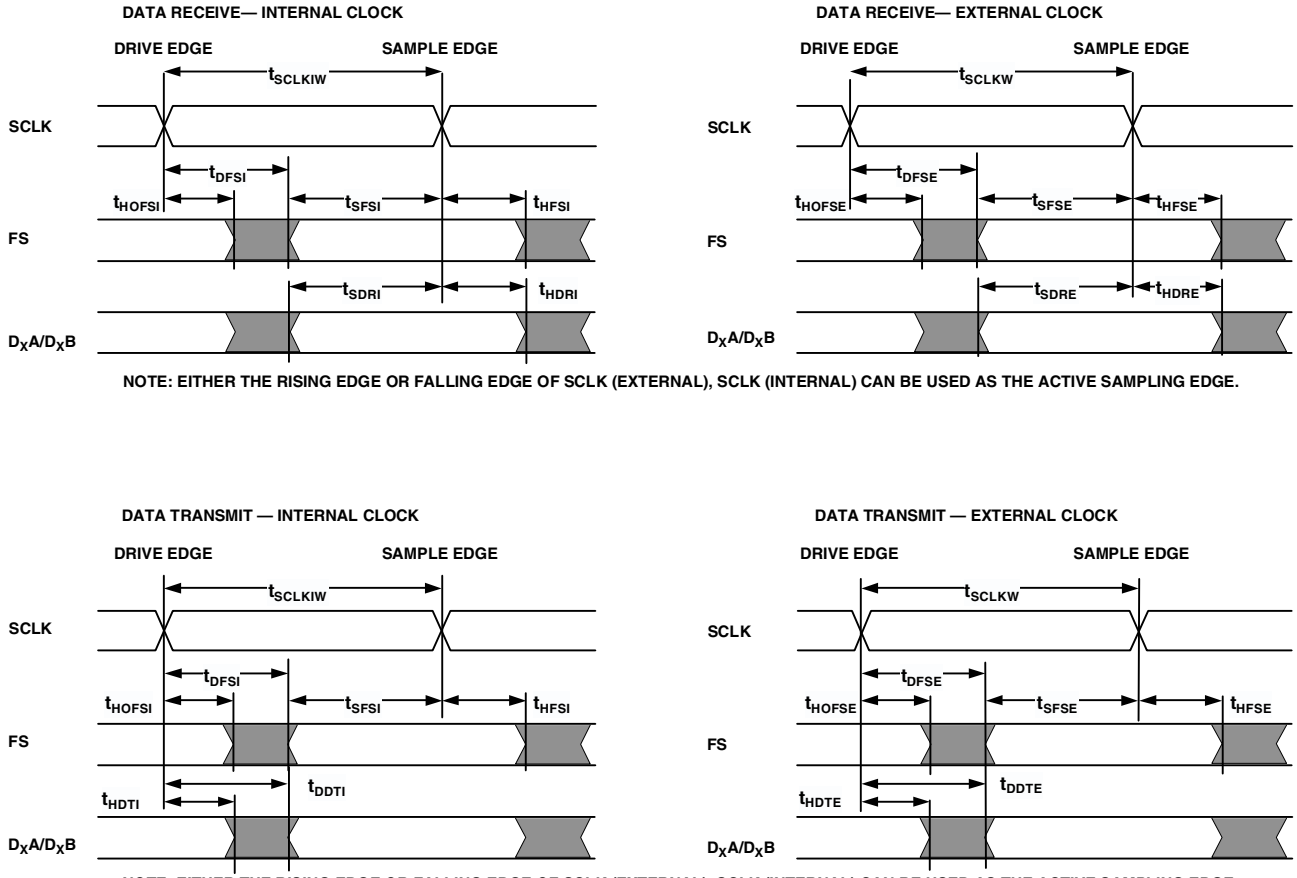
Parameter		Min	Max	Unit
Switching Characteristics				
t_{DDTEN}	Data Enable from External Transmit SCLK[1, 2]	4		ns
t_{DDTTE}	Data Disable from External Transmit SCLK[1]		10	ns
t_{DDTIN}	Data Enable from Internal Transmit SCLK[1]	0		ns
t_{DDTTI}	Data Disable from Internal Transmit SCLK[1]		3	ns

[1] Referenced to drive edge.
[2] SCLK/FS Configured as a transmit clock/frame sync with the DDIR bit = 1 in SPCTLx register.

Table 35. Serial Ports — External Late Frame Sync

Parameter		Min	Max	Unit
Switching Characteristics				
$t_{DDTLFSE}$	Data Delay from Late External Transmit FS or External Receive FS with MCE = 1, MFD = 0[1]		13	ns
$t_{DDTENFS}$	Data Enable from Late FS or MCE = 1, MFD = 0[1]	0.5		ns

[1] MCE = 1, Transmit FS enable and Transmit FS valid follow $t_{DDTLFSE}$ and $t_{DDTENFS}$.



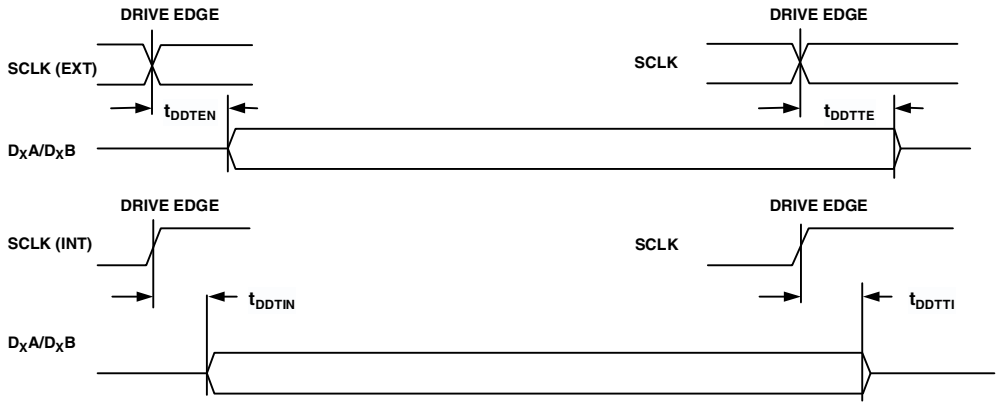


Figure 29. Serial Ports

225-BALL CSP_BGA BALL CONFIGURATIONS

Table 40. 225-Ball CSP_BGA Ball Assignments

Ball Name	Ball Number	Ball Name	Ball Number	Ball Name	Ball Number	Ball Name	Ball Number
NC	A01	$\overline{\text{TRST}}$	B01	TMS	C01	TDO	D01
BMSTR	A02	TDI	B02	$\overline{\text{EMU}}$	C02	TCK	D02
$\overline{\text{BMS}}$	A03	RPBA	B03	GND	C03	FLAG11	D03
$\overline{\text{SPIDS}}$	A04	MOSI	B04	SPICLK	C04	MISO	D04
EBOOT	A05	FS0	B05	D0B	C05	SCLK0	D05
LBOOT	A06	SCLK1	B06	D1A	C06	D1B	D06
SCLK2	A07	D2B	B07	D2A	C07	FS1	D07
D3B	A08	D3A	B08	FS2	C08	V_{DDINT}	D08
L0DAT4	A09	L0DAT7	B09	FS3	C09	SCLK3	D09
L0ACK	A10	L0CLK	B10	L0DAT6	C10	L0DAT5	D10
L0DAT2	A11	L0DAT1	B11	L1DAT7	C11	L0DAT3	D11
L1DAT6	A12	L1DAT4	B12	L1DAT3	C12	L1DAT5	D12
L1CLK	A13	L1ACK	B13	L1DAT1	C13	DATA42	D13
L1DAT2	A14	L1DAT0	B14	DATA45	C14	DATA46	D14
NC	A15	$\overline{\text{RSTOUT}}$[1]	B15	DATA47	C15	DATA44	D15
FLAG10	E01	FLAG5	F01	FLAG1	G01	FLAG0	H01
$\overline{\text{RESET}}$	E02	FLAG7	F02	FLAG2	G02	$\overline{\text{IRQ0}}$	H02
FLAG8	E03	FLAG9	F03	FLAG4	G03	V_{DDINT}	H03
D0A	E04	FLAG6	F04	FLAG3	G04	$\overline{\text{IRQ1}}$	H04
V_{DDEXT}	E05	V_{DDINT}	F05	V_{DDEXT}	G05	V_{DDINT}	H05
V_{DDINT}	E06	GND	F06	GND	G06	GND	H06
V_{DDEXT}	E07	GND	F07	GND	G07	GND	H07
V_{DDINT}	E08	GND	F08	GND	G08	GND	H08
V_{DDEXT}	E09	GND	F09	GND	G09	GND	H09
V_{DDINT}	E10	GND	F10	GND	G10	GND	H10
V_{DDEXT}	E11	V_{DDINT}	F11	V_{DDEXT}	G11	V_{DDINT}	H11
L0DAT0	E12	DATA37	F12	DATA34	G12	DATA29	H12
DATA39	E13	DATA40	F13	DATA35	G13	DATA28	H13
DATA43	E14	DATA38	F14	DATA33	G14	DATA30	H14
DATA41	E15	DATA36	F15	DATA32	G15	DATA31	H15
$\overline{\text{IRQ2}}$	J01	TIMEXP	K01	ADDR19	L01	ADDR16	M01
ID1	J02	ADDR22	K02	ADDR17	L02	ADDR12	M02
ID2	J03	ADDR20	K03	ADDR21	L03	ADDR18	M03
ID0	J04	ADDR23	K04	ADDR2	L04	ADDR6	M04
V_{DDEXT}	J05	V_{DDINT}	K05	V_{DDEXT}	L05	ADDR0	M05
GND	J06	GND	K06	V_{DDINT}	L06	$\overline{\text{MS1}}$	M06
GND	J07	GND	K07	V_{DDEXT}	L07	$\overline{\text{BR6}}$	M07
GND	J08	GND	K08	V_{DDINT}	L08	V_{DDEXT}	M08
GND	J09	GND	K09	V_{DDEXT}	L09	$\overline{\text{WR}}$	M09
GND	J10	GND	K10	V_{DDINT}	L10	SDA10	M10
V_{DDEXT}	J11	V_{DDINT}	K11	V_{DDEXT}	L11	$\overline{\text{RAS}}$	M11
DATA26	J12	DATA22	K12	$\overline{\text{CAS}}$	L12	ACK	M12
DATA24	J13	DATA19	K13	DATA20	L13	DATA17	M13
DATA25	J14	DATA21	K14	DATA16	L14	$\overline{\text{DMAG2}}$	M14
DATA27	J15	DATA23	K15	DATA18	L15	$\overline{\text{DMAG1}}$	M15