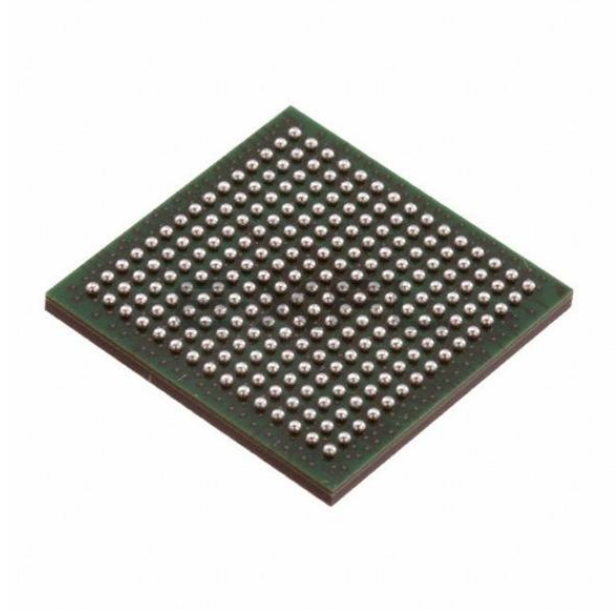

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Obsolete
Type	Floating Point
Interface	Host Interface, Link Port, Serial Port
Clock Rate	100MHz
Non-Volatile Memory	External
On-Chip RAM	128kB
Voltage - I/O	3.30V
Voltage - Core	1.80V
Operating Temperature	0°C ~ 85°C (TC)
Mounting Type	Surface Mount
Package / Case	255-BGA, CSPBGA
Supplier Device Package	255-CSPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-21161nkca-100

Instruction Cache

The ADSP-21161N includes an on-chip instruction cache that enables three-bus operation for fetching an instruction and four data values. The cache is selective—only the instructions whose fetches conflict with PM bus data accesses are cached. This cache enables full-speed execution of core, looped operations such as digital filter multiply-accumulates, and FFT butterfly processing.

Data Address Generators With Hardware Circular Buffers

The ADSP-21161N's two data address generators (DAGs) are used for indirect addressing and implementing circular data buffers in hardware. Circular buffers allow efficient programming of delay lines and other data structures required in digital signal processing, and are commonly used in digital filters and Fourier transforms. The two DAGs of the ADSP-21161N contain sufficient registers to allow the creation of up to 32 circular buffers (16 primary register sets, 16 secondary). The DAGs automatically handle address pointer wrap-around, reduce overhead, increase performance, and simplify implementation. Circular buffers can start and end at any memory location.

Flexible Instruction Set

The 48-bit instruction word accommodates a variety of parallel operations, for concise programming. For example, the ADSP-21161N can conditionally execute a multiply, an add, and a subtract in both processing elements, while branching, all in a single instruction.

ADSP-21161N MEMORY AND I/O INTERFACE FEATURES

The ADSP-21161N adds the following architectural features to the ADSP-2116x family core.

Dual-Ported On-Chip Memory

The ADSP-21161N contains one megabit of on-chip SRAM, organized as two blocks of 0.5M bits (Figure 3). Each block can be configured for different combinations of code and data storage. Each memory block is dual-ported for single-cycle, independent accesses by the core processor and I/O processor. The dual-ported memory in combination with three separate on-chip buses allow two data transfers from the core and one from the I/O processor, in a single cycle. On the ADSP-21161N, the memory can be configured as a maximum of 32K words of 32-bit data, 64K words of 16-bit data, 21K words of 48-bit instructions (or 40-bit data), or combinations of different word sizes up to one megabit. All of the memory can be accessed as 16-bit, 32-bit, 48-bit, or 64-bit words. A 16-bit floating-point storage format is supported that effectively doubles the amount of data that may be stored on-chip. Conversion between the 32-bit floating-point and 16-bit floating-point formats is done in a single instruction. While each memory block can store combinations of code and data, accesses are most efficient when one block stores data using the DM bus for transfers, and the other block stores instructions and data using the PM bus for transfers. Using the DM bus and PM bus, with one dedicated to each memory block, assures single-cycle execution with two data transfers. In this case, the instruction must be available in the cache.

Off-Chip Memory and Peripherals Interface

The ADSP-21161N's external port provides the processor's interface to off-chip memory and peripherals. The 62.7-M word off-chip address space (254.7-M word if all SDRAM) is included in the ADSP-21161N's unified address space. The separate on-chip buses—for PM addresses, PM data, DM addresses, DM data, I/O addresses, and I/O data—are multiplexed at the external port to create an external system bus with a single 24-bit address bus and a single 32-bit data bus. Every access to external memory is based on an address that fetches a 32-bit word. When fetching an instruction from external memory, two 32-bit data locations are being accessed for packed instructions. Unused link port lines can also be used as additional data lines DATA15–DATA0, allowing single-cycle execution of instructions from external memory, at up to 110 MHz. Figure 4 shows the alignment of various accesses to external memory.

The external port supports asynchronous, synchronous, and synchronous burst accesses. Synchronous burst SRAM can be interfaced gluelessly. The ADSP-21161N also can interface gluelessly to SDRAM. Addressing of external memory devices is facilitated by on-chip decoding of high-order address lines to generate memory bank select signals. The ADSP-21161N provides programmable memory wait states and external memory acknowledge controls to allow interfacing to memory and peripherals with variable access, hold, and disable time requirements.

SDRAM Interface

The SDRAM interface enables the ADSP-21161N to transfer data to and from synchronous DRAM (SDRAM) at the core clock frequency or at one-half the core clock frequency. The synchronous approach, coupled with the core clock frequency, supports data transfer at a high throughput—up to 440M bytes/s for 32-bit transfers and up to 660M bytes/s for 48-bit transfers.

The SDRAM interface provides a glueless interface with standard SDRAMs—16Mb, 64Mb, 128Mb, and 256Mb— and includes options to support additional buffers between the ADSP-21161N and SDRAM. The SDRAM interface is extremely flexible and provides capability for connecting SDRAMs to any one of the ADSP-21161N's four external memory banks, with up to all four banks mapped to SDRAM.

Systems with several SDRAM devices connected in parallel may require buffering to meet overall system timing requirements. The ADSP-21161N supports pipelining of the address and control signals to enable such buffering between itself and multiple SDRAM devices.

Target Board JTAG Emulator Connector

Analog Devices DSP Tools product line of JTAG emulators uses the IEEE 1149.1 JTAG test access port of the ADSP-21161N processor to monitor and control the target board processor during emulation. Analog Devices DSP Tools product line of

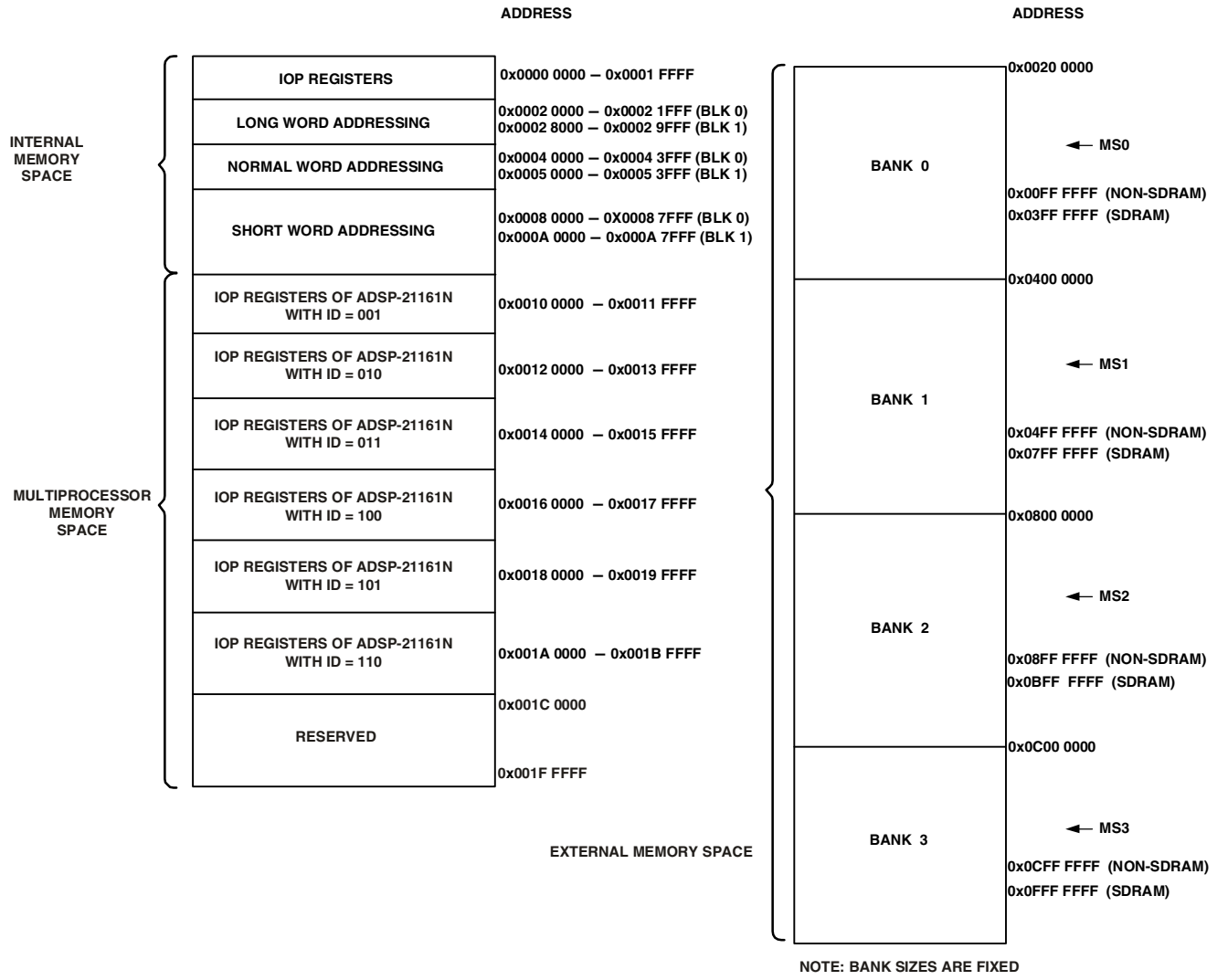


Figure 3. Memory Map

JTAG emulators provides emulation at full processor speed, allowing inspection and modification of memory, registers, and processor stacks. The processor's JTAG interface ensures that the emulator will not affect target system loading or timing.

For complete information on SHARC Analog Devices DSP Tools product line of JTAG emulator operation, see the appropriate Emulator Hardware User's Guide. For detailed information on the interfacing of Analog Devices JTAG emulators with Analog Devices DSP products with JTAG emulation ports, please refer to Engineer to Engineer Note *EE-68: Analog Devices JTAG Emulation Technical Reference*. Both of these documents can be found on the Analog Devices website.

DMA Controller

The ADSP-21161N's on-chip DMA controller enables zero-overhead data transfers without processor intervention. The DMA controller operates independently and invisibly to the processor core, allowing DMA operations to occur while the core is simultaneously executing its program instructions. DMA transfers can occur between the ADSP-21161N's internal memory and external memory, external peripherals, or a host processor. DMA transfers can also occur between the ADSP-21161N's internal memory and its serial ports, link ports, or the SPI-compatible (Serial Peripheral Interface) port. External bus packing and unpacking of 32-, 48-, or 64-bit words in internal memory is performed during DMA transfers from either 8-, 16-, or 32-bit wide external memory. Fourteen channels of DMA are available on the ADSP-21161N—two are shared between the SPI interface and the link ports, eight via the serial ports, and four via the processor's external port (for host processor, other ADSP-21161Ns, memory, or I/O transfers). Programs can be downloaded to the ADSP-21161N using DMA transfers. Asynchronous off-chip peripherals can control two DMA channels using DMA Request/Grant lines ($\overline{\text{DMAR2–1}}$, $\overline{\text{DMAG2–1}}$). Other DMA features include interrupt generation upon completion of DMA transfers, and DMA chaining for automatic linked DMA transfers.

Core Embedded Studio or VisualDSP++ installed (sold separately), engineers can develop software for supported EZ-KITs or any custom system utilizing supported Analog Devices processors.

Software Add-Ins for CrossCore Embedded Studio

Analog Devices offers software add-ins which seamlessly integrate with CrossCore Embedded Studio to extend its capabilities and reduce development time. Add-ins include board support packages for evaluation hardware, various middleware packages, and algorithmic modules. Documentation, help, configuration dialogs, and coding examples present in these add-ins are viewable through the CrossCore Embedded Studio IDE once the add-in is installed.

Board Support Packages for Evaluation Hardware

Software support for the EZ-KIT Lite evaluation boards and EZ-Extender daughter cards is provided by software add-ins called Board Support Packages (BSPs). The BSPs contain the required drivers, pertinent release notes, and select example code for the given evaluation hardware. A download link for a specific BSP is located on the web page for the associated EZ-KIT or EZ-Extender product. The link is found in the *Product Download* area of the product web page.

Middleware Packages

Analog Devices separately offers middleware add-ins such as real time operating systems, file systems, USB stacks, and TCP/IP stacks. For more information see the following web pages:

- www.analog.com/ucos3
- www.analog.com/ucfs
- www.analog.com/ucusbd
- www.analog.com/lwip

Algorithmic Modules

To speed development, Analog Devices offers add-ins that perform popular audio and video processing algorithms. These are available for use with both CrossCore Embedded Studio and VisualDSP++. For more information visit www.analog.com and search on “Blackfin software modules” or “SHARC software modules”.

Designing an Emulator-Compatible DSP Board (Target)

For embedded system test and debug, Analog Devices provides a family of emulators. On each JTAG DSP, Analog Devices supplies an IEEE 1149.1 JTAG Test Access Port (TAP). In-circuit emulation is facilitated by use of this JTAG interface. The emulator accesses the processor’s internal features via the processor’s TAP, allowing the developer to load code, set breakpoints, and view variables, memory, and registers. The processor must be halted to send data and commands, but once an operation is completed by the emulator, the DSP system is set to run at full speed with no impact on system timing. The emulators require the target board to include a header that supports connection of the DSP’s JTAG port to the emulator.

For details on target board design issues including mechanical layout, single processor connections, signal buffering, signal termination, and emulator pod logic, see the *EE-68: Analog Devices JTAG Emulation Technical Reference* on the Analog Devices website (www.analog.com)—use site search on “EE-68.” This document is updated regularly to keep pace with improvements to emulator support.

ADDITIONAL INFORMATION

This data sheet provides a general overview of the ADSP-21161N architecture and functionality. For detailed information on the ADSP-2116x Family core architecture and instruction set, refer to the *ADSP-21161 SHARC DSP Hardware Reference* and the *ADSP-21160 SHARC DSP Instruction Set Reference*.

RELATED SIGNAL CHAINS

A *signal chain* is a series of signal-conditioning electronic components that receive input (data acquired from sampling either real-time phenomena or from stored data) in tandem, with the output of one portion of the chain supplying input to the next. Signal chains are often used in signal processing applications to gather and process data or to apply system controls based on analysis of real-time phenomena. For more information about this term and related topics, see the “signal chain” entry in Wikipedia or the Glossary of EE Terms on the Analog Devices website.

Analog Devices eases signal processing system development by providing signal processing components that are designed to work together well. A tool for viewing relationships between specific applications and related components is available on the www.analog.com website.

The Application Signal Chains page in the Circuits from the Lab™ site (http://www.analog.com/signal chains) provides:

- Graphical circuit block diagram presentation of signal chains for a variety of circuit types and applications
- Drill down links for components in each chain to selection guides and application information
- Reference designs applying best practice design techniques

Table 2. Pin Function Descriptions (Continued)

Pin	Type	Function
$\overline{\text{CLKDBL}}$	I	**Crystal Double Mode Enable**. This pin is used to enable the 2× clock double circuitry, where CLKOUT can be configured as either 1× or 2× the rate of CLKIN. This CLKIN double circuit is primarily intended to be used for an external crystal in conjunction with the internal clock generator and the XTAL pin. The internal clock generator when used in conjunction with the XTAL pin and an external crystal is designed to support up to a maximum of 27.5 MHz external crystal frequency. $\overline{\text{CLKDBL}}$ can be used in XTAL mode to generate a 55 MHz input into the PLL. The 2× clock mode is enabled (during $\overline{\text{RESET}}$ low) by tying $\overline{\text{CLKDBL}}$ to GND, otherwise it is connected to V_{DDEXT} for 1× clock mode. For example, this enables the use of a 27.5 MHz crystal to enable 110 MHz core clock rates and a 55 MHz CLKOUT operation when CLK_CFG0=0, CLK_CFG1=0 and $\overline{\text{CLKDBL}}$=0. This pin can also be used to generate different clock rate ratios for external clock oscillators as well. The possible clock rate ratio options (up to 110 MHz) for either CLKIN (external clock oscillator) or XTAL (crystal input) are shown in Table 3 on Page 16. An 8:1 ratio enables the use of a 12.5 MHz crystal to generate a 100 MHz core (instruction clock) rate and a 25 MHz CLKOUT (external port) clock rate. See also Figure 8 on Page 20. **Note:** *When using an external crystal, the maximum crystal frequency cannot exceed 27.5 MHz. For all other external clock sources, the maximum CLKIN frequency is 55 MHz.*
CLKOUT	O/T	**Local Clock Out**. CLKOUT is 1× or 2× and is driven at either 1× or 2× the frequency of CLKIN frequency by the current bus master. The frequency is determined by the $\overline{\text{CLKDBL}}$ pin. This output is three-stated when the ADSP-21161N is not the bus master or when the host controls the bus ($\overline{\text{HBG}}$ asserted). A keeper latch on the DSP's CLKOUT pin maintains the output at the level it was last driven. This latch is only enabled on the ADSP-21161N with ID2–0=00x. If $\overline{\text{CLKDBL}}$ enabled, CLKOUT=2 × CLKIN If $\overline{\text{CLKDBL}}$ disabled, CLKOUT=1 × CLKIN **Note:** *CLKOUT is only controlled by the* $\overline{\text{CLKDBL}}$ *pin and operates at either 1 × CLKIN or 2 × CLKIN.* Do not use CLKOUT in multiprocessing systems. Use CLKIN instead.
$\overline{\text{RESET}}$	I/A	**Processor Reset**. Resets the ADSP-21161N to a known state and begins execution at the program memory location specified by the hardware reset vector address. The $\overline{\text{RESET}}$ input must be asserted (low) at power-up.
$\overline{\text{RSTOUT}}$[1]	O	**Reset Out**. When $\overline{\text{RSTOUT}}$ is asserted (low), this pin indicates that the core blocks are in reset. It is deasserted 4080 cycles after $\overline{\text{RESET}}$ is deasserted indicating that the PLL is stable and locked.
TCK	I	**Test Clock (JTAG)**. Provides a clock for JTAG boundary scan.
TMS	I/S	**Test Mode Select (JTAG)**. Used to control the test state machine. TMS has a 20 kΩ internal pull-up resistor.
TDI	I/S	**Test Data Input (JTAG)**. Provides serial data for the boundary scan logic. TDI has a 20 kΩ internal pull-up resistor.
TDO	O	**Test Data Output (JTAG)**. Serial scan output of the boundary scan path.
$\overline{\text{TRST}}$	I/A	**Test Reset (JTAG)**. Resets the test state machine. $\overline{\text{TRST}}$ must be asserted (pulsed low) after power-up or held low for proper operation of the ADSP-21161N. $\overline{\text{TRST}}$ has a 20 kΩ internal pull-up resistor.
$\overline{\text{EMU}}$	O (O/D)	**Emulation Status**. Must be connected to the ADSP-21161N Analog Devices DSP Tools product line of JTAG emulators target board connector only. $\overline{\text{EMU}}$ has a 50 kΩ internal pull-up resistor.
V_{DDINT}	P	**Core Power Supply**. Nominally +1.8 V dc and supplies the DSP's core processor (14 pins).
V_{DDEXT}	P	**I/O Power Supply**. Nominally +3.3 V dc. (13 pins).
AVDD	P	**Analog Power Supply**. Nominally +1.8 V dc and supplies the DSP's internal PLL (clock generator). This pin has the same specifications as V_{DDINT}, except that added filtering circuitry is required. For more information, see Power Supplies on Page 9.
AGND	G	**Analog Power Supply Return**.
GND	G	**Power Supply Return**. (26 pins).
NC		**Do Not Connect**. Reserved pins that must be left open and unconnected. (4 pins)

[1] $\overline{\text{RSTOUT}}$ exists only for silicon revisions 1.2 and greater.

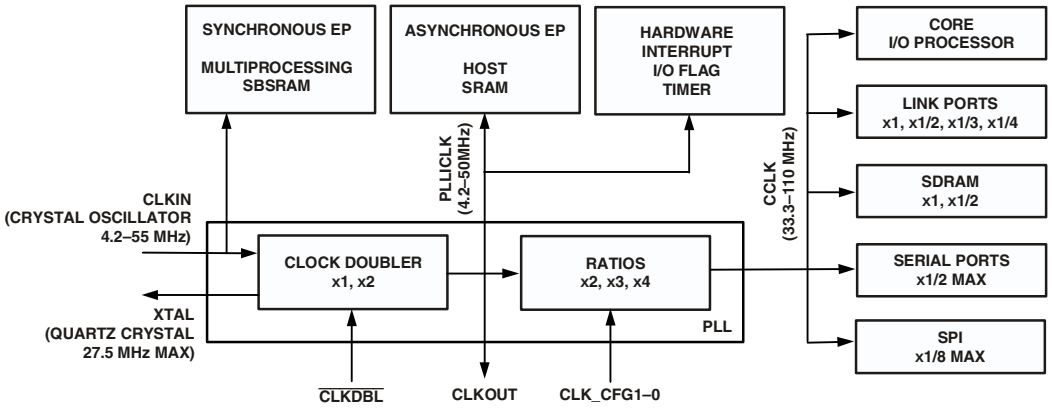


Figure 8. Core Clock and System Clock Relationship to CLKIN

Table 7. CLKOUT and CCLK Clock Generation Operation

Timing Requirements	Description[1]	Calculation
CLKIN	Input Clock	$1/t_{CK}$
CLKOUT	External Port System Clock	$1/t_{CKOP}$
PLLICLK	PLL Input Clock	$1/t_{PLLIN}$
CCLK	Core Clock	$1/t_{CCLK}$
t_{CK}	CLKIN Clock Period	1/CLKIN
t_{CCLK}	(Processor) Core Clock Period	1/CCLK
t_{LCLK}	Link Port Clock Period	$(t_{CCLK}) \times LR$
t_{SCLK}	Serial Port Clock Period	$(t_{CCLK}) \times SR$
t_{SDK}	SDRAM Clock Period	$(t_{CCLK}) \times SDCKR$
t_{SPICLK}	SPI Clock Period	$(t_{CCLK}) \times SPIR$

[1] where:
LR = link port-to-core clock ratio (1, 2, 3, or 1:4, determined by LxCLKD)
SR = serial port-to-core clock ratio (wide range, determined by CLKDIV)
SDCKR = SDRAM-to-Core Clock Ratio (1:1 or 1:2, determined by SDCTL register)
SPIR = SPI-to-Core Clock Ratio (wide range, determined by SPICTL register)
LCLK = Link Port Clock
SCLK = Serial Port Clock
SDK = SDRAM Clock
SPICLK = SPI Clock

POWER DISSIPATION

Total power dissipation has two components: one due to internal circuitry and one due to the switching of external output drivers.

Internal power dissipation depends on the instruction execution sequence and the data operands involved. Using the current specifications ($I_{DDINPEAK}$, $I_{DDINHIGH}$, $I_{DDINLOW}$, I_{DDIDLE}) from the Electrical Characteristics on Page 18 and the current-versus-operation information in Table 8, the programmer can estimate the ADSP-21161N's internal power supply (V_{DDINT}) input current for a specific application, according to the following formula:

$$\begin{aligned} &\%\ \text{Peak} \times I_{DD\text{-}INPEAK} \\ &\%\ \text{High} \times I_{DD\text{-}INHIGH} \\ &\%\ \text{Low} \times I_{DD\text{-}INLOW} \\ +\ &\%\ \text{Peak} \times I_{DD\text{-}IDLE} \\ &= I_{DDINT} \end{aligned}$$

Clock Input

In systems that use multiprocessing or SBSRAM, $\overline{\text{CLKDBL}}$ cannot be enabled nor can the systems use an external crystal as the CLKIN source.

Do not use CLKOUT as the clock source for the SBSRAM device. Using an external crystal in conjunction with $\overline{\text{CLKDBL}}$ to generate a CLKOUT frequency is not supported. Negative hold times can result from the potential skew between CLKIN and CLKOUT.

Table 11. Clock Input

Parameter		100 MHz Min	100 MHz Max	110 MHz Min	110 MHz Max	Unit
Timing Requirements						
t_{CK}	CLKIN Period[1]	20	238	18	238	ns
t_{CKL}	CLKIN Width Low[1]	7.5	119	7	119	ns
t_{CKH}	CLKIN Width High[1]	7.5	119	7	119	ns
t_{CKRF}	CLKIN Rise/Fall (0.4 V–2.0 V)		3		3	ns
t_{CCLK}	CCLK Period	10	30	9	30	ns
Switching Characteristics						
t_{DCKOO}	CLKOUT Delay After CLKIN	0	2	0	2	ns
t_{CKOP}	CLKOUT Period	$t_{CK}-1$	$t_{CK}+1$	$t_{CK}-1$	$t_{CK}+1$	ns
t_{CKWH}	CLKOUT Width High	$t_{CKOP}/2-2$	$t_{CKOP}/2+2$	$t_{CKOP}/2-2$	$t_{CKOP}/2+2$	ns
t_{CKWL}	CLKOUT Width Low	$t_{CKOP}/2-2$	$t_{CKOP}/2+2$	$t_{CKOP}/2-2$	$t_{CKOP}/2+2$	ns

[1] CLKIN is dependent on the configuration of the CLKCFGx and $\overline{\text{CLKDBL}}$ pins to achieve desired t_{CCLK}.

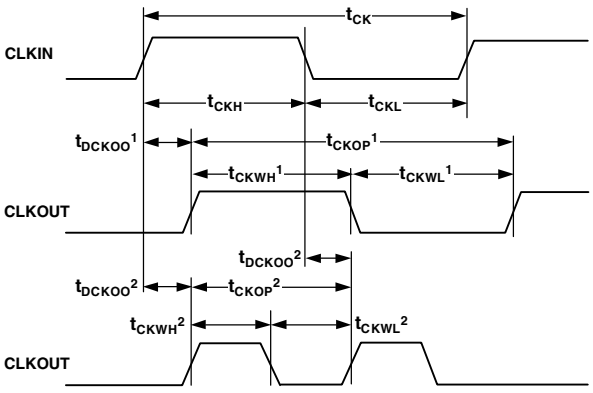


Figure 11. Clock Input

Memory Read — Bus Master

Use these specifications for asynchronous interfacing to memories (and memory-mapped peripherals) without reference to CLKIN except for ACK pin requirements listed in footnote 4 of Table 16. These specifications apply when the ADSP-21161N is the bus master accessing external memory space in asynchronous access mode.

Table 16. Memory Read — Bus Master

Parameter		100 MHz Min	100 MHz Max	110 MHz Min	110 MHz Max	Unit
Timing Requirements						
t_{DAD}	Address, Selects Delay to Data Valid[1, 2, 3]		$t_{CKOP}-0.25t_{CCLK}-8.5+W$		$t_{CKOP}-0.25t_{CCLK}-6.75+W$	ns
t_{DRLD}	$\overline{RD}$ Low to Data Valid[1,3]		$0.75t_{CKOP}-11+W$		$0.75t_{CKOP}-11+W$	ns
t_{HDA}	Data Hold from Address, Selects[4]	0		0		ns
t_{SDS}	Data Setup to $\overline{RD}$ High	8		8		ns
t_{HDRH}	Data Hold from $\overline{RD}$ High[4]	1		1		ns
t_{DAAK}	ACK Delay from Address, Selects[2, 5]		$t_{CKOP}-0.5t_{CCLK}-12+W$		$t_{CKOP}-0.5t_{CCLK}-12+W$	ns
t_{DSAK}	ACK Delay from $\overline{RD}$ Low[5]		$t_{CKOP}-0.75t_{CCLK}-11+W$		$t_{CKOP}-0.75t_{CCLK}-11+W$	ns
t_{SAKC}	ACK Setup to CLKIN[5]	$0.5t_{CCLK}+3$		$0.5t_{CCLK}+3$		ns
t_{HAKC}	ACK Hold After CLKIN	1		1		ns
Switching Characteristics						
t_{DRHA}	Address Selects Hold After $\overline{RD}$ High	$0.25t_{CCLK}-1+H$		$0.25t_{CCLK}-1+H$		ns
t_{DARL}	Address Selects to $\overline{RD}$ Low[2]	$0.25t_{CCLK}-3$		$0.25t_{CCLK}-3$		ns
t_{RW}	$\overline{RD}$ Pulsewidth	$t_{CKOP}-0.5t_{CCLK}-1+W$		$t_{CKOP}-0.5t_{CCLK}-1+W$		ns
t_{RWR}	$\overline{RD}$ High to $\overline{WR}$, $\overline{RD}$, $\overline{DMAGx}$ Low	$0.5t_{CCLK}-1+HI$		$0.5t_{CCLK}-1+HI$		ns

W = (number of wait states specified in WAIT register) × t_{CKOP}.
HI = t_{CKOP} (if an address hold cycle or bus idle cycle occurs, as specified in WAIT register; otherwise HI = 0).
H = t_{CKOP} (if an address hold cycle occurs as specified in WAIT register; otherwise H = 0).

[1] Data Delay/Setup: User must meet t_{DAD}, t_{DRLD}, or t_{SDS}.
[2] The falling edge of $\overline{MSx}$, $\overline{BMS}$ is referenced.
[3] The maximum limits of timing requirement values for t_{DAD} and t_{DRLD} parameters are applicable for the case where ACK is always high.
[4] Data Hold: User must meet t_{HDA} or t_{HDRH} in asynchronous access mode. See Example System Hold Time Calculation on Page 54 for the calculation of hold times given capacitive and dc loads.
[5] For asynchronous access, ACK is sampled only after the programmed wait states for the access have been counted. For the first CLKIN cycle of a new external memory access, ACK must be driven low (deasserted) by t_{DAAK}, t_{DSAK}, or t_{SAKC}. For the second and subsequent cycles of an asynchronous external memory access, the t_{SAKC} and t_{HAKC} must be met for both assertion and deassertion of ACK signal.

Host Bus Request

Use these specifications for asynchronous host bus requests of an ADSP-21161N ($\overline{HBR}$, $\overline{HBG}$).

Table 20. Host Bus Request

Parameter		100 MHz Min	100 MHz Max	110 MHz Min	110 MHz Max	Unit
Timing Requirements						
$t_{HBGRCSV}$	$\overline{HBG}$ Low to $\overline{RD}$/$\overline{WR}$/$\overline{CS}$ Valid		19		19	ns
t_{SHBRI}	$\overline{HBR}$ Setup Before CLKIN[1]	6		6		ns
t_{HHBRI}	$\overline{HBR}$ Hold After CLKIN[1]	1		1		ns
t_{SHBGI}	$\overline{HBG}$ Setup Before CLKIN	6		6		ns
t_{HHBGI}	$\overline{HBG}$ Hold After CLKIN	1		1		ns
Switching Characteristics						
t_{DHBGO}	$\overline{HBG}$ Delay After CLKIN		7		7	ns
t_{HHBGO}	$\overline{HBG}$ Hold After CLKIN	1.5		1.5		ns
t_{DRDYCS}	REDY (O/D) or (A/D) Low from $\overline{CS}$ and $\overline{HBR}$ Low[2]		10		10	ns
t_{TRDYHG}	REDY (O/D) Disable or REDY (A/D) High from $\overline{HBG}$[2]	t_{CKOP} + 14		t_{CKOP} + 12		ns
t_{ARDYTR}	REDY (A/D) Disable from $\overline{CS}$ or $\overline{HBR}$ High[2]		11		11	ns

[1] Only required for recognition in the current cycle.
[2] (O/D) = open drain, (A/D) = active drive.

Multiprocessor Bus Request

Use these specifications for passing of bus mastership between multiprocessing ADSP-21161Ns ($\overline{BRx}$).

Table 21. Multiprocessor Bus Request

Parameter		Min	Max	Unit
Timing Requirements				
t_{SBRI}	$\overline{BRx}$ Setup Before CLKIN High	9		ns
t_{HBRI}	$\overline{BRx}$ Hold After CLKIN High	0.5		ns
t_{SPAI}	$\overline{PA}$ Setup Before CLKIN High	9		ns
t_{HPAI}	$\overline{PA}$ Hold After CLKIN High	1		ns
t_{SRPBAI}	RPBA Setup Before CLKIN High	6		ns
t_{HRPBAI}	RPBA Hold After CLKIN High	2		ns
Switching Characteristics				
t_{DBRO}	$\overline{BRx}$ Delay After CLKIN High		8	ns
t_{HBRO}	$\overline{BRx}$ Hold After CLKIN High	1.0		ns
t_{DPASO}	$\overline{PA}$ Delay After CLKIN High, Slave		8	ns
t_{TRPAS}	$\overline{PA}$ Disable After CLKIN High, Slave	1.5		ns
t_{DPAMO}	$\overline{PA}$ Delay After CLKIN High, Master		$0.25t_{CCLK}+9$	ns
t_{PATR}	$\overline{PA}$ Disable Before CLKIN High, Master	$0.25t_{CCLK}-5$		ns

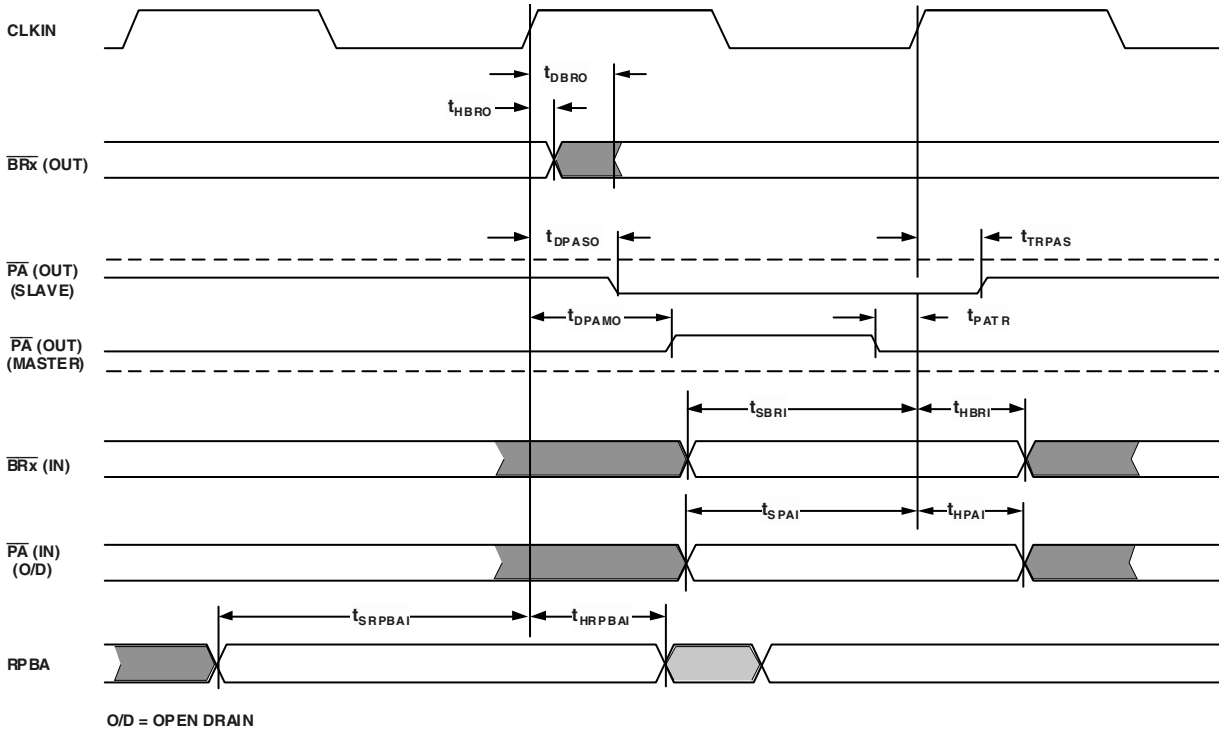


Figure 22. Multiprocessor Bus Request

Three-State Timing — Bus Master, Bus Slave

These specifications show how the memory interface is disabled (stops driving) or enabled (resumes driving) relative to CLKIN and the $\overline{\text{SBTS}}$ pin. This timing is applicable to bus master transition cycles (BTC) and host transition cycles (HTC) as well as the $\overline{\text{SBTS}}$ pin.

During reset, the DSP will not respond to $\overline{\text{SBTS}}$, $\overline{\text{HBR}}$, and MMS accesses. Although the DSP will recognize $\overline{\text{HBR}}$ asserted before reset, a $\overline{\text{HBG}}$ will not be returned by the DSP until after reset is deasserted and the DSP completes bus synchronization.

Table 24. Three-State Timing — Bus Master, Bus Slave

Parameter		Min	Max	Unit
Timing Requirements				
t_{STSCK}	$\overline{\text{SBTS}}$ Setup Before CLKIN	6		ns
t_{HTSCK}	$\overline{\text{SBTS}}$ Hold After CLKIN	2		ns
Switching Characteristics				
t_{MIENA}	Address/Select Enable After CLKIN High	1.5	9	ns
t_{MIENS}	Strobes Enable After CLKIN High[1]	–1.5	+9	ns
t_{MIENHG}	$\overline{\text{HBG}}$ Enable After CLKIN	1.5	9	ns
t_{MITRA}	Address/Select Disable After CLKIN High	$0.5t_{CKOP}$–20	$0.5t_{CKOP}$–15	ns
t_{MITRS}	Strobes Disable After CLKIN High	t_{CKOP}– $0.25t_{CCLK}$–17	t_{CKOP}– $0.25t_{CCLK}$–12.5	ns
t_{MITRHG}	$\overline{\text{HBG}}$ Disable After CLKIN[2]	$0.5t_{CKOP}$+N×t_{CCLK}–20	$0.5t_{CKOP}$+N×t_{CCLK}–15	ns
t_{DATEN}	Data Enable After CLKIN[3]	1.5	10	ns
t_{DATTR}	Data Disable After CLKIN[3]	1.5	6	ns
t_{ACKEN}	ACK Enable After CLKIN High	1.5	9	ns
t_{ACKTR}	ACK Disable After CLKIN High	0.2	5	ns
t_{CDCEN}	CLKOUT Enable After CLKIN[2]	$0.5t_{CKOP}$+N×t_{CCLK}	$0.5t_{CKOP}$+N×t_{CCLK}+5	ns
t_{CDCTR}	CLKOUT Disable After CLKIN	t_{CKOP}–5	t_{CKOP}	ns
t_{ATRHBG}	Address/Select Disable Before $\overline{\text{HBG}}$ Low[4]	$1.5t_{CKOP}$–6	$1.5t_{CKOP}$+2	ns
t_{STRHBG}	$\overline{\text{RD}}$/$\overline{\text{WR}}$/$\overline{\text{DMAGx}}$ Disable Before $\overline{\text{HBG}}$ Low[4]	t_{CKOP}+ $0.25t_{CCLK}$–4	t_{CKOP}+ $0.25t_{CCLK}$+3	ns
t_{BTRHBG}	$\overline{\text{BMS}}$ Disable Before $\overline{\text{HBG}}$ Low[4]	$0.5t_{CKOP}$–4	$0.5t_{CKOP}$+2	ns
t_{MENHBG}	Memory Interface Enable After $\overline{\text{HBG}}$ High[4]	t_{CKOP}–5	t_{CKOP}+5	ns

[1] Strobes = $\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{DMAGx}}$.
[2] Where N = 0.5, 1.0, 1.5 for 1:2, 1:3, and 1:4, respectively.
[3] In addition to bus master transition cycles, these specs also apply to bus master and bus slave synchronous read/write.
[4] Memory Interface = Address, $\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{MSx}}$, $\overline{\text{DMAGx}}$, and $\overline{\text{BMS}}$ (in EPROM boot mode). $\overline{\text{BMS}}$ is only an output in EPROM boot mode.

DMA Handshake

These specifications describe the three DMA handshake modes. In all three modes $\overline{\text{DMAR}}$ is used to initiate transfers. For handshake mode, $\overline{\text{DMAG}}$ controls the latching or enabling of data externally. For external handshake mode, the data transfer is controlled by the ADDR23–0, $\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{MS3–0}}$, ACK, and $\overline{\text{DMAG}}$ signals. For Paced Master mode, the data transfer is controlled by ADDR23–0, $\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{MS3–0}}$, and ACK (not $\overline{\text{DMAG}}$). For Paced Master mode, the Memory Read-Bus Master, Memory Write-Bus Master, and Synchronous Read/Write-Bus Master timing specifications for ADDR23–0, $\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{MS3–0}}$, DATA47–16, and ACK also apply.

Table 25. DMA Handshake

Parameter		100 MHz Min	100 MHz Max	110 MHz Min	110 MHz Max	Unit
Timing Requirements						
t_{SDRC}	$\overline{\text{DMARx}}$ Setup Before CLKIN[1]	3.5		3.5		ns
t_{WDR}	$\overline{\text{DMARx}}$ Width Low (Nonsynchronous)[2]	$t_{CCLK}+4.5$		$t_{CCLK}+4.5$		ns
$t_{SDATDGL}$	Data Setup After $\overline{\text{DMAGx}}$ Low[3]		$t_{CKOP}-0.5t_{CCLK}-7$		$t_{CKOP}-0.5t_{CCLK}-7$	ns
$t_{HDATIDG}$	Data Hold After $\overline{\text{DMAGx}}$ High	2		2		ns
t_{DATDRH}	Data Valid After $\overline{\text{DMARx}}$ High[3]		$t_{CKOP}+3$		$t_{CKOP}+3$	ns
t_{DMARLL}	$\overline{\text{DMARx}}$ Low Edge to Low Edge[4]	t_{CKOP}		t_{CKOP}		ns
t_{DMARH}	$\overline{\text{DMARx}}$ Width High[2]	$t_{CCLK}+4.5$		$t_{CCLK}+4.5$		ns
Switching Characteristics						
t_{DDGL}	$\overline{\text{DMAGx}}$ Low Delay After CLKIN	$0.25t_{CCLK}+1$	$0.25t_{CCLK}+9$	$0.25t_{CCLK}+1$	$0.25t_{CCLK}+9$	ns
t_{WDGH}	$\overline{\text{DMAGx}}$ High Width	$0.5t_{CCLK}-1+HI$		$0.5t_{CCLK}-1+HI$		ns
t_{WDGL}	$\overline{\text{DMAGx}}$ Low Width	$t_{CKOP}-0.5t_{CCLK}-1$		$t_{CKOP}-0.5t_{CCLK}-1$		ns
t_{HDGC}	$\overline{\text{DMAGx}}$ High Delay After CLKIN	$t_{CKOP}-0.25t_{CCLK}+1.0$	$t_{CKOP}-0.25t_{CCLK}+9$	$t_{CKOP}-0.25t_{CCLK}+1.0$	$t_{CKOP}-0.25t_{CCLK}+9$	ns
$t_{VDATDGH}$	Data Valid Before $\overline{\text{DMAGx}}$ High[5]	$t_{CKOP}-0.25t_{CCLK}-8$	$t_{CKOP}-0.25t_{CCLK}+5$	$t_{CKOP}-0.25t_{CCLK}-8$	$t_{CKOP}-0.25t_{CCLK}+5$	ns
$t_{DATRDGH}$	Data Disable After $\overline{\text{DMAGx}}$ High[6]	$0.25t_{CCLK}-3$	$0.25t_{CCLK}+4$	$0.25t_{CCLK}-3$	$0.25t_{CCLK}+4$	ns
t_{DGWRL}	$\overline{\text{WRx}}$ Low Before $\overline{\text{DMAGx}}$ Low	–1.5	+2	–1.5	+2	ns
t_{DGWRH}	$\overline{\text{DMAGx}}$ Low Before $\overline{\text{WRx}}$ High	$t_{CKOP}-0.5t_{CCLK}-2+W$		$t_{CKOP}-0.5t_{CCLK}-2+W$		ns
t_{DGWRR}	$\overline{\text{WRx}}$ High Before $\overline{\text{DMAGx}}$ High[7]	–1.5	+2	–1.5	+2	ns
t_{DGRDL}	$\overline{\text{RDx}}$ Low Before $\overline{\text{DMAGx}}$ Low	–1.5	+2	–1.5	+2	ns
t_{DRDGH}	$\overline{\text{RDx}}$ Low Before $\overline{\text{DMAGx}}$ High	$t_{CKOP}-0.5t_{CCLK}-2+W$		$t_{CKOP}-0.5t_{CCLK}-2+W$		ns
t_{DGRDR}	$\overline{\text{RDx}}$ High Before $\overline{\text{DMAGx}}$ High[7]	–1.5	+2	–1.5	+2	ns
t_{DGWR}	$\overline{\text{DMAGx}}$ High to $\overline{\text{WRx}}$, $\overline{\text{RDx}}$ Low	$0.5t_{CCLK}-2+HI$		$0.5t_{CCLK}-2+HI$		ns
t_{DADGH}	Address/Select Valid to $\overline{\text{DMAGx}}$ High	15		13		ns
t_{DDGHA}	Address/Select Hold After $\overline{\text{DMAGx}}$ High	1		1		ns

W = (number of wait states specified in WAIT register) × t_{CKOP}.
HI = t_{CKOP} (if data bus idle cycle occurs, as specified in WAIT register; otherwise HI = 0).

[1] Only required for recognition in the current cycle.
[2] Maximum throughput (@ 110 MHz) using $\overline{\text{DMARx/DMAGx}}$ handshaking equals $t_{WDR} + t_{DMARH} = (t_{CCLK}+4.5) + (t_{CCLK}+4.5) = 27$ ns (37 MHz). This throughput limit applies to non-synchronous access mode only.
[3] $t_{SDATDGL}$ is the data setup requirement if $\overline{\text{DMARx}}$ is not being used to hold off completion of a write. Otherwise, if $\overline{\text{DMARx}}$ low holds off completion of the write, the data can be driven t_{DATDRH} after $\overline{\text{DMARx}}$ is brought high.
[4] Use t_{DMARLL} if $\overline{\text{DMARx}}$ transitions synchronous with CLKIN. Otherwise, use t_{WDR} and t_{DMARH}.
[5] $t_{VDATDGH}$ is valid if $\overline{\text{DMARx}}$ is not being used to hold off completion of a read. If $\overline{\text{DMARx}}$ is used to prolong the read, then $t_{VDATDGH} = t_{CKOP} - 0.25t_{CCLK} - 8 + (n \times t_{CKOP})$ where n equals the number of extra cycles that the access is prolonged.
[6] See Example System Hold Time Calculation on Page 54 for calculation of hold times given capacitive and dc loads.
[7] This parameter applies for synchronous access mode only.

SDRAM Interface — Bus Master

Use these specifications for ADSP-21161N bus master accesses of SDRAM:

Table 26. SDRAM Interface — Bus Master

Parameter		100 MHz		110 MHz		Unit
		Min	Max	Min	Max	
Timing Requirements						
t_{SDSDK}	Data Setup Before SDCLK	2.0		2.0		ns
t_{HDSDK}	Data Hold After SDCLK	2.3		2.3		ns
Switching Characteristics						
t_{DSDK1}	First SDCLK Rise Delay After CLKIN[1, 2]	$0.75t_{CCLK} + 1.5$	$0.75t_{CCLK} + 8.0$	$0.75t_{CCLK} + 1.5$	$0.75t_{CCLK} + 8.0$	ns
t_{SDK}	SDCLK Period	t_{CCLK}	$2 \times t_{CCLK}$	t_{CCLK}	$2 \times t_{CCLK}$	ns
t_{SDKH}	SDCLK Width High	4		3		ns
t_{SDKL}	SDCLK Width Low	4		3		ns
$t_{DCADSDK}$	Command, Address, Data, Delay After SDCLK[3]		$0.25t_{CCLK} + 2.5$		$0.25t_{CCLK} + 2.5$	ns
$t_{HCADSDK}$	Command, Address, Data, Hold After SDCLK[3]	2.0		2.0		ns
$t_{SDTRSDK}$	Data Three-State After SDCLK[4]		$0.5t_{CCLK} + 2.0$		$0.5t_{CCLK} + 2.0$	ns
$t_{SDENSDK}$	Data Enable After SDCLK[5]	$0.75t_{CCLK}$		$0.75t_{CCLK}$		ns
t_{SDCTR}	Command Three-State After CLKIN	$0.5t_{CCLK} - 1.5$	$0.5t_{CCLK} + 6.0$	$0.5t_{CCLK} - 1.5$	$0.5t_{CCLK} + 6.0$	ns
t_{SDCEN}	Command Enable After CLKIN	2	5	2	5	ns
$t_{SDSDKTR}$	SDCLK Three-State After CLKIN	0	3	0	3	ns
$t_{SDSDKEN}$	SDCLK Enable After CLKIN	1	4	1	4	ns
t_{SDATR}	Address Three-State After CLKIN	$-0.25\ t_{CCLK} - 5$	$-0.25t_{CCLK}$	$-0.25\ t_{CCLK} - 5$	$-0.25t_{CCLK}$	ns
t_{SDAEN}	Address Enable After CLKIN	−0.4	+7.2	−0.4	+7.2	ns

[1] For the second, third, and fourth rising edges of SDCLK delay from CLKIN, add appropriate number of SDCLK period to the t_{DSDK1} and t_{SSDKC1} values, depending upon the SDCKR value and the core clock to CLKIN ratio.
[2] Subtract t_{CCLK} from result if value is greater than or equal to t_{CCLK}.
[3] Command = SDCKE, $\overline{MSx}$, DQM, $\overline{RAS}$, $\overline{CAS}$, SDA10, and $\overline{SDWE}$.
[4] SDRAM Controller adds one SDRAM CLK three-stated cycle delay on a read, followed by a write.
[5] Valid when DSP transitions to SDRAM master from SDRAM slave.

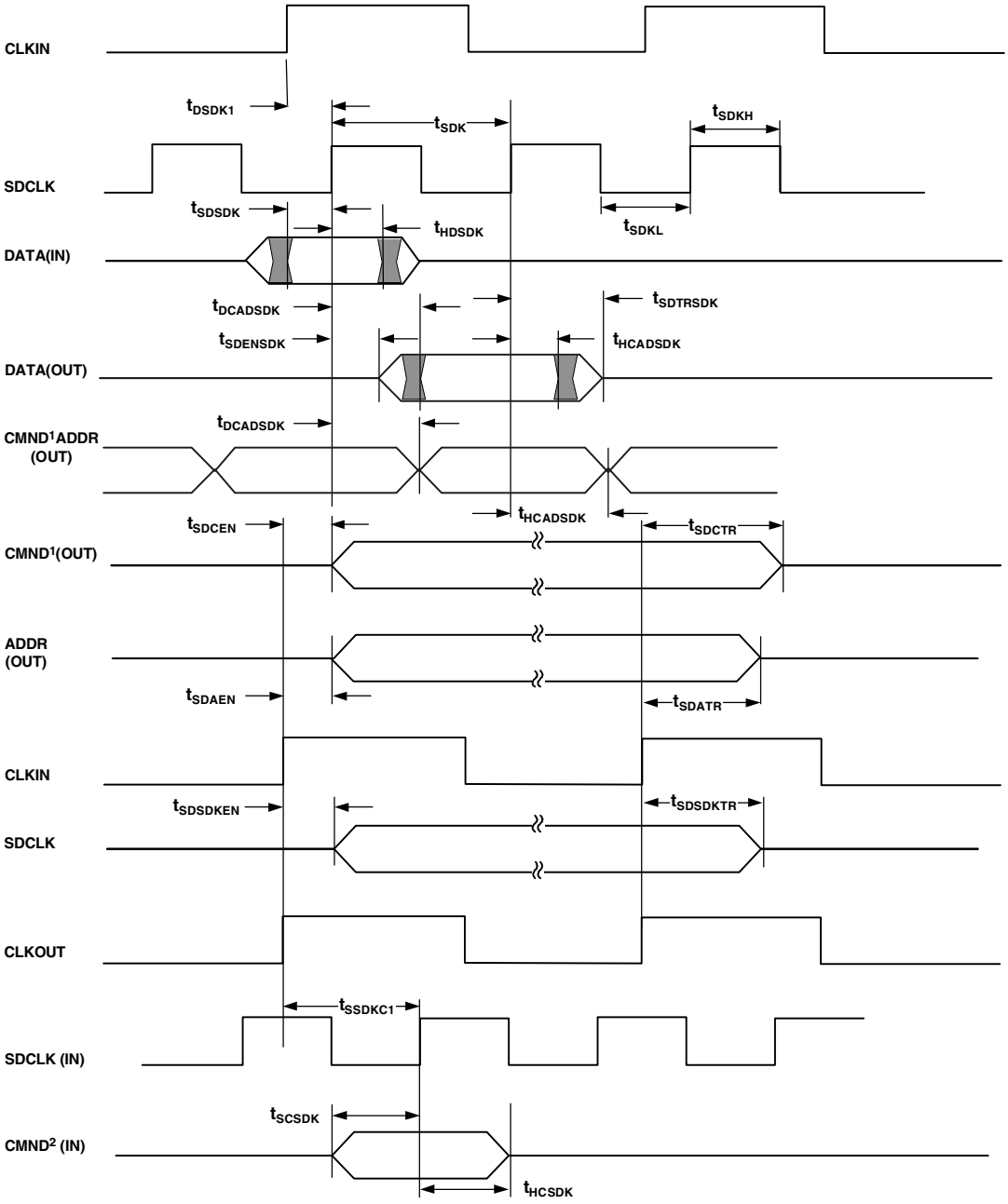
SDRAM Interface — Bus Slave

These timing requirements allow a bus slave to sample the bus master's SDRAM command and detect when a refresh occurs:

Table 27. SDRAM Interface — Bus Slave

Parameter		Min	Max	Unit
Timing Requirements				
t_{SSDKC1}	First SDCLK Rise after CLKOUT[1, 2, 3]	$SDCK \times t_{CCLK} - 0.5t_{CCLK} - 0.5$	$SDCKR \times t_{CCLK} - 0.25t_{CCLK} + 2.0$	ns
t_{SCSDK}	Command Setup before SDCLK[4]	2		ns
t_{HCSDK}	Command Hold after SDCLK[4]	1		ns

[1] For the second, third, and fourth rising edges of SDCLK delay from CLKOUT, add appropriate number of SDCLK period to the t_{DSDK1} and t_{SSDKC1} values, depending upon the SDCKR value and the Core clock to CLKOUT ratio.
[2] SDCKR = 1 for SDCLK equal to core clock frequency and SDCKR = 2 for SDCLK equal to half core clock frequency.
[3] Subtract t_{CCLK} from result if value is greater than or equal to t_{CCLK}.
[4] Command = SDCKE, $\overline{RAS}$, $\overline{CAS}$, and $\overline{SDWE}$.



1COMMAND = SDCKE, $\overline{MSx}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{SDWE}$, DQM, AND SDA10.
2COMMAND = SDCKE, $\overline{RAS}$, $\overline{CAS}$, AND $\overline{SDWE}$.

Figure 26. SDRAM Interface

Table 29. Link Ports — Transmit

Parameter		Min	Max	Unit
Timing Requirements				
t_{SLACH}	LACK Setup Before LCLK High	8		ns
t_{HLACH}	LACK Hold After LCLK High	–2		ns
Switching Characteristics				
t_{DLDCH}	Data Delay After LCLK High		3	ns
t_{HLDCH}	Data Hold After LCLK High	0		ns
$t_{LCLKTWL}$	LCLK Width Low	$0.5t_{LCLK}$–1.0	$0.5t_{LCLK}$+1.0	ns
$t_{LCLKTWH}$	LCLK Width High	$0.5t_{LCLK}$–1.0	$0.5t_{LCLK}$+1.0	ns
t_{DLACLK}	LCLK Low Delay After LACK High	$0.5t_{LCLK}$+3	$3t_{LCLK}$+11	ns

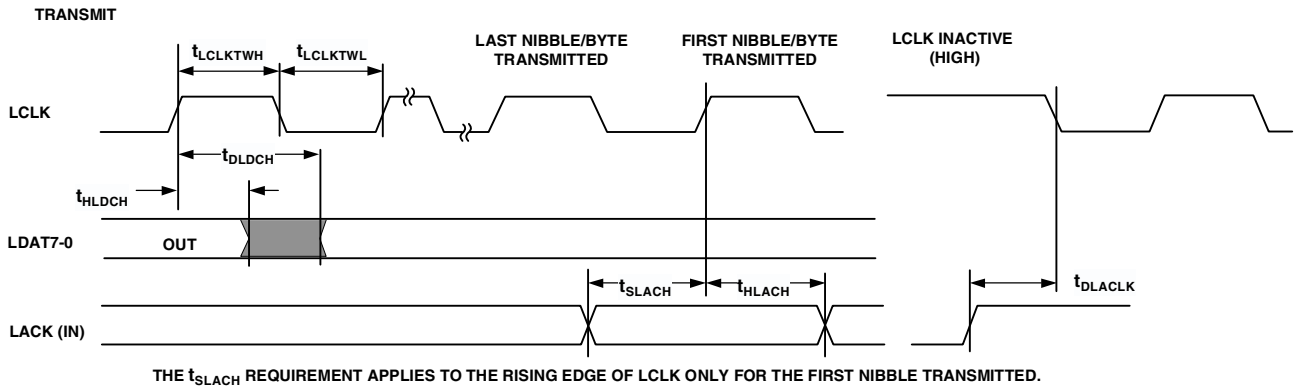
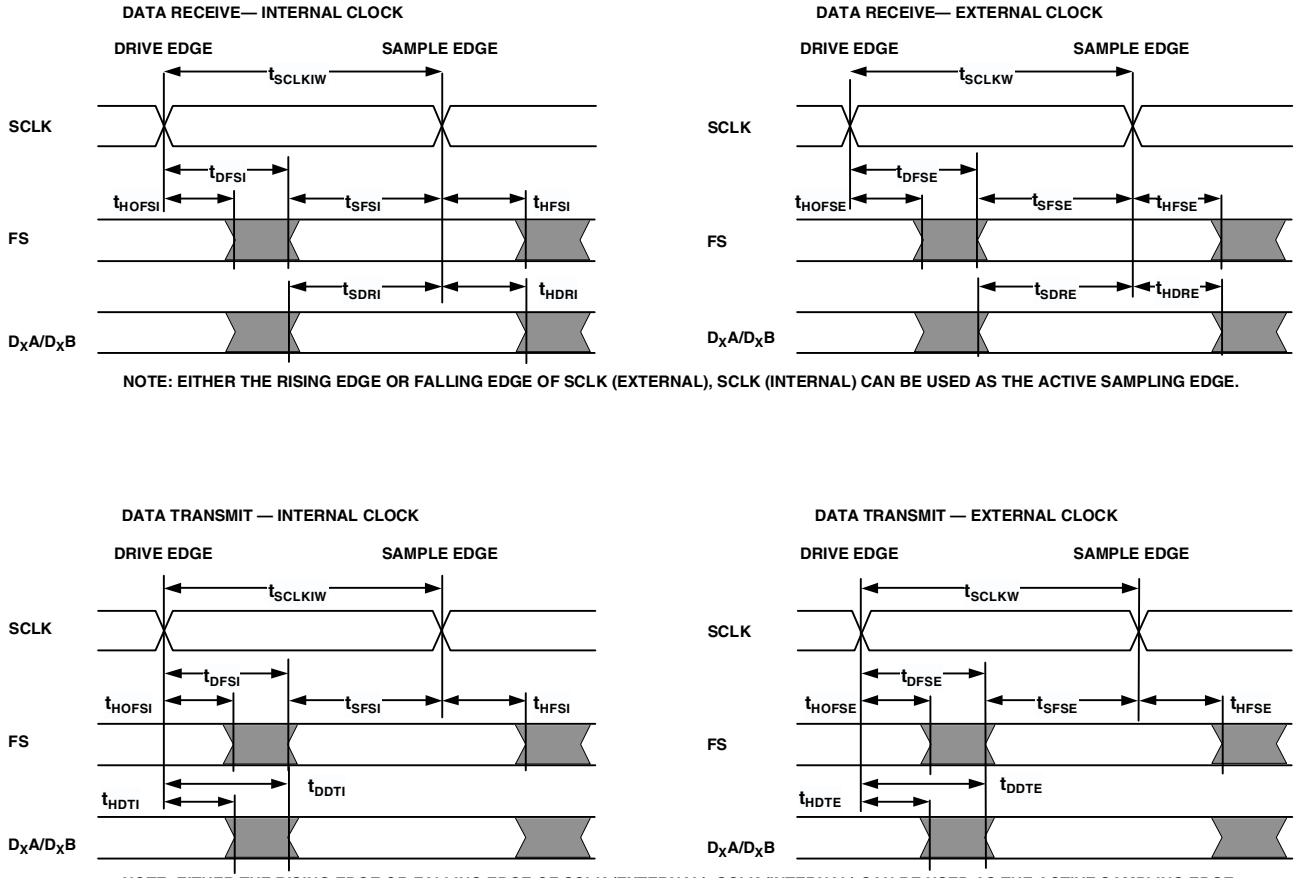


Figure 28. Link Ports—Transmit



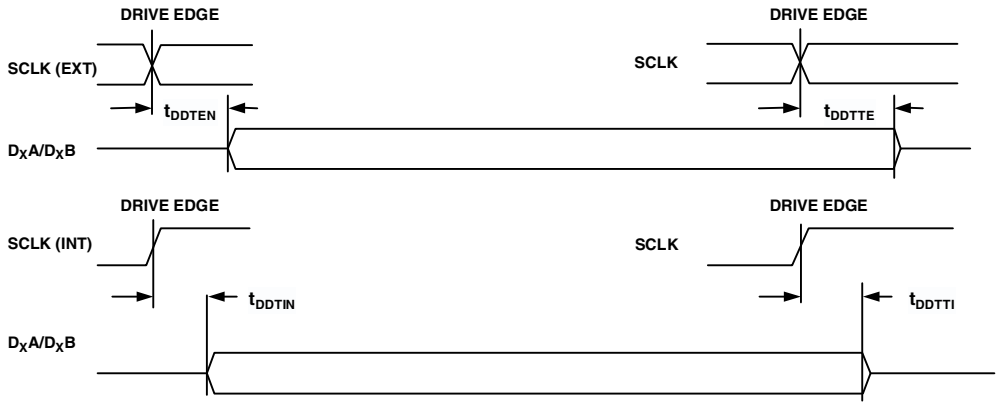


Figure 29. Serial Ports

OUTPUT DRIVE CURRENTS

Figure 34 shows typical I-V characteristics for the output drivers of the ADSP-21161N. The curves represent the current drive capability of the output drivers as a function of output voltage.

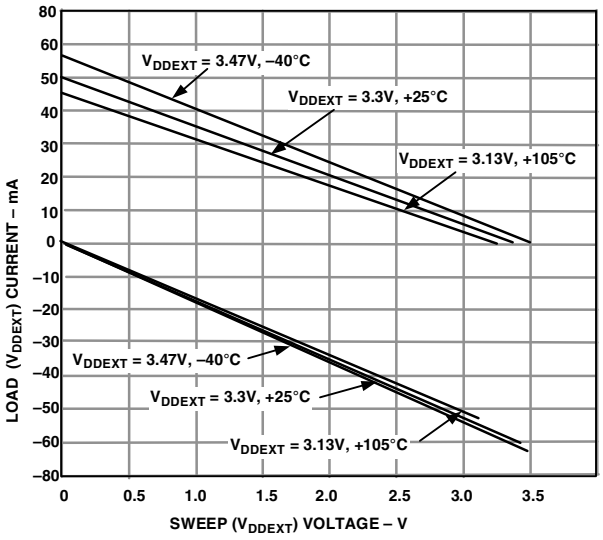


Figure 34. Typical Drive Currents

TEST CONDITIONS

The DSP is tested for output enable, disable, and hold time.

Output Enable Time

Output pins are considered to be enabled when they have made a transition from a high impedance state to the point when they start driving. The output enable time t_{ENA} is the interval from the point when a reference signal reaches a high or low voltage level to the point when the output has reached a specified high or low trip point, as shown in the Output Enable/Disable diagram (Figure 35). If multiple pins (such as the data bus) are enabled, the measurement value is that of the first pin to start driving.

Output Disable Time

Output pins are considered to be disabled when they stop driving, go into a high-impedance state, and start to decay from their output high or low voltage. The time for the voltage on the bus to decay by ΔV is dependent on the capacitive load, C_L and the load current, I_L. This decay time can be approximated by the following equation:

$$t_{DECAY} = (C_L \Delta V)/I_L$$

The output disable time t_{DIS} is the difference between $t_{MEASURED}$ and t_{DECAY} as shown in Figure 35. The time $t_{MEASURED}$ is the interval from when the reference signal switches to when the output voltage decays ΔV from the measured output high or output low voltage. t_{DECAY} is calculated with test loads C_L and I_L, and with ΔV equal to 0.5 V.

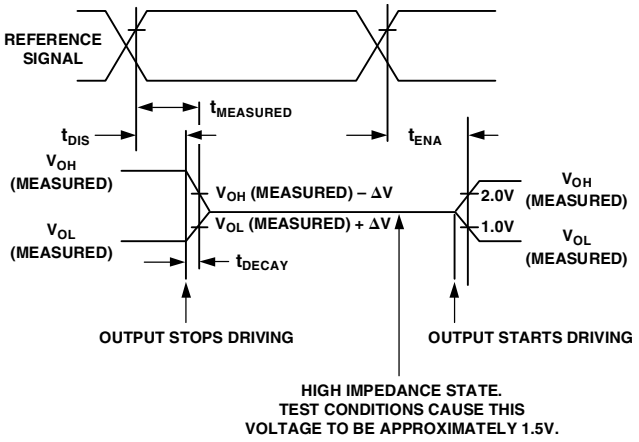


Figure 35. Output Enable/Disable

Example System Hold Time Calculation

To determine the data output hold time in a particular system, first calculate t_{DECAY} using the equation given above. Choose ΔV to be the difference between the ADSP-21161N's output voltage and the input threshold for the device requiring the hold time. A typical ΔV will be 0.4 V. C_L is the total bus capacitance (per data line), and I_L is the total leakage or three-state current (per data line). The hold time will be t_{DECAY} plus the minimum disable time (i.e., t_{DATRWH} for the write cycle).

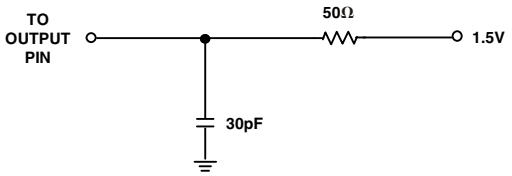


Figure 36. Equivalent Device Loading for AC Measurements (Includes All Fixtures)

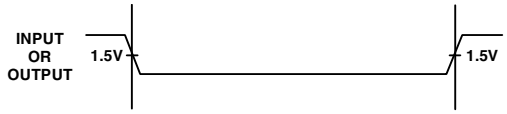


Figure 37. Voltage Reference Levels for AC Measurements (Except Output Enable/Disable)

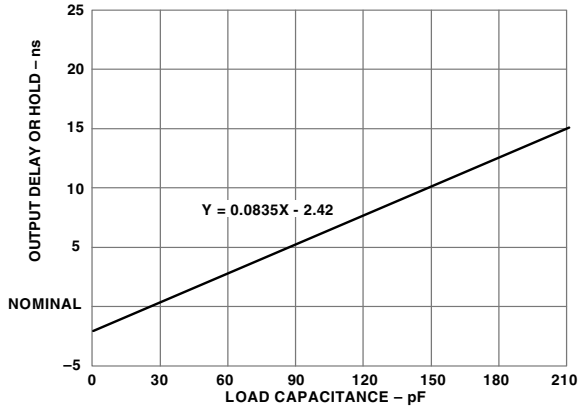


Figure 38. Typical Output Delay or Hold vs. Load Capacitance (at Max Case Temperature)

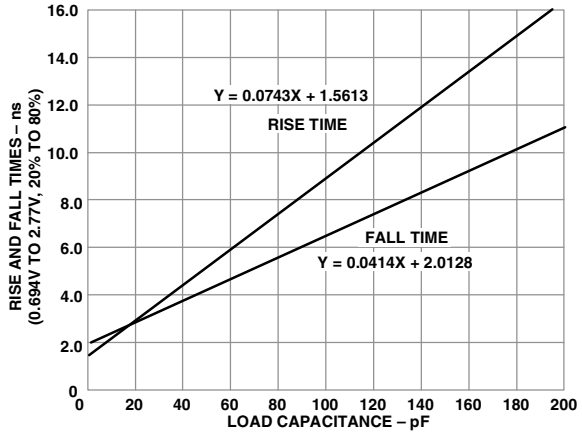


Figure 39. Typical Output Rise/Fall Time (20% – 80%, V_{DDEXT} = Max)

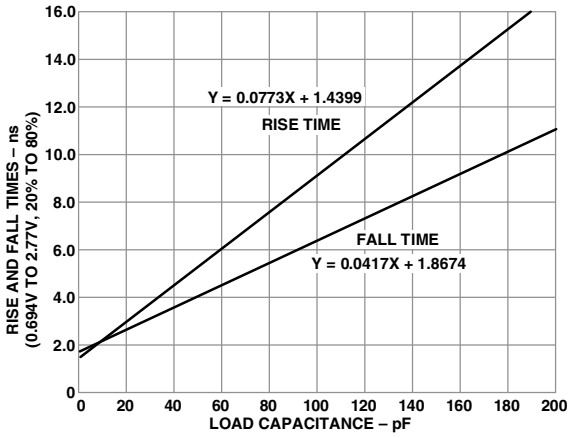


Figure 40. Typical Output Rise/Fall Time (20% – 80%, V_{DDEXT} = Min)

Capacitive Loading

Output delays and holds are based on standard capacitive loads: 30 pF on all pins (see Figure 36 on Page 54). Figure 38 shows graphically how output delays and holds vary with load capacitance. (Note that this graph or derating does not apply to output disable delays; see Output Disable Time on Page 54.) The graphs of Figure 38, Figure 39, and Figure 40 may not be linear outside the ranges shown for Typical Output Delay vs. Load Capacitance and Typical Output Rise Time (20% – 80%, V = Min) vs. Load Capacitance.

ENVIRONMENTAL CONDITIONS

The thermal characteristics in which the DSP is operating influence performance.

Thermal Characteristics

The ADSP-21161N is packaged in a 225-ball chip scale package ball grid array (CSP_BGA). The ADSP-21161N is specified for a case temperature (T_{CASE}). To ensure that the T_{CASE} data sheet specification is not exceeded, a heatsink and/or an air flow source may be used. Use the center block of ground pins (CSP_BGA balls: F6-10, G6-10, H6-10, J6-10, K6-10) to provide thermal pathways to the printed circuit board's ground plane. A heatsink should be attached to the ground plane (as close as possible to the thermal pathways) with a thermal adhesive.

$$T_{CASE} = T_{AMB} + (PD \times \theta_{CA})$$

where:

- T_{CASE} = Case temperature (measured on top surface of package)
- T_{AMB} = Ambient temperature °C
- *PD* = Power dissipation in W (this value depends upon the specific application; a method for calculating PD is shown under Power Dissipation).
- θ_{CA} = Value from Table 39.

Table 39. Airflow Over Package Versus θ_{CA}

Airflow (Linear Ft./Min.)	0	200	400
θ_{CA} (°C/W)θ_{JC}[1]	17.9	15.2	13.7

[1] = 6.8°C/W.

225-BALL CSP_BGA BALL CONFIGURATIONS

Table 40. 225-Ball CSP_BGA Ball Assignments

Ball Name	Ball Number	Ball Name	Ball Number	Ball Name	Ball Number	Ball Name	Ball Number
NC	A01	$\overline{\text{TRST}}$	B01	TMS	C01	TDO	D01
BMSTR	A02	TDI	B02	$\overline{\text{EMU}}$	C02	TCK	D02
$\overline{\text{BMS}}$	A03	RPBA	B03	GND	C03	FLAG11	D03
$\overline{\text{SPIDS}}$	A04	MOSI	B04	SPICLK	C04	MISO	D04
EBOOT	A05	FS0	B05	D0B	C05	SCLK0	D05
LBOOT	A06	SCLK1	B06	D1A	C06	D1B	D06
SCLK2	A07	D2B	B07	D2A	C07	FS1	D07
D3B	A08	D3A	B08	FS2	C08	V_{DDINT}	D08
L0DAT4	A09	L0DAT7	B09	FS3	C09	SCLK3	D09
L0ACK	A10	L0CLK	B10	L0DAT6	C10	L0DAT5	D10
L0DAT2	A11	L0DAT1	B11	L1DAT7	C11	L0DAT3	D11
L1DAT6	A12	L1DAT4	B12	L1DAT3	C12	L1DAT5	D12
L1CLK	A13	L1ACK	B13	L1DAT1	C13	DATA42	D13
L1DAT2	A14	L1DAT0	B14	DATA45	C14	DATA46	D14
NC	A15	$\overline{\text{RSTOUT}}$[1]	B15	DATA47	C15	DATA44	D15
FLAG10	E01	FLAG5	F01	FLAG1	G01	FLAG0	H01
$\overline{\text{RESET}}$	E02	FLAG7	F02	FLAG2	G02	$\overline{\text{IRQ0}}$	H02
FLAG8	E03	FLAG9	F03	FLAG4	G03	V_{DDINT}	H03
D0A	E04	FLAG6	F04	FLAG3	G04	$\overline{\text{IRQ1}}$	H04
V_{DDEXT}	E05	V_{DDINT}	F05	V_{DDEXT}	G05	V_{DDINT}	H05
V_{DDINT}	E06	GND	F06	GND	G06	GND	H06
V_{DDEXT}	E07	GND	F07	GND	G07	GND	H07
V_{DDINT}	E08	GND	F08	GND	G08	GND	H08
V_{DDEXT}	E09	GND	F09	GND	G09	GND	H09
V_{DDINT}	E10	GND	F10	GND	G10	GND	H10
V_{DDEXT}	E11	V_{DDINT}	F11	V_{DDEXT}	G11	V_{DDINT}	H11
L0DAT0	E12	DATA37	F12	DATA34	G12	DATA29	H12
DATA39	E13	DATA40	F13	DATA35	G13	DATA28	H13
DATA43	E14	DATA38	F14	DATA33	G14	DATA30	H14
DATA41	E15	DATA36	F15	DATA32	G15	DATA31	H15
$\overline{\text{IRQ2}}$	J01	TIMEXP	K01	ADDR19	L01	ADDR16	M01
ID1	J02	ADDR22	K02	ADDR17	L02	ADDR12	M02
ID2	J03	ADDR20	K03	ADDR21	L03	ADDR18	M03
ID0	J04	ADDR23	K04	ADDR2	L04	ADDR6	M04
V_{DDEXT}	J05	V_{DDINT}	K05	V_{DDEXT}	L05	ADDR0	M05
GND	J06	GND	K06	V_{DDINT}	L06	$\overline{\text{MS1}}$	M06
GND	J07	GND	K07	V_{DDEXT}	L07	$\overline{\text{BR6}}$	M07
GND	J08	GND	K08	V_{DDINT}	L08	V_{DDEXT}	M08
GND	J09	GND	K09	V_{DDEXT}	L09	$\overline{\text{WR}}$	M09
GND	J10	GND	K10	V_{DDINT}	L10	SDA10	M10
V_{DDEXT}	J11	V_{DDINT}	K11	V_{DDEXT}	L11	$\overline{\text{RAS}}$	M11
DATA26	J12	DATA22	K12	$\overline{\text{CAS}}$	L12	ACK	M12
DATA24	J13	DATA19	K13	DATA20	L13	DATA17	M13
DATA25	J14	DATA21	K14	DATA16	L14	$\overline{\text{DMAG2}}$	M14
DATA27	J15	DATA23	K15	DATA18	L15	$\overline{\text{DMAG1}}$	M15

Table 40. 225-Ball CSP_BGA Ball Assignments (Continued)

Ball Name	Ball Number	Ball Name	Ball Number	Ball Name	Ball Number	Ball Name	Ball Number
ADDR14	N01	ADDR13	P01	NC	R01		
ADDR15	N02	ADDR9	P02	ADDR11	R02		
ADDR10	N03	ADDR8	P03	ADDR7	R03		
ADDR5	N04	ADDR4	P04	ADDR3	R04		
ADDR1	N05	$\overline{MS2}$	P05	$\overline{MS3}$	R05		
$\overline{MS0}$	N06	$\overline{SBTS}$	P06	$\overline{PA}$	R06		
$\overline{BR5}$	N07	$\overline{BR4}$	P07	$\overline{BR3}$	R07		
$\overline{BR2}$	N08	$\overline{BR1}$	P08	$\overline{RD}$	R08		
BRST	N09	SDCLK1	P09	CLKOUT	R09		
SDCKE	N10	SDCLK0	P10	$\overline{HBR}$	R10		
$\overline{CS}$	N11	REDY	P11	$\overline{HBG}$	R11		
CLK_CFG1	N12	CLKIN	P12	$\overline{CLKDBL}$	R12		
CLK_CFG0	N13	DQM	P13	XTAL	R13		
AVDD	N14	AGND	P14	$\overline{SDWE}$	R14		
$\overline{DMAR1}$	N15	$\overline{DMAR2}$	P15	NC	R15		

[1] $\overline{RSTOUT}$ exists only for silicon revisions 1.2 and greater. Leave this ball unconnected for silicon revisions 0.3, 1.0, and 1.1.

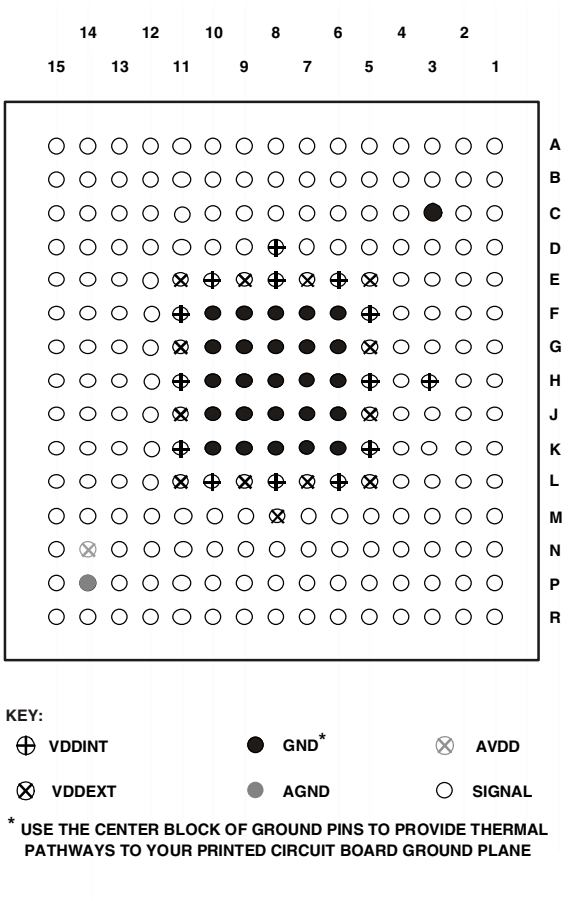


Figure 41. 225-Ball CSP_BGA Ball Assignments (Bottom View, Summary)

D02935-0-1/13 (C)