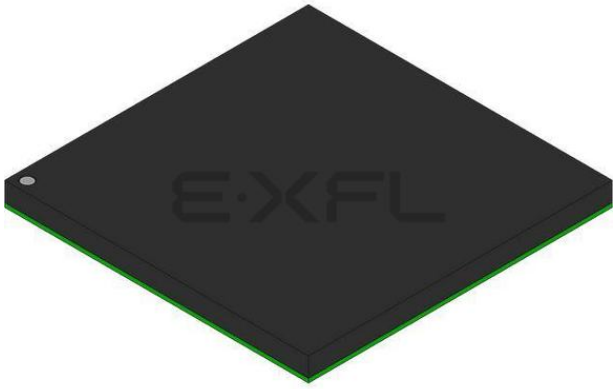

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Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

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Details	
Product Status	Active
Type	-
Interface	-
Clock Rate	-
Non-Volatile Memory	-
On-Chip RAM	-
Voltage - I/O	-
Voltage - Core	-
Operating Temperature	-
Mounting Type	-
Package / Case	-
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-21161nkcaz100

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- EE-128: DSP in C++: Calling Assembly Class Member Functions From C++
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Data Sheet

- ADSP-21161N: SHARC® Processor Data Sheet

Evaluation Kit Manuals

- ADSP-21161N EZ-KIT Lite® Evaluation System Manual

Integrated Circuit Anomalies

- ADSP-21161N_SHARC_Anomaly_List_for_Revisions 0.3,1.0,1.1,1.2,1.3

Processor Manuals

- ADSP-21160 SHARC® DSP Instruction Set Reference
- ADSP-21161 SHARC® Processor Hardware Reference
- SHARC Processors: Manuals

Product Highlight

- EZ-KIT Lite for Analog Devices ADSP-21161N SHARC Processor
- SHARC Processor Family

SOFTWARE AND SYSTEMS REQUIREMENTS

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When using the DAGs to transfer data in SIMD mode, two data values are transferred with each access of memory or the register file.

SIMD is supported only for internal memory accesses and is not supported for off-chip accesses.

Independent, Parallel Computation Units

Within each processing element is a set of computational units. The computational units consist of an arithmetic/logic unit (ALU), multiplier, and shifter. These units perform single-cycle instructions. The three units within each processing element are arranged in parallel, maximizing computational throughput. Single multifunction instructions execute parallel ALU and multiplier operations. In SIMD mode, the parallel ALU and multiplier operations occur in both processing elements. These computation units support IEEE 32-bit single-precision floating-point, 40-bit extended precision floating-point, and 32-bit fixed-point data formats.

Data Register File

A general-purpose data register file is contained in each processing element. The register files transfer data between the computation units and the data buses, and store intermediate results. These 10-port, 32-register (16 primary, 16 secondary) register files, combined with the SHARC enhanced Harvard architecture, allow unconstrained data flow between computation units and internal memory. The registers in PEX are referred to as R0–R15 and in PEY as S0–S15.

Single-Cycle Fetch of Instruction and Four Operands

The ADSP-21161N features an enhanced Harvard architecture in which the data memory (DM) bus transfers data and the program memory (PM) bus transfers both instructions and data (see Figure 2). With the ADSP-21161N's separate program and data memory buses and on-chip instruction cache, the processor can simultaneously fetch four operands (two over each data bus) and an instruction (from the cache), all in a single cycle.

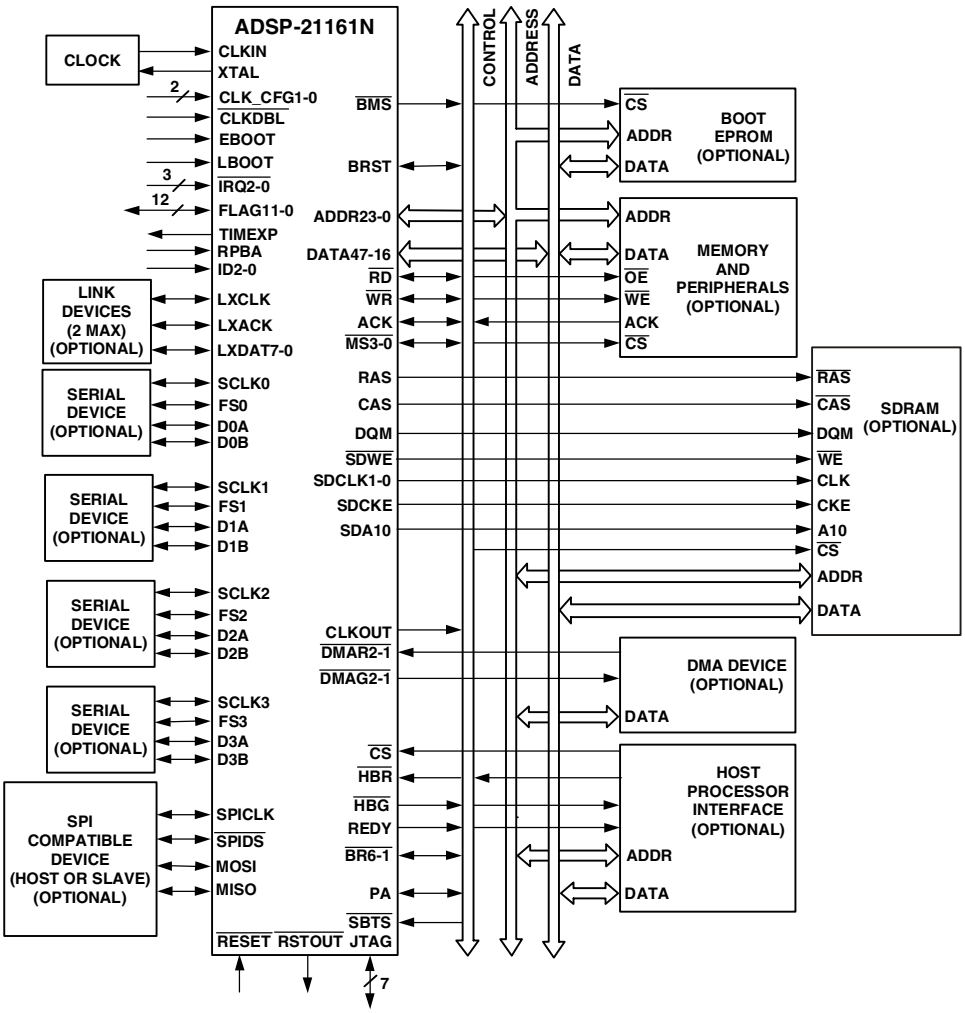


Figure 2. System Diagram

(for example 10k ohm). These pins must be driven low with a strong enough drive strength (10–50 ohms) to overcome the SHARC keeper latches present on these pins. If the drive strength provided is not strong enough, data access failures can occur.

For single processor SHARC systems using this host access feature, address pins ADDR17, ADDR18, ADDR19, and ADDR20 may be tied low (for example through a 10k ohm resistor), driven low by a buffer/driver, or left floating. Any of these options is sufficient.

General-Purpose I/O Ports

The ADSP-21161N also contains 12 programmable, general purpose I/O pins that can function as either input or output. As output, these pins can signal peripheral devices; as input, these pins can provide the test for conditional branching.

Program Booting

The internal memory of the ADSP-21161N can be booted at system power-up from either an 8-bit EPROM, a host processor, the SPI interface, or through one of the link ports. Selection of the boot source is controlled by the Boot Memory Select ($\overline{BMS}$), EBOOT (EPROM Boot), and Link/Host Boot (LBOOT) pins. 8-, 16-, or 32-bit host processors can also be used for booting.

Phase-Locked Loop and Crystal Double Enable

The ADSP-21161N uses an on-chip phase-locked loop (PLL) to generate the internal clock for the core. The CLK_CFG1–0 pins are used to select ratios of 2:1, 3:1, and 4:1. In addition to the PLL ratios, the $\overline{CLKDBL}$ pin can be used for more clock ratio options. The (1×/2× CLKIN) rate set by the $\overline{CLKDBL}$ pin determines the rate of the PLL input clock and the rate at which the external port operates. With the combination of CLK_CFG1–0 and $\overline{CLKDBL}$, ratios of 2:1, 3:1, 4:1, 6:1, and 8:1 between the core and CLKIN are supported. See also Figure 8 on Page 20.

Power Supplies

The ADSP-21161N has separate power supply connections for the analog (AV_{DD}/AGND), internal (V_{DDINT}), and external (V_{DDEXT}) power supplies. The internal and analog supplies must meet the 1.8 V requirement. The external supply must meet the 3.3 V requirement. All external supply pins must be connected to the same supply.

Note that the analog supply (AV_{DD}) powers the ADSP-21161N's clock generator PLL. To produce a stable clock, provide an external circuit to filter the power input to the AV_{DD} pin. Place the filter as close as possible to the pin. The AV_{DD} filter circuit shown in Figure 6 must be added for each ADSP-21161N in the multiprocessor system. To prevent noise coupling, use a wide trace for the analog ground (AGND) signal and install a decoupling capacitor as close as possible to the pin.

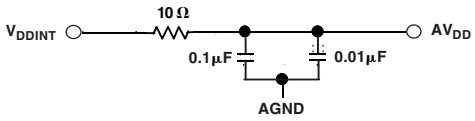


Figure 6. Analog Power (AV_{DD}) Filter Circuit

DEVELOPMENT TOOLS

Analog Devices supports its processors with a complete line of software and hardware development tools, including integrated development environments (which include CrossCore® Embedded Studio and/or VisualDSP++®), evaluation products, emulators, and a wide variety of software add-ins.

Integrated Development Environments (IDEs)

For C/C++ software writing and editing, code generation, and debug support, Analog Devices offers two IDEs.

The newest IDE, CrossCore Embedded Studio, is based on the Eclipse™ framework. Supporting most Analog Devices processor families, it is the IDE of choice for future processors, including multicore devices. CrossCore Embedded Studio seamlessly integrates available software add-ins to support real time operating systems, file systems, TCP/IP stacks, USB stacks, algorithmic software modules, and evaluation hardware board support packages. For more information visit www.analog.com/cces.

The other Analog Devices IDE, VisualDSP++, supports processor families introduced prior to the release of CrossCore Embedded Studio. This IDE includes the Analog Devices VDK real time operating system and an open source TCP/IP stack. For more information visit www.analog.com/visualdsp. Note that VisualDSP++ will not support future Analog Devices processors.

EZ-KIT Lite Evaluation Board

For processor evaluation, Analog Devices provides wide range of EZ-KIT Lite® evaluation boards. Including the processor and key peripherals, the evaluation board also supports on-chip emulation capabilities and other evaluation and development features. Also available are various EZ-Extenders®, which are daughter cards delivering additional specialized functionality, including audio and video processing. For more information visit www.analog.com and search on "ezkit" or "ezextender".

EZ-KIT Lite Evaluation Kits

For a cost-effective way to learn more about developing with Analog Devices processors, Analog Devices offer a range of EZ-KIT Lite evaluation kits. Each evaluation kit includes an EZ-KIT Lite evaluation board, directions for downloading an evaluation version of the available IDE(s), a USB cable, and a power supply. The USB controller on the EZ-KIT Lite board connects to the USB port of the user's PC, enabling the chosen IDE evaluation suite to emulate the on-board processor in-circuit. This permits the customer to download, execute, and debug programs for the EZ-KIT Lite system. It also supports in-circuit programming of the on-board Flash device to store user-specific boot code, enabling standalone operation. With the full version of Cross-

Table 2. Pin Function Descriptions (Continued)

Pin	Type	Function
$\overline{\text{SPIDS}}$	I	**Serial Peripheral Interface Slave Device Select**. An active low signal used to enable slave devices. This input signal behaves like a chip select, and is provided by the master device for the slave devices. In multimaster mode $\overline{\text{SPIDS}}$ signal can be asserted to a master device to signal that an error has occurred, as some other device is also trying to be the master device. If asserted low when the device is in master mode, it is considered a multimaster error. For a single-master, multiple-slave configuration where FLAG3–0 are used, this pin must be tied or pulled high to V_{DDEXT} on the master device. For ADSP-21161N to ADSP-21161N SPI interaction, any of the master ADSP-21161N's FLAG3–0 pins can be used to drive the $\overline{\text{SPIDS}}$ signal on the ADSP-21161N SPI slave device.
MOSI	I/O (o/d)	**SPI Master Out Slave**. If the ADSP-21161N is configured as a master, the MOSI pin becomes a data transmit (output) pin, transmitting output data. If the ADSP-21161N is configured as a slave, the MOSI pin becomes a data receive (input) pin, receiving input data. In an ADSP-21161N SPI interconnection, the data is shifted out from the MOSI output pin of the master and shifted into the MOSI input(s) of the slave(s). MOSI has an internal pull-up resistor.
MISO	I/O (o/d)	**SPI Master In Slave Out**. If the ADSP-21161N is configured as a master, the MISO pin becomes a data receive (input) pin, receiving input data. If the ADSP-21161N is configured as a slave, the MISO pin becomes a data transmit (output) pin, transmitting output data. In an ADSP-21161N SPI interconnection, the data is shifted out from the MISO output pin of the slave and shifted into the MISO input pin of the master. MISO has an internal pull-up resistor. MISO can be configured as o/d by setting the OPD bit in the SPICTL register. **Note:** *Only one slave is allowed to transmit data at any given time.*
LxDAT7–0 [DATA15–0]	I/O [I/O/T]	Link Port Data (Link Ports 0–1). For silicon revisions 1.2 and higher, each LxDAT pin has a keeper latch that is enabled when used as a data pin; or a 20 kΩ internal pull-down resistor that is enabled or disabled by the LxPDRDE bit of the LCTL register. For silicon revisions 0.3, 1.0, and 1.1 each LxDAT pin has a 50 kΩ internal pull-down resistor that is enabled or disabled by the LxPDRDE bit of the LCTL register. **Note:** *L1DAT7–0 are multiplexed with the DATA15–8 pins L0DAT7–0 are multiplexed with the DATA7–0 pins. If link ports are disabled and are not used, these pins can be used as additional data lines for executing instructions at up to the full clock rate from external memory. See DATA47–16 for more information.*
LxCLK	I/O	**Link Port Clock** (Link Ports 0–1). Each LxCLK pin has an internal pull-down 50 kΩ resistor that is enabled or disabled by the LxPDRDE bit of the LCTL register.
LxACK	I/O	**Link Port Acknowledge** (Link Ports 0–1). Each LxACK pin has an internal pull-down 50 kΩ resistor that is enabled or disabled by the LxPDRDE bit of the LCTL register.
EBOOT	I	**EPROM Boot Select**. For a description of how this pin operates, see the table in the $\overline{\text{BMS}}$ pin description. This signal is a system configuration selection that should be hardwired.
LBOOT	I	**Link Boot**. For a description of how this pin operates, see the table in the $\overline{\text{BMS}}$ pin description. This signal is a system configuration selection that should be hardwired.
$\overline{\text{BMS}}$	I/O/T	**Boot Memory Select**. Serves as an output or input as selected with the EBOOT and LBOOT pins (see Table 4). This input is a system configuration selection that should be hardwired. For Host and PROM boot, DMA channel 10 (EPB0) is used. For Link boot and SPI boot, DMA channel 8 is used. Three-state only in EPROM boot mode (when $\overline{\text{BMS}}$ is an output).
CLKIN	I	**Local Clock In**. Used in conjunction with XTAL. CLKIN is the ADSP-21161N clock input. It configures the ADSP-21161N to use either its internal clock generator or an external clock source. Connecting the necessary components to CLKIN and XTAL enables the internal clock generator. Connecting the external clock to CLKIN while leaving XTAL unconnected configures the ADSP-21161N to use the external clock source such as an external clock oscillator.The ADSP-21161N external port cycles at the frequency of CLKIN. The instruction cycle rate is a multiple of the CLKIN frequency; it is programmable at power-up via the CLK_CFG1–0 pins. CLKIN may not be halted, changed, or operated below the specified frequency.
XTAL	O	**Crystal Oscillator Terminal 2**. Used in conjunction with CLKIN to enable the ADSP-21161N's internal clock oscillator or to disable it to use an external clock source. See CLKIN.
CLK_CFG1-0	I	**Core/CLKIN Ratio Control**. ADSP-21161N core clock (instruction cycle) rate is equal to n × PLLICLK where n is user selectable to 2, 3, or 4, using the CLK_CFG1–0 inputs. These pins can also be used in combination with the $\overline{\text{CLKDBL}}$ pin to generate additional core clock rates of 6 × CLKIN and 8 × CLKIN (see the Clock Rate Ratios table in the $\overline{\text{CLKDBL}}$ description).

Table 2. Pin Function Descriptions (Continued)

Pin	Type	Function
$\overline{\text{CLKDBL}}$	I	**Crystal Double Mode Enable**. This pin is used to enable the 2× clock double circuitry, where CLKOUT can be configured as either 1× or 2× the rate of CLKIN. This CLKIN double circuit is primarily intended to be used for an external crystal in conjunction with the internal clock generator and the XTAL pin. The internal clock generator when used in conjunction with the XTAL pin and an external crystal is designed to support up to a maximum of 27.5 MHz external crystal frequency. $\overline{\text{CLKDBL}}$ can be used in XTAL mode to generate a 55 MHz input into the PLL. The 2× clock mode is enabled (during $\overline{\text{RESET}}$ low) by tying $\overline{\text{CLKDBL}}$ to GND, otherwise it is connected to V_{DDEXT} for 1× clock mode. For example, this enables the use of a 27.5 MHz crystal to enable 110 MHz core clock rates and a 55 MHz CLKOUT operation when CLK_CFG0=0, CLK_CFG1=0 and $\overline{\text{CLKDBL}}$=0. This pin can also be used to generate different clock rate ratios for external clock oscillators as well. The possible clock rate ratio options (up to 110 MHz) for either CLKIN (external clock oscillator) or XTAL (crystal input) are shown in Table 3 on Page 16. An 8:1 ratio enables the use of a 12.5 MHz crystal to generate a 100 MHz core (instruction clock) rate and a 25 MHz CLKOUT (external port) clock rate. See also Figure 8 on Page 20. **Note:** *When using an external crystal, the maximum crystal frequency cannot exceed 27.5 MHz. For all other external clock sources, the maximum CLKIN frequency is 55 MHz.*
CLKOUT	O/T	**Local Clock Out**. CLKOUT is 1× or 2× and is driven at either 1× or 2× the frequency of CLKIN frequency by the current bus master. The frequency is determined by the $\overline{\text{CLKDBL}}$ pin. This output is three-stated when the ADSP-21161N is not the bus master or when the host controls the bus ($\overline{\text{HBG}}$ asserted). A keeper latch on the DSP's CLKOUT pin maintains the output at the level it was last driven. This latch is only enabled on the ADSP-21161N with ID2–0=00x. If $\overline{\text{CLKDBL}}$ enabled, CLKOUT=2 × CLKIN If $\overline{\text{CLKDBL}}$ disabled, CLKOUT=1 × CLKIN **Note:** *CLKOUT is only controlled by the* $\overline{\text{CLKDBL}}$ *pin and operates at either 1 × CLKIN or 2 × CLKIN.* Do not use CLKOUT in multiprocessing systems. Use CLKIN instead.
$\overline{\text{RESET}}$	I/A	**Processor Reset**. Resets the ADSP-21161N to a known state and begins execution at the program memory location specified by the hardware reset vector address. The $\overline{\text{RESET}}$ input must be asserted (low) at power-up.
$\overline{\text{RSTOUT}}$[1]	O	**Reset Out**. When $\overline{\text{RSTOUT}}$ is asserted (low), this pin indicates that the core blocks are in reset. It is deasserted 4080 cycles after $\overline{\text{RESET}}$ is deasserted indicating that the PLL is stable and locked.
TCK	I	**Test Clock (JTAG)**. Provides a clock for JTAG boundary scan.
TMS	I/S	**Test Mode Select (JTAG)**. Used to control the test state machine. TMS has a 20 kΩ internal pull-up resistor.
TDI	I/S	**Test Data Input (JTAG)**. Provides serial data for the boundary scan logic. TDI has a 20 kΩ internal pull-up resistor.
TDO	O	**Test Data Output (JTAG)**. Serial scan output of the boundary scan path.
$\overline{\text{TRST}}$	I/A	**Test Reset (JTAG)**. Resets the test state machine. $\overline{\text{TRST}}$ must be asserted (pulsed low) after power-up or held low for proper operation of the ADSP-21161N. $\overline{\text{TRST}}$ has a 20 kΩ internal pull-up resistor.
$\overline{\text{EMU}}$	O (O/D)	**Emulation Status**. Must be connected to the ADSP-21161N Analog Devices DSP Tools product line of JTAG emulators target board connector only. $\overline{\text{EMU}}$ has a 50 kΩ internal pull-up resistor.
V_{DDINT}	P	**Core Power Supply**. Nominally +1.8 V dc and supplies the DSP's core processor (14 pins).
V_{DDEXT}	P	**I/O Power Supply**. Nominally +3.3 V dc. (13 pins).
AVDD	P	**Analog Power Supply**. Nominally +1.8 V dc and supplies the DSP's internal PLL (clock generator). This pin has the same specifications as V_{DDINT}, except that added filtering circuitry is required. For more information, see Power Supplies on Page 9.
AGND	G	**Analog Power Supply Return**.
GND	G	**Power Supply Return**. (26 pins).
NC		**Do Not Connect**. Reserved pins that must be left open and unconnected. (4 pins)

[1] $\overline{\text{RSTOUT}}$ exists only for silicon revisions 1.2 and greater.

Table 3. Clock Rate Ratios

$\overline{\text{CLKDBL}}$	CLK_CFG1	CLK_CFG0	Core:CLKIN	CLKIN:CLKOUT
1	0	0	2:1	1:1
1	0	1	3:1	1:1
1	1	0	4:1	1:1
0	0	0	4:1	1:2
0	0	1	6:1	1:2
0	1	0	8:1	1:2

BOOT MODES

Table 4. Boot Mode Selection

EBOOT	LBOOT	$\overline{\text{BMS}}$	Booting Mode
1	0	Output	EPROM (Connect $\overline{\text{BMS}}$ to EPROM chip select.)
0	0	1 (Input)	Host Processor
0	1	0 (Input)	Serial Boot via SPI
0	1	1 (Input)	Link Port
0	0	0 (Input)	No Booting. Processor executes from external memory.
1	1	x (Input)	Reserved

SPECIFICATIONS

OPERATING CONDITIONS

Parameter[1]	Description	Test Conditions	100 MHz		110 MHz		Unit
			Min	Max	Min	Max	
V_{DDINT}	Internal (Core) Supply Voltage		1.71	1.89	1.71	1.89	V
AV_{DD}	Analog (PLL) Supply Voltage		1.71	1.89	1.71	1.89	V
V_{DDEXT}	External (I/O) Supply Voltage		3.13	3.47	3.13	3.47	V
V_{IH}	High Level Input Voltage[2]	@ V_{DDEXT} = Max	2.0	V_{DDEXT}+0.5	2.0	V_{DDEXT}+0.5	V
V_{IL}	Low Level Input Voltage[2]	@ V_{DDEXT} = Min	–0.5	+0.8	–0.5	+0.8	V
T_{CASE}	Case Operating Temperature[3]		–40	+105	–40	+125	°C

[1] Specifications subject to change without notice.

[2] Applies to input and bidirectional pins: DATA47–16, ADDR23–0, $\overline{MS3–0}$, $\overline{RD}$, $\overline{WR}$, ACK, $\overline{SBTS}$, $\overline{IRQ2–0}$, FLAG11–0, $\overline{HBG}$, $\overline{HBR}$, $\overline{CS}$, $\overline{DMAR1}$, $\overline{DMAR2}$, $\overline{BR6–1}$, ID2–0, RPBA, $\overline{PA}$, BRST, FSx, DxA, DxB, SCLKx, $\overline{RAS}$, $\overline{CAS}$, $\overline{SDWE}$, SDCLK0, LxDAT7–0, LxCLK, LxACK, SPICLK, MOSI, MISO, $\overline{SPIDS}$, EBOOT, LBOOT, $\overline{BMS}$, SDCKE, CLK_CFGx, $\overline{CLKDBL}$, CLKIN, $\overline{RESET}$, TRST, TCK, TMS, TDI.

[3] See Thermal Characteristics on Page 55 for information on thermal specifications.

ELECTRICAL CHARACTERISTICS

Parameter	Description	Test Conditions	Min	Max	Unit
V_{OH}	High Level Output Voltage[1]	@ V_{DDEXT} = Min, I_{OH} = –2.0 mA[2]	2.4		V
V_{OL}	Low Level Output Voltage[1]	@ V_{DDEXT} = Min, I_{OL} = 4.0 mA[2]		0.4	V
I_{IH}	High Level Input Current[3, 4]	@ V_{DDEXT} = Max, V_{IN} = V_{DDEXT} Max		10	µA
I_{IL}	Low Level Input Current[3]	@ V_{DDEXT} = Max, V_{IN} = 0 V		10	µA
I_{IHC}	CLKIN High Level Input Current[5]	@ V_{DDEXT} = Max, V_{IN} = V_{DDEXT} Max		35	µA
I_{ILC}	CLKIN Low Level Input Current[5]	@ V_{DDEXT} = Max, V_{IN} = 0 V		35	µA
I_{IKH}	Keeper High Load Current[6]	@ V_{DDEXT} = Max, V_{IN} = 2.0 V	–250	–100	µA
I_{IKL}	Keeper Low Load Current[6]	@ V_{DDEXT} = Max, V_{IN} = 0.8 V	50	200	µA
I_{IKH-OD}	Keeper High Overdrive Current[6, 7, 8]	@ V_{DDEXT} = Max	–300		µA
I_{IKL-OD}	Keeper Low Overdrive Current[6, 7, 8]	@ V_{DDEXT} = Max	300		µA
I_{ILPU}	Low Level Input Current Pull-Up[4]	@ V_{DDEXT} = Max, V_{IN} = 0 V		350	µA
I_{OZH}	Three-State Leakage Current[9, 10, 11]	@ V_{DDEXT} = Max, V_{IN} = V_{DDEXT} Max		10	µA
I_{OZL}	Three-State Leakage Current[9, 12, 13]	@ V_{DDEXT} = Max, V_{IN} = 0 V		10	µA
I_{OZLPU1}	Three-State Leakage Current Pull-Up1[10]	@ V_{DDEXT} = Max, V_{IN} = 0 V		500	µA
I_{OZLPU2}	Three-State Leakage Current Pull-Up2[11]	@ V_{DDEXT} = Max, V_{IN} = 0 V		350	µA
I_{OZHPD1}	Three-State Leakage Current Pull-Down1[12]	@ V_{DDEXT} = Max, V_{IN} = V_{DDEXT} Max		350	µA
I_{OZHPD2}	Three-State Leakage Current Pull-Down2[13]	@ V_{DDEXT} = Max, V_{IN} = V_{DDEXT} Max		500	µA
$I_{DD-INPEAK}$	Supply Current (Internal)[14, 15]	t_{CCLK} = 9.0 ns, V_{DDINT} = Max		965	mA
		t_{CCLK} = 10.0 ns, V_{DDINT} = Max		900	
$I_{DD-INHIGH}$	Supply Current (Internal)[15, 16]	t_{CCLK} = 9.0 ns, V_{DDINT} = Max		700	mA
		t_{CCLK} = 10.0 ns, V_{DDINT} = Max		650	
$I_{DD-INLOW}$	Supply Current (Internal)[15, 17]	t_{CCLK} = 9.0 ns, V_{DDINT} = Max		535	mA
		t_{CCLK} = 10.0 ns, V_{DDINT} = Max		500	
$I_{DD-IDLE}$	Supply Current (Idle)[15, 18]	t_{CCLK} = 9.0 ns, V_{DDINT} = Max		425	mA
		t_{CCLK} = 10.0 ns, V_{DDINT} = Max		400	
AI_{DD}	Supply Current (Analog)[19]	@ AV_{DD} = Max		10	mA
C_{IN}	Input Capacitance[20, 21]	f_{IN} = 1 MHz, T_{CASE} = 25°C, V_{IN} = 1.8 V		4.7	pF

[1] Applies to output and bidirectional pins: DATA47–16, ADDR23–0, $\overline{MS3–0}$, $\overline{RD}$, $\overline{WR}$, ACK, DQM, FLAG11–0, $\overline{HBG}$, REDY, $\overline{DMAG1}$, $\overline{DMAG2}$, $\overline{BR6–1}$, BMSTR, $\overline{PA}$, BRST, FSx, DxA, DxB, SCLKx, $\overline{RAS}$, $\overline{CAS}$, $\overline{SDWE}$, SDA10, LxDAT7–0, LxCLK, LxACK, SPICLK, MOSI, MISO, $\overline{BMS}$, SDCLKx, SDCKE, $\overline{EMU}$, XTAL, TDO, CLKOUT, TIMEXP, $\overline{RSTOUT}$.

[2] See Output Drive Currents on Page 54 for typical drive current capabilities.

[3] Applies to input pins: DATA47–16, ADDR23–0, $\overline{MS3–0}$, $\overline{SBTS}$, $\overline{IRQ2–0}$, FLAG11–0, $\overline{HBG}$, $\overline{HBR}$, $\overline{CS}$, $\overline{BR6–1}$, ID2–0, RPBA, $\overline{BRST}$, FSx, DxA, DxB, SCLKx, $\overline{RAS}$, $\overline{CAS}$, $\overline{SDWE}$, SDCLK0, LxDAT7–0, LxCLK, LxACK, SPICLK, MOSI, MISO, $\overline{SPIDS}$, EBOOT, LBOOT, $\overline{BMS}$, SDCKE, CLK_CFGx, $\overline{CLKDBL}$, TCK, $\overline{RESET}$, CLKIN.

[4] Applies to input pins with 20 kΩ internal pull-ups: $\overline{RD}$, $\overline{WR}$, ACK, $\overline{DMAR1}$, $\overline{DMAR2}$, $\overline{PA}$, $\overline{TRST}$, TMS, TDI.

[5] Applies to CLKIN only.

[6] Applies to all pins with keeper latches: ADDR23–0, DATA47–0, $\overline{MS3–0}$, BRST, CLKOUT.

[7] Current required to switch from kept high to low or from kept low to high.

[8] Characterized, but not tested.

[9] Applies to three-statable pins: DATA47–16, ADDR23–0, $\overline{MS3–0}$, CLKOUT, FLAG11–0, REDY, $\overline{HBG}$, $\overline{BMS}$, $\overline{BR6–1}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{SDWE}$, DQM, SDCLKx, SDCKE, SDA10, BRST.

[10] Applies to three-statable pins with 20 kΩ pull-ups: $\overline{RD}$, $\overline{WR}$, $\overline{DMAG1}$, $\overline{DMAG2}$, $\overline{PA}$.

[11] Applies to three-statable pins with 50 kΩ internal pull-ups: DxA, DxB, SCLKx, SPICLK., $\overline{EMU}$, MISO, MOSI.

[12] Applies to three-statable pins with 50 kΩ internal pull-downs: LxDAT7–0 (below Revision1.2), LxCLK, LxACK. Use I_{OZHPD2} for Rev. 1.2 and higher.

[13] Applies to three-statable pins with 20 kΩ internal pull-downs: LxDAT7-0 (Revision 1.2 and higher).

[14] The test program used to measure $I_{DDINPEAK}$ represents worst-case processor operation and is not sustainable under normal application conditions. Actual internal power measurements made using typical applications are less than specified. For more information, see Power Dissipation on Page 20.

[15] Current numbers are for V_{DDINT} and AVDD supplies combined.

[16] $I_{DDINHIGH}$ is a composite average based on a range of high activity code. For more information, see Power Dissipation on Page 20.

[17] $I_{DDINLOW}$ is a composite average based on a range of low activity code. For more information, see Power Dissipation on Page 20.

[18] Idle denotes ADSP-21161N state during execution of IDLE instruction. For more information, see Power Dissipation on Page 20.

[19] Characterized, but not tested.

[20] Applies to all signal pins.

[21] Guaranteed, but not tested.

Clock Input

In systems that use multiprocessing or SBSRAM, $\overline{\text{CLKDBL}}$ cannot be enabled nor can the systems use an external crystal as the CLKIN source.

Do not use CLKOUT as the clock source for the SBSRAM device. Using an external crystal in conjunction with $\overline{\text{CLKDBL}}$ to generate a CLKOUT frequency is not supported. Negative hold times can result from the potential skew between CLKIN and CLKOUT.

Table 11. Clock Input

Parameter		100 MHz Min	100 MHz Max	110 MHz Min	110 MHz Max	Unit
Timing Requirements						
t_{CK}	CLKIN Period[1]	20	238	18	238	ns
t_{CKL}	CLKIN Width Low[1]	7.5	119	7	119	ns
t_{CKH}	CLKIN Width High[1]	7.5	119	7	119	ns
t_{CKRF}	CLKIN Rise/Fall (0.4 V–2.0 V)		3		3	ns
t_{CCLK}	CCLK Period	10	30	9	30	ns
Switching Characteristics						
t_{DCKOO}	CLKOUT Delay After CLKIN	0	2	0	2	ns
t_{CKOP}	CLKOUT Period	$t_{CK}-1$	$t_{CK}+1$	$t_{CK}-1$	$t_{CK}+1$	ns
t_{CKWH}	CLKOUT Width High	$t_{CKOP}/2-2$	$t_{CKOP}/2+2$	$t_{CKOP}/2-2$	$t_{CKOP}/2+2$	ns
t_{CKWL}	CLKOUT Width Low	$t_{CKOP}/2-2$	$t_{CKOP}/2+2$	$t_{CKOP}/2-2$	$t_{CKOP}/2+2$	ns

[1] CLKIN is dependent on the configuration of the CLKCFGx and $\overline{\text{CLKDBL}}$ pins to achieve desired t_{CCLK}.

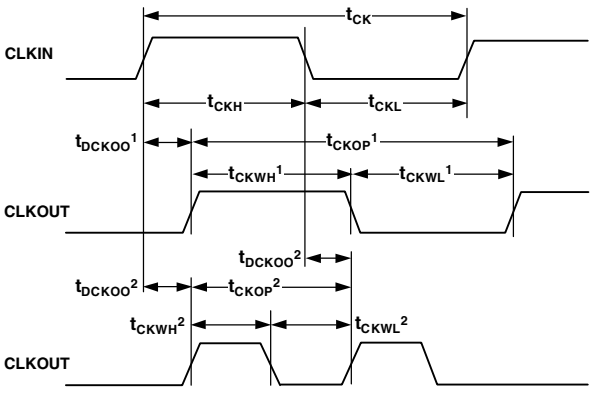
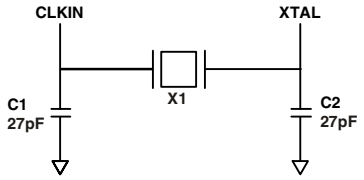


Figure 11. Clock Input

Clock Signals

The ADSP-21161N can use an external clock or a crystal. See CLKIN pin description. The programmer can configure the ADSP-21161N to use its internal clock generator by connecting the necessary components to CLKIN and XTAL. Figure 12 shows the component connections used for a crystal operating in fundamental mode.



SUGGESTED COMPONENTS FOR 100MHz OPERATION:
ECLIPTEK EC2SM-25.000M (SURFACE MOUNT PACKAGE)
ECLIPTEK EC-25.000M (THROUGH-HOLE PACKAGE)
C1 = 27pF
C2 = 27pF

NOTE: C1 AND C2 ARE SPECIFIC TO CRYSTAL SPECIFIED FOR X1. CONTACT CRYSTAL MANUFACTURER FOR DETAILS. THIS 25MHz CRYSTAL GENERATES A 100MHz CCLK AND A 50MHz EP CLOCK WITH $\overline{\text{CLKDBL}}$ ENABLED AND A 2:1 PLL MULTIPLY RATIO.

Figure 12. 100 MHz Operation (Fundamental Mode Crystal)

Reset

Table 12. Reset

Parameter		Min	Max	Unit
Timing Requirements				
t_{WRST}	$\overline{\text{RESET}}$ Pulsewidth Low[1]	$4t_{CK}$		ns
t_{SRST}	$\overline{\text{RESET}}$ Setup Before CLKIN High[2]	8.5		ns

[1] Applies after the power-up sequence is complete.
[2] Only required if multiple ADSP-21161Ns must come out of reset synchronous to CLKIN with program counters (PC) equal. Not required for multiple ADSP-21161Ns communicating over the shared bus (through the external port), because the bus arbitration logic synchronizes itself automatically after reset.

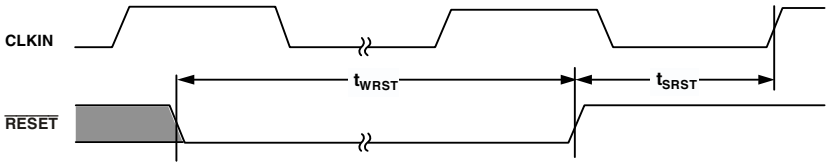


Figure 13. Reset

Memory Read — Bus Master

Use these specifications for asynchronous interfacing to memories (and memory-mapped peripherals) without reference to CLKIN except for ACK pin requirements listed in footnote 4 of Table 16. These specifications apply when the ADSP-21161N is the bus master accessing external memory space in asynchronous access mode.

Table 16. Memory Read — Bus Master

Parameter		100 MHz Min	100 MHz Max	110 MHz Min	110 MHz Max	Unit
Timing Requirements						
t_{DAD}	Address, Selects Delay to Data Valid[1, 2, 3]		$t_{CKOP}-0.25t_{CCLK}-8.5+W$		$t_{CKOP}-0.25t_{CCLK}-6.75+W$	ns
t_{DRLD}	$\overline{RD}$ Low to Data Valid[1,3]		$0.75t_{CKOP}-11+W$		$0.75t_{CKOP}-11+W$	ns
t_{HDA}	Data Hold from Address, Selects[4]	0		0		ns
t_{SDS}	Data Setup to $\overline{RD}$ High	8		8		ns
t_{HDRH}	Data Hold from $\overline{RD}$ High[4]	1		1		ns
t_{DAAK}	ACK Delay from Address, Selects[2, 5]		$t_{CKOP}-0.5t_{CCLK}-12+W$		$t_{CKOP}-0.5t_{CCLK}-12+W$	ns
t_{DSAK}	ACK Delay from $\overline{RD}$ Low[5]		$t_{CKOP}-0.75t_{CCLK}-11+W$		$t_{CKOP}-0.75t_{CCLK}-11+W$	ns
t_{SAKC}	ACK Setup to CLKIN[5]	$0.5t_{CCLK}+3$		$0.5t_{CCLK}+3$		ns
t_{HAKC}	ACK Hold After CLKIN	1		1		ns
Switching Characteristics						
t_{DRHA}	Address Selects Hold After $\overline{RD}$ High	$0.25t_{CCLK}-1+H$		$0.25t_{CCLK}-1+H$		ns
t_{DARL}	Address Selects to $\overline{RD}$ Low[2]	$0.25t_{CCLK}-3$		$0.25t_{CCLK}-3$		ns
t_{RW}	$\overline{RD}$ Pulsewidth	$t_{CKOP}-0.5t_{CCLK}-1+W$		$t_{CKOP}-0.5t_{CCLK}-1+W$		ns
t_{RWR}	$\overline{RD}$ High to $\overline{WR}$, $\overline{RD}$, $\overline{DMAGx}$ Low	$0.5t_{CCLK}-1+HI$		$0.5t_{CCLK}-1+HI$		ns

W = (number of wait states specified in WAIT register) × t_{CKOP}.
HI = t_{CKOP} (if an address hold cycle or bus idle cycle occurs, as specified in WAIT register; otherwise HI = 0).
H = t_{CKOP} (if an address hold cycle occurs as specified in WAIT register; otherwise H = 0).

[1] Data Delay/Setup: User must meet t_{DAD}, t_{DRLD}, or t_{SDS}.
[2] The falling edge of $\overline{MSx}$, $\overline{BMS}$ is referenced.
[3] The maximum limits of timing requirement values for t_{DAD} and t_{DRLD} parameters are applicable for the case where ACK is always high.
[4] Data Hold: User must meet t_{HDA} or t_{HDRH} in asynchronous access mode. See Example System Hold Time Calculation on Page 54 for the calculation of hold times given capacitive and dc loads.
[5] For asynchronous access, ACK is sampled only after the programmed wait states for the access have been counted. For the first CLKIN cycle of a new external memory access, ACK must be driven low (deasserted) by t_{DAAK}, t_{DSAK}, or t_{SAKC}. For the second and subsequent cycles of an asynchronous external memory access, the t_{SAKC} and t_{HAKC} must be met for both assertion and deassertion of ACK signal.

Memory Write — Bus Master

Use these specifications for asynchronous interfacing to memories (and memory-mapped peripherals) without reference to CLKIN except for ACK pin requirements listed in footnote 1 of Table 17. These specifications apply when the ADSP-21161N is the bus master accessing external memory space in asynchronous access mode.

Table 17. Memory Write — Bus Master

Parameter		Min	Max	Unit
Timing Requirements				
t_{DAAK}	ACK Delay from Address, Selects[1,2]		t_{CKOP}–0.5t_{CCLK}–12+W	ns
t_{DSAK}	ACK Delay from $\overline{WR}$ Low[1]		t_{CKOP}–0.75t_{CCLK}–11+W	ns
t_{SAKC}	ACK Setup to CLKIN[1]	0.5t_{CCLK}+3		ns
t_{HAKC}	ACK Hold After CLKIN[1]	1		ns
Switching Characteristics				
t_{DAWH}	Address, Selects to $\overline{WR}$ Deasserted[2]	t_{CKOP} – 0.25t_{CCLK} – 3+W		ns
t_{DAWL}	Address, Selects to $\overline{WR}$ Low[2]	0.25t_{CCLK} – 3		ns
t_{WW}	$\overline{WR}$ Pulsewidth	t_{CKOP} – 0.5t_{CCLK} – 1+W		ns
t_{DDWH}	Data Setup Before $\overline{WR}$ High	t_{CKOP}–0.25t_{CCLK} – 13.5+W		ns
t_{DWHA}	Address Hold After $\overline{WR}$ Deasserted	0.25t_{CCLK} – 1+H		ns
t_{DWHD}	Data Hold After $\overline{WR}$ Deasserted	0.25t_{CCLK} – 1+H		ns
t_{DATRWH}	Data Disable After $\overline{WR}$ Deasserted[3]	0.25t_{CCLK} – 2+H	0.25t_{CCLK}+2.5+H	ns
t_{WWR}	$\overline{WR}$ High to $\overline{WR}$, $\overline{RD}$, $\overline{DMAGx}$ Low	0.5t_{CCLK} – 1.25+HI		ns
t_{DDWR}	Data Disable Before $\overline{WR}$ or $\overline{RD}$ Low	0.25t_{CCLK} – 3+I		ns
t_{WDE}	$\overline{WR}$ Low to Data Enabled	–0.25t_{CCLK} – 1		ns

W = (number of wait states specified in WAIT register) × t_{CKOP}.
H = t_{CKOP} (if an address hold cycle occurs, as specified in WAIT register; otherwise H = 0).
HI = t_{CKOP} (if an address hold cycle or bus idle cycle occurs, as specified in WAIT register; otherwise HI = 0).
I = t_{CKOP} (if a bus idle cycle occurs, as specified in WAIT register; otherwise I = 0).

[1] For asynchronous access, ACK is sampled only after the programmed wait states for the access have been counted. For the first CLKIN cycle of a new external memory access, ACK must be driven low (deasserted) by t_{DAAK}, t_{DSAK}, or t_{SAKC}. For the second and subsequent cycles of an asynchronous external memory access, the t_{SAKC} and t_{HAKC} must be met for both assertion and deassertion of ACK signal.
[2] The falling edge of $\overline{MSx}$, $\overline{BMS}$ is referenced.
[3] See Example System Hold Time Calculation on Page 54 for calculation of hold times given capacitive and dc loads.

Host Bus Request

Use these specifications for asynchronous host bus requests of an ADSP-21161N ($\overline{HBR}$, $\overline{HBG}$).

Table 20. Host Bus Request

Parameter		100 MHz Min	100 MHz Max	110 MHz Min	110 MHz Max	Unit
Timing Requirements						
$t_{HBGRCSV}$	$\overline{HBG}$ Low to $\overline{RD}$/$\overline{WR}$/$\overline{CS}$ Valid		19		19	ns
t_{SHBRI}	$\overline{HBR}$ Setup Before CLKIN[1]	6		6		ns
t_{HHBRI}	$\overline{HBR}$ Hold After CLKIN[1]	1		1		ns
t_{SHBGI}	$\overline{HBG}$ Setup Before CLKIN	6		6		ns
t_{HHBGI}	$\overline{HBG}$ Hold After CLKIN	1		1		ns
Switching Characteristics						
t_{DHBGO}	$\overline{HBG}$ Delay After CLKIN		7		7	ns
t_{HHBGO}	$\overline{HBG}$ Hold After CLKIN	1.5		1.5		ns
t_{DRDYCS}	REDY (O/D) or (A/D) Low from $\overline{CS}$ and $\overline{HBR}$ Low[2]		10		10	ns
t_{TRDYHG}	REDY (O/D) Disable or REDY (A/D) High from $\overline{HBG}$[2]	t_{CKOP} + 14		t_{CKOP} + 12		ns
t_{ARDYTR}	REDY (A/D) Disable from $\overline{CS}$ or $\overline{HBR}$ High[2]		11		11	ns

[1] Only required for recognition in the current cycle.
[2] (O/D) = open drain, (A/D) = active drive.

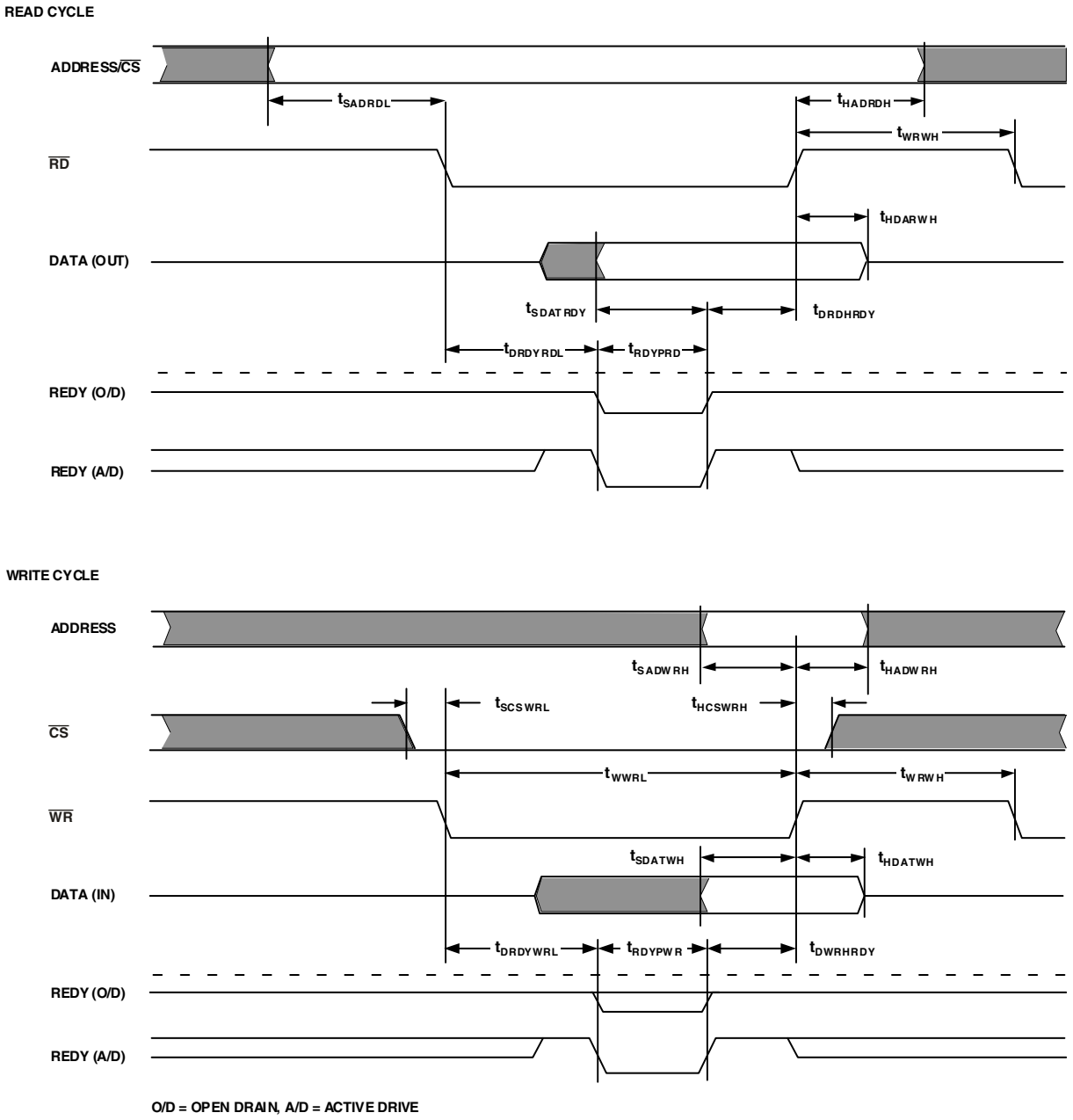
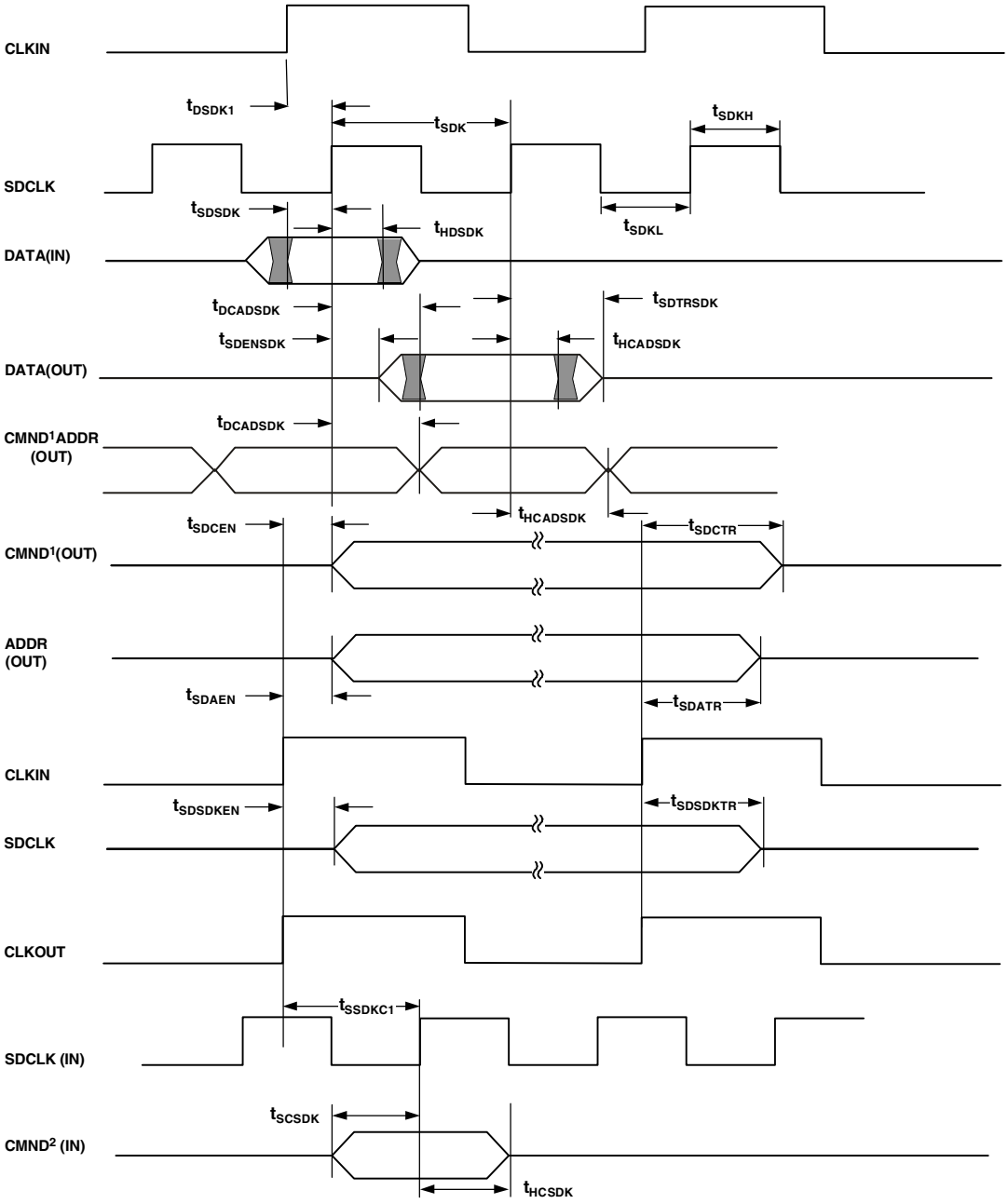


Figure 23. Asynchronous Read/Write — Host to ADSP-21161N



1COMMAND = SDCKE, $\overline{MSx}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{SDWE}$, DQM, AND SDA10.
2COMMAND = SDCKE, $\overline{RAS}$, $\overline{CAS}$, AND $\overline{SDWE}$.

Figure 26. SDRAM Interface

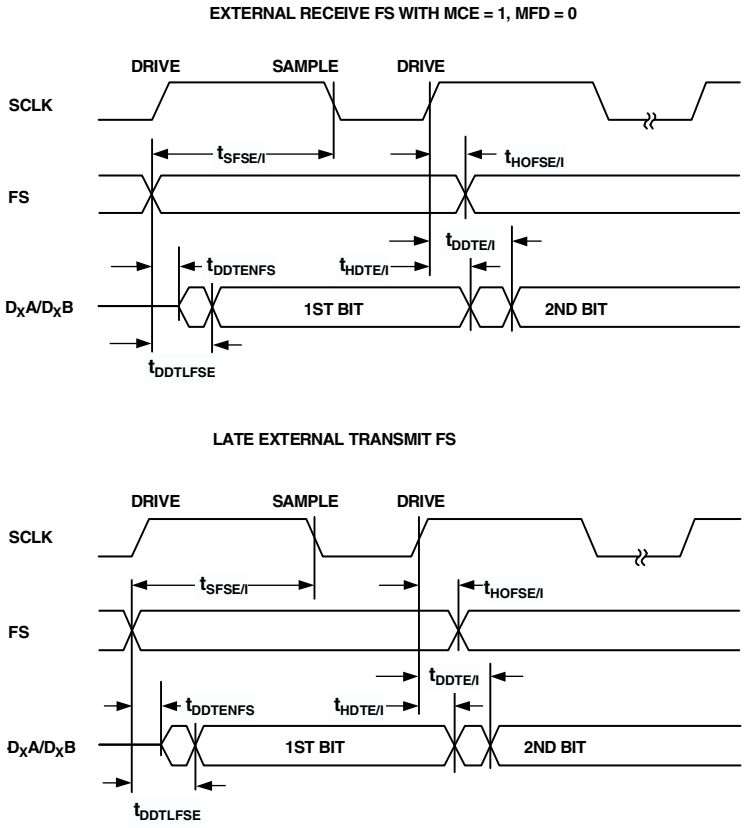


Figure 30. Serial Ports — External Late Frame Sync

Table 37. SPI Interface Protocol — Slave Switching and Timing

Parameter		Min	Max	Unit
Timing Requirements				
$t_{SPICLKS}$	Serial Clock Cycle	$8t_{CCLK}$		ns
t_{SPICHS}	Serial Clock High Period	$4t_{CCLK}-4$		ns
t_{SPICLS}	Serial Clock Low Period	$4t_{CCLK}-4$		ns
t_{SDSCO}	$\overline{SPIDS}$ Assertion to First SPICLK Edge			
	CPHASE = 0	$3.5t_{CCLK}+8$		ns
	CPHASE = 1	$1.5t_{CCLK}+8$		ns
t_{HDS}	Last SPICLK Edge to $\overline{SPIDS}$ Not Asserted CPHASE = 0	0		ns
t_{SSPIDS}	Data Input Valid to SPICLK Edge (Data Input Set-up Time)	0		ns
t_{HSPIDS}	SPICLK Last Sampling Edge to Data Input Not Valid	$t_{CCLK}+1$		ns
t_{SDPPW}	$\overline{SPIDS}$ Deassertion Pulsewidth (CPHASE = 0)	t_{CCLK}		ns
Switching Characteristics				
t_{DSOE}	$\overline{SPIDS}$ Assertion to Data Out Active	2	$0.5t_{CCLK}+5.5$	ns
t_{DSDHI}	$\overline{SPIDS}$ Deassertion to Data High Impedance	1.5	$0.5t_{CCLK}+5.5$	ns
$t_{DDSPIDS}$	SPICLK Edge to Data Out Valid (Data Out Delay Time)		$0.75t_{CCLK}+3$	ns
$t_{HDSPIDS}$[1]	SPICLK Edge to Data Out Not Valid (Data Out Hold Time)	$0.25t_{CCLK}+3$		ns
t_{HDLSBS}[1]	SPICLK Edge to Last Bit Out Not Valid (Data Out Hold Time) for LSB	$0.5t_{SPICLK}+4.5t_{CCLK}$		ns
t_{DSOV}[2]	$\overline{SPIDS}$ Assertion to Data Out Valid (CPHASE = 0)		$1.5t_{CCLK}+7$	ns

[1] When CPHASE = 0 and baud rate is greater than 1, t_{HDLSBS} affects the length of the last bit transmitted.
[2] Applies to the first deassertion of $\overline{SPIDS}$ only.

JTAG Test Access Port and Emulation

Table 38. JTAG Test Access Port and Emulation

Parameter		Min	Max	Unit
Timing Requirements				
t_{TCK}	TCK Period	t_{CK}		ns
t_{STAP}	TDI, TMS Setup Before TCK High	5		ns
t_{HTAP}	TDI, TMS Hold After TCK High	6		ns
t_{SSYS}	System Inputs Setup Before TCK Low[1]	2		ns
t_{HSYS}	System Inputs Hold After TCK Low[1]	15		ns
t_{TRSTW}	$\overline{TRST}$ Pulsewidth	$4t_{CK}$		ns
Switching Characteristics				
t_{DTDO}	TDO Delay from TCK Low		13	ns
t_{DSYS}	System Outputs Delay After TCK Low[2]		30	ns

[1] System Inputs = DATA47–16, ADDR23–0, $\overline{RD}$, $\overline{WR}$, ACK, RPBA, $\overline{SPIDS}$, EBOOT, LBOOT, $\overline{DMAR2–1}$, CLK_CFG1–0, $\overline{CLKDBL}$, $\overline{CS}$, $\overline{HBR}$, $\overline{SBTS}$, ID2–0, $\overline{IRQ2–0}$, $\overline{RESET}$, $\overline{BMS}$, MISO, MOSI, SPICLK, DxA, DxB, SCLKx, FSx, LxDAT7–0, LxCLK, LxACK, $\overline{SDWE}$, $\overline{HBG}$, $\overline{RAS}$, $\overline{CAS}$, SDCLK0, SDCKE, BRST, $\overline{BR6–1}$, $\overline{PA}$, $\overline{MS3–0}$, FLAG11–0.
[2] System Outputs = $\overline{BMS}$, MISO, MOSI, SPICLK, DxA, DxB, SCLKx, FSx, LxDAT7–0, LxCLK, LxACK, DATA47–16, $\overline{SDWE}$, ACK, $\overline{HBG}$, $\overline{RAS}$, $\overline{CAS}$, SDCLK1–0, SDCKE, BRST, $\overline{RD}$, $\overline{WR}$, $\overline{BR6–1}$, $\overline{PA}$, $\overline{MS3–0}$, ADDR23–0, FLAG11–0, $\overline{DMAG2–1}$, DQM, REDY, CLKOUT, SDA10, TIMEXP, $\overline{EMU}$, BMSTR, $\overline{RSTOUT}$.

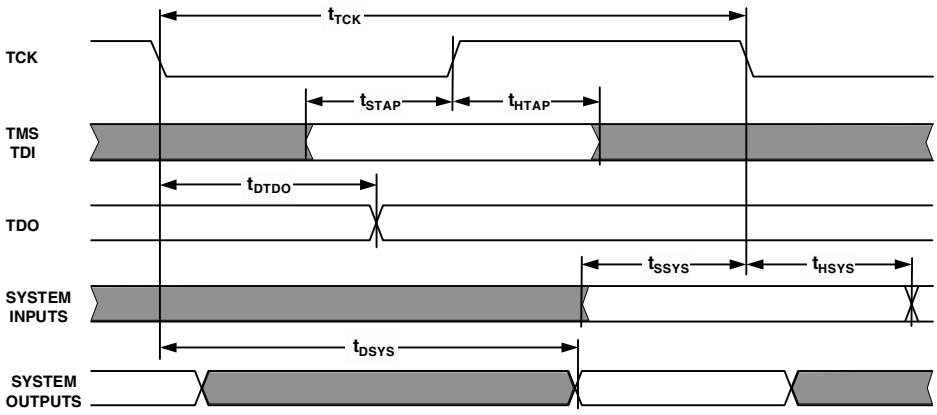


Figure 33. JTAG Test Access Port and Emulation

OUTPUT DRIVE CURRENTS

Figure 34 shows typical I-V characteristics for the output drivers of the ADSP-21161N. The curves represent the current drive capability of the output drivers as a function of output voltage.

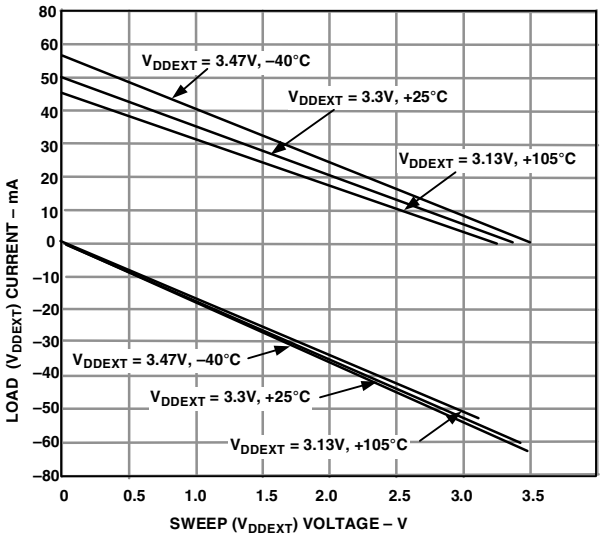


Figure 34. Typical Drive Currents

TEST CONDITIONS

The DSP is tested for output enable, disable, and hold time.

Output Enable Time

Output pins are considered to be enabled when they have made a transition from a high impedance state to the point when they start driving. The output enable time t_{ENA} is the interval from the point when a reference signal reaches a high or low voltage level to the point when the output has reached a specified high or low trip point, as shown in the Output Enable/Disable diagram (Figure 35). If multiple pins (such as the data bus) are enabled, the measurement value is that of the first pin to start driving.

Output Disable Time

Output pins are considered to be disabled when they stop driving, go into a high-impedance state, and start to decay from their output high or low voltage. The time for the voltage on the bus to decay by ΔV is dependent on the capacitive load, C_L and the load current, I_L. This decay time can be approximated by the following equation:

$$t_{DECAY} = (C_L \Delta V)/I_L$$

The output disable time t_{DIS} is the difference between $t_{MEASURED}$ and t_{DECAY} as shown in Figure 35. The time $t_{MEASURED}$ is the interval from when the reference signal switches to when the output voltage decays ΔV from the measured output high or output low voltage. t_{DECAY} is calculated with test loads C_L and I_L, and with ΔV equal to 0.5 V.

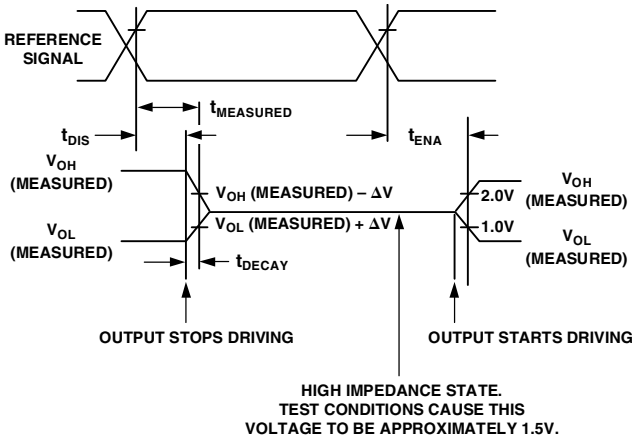


Figure 35. Output Enable/Disable

Example System Hold Time Calculation

To determine the data output hold time in a particular system, first calculate t_{DECAY} using the equation given above. Choose ΔV to be the difference between the ADSP-21161N's output voltage and the input threshold for the device requiring the hold time. A typical ΔV will be 0.4 V. C_L is the total bus capacitance (per data line), and I_L is the total leakage or three-state current (per data line). The hold time will be t_{DECAY} plus the minimum disable time (i.e., t_{DATRWH} for the write cycle).

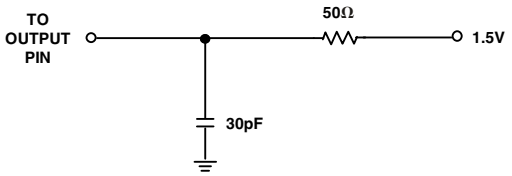


Figure 36. Equivalent Device Loading for AC Measurements (Includes All Fixtures)

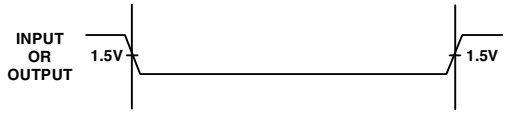


Figure 37. Voltage Reference Levels for AC Measurements (Except Output Enable/Disable)

OUTLINE DIMENSIONS

The ADSP-21161N comes in a 17 mm × 17 mm, 225-ball CSP_BGA package with 15 rows of balls.

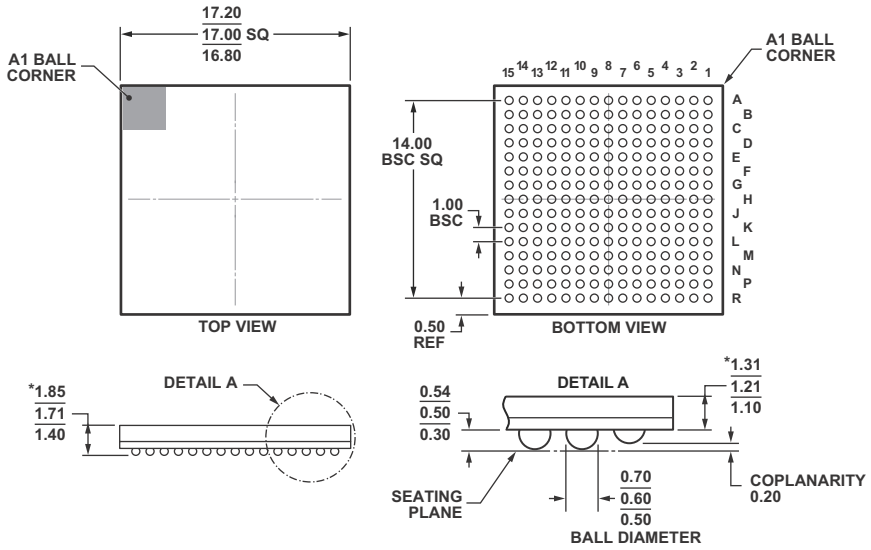


Figure 42. 225-Ball CSP_BGA (BC-225-1)

SURFACE-MOUNT DESIGN

Table 41 is provided as an aid to PCB design. For industry standard design recommendations, refer to IPC-7351, *Generic Requirements for Surface-Mount Design and Land Pattern Standard.*

Table 41. BGA Data for Use with Surface-Mount Design

Package	Ball Attach Type	Solder Mask Opening	Ball Pad Size
225-Ball CSP_BGA (BC-225-1)	Solder Mask Defined	0.40 mm diameter	0.53 mm diameter

ORDERING GUIDE

Model[1]	Temperature Range[2]	Instruction Rate	On-Chip SRAM	Package Description	Package Option
ADSP-21161NKCA-100	0°C to 85°C	100 MHz	1M bit	225-Ball CSP_BGA	BC-225-1
ADSP-21161NCCA-100	–40°C to +105°C	100 MHz	1M bit	225-Ball CSP_BGA	BC-225-1
ADSP-21161NKCAZ100	0°C to 85°C	100 MHz	1M bit	225-Ball CSP_BGA	BC-225-1
ADSP-21161NCCAZ100	–40°C to +105°C	100 MHz	1M bit	225-Ball CSP_BGA	BC-225-1
ADSP-21161NYCAZ110	–40°C to +125°C	110 MHz	1M bit	225-Ball CSP_BGA	BC-225-1

[1] Z = RoHS Compliant Part.
[2] Referenced temperature is case temperature.