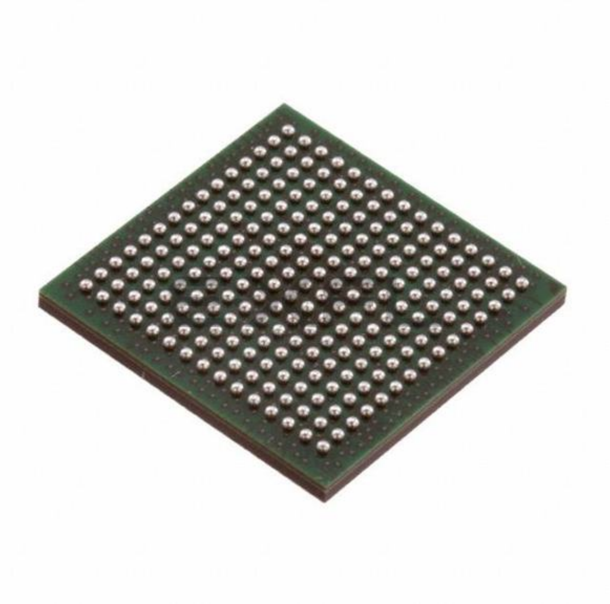

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Active
Type	Floating Point
Interface	Host Interface, Link Port, Serial Port
Clock Rate	110MHz
Non-Volatile Memory	External
On-Chip RAM	128kB
Voltage - I/O	3.30V
Voltage - Core	1.80V
Operating Temperature	-40°C ~ 125°C (TC)
Mounting Type	Surface Mount
Package / Case	255-BGA, CSPBGA
Supplier Device Package	255-CSPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-21161nycaz110

TOOLS AND SIMULATIONS

- ADSP-21161: 225 ball PBGA and MBGA Packages Silicon
- Designing with BGA
- SHARC Processors Software and Tools
- ADSP-21161N R1.1 IBIS Datafile BGA Package
- ADSP-21161N R1.2 IBIS Datafile BGA Package

REFERENCE MATERIALS

Product Selection Guide

- ADI Complementary Parts Guide - Supervisory Devices and DSP Processors

Technical Articles

- An Efficient Asynchronous Sampling-rate Conversion Algorithm for Multi-channel Audio Applications

DESIGN RESOURCES

- ADSP-21161N Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

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GENERAL DESCRIPTION

The ADSP-21161N SHARC® DSP is a low cost derivative of the ADSP-21160 featuring Analog Devices Super Harvard Architecture. Easing portability, the ADSP-21161N is source code compatible with the ADSP-21160 and with first generation ADSP-2106x SHARC processors in SISD (Single-Instruction, Single-Data) mode. Like other SHARC DSPs, the ADSP-21161N is a 32-bit processor that is optimized for high performance DSP applications. The ADSP-21161N includes a 100 MHz or 110 MHz core, a dual-ported on-chip SRAM, an integrated I/O processor with multiprocessing support, and multiple internal buses to eliminate I/O bottlenecks.

As was first offered in the ADSP-21160, the ADSP-21161N offers a single-instruction multiple-data (SIMD) architecture. Using two computational units (ADSP-2106x SHARC processors have one), the ADSP-21161N can double cycle performance versus the ADSP-2106x on a range of DSP algorithms.

Fabricated in a state of the art, high speed, low power CMOS process, the ADSP-21161N has a 10 ns or 9 ns instruction cycle time. With its SIMD computational hardware running at 110 MHz, the ADSP-21161N can perform 660 million floating-point operations per second. Table 1 shows performance benchmarks for the ADSP-21161N.

These benchmarks provide single-channel extrapolations of measured dual-channel processing performance. For more information on benchmarking and optimizing DSP code, for both single and dual-channel processing, see the Analog Devices Inc. website.

Table 1. Benchmarks

Benchmark Algorithm	100 MHz Instruction Rate	110 MHz Instruction Rate
1024 Point Complex FFT (Radix 4, with Reversal)	92 μs	83.6 μs
FIR Filter (Per Tap)	5 ns	4.5 ns
IIR Filter (Per Biquad)	20 ns	18.18 ns
Matrix Multiply (Pipelined)		
[3 × 3] × [3 × 1]	45 ns	40.9 ns
[4 × 4] × [4 × 1]	80 ns	72.72 ns
Divide (y/x)	60 ns	54.54 ns
Inverse Square Root	40 ns	36.36 ns
DMA Transfers	800M bytes/s	880M bytes/s

The ADSP-21161N continues SHARC's industry-leading standards of integration for DSPs, combining a high performance 32-bit DSP core with integrated, on-chip system features. These features include a 1M bit dual ported SRAM memory, host processor interface, I/O processor that supports 14 DMA channels, four serial ports, two link ports, SDRAM controller, SPI interface, external parallel bus, and glueless multiprocessing.

The block diagram of the ADSP-21161N on Page 1 illustrates the following architectural features:

- Two processing elements, each made up of an ALU, multiplier, shifter, and data register file
- Data address generators (DAG1, DAG2)
- Program sequencer with instruction cache
- PM and DM buses capable of supporting four 32-bit data transfers between memory and the core every core processor cycle
- Interval timer
- On-Chip SRAM (1M bit)
- SDRAM controller for glueless interface to SDRAMs
- External port that supports:
  - Interfacing to off-chip memory peripherals
  - Glueless multiprocessing support for six ADSP-21161N SHARCs
  - Host port read/write of IOP registers
- DMA controller
- Four serial ports
- Two link ports
- SPI compatible interface
- JTAG test access port
- 12 general-purpose I/O pins

Figure 2 shows a typical single-processor system. A multiprocessing system appears in Figure 5 on Page 8.

ADSP-21161N FAMILY CORE ARCHITECTURE

The ADSP-21161N includes the following architectural features of the ADSP-2116x family core. The ADSP-21161N is code compatible at the assembly level with the ADSP-21160, ADSP-21060, ADSP-21061, ADSP-21062, and ADSP-21065L.

SIMD Computational Engine

The ADSP-21161N contains two computational processing elements that operate as a single-instruction multiple-data (SIMD) engine. The processing elements are referred to as PEX and PEY, and each contains an ALU, multiplier, shifter, and register file. PEX is always active, and PEY may be enabled by setting the PEYEN mode bit in the MODE1 register. When this mode is enabled, the same instruction is executed in both processing elements, but each processing element operates on different data. This architecture is efficient at executing math intensive DSP algorithms.

Entering SIMD mode also has an effect on the way data is transferred between memory and the processing elements. When in SIMD mode, twice the data bandwidth is required to sustain computational operation in the processing elements. Because of this requirement, entering SIMD mode also doubles the bandwidth between memory and the processing elements.

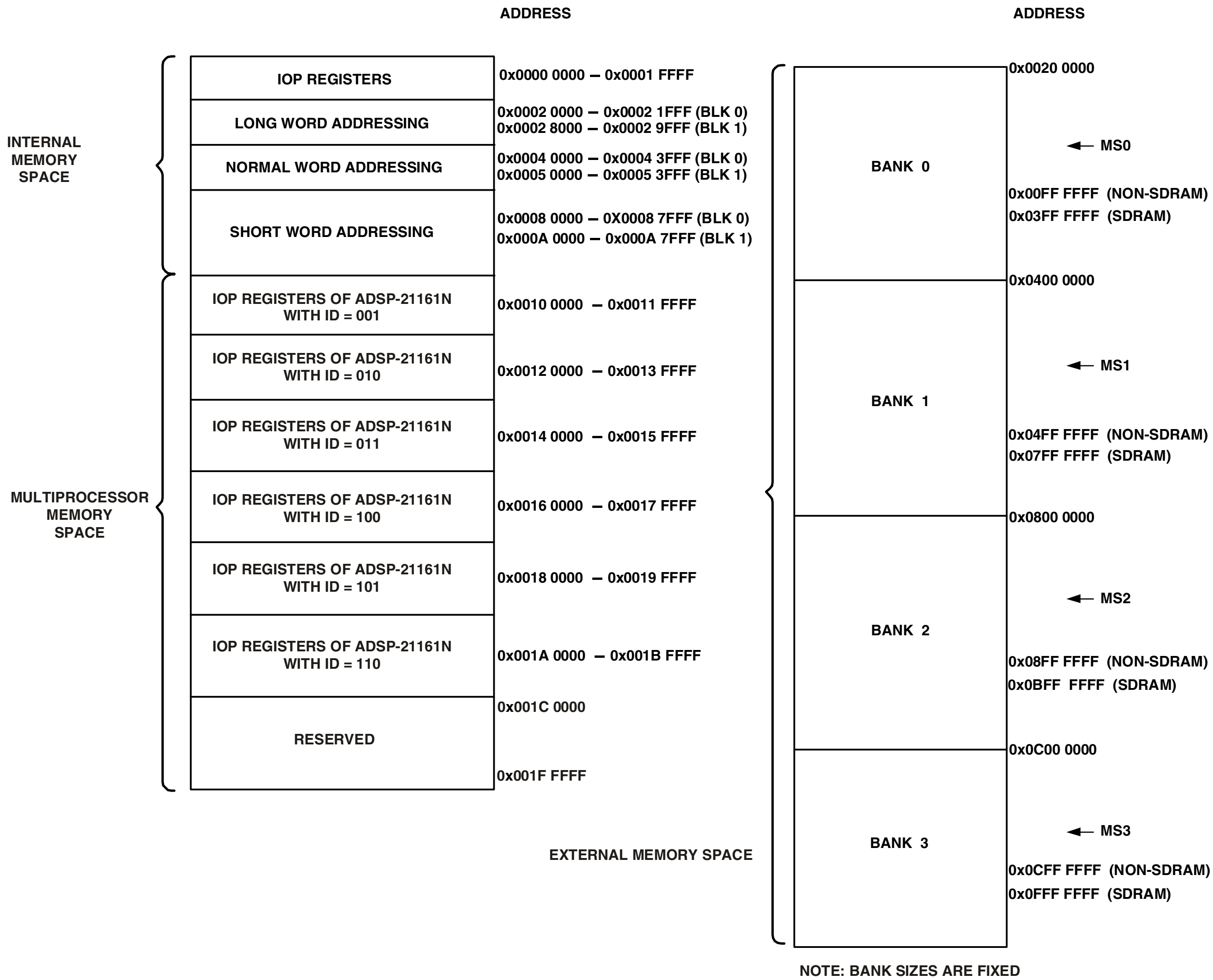


Figure 3. Memory Map

JTAG emulators provides emulation at full processor speed, allowing inspection and modification of memory, registers, and processor stacks. The processor's JTAG interface ensures that the emulator will not affect target system loading or timing.

For complete information on SHARC Analog Devices DSP Tools product line of JTAG emulator operation, see the appropriate Emulator Hardware User's Guide. For detailed information on the interfacing of Analog Devices JTAG emulators with Analog Devices DSP products with JTAG emulation ports, please refer to Engineer to Engineer Note *EE-68: Analog Devices JTAG Emulation Technical Reference*. Both of these documents can be found on the Analog Devices website.

DMA Controller

The ADSP-21161N's on-chip DMA controller enables zero-overhead data transfers without processor intervention. The DMA controller operates independently and invisibly to the processor core, allowing DMA operations to occur while the core is simultaneously executing its program instructions. DMA transfers can occur between the ADSP-21161N's internal memory and external memory, external peripherals, or a host processor. DMA transfers can also occur between the ADSP-21161N's internal memory and its serial ports, link ports, or the SPI-compatible (Serial Peripheral Interface) port. External bus packing and unpacking of 32-, 48-, or 64-bit words in internal memory is performed during DMA transfers from either 8-, 16-, or 32-bit wide external memory. Fourteen channels of DMA are available on the ADSP-21161N—two are shared between the SPI interface and the link ports, eight via the serial ports, and four via the processor's external port (for host processor, other ADSP-21161Ns, memory, or I/O transfers). Programs can be downloaded to the ADSP-21161N using DMA transfers. Asynchronous off-chip peripherals can control two DMA channels using DMA Request/Grant lines ($\overline{\text{DMAR2–1}}$, $\overline{\text{DMAG2–1}}$). Other DMA features include interrupt generation upon completion of DMA transfers, and DMA chaining for automatic linked DMA transfers.

(for example 10k ohm). These pins must be driven low with a strong enough drive strength (10–50 ohms) to overcome the SHARC keeper latches present on these pins. If the drive strength provided is not strong enough, data access failures can occur.

For single processor SHARC systems using this host access feature, address pins ADDR17, ADDR18, ADDR19, and ADDR20 may be tied low (for example through a 10k ohm resistor), driven low by a buffer/driver, or left floating. Any of these options is sufficient.

General-Purpose I/O Ports

The ADSP-21161N also contains 12 programmable, general purpose I/O pins that can function as either input or output. As output, these pins can signal peripheral devices; as input, these pins can provide the test for conditional branching.

Program Booting

The internal memory of the ADSP-21161N can be booted at system power-up from either an 8-bit EPROM, a host processor, the SPI interface, or through one of the link ports. Selection of the boot source is controlled by the Boot Memory Select ($\overline{\text{BMS}}$), EBOOT (EPROM Boot), and Link/Host Boot (LBOOT) pins. 8-, 16-, or 32-bit host processors can also be used for booting.

Phase-Locked Loop and Crystal Double Enable

The ADSP-21161N uses an on-chip phase-locked loop (PLL) to generate the internal clock for the core. The CLK_CFG1–0 pins are used to select ratios of 2:1, 3:1, and 4:1. In addition to the PLL ratios, the $\overline{\text{CLKDBL}}$ pin can be used for more clock ratio options. The (1×/2× CLKIN) rate set by the $\overline{\text{CLKDBL}}$ pin determines the rate of the PLL input clock and the rate at which the external port operates. With the combination of CLK_CFG1–0 and $\overline{\text{CLKDBL}}$, ratios of 2:1, 3:1, 4:1, 6:1, and 8:1 between the core and CLKIN are supported. See also Figure 8 on Page 20.

Power Supplies

The ADSP-21161N has separate power supply connections for the analog (AV_{DD}/AGND), internal (V_{DDINT}), and external (V_{DDEXT}) power supplies. The internal and analog supplies must meet the 1.8 V requirement. The external supply must meet the 3.3 V requirement. All external supply pins must be connected to the same supply.

Note that the analog supply (AV_{DD}) powers the ADSP-21161N's clock generator PLL. To produce a stable clock, provide an external circuit to filter the power input to the AV_{DD} pin. Place the filter as close as possible to the pin. The AV_{DD} filter circuit shown in Figure 6 must be added for each ADSP-21161N in the multiprocessor system. To prevent noise coupling, use a wide trace for the analog ground (AGND) signal and install a decoupling capacitor as close as possible to the pin.

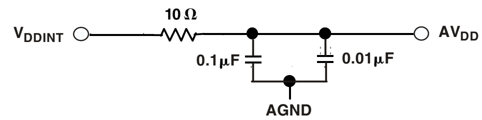


Figure 6. Analog Power (AV_{DD}) Filter Circuit

DEVELOPMENT TOOLS

Analog Devices supports its processors with a complete line of software and hardware development tools, including integrated development environments (which include CrossCore® Embedded Studio and/or VisualDSP++®), evaluation products, emulators, and a wide variety of software add-ins.

Integrated Development Environments (IDEs)

For C/C++ software writing and editing, code generation, and debug support, Analog Devices offers two IDEs.

The newest IDE, CrossCore Embedded Studio, is based on the Eclipse™ framework. Supporting most Analog Devices processor families, it is the IDE of choice for future processors, including multicore devices. CrossCore Embedded Studio seamlessly integrates available software add-ins to support real time operating systems, file systems, TCP/IP stacks, USB stacks, algorithmic software modules, and evaluation hardware board support packages. For more information visit www.analog.com/cces.

The other Analog Devices IDE, VisualDSP++, supports processor families introduced prior to the release of CrossCore Embedded Studio. This IDE includes the Analog Devices VDK real time operating system and an open source TCP/IP stack. For more information visit www.analog.com/visualdsp. Note that VisualDSP++ will not support future Analog Devices processors.

EZ-KIT Lite Evaluation Board

For processor evaluation, Analog Devices provides wide range of EZ-KIT Lite® evaluation boards. Including the processor and key peripherals, the evaluation board also supports on-chip emulation capabilities and other evaluation and development features. Also available are various EZ-Extenders®, which are daughter cards delivering additional specialized functionality, including audio and video processing. For more information visit www.analog.com and search on "ezkit" or "ezextender".

EZ-KIT Lite Evaluation Kits

For a cost-effective way to learn more about developing with Analog Devices processors, Analog Devices offer a range of EZ-KIT Lite evaluation kits. Each evaluation kit includes an EZ-KIT Lite evaluation board, directions for downloading an evaluation version of the available IDE(s), a USB cable, and a power supply. The USB controller on the EZ-KIT Lite board connects to the USB port of the user's PC, enabling the chosen IDE evaluation suite to emulate the on-board processor in-circuit. This permits the customer to download, execute, and debug programs for the EZ-KIT Lite system. It also supports in-circuit programming of the on-board Flash device to store user-specific boot code, enabling standalone operation. With the full version of Cross-

PIN FUNCTION DESCRIPTIONS

ADSP-21161N pin definitions are listed below. Inputs identified as synchronous (S) must meet timing requirements with respect to CLKIN (or with respect to TCK for TMS, TDI). Inputs identified as asynchronous (A) can be asserted asynchronously to CLKIN (or to TCK for $\overline{\text{TRST}}$). Tie or pull unused inputs to V_{DDEXT} or GND, except for the following:

- ADDR23–0, DATA47–0, BRST, CLKOUT (Note: These pins have a logic-level hold circuit enabled on the ADSP-21161N DSP with ID2–0 = 00x.)
- $\overline{\text{PA}}$, ACK, $\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{DMARx}}$, $\overline{\text{DMAGx}}$, (ID2–0 = 00x) (Note: These pins have a pull-up enabled on the ADSP-21161N DSP with ID2–0 = 00x.)
- LxCLK, LxACK, LxDAT7–0 (LxPDRDE = 0) (Note: See Link Port Buffer Control Register Bit definitions in the ADSP-21161N *SHARC DSP Hardware Reference.*)
- DxA, DxB, SCLKx, SPICLK, MISO, MOSI, $\overline{\text{EMU}}$, TMS,$\overline{\text{TRST}}$, TDI (Note: These pins have a pull-up.)

The following symbols appear in the Type column of Table 2: A = Asynchronous, G = Ground, I = Input, O = Output, P = Power Supply, S = Synchronous, (A/D) = Active Drive, (O/D) = Open Drain, and T = Three-State (when $\overline{\text{SBTS}}$ is asserted or when the ADSP-21161N is a bus slave).

Unlike previous SHARC processors, the ADSP-21161N contains internal series resistance equivalent to 50 Ω on all input/output drivers except the CLKIN and XTAL pins. Therefore, for traces longer than six inches, external series resistors on control, data, clock, or frame sync pins are not required to dampen reflections from transmission line effects for point-to-point connections. However, for more complex networks such as a star configuration, series termination is still recommended.

Table 2. Pin Function Descriptions

Pin	Type	Function
ADDR23–0	I/O/T	**External Bus Address.** The ADSP-21161N outputs addresses for external memory and peripherals on these pins. In a multiprocessor system the bus master outputs addresses for read/writes of the IOP registers of other ADSP-21161Ns while all other internal memory resources can be accessed indirectly via DMA control (that is, accessing IOP DMA parameter registers). The ADSP-21161N inputs addresses when a host processor or multiprocessing bus master is reading or writing its IOP registers. A keeper latch on the DSP's ADDR23-0 pins maintains the input at the level it was last driven. This latch is only enabled on the ADSP-21161N with ID2–0=00x.
DATA47–16	I/O/T	**External Bus Data.** The ADSP-21161N inputs and outputs data and instructions on these pins. Pull-up resistors on unused data pins are not necessary. A keeper latch on the DSP's DATA47–16 pins maintains the input at the level it was last driven. This latch is only enabled on the ADSP-21161N with ID2–0=00x. **Note:** *DATA15–8 pins (multiplexed with L1DAT7–0) can also be used to extend the data bus if the link ports are disabled and will not be used. In addition, DATA7–0 pins (multiplexed with L0DAT7–0) can also be used to extend the data bus if the link ports are not used. This enables execution of 48-bit instructions from external SBSRAM (system clock speed-external port), SRAM (system clock speed-external port) and SDRAM (core clock or one-half the core clock speed). The IPACKx Instruction Packing Mode Bits in SYSCON should be set correctly (IPACK1–0=0x1) to enable this full instruction Width/No-packing Mode of operation.*
$\overline{\text{MS3–0}}$	I/O/T	**Memory Select Lines.** These outputs are asserted (low) as chip selects for the corresponding banks of external memory. Memory bank sizes are fixed to 16 M words for non-SDRAM and 64M words for SDRAM. The $\overline{\text{MS3–0}}$ outputs are decoded memory address lines. In asynchronous access mode, the $\overline{\text{MS3–0}}$ outputs transition with the other address outputs. In synchronous access modes, the $\overline{\text{MS3–0}}$ outputs assert with the other address lines; however, they deassert after the first CLKIN cycle in which ACK is sampled asserted. In a multiprocessor system, the $\overline{\text{MSx}}$ signals are tracked by slave SHARCs.
$\overline{\text{RD}}$	I/O/T	**Memory Read Strobe.** $\overline{\text{RD}}$ is asserted whenever ADSP-21161N reads a word from external memory or from the IOP registers of other ADSP-21161Ns. External devices, including other ADSP-21161Ns, must assert $\overline{\text{RD}}$ for reading from a word of the ADSP-21161N IOP register memory. In a multiprocessing system, $\overline{\text{RD}}$ is driven by the bus master. $\overline{\text{RD}}$ has a 20 kΩ internal pull-up resistor that is enabled for DSPs with ID2–0=00x.
$\overline{\text{WR}}$	I/O/T	**Memory Write Low Strobe.** $\overline{\text{WR}}$ is asserted when ADSP-21161N writes a word to external memory or IOP registers of other ADSP-21161Ns. External devices must assert $\overline{\text{WR}}$ for writing to ADSP-21161N IOP registers. In a multiprocessing system, the bus master drives WR. $\overline{\text{WR}}$ has a 20 kΩ internal pull-up resistor that is enabled for DSPs with ID2–0=00x.

Table 2. Pin Function Descriptions (Continued)

Pin	Type	Function
BRST	I/O/T	**Sequential Burst Access.** BRST is asserted by ADSP-21161N to indicate that data associated with consecutive addresses is being read or written. A slave device samples the initial address and increments an internal address counter after each transfer. The incremented address is not pipelined on the bus. A master ADSP-21161N in a multiprocessor environment can read slave external port buffers (EPBx) using the burst protocol. BRST is asserted after the initial access of a burst transfer. It is asserted for every cycle after that, except for the last data request cycle (denoted by $\overline{\text{RD}}$ or $\overline{\text{WR}}$ asserted and BRST negated). A keeper latch on the DSP's BRST pin maintains the input at the level it was last driven. This latch is only enabled on the ADSP-21161N with ID2–0=00x.
ACK	I/O/S	**Memory Acknowledge.** External devices can de-assert ACK (low) to add wait states to an external memory access. ACK is used by I/O devices, memory controllers, or other peripherals to hold off completion of an external memory access. The ADSP-21161N deasserts ACK as an output to add wait states to a synchronous access of its IOP registers. ACK has a 20 kΩ internal pull-up resistor that is enabled during reset or on DSPs with ID2–0=00x.
$\overline{\text{SBTS}}$	I/S	**Suspend Bus and Three-State.** External devices can assert $\overline{\text{SBTS}}$ (low) to place the external bus address, data, selects, and strobes in a high impedance state for the following cycle. If the ADSP-21161N attempts to access external memory while $\overline{\text{SBTS}}$ is asserted, the processor will halt and the memory access will not be completed until $\overline{\text{SBTS}}$ is deasserted. $\overline{\text{SBTS}}$ should only be used to recover from host processor/ADSP-21161N deadlock.
$\overline{\text{CAS}}$	I/O/T	**SDRAM Column Access Strobe.** In conjunction with $\overline{\text{RAS}}$, $\overline{\text{MSx}}$, $\overline{\text{SDWE}}$, SDCLKx, and sometimes SDA10, defines the operation for the SDRAM to perform.
$\overline{\text{RAS}}$	I/O/T	**SDRAM Row Access Strobe.** In conjunction with $\overline{\text{CAS}}$, $\overline{\text{MSx}}$, $\overline{\text{SDWE}}$, SDCLKx, and sometimes SDA10, defines the operation for the SDRAM to perform.
$\overline{\text{SDWE}}$	I/O/T	**SDRAM Write Enable.** In conjunction with $\overline{\text{CAS}}$, $\overline{\text{RAS}}$, $\overline{\text{MSx}}$, SDCLKx, and sometimes SDA10, defines the operation for the SDRAM to perform.
DQM	O/T	**SDRAM Data Mask.** In write mode, DQM has a latency of zero and is used during a precharge command and during SDRAM power-up initialization.
SDCLK0	I/O/S/T	**SDRAM Clock Output 0.** Clock for SDRAM devices.
SDCLK1	O/S/T	**SDRAM Clock Output 1.** Additional clock for SDRAM devices. For systems with multiple SDRAM devices, handles the increased clock load requirements, eliminating need of off-chip clock buffers. Either SDCLK1 or both SDCLKx pins can be three-stated.
SDCKE	I/O/T	**SDRAM Clock Enable.** Enables and disables the CLK signal. For details, see the data sheet supplied with the SDRAM device.
SDA10	O/T	**SDRAM A10 Pin.** Enables applications to refresh an SDRAM in parallel with a non-SDRAM accesses or host accesses. This pin replaces the DSP's A10 pin only during SDRAM accesses.
$\overline{\text{IRQ2–0}}$	I/A	**Interrupt Request Lines.** These are sampled on the rising edge of CLKIN and may be either edge-triggered or level-sensitive.
FLAG11–0	I/O/A	**Flag Pins.** Each is configured via control bits as either an input or output. As an input, it can be tested as a condition. As an output, it can be used to signal external peripherals.
TIMEXP	O	**Timer Expired.** Asserted for four core clock cycles when the timer is enabled and TCOUNT decrements to zero.
$\overline{\text{HBR}}$	I/A	**Host Bus Request.** Must be asserted by a host processor to request control of the ADSP-21161N's external bus. When $\overline{\text{HBR}}$ is asserted in a multiprocessing system, the ADSP-21161N that is bus master will relinquish the bus and assert $\overline{\text{HBG}}$. To relinquish the bus, the ADSP-21161N places the address, data, select, and strobe lines in a high impedance state. $\overline{\text{HBR}}$ has priority over all ADSP-21161N bus requests ($\overline{\text{BR6–1}}$) in a multiprocessing system.
$\overline{\text{HBG}}$	I/O	**Host Bus Grant.** Acknowledges an $\overline{\text{HBR}}$ bus request, indicating that the host processor may take control of the external bus. $\overline{\text{HBG}}$ is asserted (held low) by the ADSP-21161N until $\overline{\text{HBR}}$ is released. In a multiprocessing system, $\overline{\text{HBG}}$ is output by the ADSP-21161N bus master and is monitored by all others. After $\overline{\text{HBR}}$ is asserted, and before $\overline{\text{HBG}}$ is given, $\overline{\text{HBG}}$ will float for 1 t_{CK} (1 CLKIN cycle). To avoid erroneous grants, $\overline{\text{HBG}}$ should be pulled up with a 20 kΩ to 50 kΩ external resistor.
$\overline{\text{CS}}$	I/A	**Chip Select.** Asserted by host processor to select the ADSP-21161N.

SPECIFICATIONS

OPERATING CONDITIONS

Parameter[1]	Description	Test Conditions	100 MHz		110 MHz		Unit
			Min	Max	Min	Max	
V_{DDINT}	Internal (Core) Supply Voltage		1.71	1.89	1.71	1.89	V
AV_{DD}	Analog (PLL) Supply Voltage		1.71	1.89	1.71	1.89	V
V_{DDEXT}	External (I/O) Supply Voltage		3.13	3.47	3.13	3.47	V
V_{IH}	High Level Input Voltage[2]	@ V_{DDEXT} = Max	2.0	V_{DDEXT}+0.5	2.0	V_{DDEXT}+0.5	V
V_{IL}	Low Level Input Voltage[2]	@ V_{DDEXT} = Min	–0.5	+0.8	–0.5	+0.8	V
T_{CASE}	Case Operating Temperature[3]		–40	+105	–40	+125	°C

[1] Specifications subject to change without notice.

[2] Applies to input and bidirectional pins: DATA47–16, ADDR23–0, $\overline{\text{MS3–0}}$, $\overline{\text{RD}}$, $\overline{\text{WR}}$, ACK, $\overline{\text{SBTS}}$, $\overline{\text{IRQ2–0}}$, FLAG11–0, $\overline{\text{HBG}}$, $\overline{\text{HBR}}$, $\overline{\text{CS}}$, $\overline{\text{DMAR1}}$, $\overline{\text{DMAR2}}$, $\overline{\text{BR6–1}}$, ID2–0, RPBA, $\overline{\text{PA}}$, BRST, FSx, DxA, DxB, SCLKx, $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{SDWE}}$, SDCLK0, LxDAT7–0, LxCLK, LxACK, SPICLK, MOSI, MISO, $\overline{\text{SPIDS}}$, EBOOT, LBOOT, $\overline{\text{BMS}}$, SDCKE, CLK_CFGx, $\overline{\text{CLKDBL}}$, CLKIN, $\overline{\text{RESET}}$, TRST, TCK, TMS, TDI.

[3] See Thermal Characteristics on Page 55 for information on thermal specifications.

ELECTRICAL CHARACTERISTICS

Parameter	Description	Test Conditions	Min	Max	Unit
V_{OH}	High Level Output Voltage[1]	@ V_{DDEXT} = Min, I_{OH} = –2.0 mA[2]	2.4		V
V_{OL}	Low Level Output Voltage[1]	@ V_{DDEXT} = Min, I_{OL} = 4.0 mA[2]		0.4	V
I_{IH}	High Level Input Current[3, 4]	@ V_{DDEXT} = Max, V_{IN} = V_{DDEXT} Max		10	μA
I_{IL}	Low Level Input Current[3]	@ V_{DDEXT} = Max, V_{IN} = 0 V		10	μA
I_{IHC}	CLKIN High Level Input Current[5]	@ V_{DDEXT} = Max, V_{IN} = V_{DDEXT} Max		35	μA
I_{ILC}	CLKIN Low Level Input Current[5]	@ V_{DDEXT} = Max, V_{IN} = 0 V		35	μA
I_{IKH}	Keeper High Load Current[6]	@ V_{DDEXT} = Max, V_{IN} = 2.0 V	–250	–100	μA
I_{IKL}	Keeper Low Load Current[6]	@ V_{DDEXT} = Max, V_{IN} = 0.8 V	50	200	μA
I_{IKH-OD}	Keeper High Overdrive Current[6, 7, 8]	@ V_{DDEXT} = Max	–300		μA
I_{IKL-OD}	Keeper Low Overdrive Current[6, 7, 8]	@ V_{DDEXT} = Max	300		μA
I_{ILPU}	Low Level Input Current Pull-Up[4]	@ V_{DDEXT} = Max, V_{IN} = 0 V		350	μA
I_{OZH}	Three-State Leakage Current[9, 10, 11]	@ V_{DDEXT} = Max, V_{IN} = V_{DDEXT} Max		10	μA
I_{OZL}	Three-State Leakage Current[9, 12, 13]	@ V_{DDEXT} = Max, V_{IN} = 0 V		10	μA
I_{OZLPU1}	Three-State Leakage Current Pull-Up1[10]	@ V_{DDEXT} = Max, V_{IN} = 0 V		500	μA
I_{OZLPU2}	Three-State Leakage Current Pull-Up2[11]	@ V_{DDEXT} = Max, V_{IN} = 0 V		350	μA
I_{OZHPD1}	Three-State Leakage Current Pull-Down1[12]	@ V_{DDEXT} = Max, V_{IN} = V_{DDEXT} Max		350	μA
I_{OZHPD2}	Three-State Leakage Current Pull-Down2[13]	@ V_{DDEXT} = Max, V_{IN} = V_{DDEXT} Max		500	μA
$I_{DD-INPEAK}$	Supply Current (Internal)[14, 15]	t_{CCLK} = 9.0 ns, V_{DDINT} = Max		965	mA
		t_{CCLK} = 10.0 ns, V_{DDINT} = Max		900	
$I_{DD-INHIGH}$	Supply Current (Internal)[15, 16]	t_{CCLK} = 9.0 ns, V_{DDINT} = Max		700	mA
		t_{CCLK} = 10.0 ns, V_{DDINT} = Max		650	
$I_{DD-INLOW}$	Supply Current (Internal)[15, 17]	t_{CCLK} = 9.0 ns, V_{DDINT} = Max		535	mA
		t_{CCLK} = 10.0 ns, V_{DDINT} = Max		500	
$I_{DD-IDLE}$	Supply Current (Idle)[15, 18]	t_{CCLK} = 9.0 ns, V_{DDINT} = Max		425	mA
		t_{CCLK} = 10.0 ns, V_{DDINT} = Max		400	
AI_{DD}	Supply Current (Analog)[19]	@ AV_{DD} = Max		10	mA
C_{IN}	Input Capacitance[20, 21]	f_{IN} = 1 MHz, T_{CASE} = 25°C, V_{IN} = 1.8 V		4.7	pF

1 Applies to output and bidirectional pins: DATA47–16, ADDR23–0, $\overline{\text{MS3–0}}$, $\overline{\text{RD}}$, $\overline{\text{WR}}$, ACK, DQM, FLAG11–0, $\overline{\text{HBG}}$, REDY, $\overline{\text{DMAG1}}$, $\overline{\text{DMAG2}}$, $\overline{\text{BR6–1}}$, BMSTR, $\overline{\text{PA}}$, BRST, FSx, DxA, DxB, SCLKx, $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{SDWE}}$, SDA10, LxDAT7–0, LxCLK, LxACK, SPICLK, MOSI, MISO, $\overline{\text{BMS}}$, SDCLKx, SDCKE, $\overline{\text{EMU}}$, XTAL, TDO, CLKOUT, TIMEXP, $\overline{\text{RSTOUT}}$.

2 See Output Drive Currents on Page 54 for typical drive current capabilities.

3 Applies to input pins: DATA47–16, ADDR23–0, $\overline{\text{MS3–0}}$, $\overline{\text{SBTS}}$, $\overline{\text{IRQ2–0}}$, FLAG11–0, $\overline{\text{HBG}}$, $\overline{\text{HBR}}$, $\overline{\text{CS}}$, $\overline{\text{BR6–1}}$, ID2–0, RPBA, BRST, FSx, DxA, DxB, SCLKx, $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{SDWE}}$, SDCLK0, LxDAT7–0, LxCLK, LxACK, SPICLK, MOSI, MISO, $\overline{\text{SPIDS}}$, EBOOT, LBOOT, $\overline{\text{BMS}}$, SDCKE, CLK_CFGx, $\overline{\text{CLKDBL}}$, TCK, $\overline{\text{RESET}}$, CLKIN.

4 Applies to input pins with 20 kΩ internal pull-ups: $\overline{\text{RD}}$, $\overline{\text{WR}}$, ACK, $\overline{\text{DMAR1}}$, $\overline{\text{DMAR2}}$, $\overline{\text{PA}}$, $\overline{\text{TRST}}$, TMS, TDI.

5 Applies to CLKIN only.

6 Applies to all pins with keeper latches: ADDR23–0, DATA47–0, $\overline{\text{MS3–0}}$, BRST, CLKOUT.

7 Current required to switch from kept high to low or from kept low to high.

8 Characterized, but not tested.

9 Applies to three-statable pins: DATA47–16, ADDR23–0, $\overline{\text{MS3–0}}$, CLKOUT, FLAG11–0, REDY, $\overline{\text{HBG}}$, $\overline{\text{BMS}}$, $\overline{\text{BR6–1}}$, $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{SDWE}}$, DQM, SDCLKx, SDCKE, SDA10, BRST.

10 Applies to three-statable pins with 20 kΩ pull-ups: $\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{DMAG1}}$, $\overline{\text{DMAG2}}$, $\overline{\text{PA}}$.

11 Applies to three-statable pins with 50 kΩ internal pull-ups: DxA, DxB, SCLKx, SPICLK., $\overline{\text{EMU}}$, MISO, MOSI.

12 Applies to three-statable pins with 50 kΩ internal pull-downs: LxDAT7–0 (below Revision1.2), LxCLK, LxACK. Use I_{OZHPD2} for Rev. 1.2 and higher.

13 Applies to three-statable pins with 20 kΩ internal pull-downs: LxDAT7-0 (Revision 1.2 and higher).

14 The test program used to measure $I_{DDINPEAK}$ represents worst-case processor operation and is not sustainable under normal application conditions. Actual internal power measurements made using typical applications are less than specified. For more information, see Power Dissipation on Page 20.

15 Current numbers are for V_{DDINT} and AVDD supplies combined.

16 $I_{DDINHIGH}$ is a composite average based on a range of high activity code. For more information, see Power Dissipation on Page 20.

17 $I_{DDINLOW}$ is a composite average based on a range of low activity code. For more information, see Power Dissipation on Page 20.

18 Idle denotes ADSP-21161N state during execution of IDLE instruction. For more information, see Power Dissipation on Page 20.

19 Characterized, but not tested.

20 Applies to all signal pins.

21 Guaranteed, but not tested.

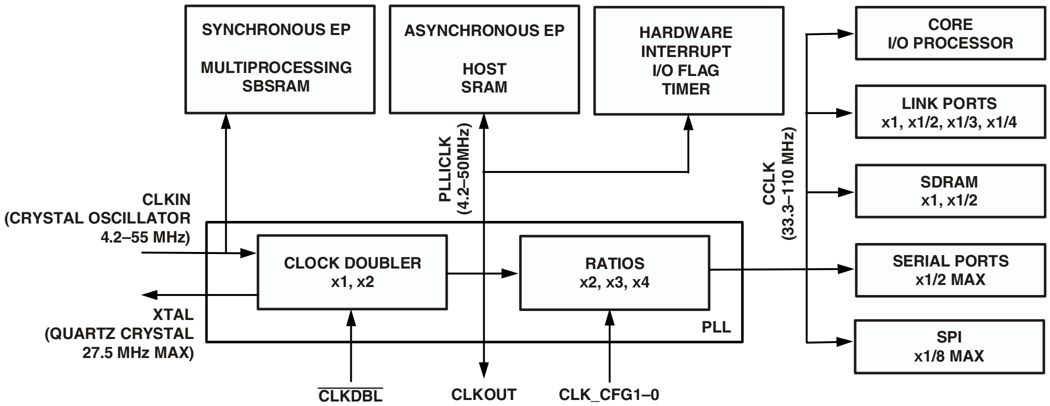


Figure 8. Core Clock and System Clock Relationship to CLKIN

Table 7. CLKOUT and CCLK Clock Generation Operation

Timing Requirements	Description[1]	Calculation
CLKIN	Input Clock	$1/t_{CK}$
CLKOUT	External Port System Clock	$1/t_{CKOP}$
PLLICLK	PLL Input Clock	$1/t_{PLLIN}$
CCLK	Core Clock	$1/t_{CCLK}$
t_{CK}	CLKIN Clock Period	1/CLKIN
t_{CCLK}	(Processor) Core Clock Period	1/CCLK
t_{LCLK}	Link Port Clock Period	$(t_{CCLK}) \times$ LR
t_{SCLK}	Serial Port Clock Period	$(t_{CCLK}) \times$ SR
t_{SDK}	SDRAM Clock Period	$(t_{CCLK}) \times$ SDCKR
t_{SPICLK}	SPI Clock Period	$(t_{CCLK}) \times$ SPIR

[1] where:
LR = link port-to-core clock ratio (1, 2, 3, or 1:4, determined by LxCLKD)
SR = serial port-to-core clock ratio (wide range, determined by CLKDIV)
SDCKR = SDRAM-to-Core Clock Ratio (1:1 or 1:2, determined by SDCTL register)
SPIR = SPI-to-Core Clock Ratio (wide range, determined by SPICTL register)
LCLK = Link Port Clock
SCLK = Serial Port Clock
SDK = SDRAM Clock
SPICLK = SPI Clock

POWER DISSIPATION

Total power dissipation has two components: one due to internal circuitry and one due to the switching of external output drivers.

Internal power dissipation depends on the instruction execution sequence and the data operands involved. Using the current specifications ($I_{DDINPEAK}$, $I_{DDINHIGH}$, $I_{DDINLOW}$, I_{DDIDLE}) from the Electrical Characteristics on Page 18 and the current-versus-operation information in Table 8, the programmer can estimate the ADSP-21161N's internal power supply (V_{DDINT}) input current for a specific application, according to the following formula:

$$
\begin{aligned}
& \%\,\text{Peak} \times I_{DD\text{-}INPEAK} \\
& \%\,\text{High} \times I_{DD\text{-}INHIGH} \\
& \%\,\text{Low} \times I_{DD\text{-}INLOW} \\
+\ & \%\,\text{Peak} \times I_{DD\text{-}IDLE} \\
& = I_{DDINT}
\end{aligned}
$$

Table 8. Operation Types Versus Input Current

Operation	Peak Activity[1] ($I_{DDINPEAK}$)	High Activity[1] ($I_{DDINHIGH}$)	Low Activity[1] ($I_{DDINLOW}$)
Instruction Type	Multifunction	Multifunction	Single Function
Instruction Fetch	Cache	Internal Memory	Internal Memory
Core Memory Access[2]	2 per t_{CK} cycle (DM×64 and PM×64)	1 per t_{CK} cycle (DM×64)	None
Internal Memory DMA	1 per 2 t_{CCLK} cycles	1 per 2 t_{CCLK} cycles	N/A
External Memory DMA	1 per external port cycle (×32)	1 per external port cycle (×32)	N/A
Data bit pattern for core memory access and DMA	Worst case	Random	N/A

[1] The state of the PEYEN bit (SIMD versus SISD mode) does not influence these calculations.
[2] These assume a 2:1 core clock ratio. For more information on ratios and clocks (t_{CK} and t_{CCLK}), see the timing ratio definitions on Page 19.

The external component of total power dissipation is caused by the switching of output pins. Its magnitude depends on:

- The number of output pins that switch during each cycle (O)
- The maximum frequency at which they can switch (f)
- Their load capacitance (C)
- Their voltage swing (V_{DD})

and is calculated by:

$$P_{EXT} = O \times C \times V_{DD}^{2} \times f$$

The load capacitance should include the processor package capacitance (C_{IN}). The switching frequency includes driving the load high and then back low. At a maximum rate of $1/t_{CK}$, address and data pins can drive high and low, while writing to a SDRAM memory.

Example: Estimate P_{EXT} with the following assumptions:

- A system with one bank of external memory (32 bit)
- Two 1M × 16 SDRAM chips are used, each with a load of 10 pF (ignoring trace capacitance)
- External Data Memory writes can occur every cycle at a rate of $1/t_{CK}$ with 50% of the pins switching
- The bus cycle time is 55 MHz
- The external SDRAM clock rate is 110 MHz
- Ignoring SDRAM refresh cycles
- Addresses are incremental and on the same page

The P_{EXT} equation is calculated for each class of pins that can drive, as shown in Table 9.

A typical power consumption can now be calculated for these conditions by adding a typical internal power dissipation:

$$P_{TOTAL} = P_{EXT} + P_{INT} + P_{PLL}$$

Where:

P_{EXT} is from Table 9.

P_{INT} is I_{DDINT} × 1.8 V, using the calculation I_{DDINT} listed in Power Dissipation on Page 20.

P_{PLL} is AI_{DD} × 1.8 V, using the value for AI_{DD} listed in the Electrical Characteristics on Page 18.

Note that the conditions causing a worst-case P_{EXT} are different from those causing a worst-case P_{INT}. Maximum P_{INT} cannot occur while 100% of the output pins are switching from all ones to all zeros. Note also that it is not common for an application to have 100% or even 50% of the outputs switching simultaneously.

Table 9. External Power Calculations—110 MHz Instruction Rate

Pin Type	Number of Pins	% Switching	× C	× f	× V_{DD}^2	= P_{EXT}
Address	11	20	24.7 pF	55 MHz	10.9 V	= 0.033 W
$\overline{\text{MSx}}$	4	0	24.7 pF	N/A	10.9 V	= 0.000 W
$\overline{\text{SDWE}}$	1	0	24.7 pF	N/A	10.9 V	= 0.000 W
Data	32	50	14.7 pF	55 MHz	10.9 V	= 0.141 W
SDCLK0	1	100	24.7 pF	110 MHz	10.9 V	= 0.030 W

P_{EXT} = 0.204 W

Power-Up Sequencing — Silicon Revision 1.2 and Greater

The timing requirements for DSP startup are given in Table 10.

During the power-up sequence of the DSP, differences in the ramp-up rates and activation time between the two supplies can cause current to flow in the I/O ESD protection circuitry. To prevent damage to the ESD diode protection circuitry, Analog Devices recommends including a bootstrap Schottky diode.

The bootstrap Schottky diode is connected between the 1.8 V and 3.3 V power supplies as shown in Figure 9. It protects the ADSP-21161N from partially powering the 3.3 V supply. Including a Schottky diode will shorten the delay between the supply ramps and thus prevent damage to the ESD diode protection circuitry. With this technique, if the 1.8 V rail rises ahead of the 3.3 V rail, the Schottky diode pulls the 3.3 V rail along with the 1.8 V rail.

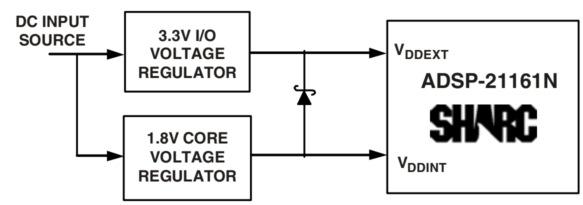


Figure 9. Dual Voltage Schottky Diode

Table 10. Power-Up Sequencing Silicon Revision 1.2 and Greater (DSP Startup)

Parameter		Min	Max	Unit
Timing Requirements				
t_{RSTVDD}	$\overline{RESET}$ Low Before V_{DDINT}/V_{DDEXT} on	0		ns
$t_{IVDDEVDD}$	V_{DDINT} on Before V_{DDEXT}	–50	+200	ms
t_{CLKVDD}	CLKIN Valid After V_{DDINT}/V_{DDEXT} Valid[1]	0	200	ms
t_{CLKRST}	CLKIN Valid Before $\overline{RESET}$ Deasserted[2]	10		µs
t_{PLLRST}	PLL Control Setup Before $\overline{RESET}$ Deasserted[3]	20		µs
t_{WRST}	Subsequent $\overline{RESET}$ Low Pulsewidth[4]	$4t_{CK}$		ns
Switching Requirements				
$t_{CORERST}$	DSP core reset deasserted after $\overline{RESET}$ deasserted	$4080t_{CK}$[3, 5]		

[1] Valid V_{DDINT}/V_{DDEXT} assumes that the supplies are fully ramped to their 1.8 and 3.3 volt rails. Voltage ramp rates can vary from microseconds to hundreds of milliseconds depending on the design of the power supply subsystem.

[2] Assumes a stable CLKIN signal, after meeting worst-case start-up timing of crystal oscillators. Refer to the crystal oscillator manufacturer's data sheet for start-up time. Assume a 25 ms maximum oscillator start-up time if using the XTAL pin and internal oscillator circuit in conjunction with an external crystal.

[3] Based on CLKIN cycles.

[4] Applies after the power-up sequence is complete. Subsequent resets require a minimum of 4 CLKIN cycles for $\overline{RESET}$ to be held low in order to properly initialize and propagate default states at all I/O pins.

[5] The 4080 cycle count depends on t_{SRST} specification in Table 12. If setup time is not met, one additional CLKIN cycle may be added to the core reset time, resulting in 4081 cycles maximum.

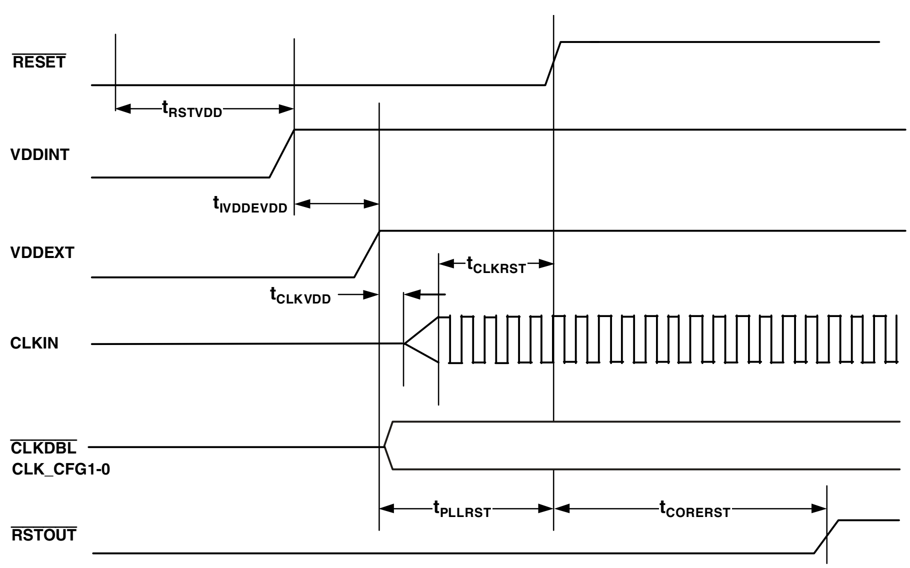


Figure 10. Power-Up Sequencing for Silicon Revision 1.2 and Greater (DSP Startup)

Clock Input

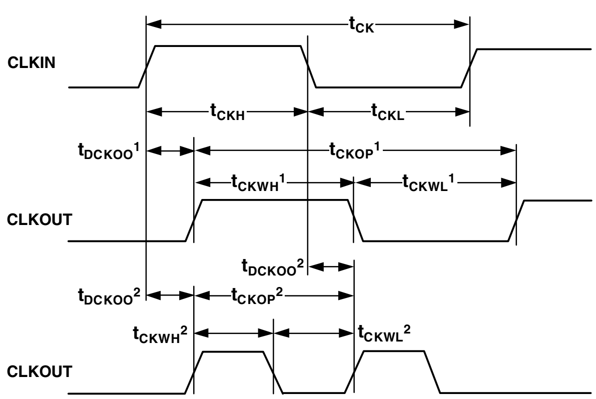
In systems that use multiprocessing or SBSRAM, $\overline{\text{CLKDBL}}$ cannot be enabled nor can the systems use an external crystal as the CLKIN source.

Do not use CLKOUT as the clock source for the SBSRAM device. Using an external crystal in conjunction with $\overline{\text{CLKDBL}}$ to generate a CLKOUT frequency is not supported. Negative hold times can result from the potential skew between CLKIN and CLKOUT.

Table 11. Clock Input

Parameter		100 MHz Min	100 MHz Max	110 MHz Min	110 MHz Max	Unit
Timing Requirements						
t_{CK}	CLKIN Period[1]	20	238	18	238	ns
t_{CKL}	CLKIN Width Low[1]	7.5	119	7	119	ns
t_{CKH}	CLKIN Width High[1]	7.5	119	7	119	ns
t_{CKRF}	CLKIN Rise/Fall (0.4 V–2.0 V)		3		3	ns
t_{CCLK}	CCLK Period	10	30	9	30	ns
Switching Characteristics						
t_{DCKOO}	CLKOUT Delay After CLKIN	0	2	0	2	ns
t_{CKOP}	CLKOUT Period	$t_{CK}-1$	$t_{CK}+1$	$t_{CK}-1$	$t_{CK}+1$	ns
t_{CKWH}	CLKOUT Width High	$t_{CKOP}/2-2$	$t_{CKOP}/2+2$	$t_{CKOP}/2-2$	$t_{CKOP}/2+2$	ns
t_{CKWL}	CLKOUT Width Low	$t_{CKOP}/2-2$	$t_{CKOP}/2+2$	$t_{CKOP}/2-2$	$t_{CKOP}/2+2$	ns

[1] CLKIN is dependent on the configuration of the CLKCFGx and $\overline{\text{CLKDBL}}$ pins to achieve desired t_{CCLK}.



NOTES:
1. WHEN CLKDBL IS DISABLED, ANY SPECIFICATION TO CLKIN APPLIES TO THE RISING EDGE, ONLY.
2. WHEN CLKDBL IS ENABLED, ANY SPECIFICATION TO CLKIN APPLIES TO THE RISING OR FALLING EDGE.

Figure 11. Clock Input

Flags

Table 15. Flags

Parameter		100 MHz Min	100 MHz Max	110 MHz Min	110 MHz Max	Unit
Timing Requirement						
t_{SFI}	FLAG11–0$_{IN}$ Setup Before CLKIN[1]	4		4		ns
t_{HFI}	FLAG11–0$_{IN}$ Hold After CLKIN[1]	1		1		ns
t_{DWRFI}	FLAG11–0$_{IN}$ Delay After $\overline{RD}$/$\overline{WR}$ Low[1]		12		9	ns
t_{HFIWR}	FLAG11–0$_{IN}$ Hold After $\overline{RD}$/$\overline{WR}$ Deasserted[1]	0		0		ns
Switching Characteristics						
t_{DFO}	FLAG11–0$_{OUT}$ Delay After CLKIN		9		9	ns
t_{HFO}	FLAG11–0$_{OUT}$ Hold After CLKIN	1		1		ns
t_{DFOE}	CLKIN to FLAG11–0$_{OUT}$ Enable	1		1		ns
t_{DFOD}	CLKIN to FLAG11–0$_{OUT}$ Disable		5		5	ns

[1] Flag inputs meeting these setup and hold times for instruction cycle N will affect conditional instructions in instruction cycle N+2.

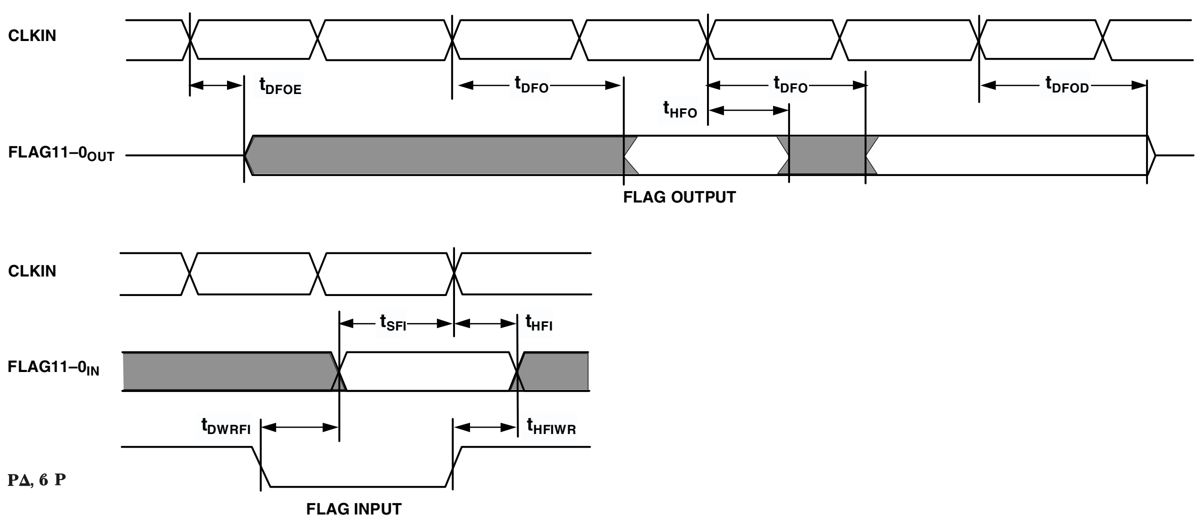


Figure 16. Flags

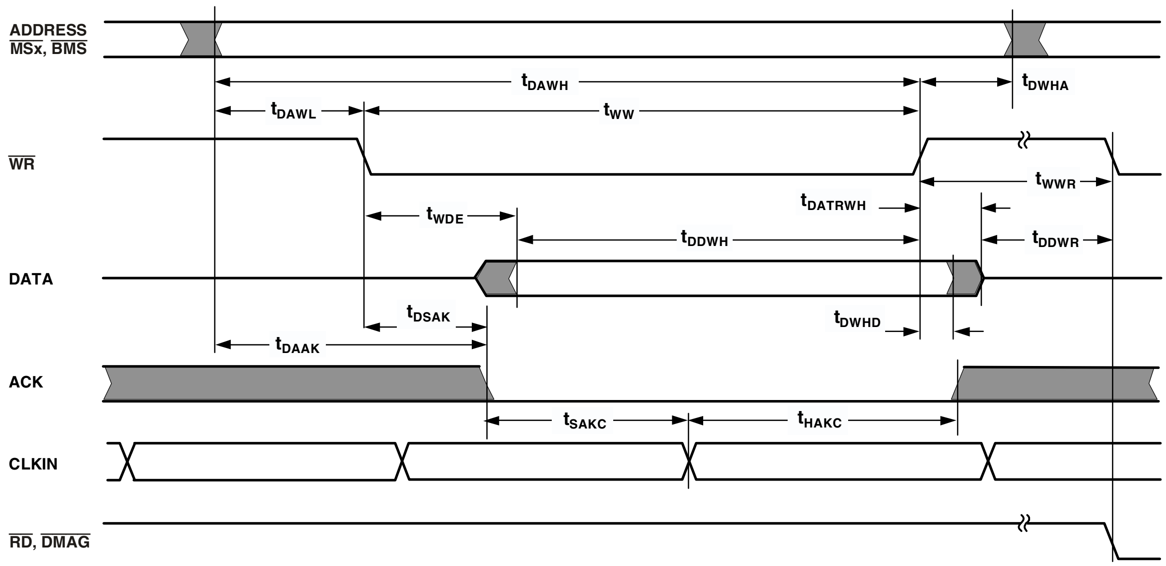


Figure 18. Memory Write — Bus Master

Multiprocessor Bus Request

Use these specifications for passing of bus mastership between multiprocessing ADSP-21161Ns ($\overline{BRx}$).

Table 21. Multiprocessor Bus Request

Parameter		Min	Max	Unit
Timing Requirements				
t_{SBRI}	$\overline{BRx}$ Setup Before CLKIN High	9		ns
t_{HBRI}	$\overline{BRx}$ Hold After CLKIN High	0.5		ns
t_{SPAI}	$\overline{PA}$ Setup Before CLKIN High	9		ns
t_{HPAI}	$\overline{PA}$ Hold After CLKIN High	1		ns
t_{SRPBAI}	RPBA Setup Before CLKIN High	6		ns
t_{HRPBAI}	RPBA Hold After CLKIN High	2		ns
Switching Characteristics				
t_{DBRO}	$\overline{BRx}$ Delay After CLKIN High		8	ns
t_{HBRO}	$\overline{BRx}$ Hold After CLKIN High	1.0		ns
t_{DPASO}	$\overline{PA}$ Delay After CLKIN High, Slave		8	ns
t_{TRPAS}	$\overline{PA}$ Disable After CLKIN High, Slave	1.5		ns
t_{DPAMO}	$\overline{PA}$ Delay After CLKIN High, Master		$0.25t_{CCLK}+9$	ns
t_{PATR}	$\overline{PA}$ Disable Before CLKIN High, Master	$0.25t_{CCLK}-5$		ns

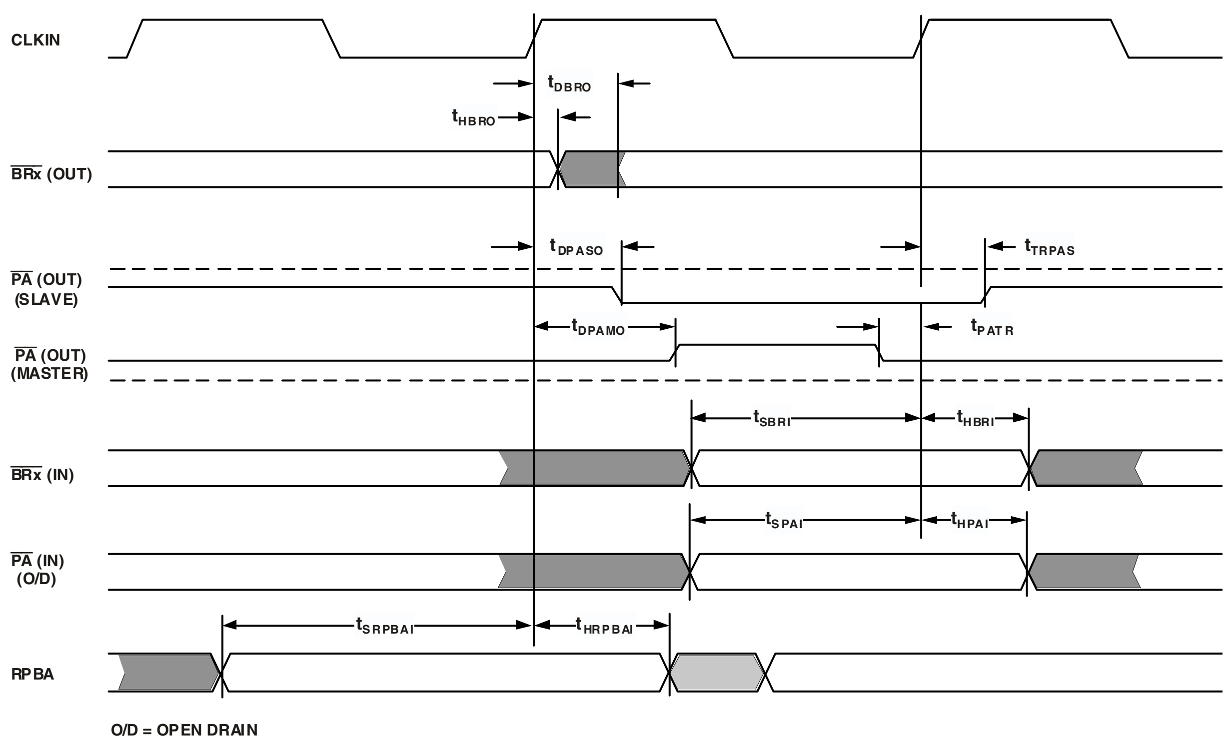


Figure 22. Multiprocessor Bus Request

Three-State Timing — Bus Master, Bus Slave

These specifications show how the memory interface is disabled (stops driving) or enabled (resumes driving) relative to CLKIN and the $\overline{\text{SBTS}}$ pin. This timing is applicable to bus master transition cycles (BTC) and host transition cycles (HTC) as well as the $\overline{\text{SBTS}}$ pin.

During reset, the DSP will not respond to $\overline{\text{SBTS}}$, $\overline{\text{HBR}}$, and MMS accesses. Although the DSP will recognize $\overline{\text{HBR}}$ asserted before reset, a $\overline{\text{HBG}}$ will not be returned by the DSP until after reset is deasserted and the DSP completes bus synchronization.

Table 24. Three-State Timing — Bus Master, Bus Slave

Parameter		Min	Max	Unit
Timing Requirements				
t_{STSCK}	$\overline{\text{SBTS}}$ Setup Before CLKIN	6		ns
t_{HTSCK}	$\overline{\text{SBTS}}$ Hold After CLKIN	2		ns
Switching Characteristics				
t_{MIENA}	Address/Select Enable After CLKIN High	1.5	9	ns
t_{MIENS}	Strobes Enable After CLKIN High[1]	–1.5	+9	ns
t_{MIENHG}	$\overline{\text{HBG}}$ Enable After CLKIN	1.5	9	ns
t_{MITRA}	Address/Select Disable After CLKIN High	$0.5t_{CKOP}–20$	$0.5t_{CKOP}–15$	ns
t_{MITRS}	Strobes Disable After CLKIN High	$t_{CKOP}– 0.25t_{CCLK}–17$	$t_{CKOP}– 0.25t_{CCLK}–12.5$	ns
t_{MITRHG}	$\overline{\text{HBG}}$ Disable After CLKIN[2]	$0.5t_{CKOP}+N \times t_{CCLK}–20$	$0.5t_{CKOP}+N \times t_{CCLK}–15$	ns
t_{DATEN}	Data Enable After CLKIN[3]	1.5	10	ns
t_{DATTR}	Data Disable After CLKIN[3]	1.5	6	ns
t_{ACKEN}	ACK Enable After CLKIN High	1.5	9	ns
t_{ACKTR}	ACK Disable After CLKIN High	0.2	5	ns
t_{CDCEN}	CLKOUT Enable After CLKIN[2]	$0.5t_{CKOP}+N \times t_{CCLK}$	$0.5t_{CKOP}+N \times t_{CCLK}+5$	ns
t_{CDCTR}	CLKOUT Disable After CLKIN	$t_{CKOP}–5$	t_{CKOP}	ns
t_{ATRHBG}	Address/Select Disable Before $\overline{\text{HBG}}$ Low[4]	$1.5t_{CKOP}–6$	$1.5t_{CKOP}+2$	ns
t_{STRHBG}	$\overline{\text{RD}}$/$\overline{\text{WR}}$/$\overline{\text{DMAGx}}$ Disable Before $\overline{\text{HBG}}$ Low[4]	$t_{CKOP}+ 0.25t_{CCLK}–4$	$t_{CKOP}+ 0.25t_{CCLK}+3$	ns
t_{BTRHBG}	$\overline{\text{BMS}}$ Disable Before $\overline{\text{HBG}}$ Low[4]	$0.5t_{CKOP}–4$	$0.5t_{CKOP}+2$	ns
t_{MENHBG}	Memory Interface Enable After $\overline{\text{HBG}}$ High[4]	$t_{CKOP}–5$	$t_{CKOP}+5$	ns

[1] Strobes = $\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{DMAGx}}$.
[2] Where N = 0.5, 1.0, 1.5 for 1:2, 1:3, and 1:4, respectively.
[3] In addition to bus master transition cycles, these specs also apply to bus master and bus slave synchronous read/write.
[4] Memory Interface = Address, $\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{MSx}}$, $\overline{\text{DMAGx}}$, and $\overline{\text{BMS}}$ (in EPROM boot mode). $\overline{\text{BMS}}$ is only an output in EPROM boot mode.

DMA Handshake

These specifications describe the three DMA handshake modes. In all three modes $\overline{DMAR}$ is used to initiate transfers. For handshake mode, $\overline{DMAG}$ controls the latching or enabling of data externally. For external handshake mode, the data transfer is controlled by the ADDR23–0, $\overline{RD}$, $\overline{WR}$, $\overline{MS3-0}$, ACK, and $\overline{DMAG}$ signals. For Paced Master mode, the data transfer is controlled by ADDR23–0, $\overline{RD}$, $\overline{WR}$, $\overline{MS3-0}$, and ACK (not $\overline{DMAG}$). For Paced Master mode, the Memory Read-Bus Master, Memory Write-Bus Master, and Synchronous Read/Write-Bus Master timing specifications for ADDR23–0, $\overline{RD}$, $\overline{WR}$, $\overline{MS3-0}$, DATA47–16, and ACK also apply.

Table 25. DMA Handshake

Parameter		100 MHz Min	100 MHz Max	110 MHz Min	110 MHz Max	Unit
Timing Requirements						
t_{SDRC}	$\overline{DMARx}$ Setup Before CLKIN[1]	3.5		3.5		ns
t_{WDR}	$\overline{DMARx}$ Width Low (Nonsynchronous)[2]	$t_{CCLK}+4.5$		$t_{CCLK}+4.5$		ns
$t_{SDATDGL}$	Data Setup After $\overline{DMAGx}$ Low[3]		$t_{CKOP}-0.5t_{CCLK}-7$		$t_{CKOP}-0.5t_{CCLK}-7$	ns
$t_{HDATIDG}$	Data Hold After $\overline{DMAGx}$ High	2		2		ns
t_{DATDRH}	Data Valid After $\overline{DMARx}$ High[3]		$t_{CKOP}+3$		$t_{CKOP}+3$	ns
t_{DMARLL}	$\overline{DMARx}$ Low Edge to Low Edge[4]	t_{CKOP}		t_{CKOP}		ns
t_{DMARH}	$\overline{DMARx}$ Width High[2]	$t_{CCLK}+4.5$		$t_{CCLK}+4.5$		ns
Switching Characteristics						
t_{DDGL}	$\overline{DMAGx}$ Low Delay After CLKIN	$0.25t_{CCLK}+1$	$0.25t_{CCLK}+9$	$0.25t_{CCLK}+1$	$0.25t_{CCLK}+9$	ns
t_{WDGH}	$\overline{DMAGx}$ High Width	$0.5t_{CCLK}-1+HI$		$0.5t_{CCLK}-1+HI$		ns
t_{WDGL}	$\overline{DMAGx}$ Low Width	$t_{CKOP}-0.5t_{CCLK}-1$		$t_{CKOP}-0.5t_{CCLK}-1$		ns
t_{HDGC}	$\overline{DMAGx}$ High Delay After CLKIN	$t_{CKOP}-0.25t_{CCLK}+1.0$	$t_{CKOP}-0.25t_{CCLK}+9$	$t_{CKOP}-0.25t_{CCLK}+1.0$	$t_{CKOP}-0.25t_{CCLK}+9$	ns
$t_{VDATDGH}$	Data Valid Before $\overline{DMAGx}$ High[5]	$t_{CKOP}-0.25t_{CCLK}-8$	$t_{CKOP}-0.25t_{CCLK}+5$	$t_{CKOP}-0.25t_{CCLK}-8$	$t_{CKOP}-0.25t_{CCLK}+5$	ns
$t_{DATRDGH}$	Data Disable After $\overline{DMAGx}$ High[6]	$0.25t_{CCLK}-3$	$0.25t_{CCLK}+4$	$0.25t_{CCLK}-3$	$0.25t_{CCLK}+4$	ns
t_{DGWRL}	$\overline{WRx}$ Low Before $\overline{DMAGx}$ Low	–1.5	+2	–1.5	+2	ns
t_{DGWRH}	$\overline{DMAGx}$ Low Before $\overline{WRx}$ High	$t_{CKOP}-0.5t_{CCLK}-2+W$		$t_{CKOP}-0.5t_{CCLK}-2+W$		ns
t_{DGWRR}	$\overline{WRx}$ High Before $\overline{DMAGx}$ High[7]	–1.5	+2	–1.5	+2	ns
t_{DGRDL}	$\overline{RDx}$ Low Before $\overline{DMAGx}$ Low	–1.5	+2	–1.5	+2	ns
t_{DRDGH}	$\overline{RDx}$ Low Before $\overline{DMAGx}$ High	$t_{CKOP}-0.5t_{CCLK}-2+W$		$t_{CKOP}-0.5t_{CCLK}-2+W$		ns
t_{DGRDR}	$\overline{RDx}$ High Before $\overline{DMAGx}$ High[7]	–1.5	+2	–1.5	+2	ns
t_{DGWR}	$\overline{DMAGx}$ High to $\overline{WRx}$, $\overline{RDx}$ Low	$0.5t_{CCLK}-2+HI$		$0.5t_{CCLK}-2+HI$		ns
t_{DADGH}	Address/Select Valid to $\overline{DMAGx}$ High	15		13		ns
t_{DDGHA}	Address/Select Hold After $\overline{DMAGx}$ High	1		1		ns

W = (number of wait states specified in WAIT register) × t_{CKOP}.
HI = t_{CKOP} (if data bus idle cycle occurs, as specified in WAIT register; otherwise HI = 0).

[1] Only required for recognition in the current cycle.

[2] Maximum throughput (@ 110 MHz) using $\overline{DMARx}/\overline{DMAGx}$ handshaking equals t_{WDR} + t_{DMARH} = (t_{CCLK}+4.5) + (t_{CCLK}+4.5) = 27 ns (37 MHz). This throughput limit applies to non-synchronous access mode only.

[3] $t_{SDATDGL}$ is the data setup requirement if $\overline{DMARx}$ is not being used to hold off completion of a write. Otherwise, if $\overline{DMARx}$ low holds off completion of the write, the data can be driven t_{DATDRH} after $\overline{DMARx}$ is brought high.

[4] Use t_{DMARLL} if $\overline{DMARx}$ transitions synchronous with CLKIN. Otherwise, use t_{WDR} and t_{DMARH}.

[5] $t_{VDATDGH}$ is valid if $\overline{DMARx}$ is not being used to hold off completion of a read. If $\overline{DMARx}$ is used to prolong the read, then $t_{VDATDGH} = t_{CKOP} - 0.25t_{CCLK} - 8 + (n \times t_{CKOP})$ where n equals the number of extra cycles that the access is prolonged.

[6] See Example System Hold Time Calculation on Page 54 for calculation of hold times given capacitive and dc loads.

[7] This parameter applies for synchronous access mode only.

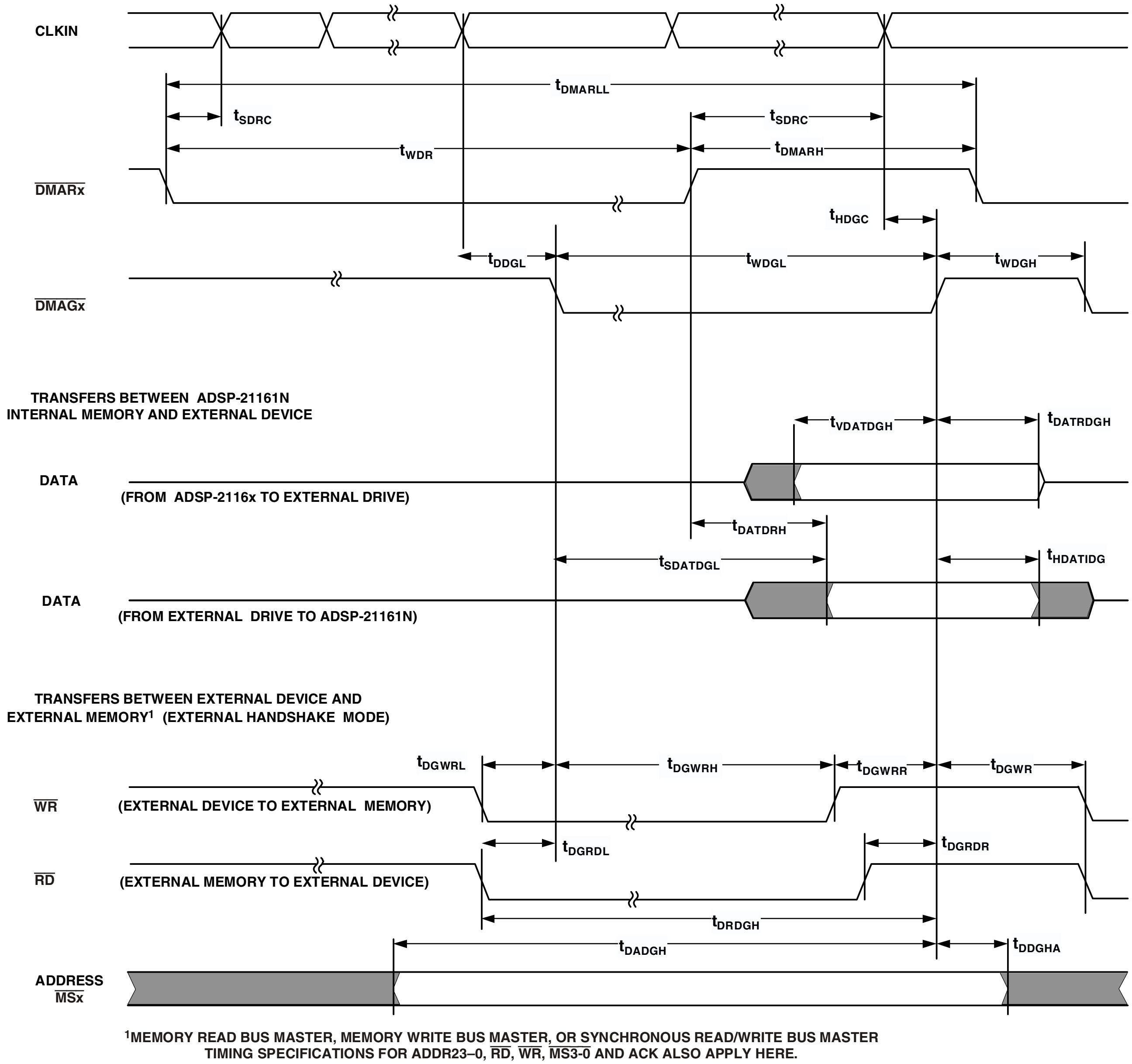


Figure 25. DMA Handshake

Table 29. Link Ports — Transmit

Parameter		Min	Max	Unit
Timing Requirements				
t_{SLACH}	LACK Setup Before LCLK High	8		ns
t_{HLACH}	LACK Hold After LCLK High	−2		ns
Switching Characteristics				
t_{DLDCH}	Data Delay After LCLK High		3	ns
t_{HLDCH}	Data Hold After LCLK High	0		ns
$t_{LCLKTWL}$	LCLK Width Low	$0.5t_{LCLK}-1.0$	$0.5t_{LCLK}+1.0$	ns
$t_{LCLKTWH}$	LCLK Width High	$0.5t_{LCLK}-1.0$	$0.5t_{LCLK}+1.0$	ns
t_{DLACLK}	LCLK Low Delay After LACK High	$0.5t_{LCLK}+3$	$3t_{LCLK}+11$	ns

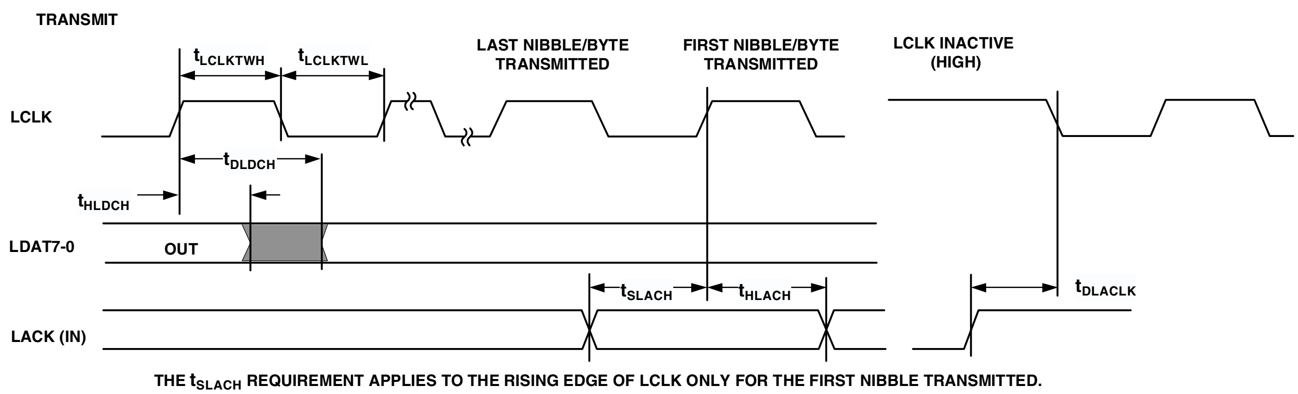


Figure 28. Link Ports—Transmit

Serial Ports

To determine whether communication is possible between two devices at clock speed n, the following specifications must be confirmed: 1) frame sync delay and frame sync setup and hold, 2) data delay and data setup and hold, and 3) SCLK width.

Table 30. Serial Ports — External Clock

Parameter		Min	Max	Unit
Timing Requirements				
t_{SFSE}	Transmit/Receive FS Setup Before Transmit/Receive SCLK[1]	3.5		ns
t_{HFSE}	Transmit/Receive FS Hold After Transmit/Receive SCLK[1]	2		ns
t_{SDRE}	Receive Data Setup Before Receive SCLK[1]	1.5		ns
t_{HDRE}	Receive Data Hold After Receive SCLK[1]	4		ns
t_{SCLKW}	SCLKx Width	7		ns
t_{SCLK}	SCLKx Period	$2t_{CCLK}$		ns

[1] Referenced to sample edge.

Table 31. Serial Ports — Internal Clock

Parameter		Min	Max	Unit
Timing Requirements				
t_{SFSI}	FS Setup Time Before SCLK (Transmit/Receive Mode)[1]	8		ns
t_{HFSI}	FS Hold After SCLK (Transmit/Receive Mode)[1]	$0.5t_{CCLK}+1$		ns
t_{SDRI}	Receive Data Setup Before SCLK[1]	4		ns
t_{HDRI}	Receive Data Hold After SCLK[1]	3		ns

[1] Referenced to sample edge.

Table 32. Serial Ports — External Clock

		100 MHz		110 MHz		
Parameter		Min	Max	Min	Max	Unit
Switching Characteristics						
t_{DFSE}	FS Delay After SCLK (Internally Generated FS) [1,2,3]		13		13	ns
t_{HOFSE}	FS Hold After SCLK (Internally Generated FS)[1,2,3]	3		2.75		ns
t_{DDTE}	Transmit Data Delay After SCLK [1,2]		16		16	ns
t_{HDTE}	Transmit Data Hold After SCLK [1,2]	0		0		ns

[1] Referenced to drive edge.
[2] SCLK/FS Configured as a transmit clock/frame sync with the DDIR bit = 1 in SPCTLx register.
[3] SCLK/FS Configured as a receive clock/frame sync with the DDIR bit = 0 in SPCTLx register.

Table 33. Serial Ports — Internal Clock

Parameter		Min	Max	Unit
Switching Characteristics				
t_{DFSI}	FS Delay After SCLK (Internally Generated FS)[1,2,3]		4.5	ns
t_{HOFSI}	FS Hold After SCLK (Internally Generated FS)[1,2,3]	−1.5		ns
t_{DDTI}	Transmit Data Delay After SCLK[1,2]		7.5	ns
t_{HDTI}	Transmit Data Hold After SCLK[1,2]	0		ns
t_{SCLKIW}	SCLK Width[2]	$0.5t_{SCLK}–2.5$	$0.5t_{SCLK}+2$	ns

[1] Referenced to drive edge.
[2] SCLK/FS Configured as a transmit clock/frame sync with the DDIR bit = 1 in SPCTLx register.
[3] SCLK/FS Configured as a receive clock/frame sync with the DDIR bit = 0 in SPCTLx register.