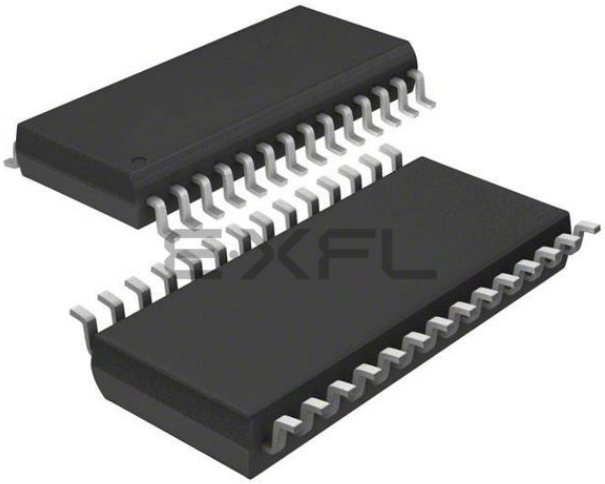


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	M8C
Core Size	8-Bit
Speed	12MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	24
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.25V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SSOP (0.209", 5.30mm Width)
Supplier Device Package	28-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c21512-12pvxet

Contents

PSoC Device Characteristics

Depending on your PSoC device characteristics, the digital and analog systems can have a varying number of digital and analog blocks. Table 1 lists the resources available for specific PSoC device groups. The PSoC device covered by this datasheet is highlighted in Table 1

Table 1. PSoC Device Characteristics

PSoC Part Number	Digital I/O	Digital Rows	Digital Blocks	Analog Inputs	Analog Outputs	Analog Columns	Analog Blocks	SRAM Size	Flash Size
CY8C29x66 [1]	up to 64	4	16	up to 12	4	4	12	2 K	32 K
CY8C28xxx	up to 44	up to 3	up to 12	up to 44	up to 4	up to 6	up to 12 + 4 [2]	1 K	16 K
CY8C27x43	up to 44	2	8	up to 12	4	4	12	256	16 K
CY8C24x94 [1]	up to 56	1	4	up to 48	2	2	6	1 K	16 K
CY8C24x23A [1]	up to 24	1	4	up to 12	2	2	6	256	4 K
CY8C23x33	up to 26	1	4	up to 12	2	2	4	256	8 K
CY8C22x45 [1]	up to 38	2	8	up to 38	0	4	6 [2]	1 K	16 K
CY8C21x45 [1]	up to 24	1	4	up to 24	0	4	6 [2]	512	8 K
CY8C21x34 [1]	up to 28	1	4	28	0	2	4 [2]	512	8 K
CY8C21x23	up to 16	1	4	up to 8	0	2	4 [2]	256	4 K
CY8C21x12 [1]	up to 24	1	1 [2]	24	0	0	1 [2]	512	8 K
CY8C20x34 [1]	up to 28	0	0	up to 28	0	0	3 [2, 3]	512	8 K
CY8C20xx6	up to 36	0	0	up to 36	0	0	3 [2, 3]	up to 2 K	up to 32 K

Getting Started

For in-depth information, along with detailed programming details, see the *PSoC® Technical Reference Manual*.

For up-to-date ordering, packaging, and electrical specification information, see the latest PSoC device datasheets on the web.

Application Notes

Cypress application notes are an excellent introduction to the wide variety of possible PSoC designs.

Development Kits

PSoC Development Kits are available online from and through a growing number of regional and global distributors, which include Arrow, Avnet, Digi-Key, Farnell, Future Electronics, and Newark.

Training

Free PSoC technical training (on demand, webinars, and workshops), which is available online via www.cypress.com, covers a wide variety of topics and skill levels to assist you in your designs.

CYPros Consultants

Certified PSoC consultants offer everything from technical assistance to completed PSoC designs. To contact or become a PSoC consultant go to the CYPros Consultants web site.

Solutions Library

Visit our growing library of solution focused designs. Here you can find various application designs that include firmware and hardware design files that enable you to complete your designs quickly.

Technical Support

Technical support – including a searchable Knowledge Base articles and technical forums – is also available online. If you cannot find an answer to your question, call our Technical Support hotline at 1-800-541-4736.

Notes
1. Automotive qualified devices available in this group.
2. Limited analog functionality.
3. Two analog blocks and one CapSense® block.

Pinouts

The CY8C21x12 PSoC device is available in a variety of packages which are listed and illustrated in the following tables. Every port pin (labeled with a “P”) is capable of digital I/O and connection to the common analog bus. However, V_{SS}, V_{DD}, and XRES are not capable of digital I/O.

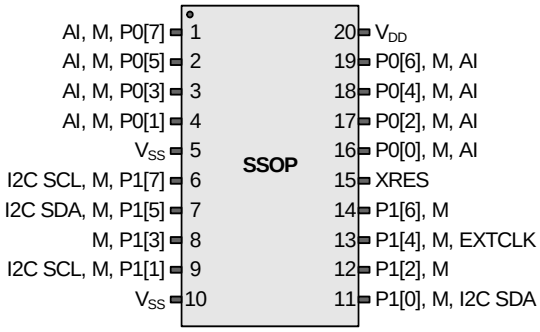
20-pin Part Pinout

Table 2. 20-pin Part Pinout (shrink small-outline package (SSOP))

Pin No.	Type		Name	Description
	Digital	Analog		
1	I/O	I, M	P0[7]	Analog column mux input
2	I/O	I, M	P0[5]	Analog column mux input
3	I/O	I, M	P0[3]	Analog column mux input, C_{MOD} capacitor pin
4	I/O	I, M	P0[1]	Analog column mux input, C_{MOD} capacitor pin
5	Power		V_{SS}	Ground connection
6	I/O	M	P1[7]	I^2C serial clock (SCL)
7	I/O	M	P1[5]	I^2C serial data (SDA)
8	I/O	M	P1[3]	
9	I/O	M	P1[1]	I^2C SCL, ISSP-SCLK[4]
10	Power		V_{SS}	Ground connection
11	I/O	M	P1[0]	I^2C SDA, ISSP-SDATA[4]
12	I/O	M	P1[2]	
13	I/O	M	P1[4]	Optional external clock input (EXTCLK)
14	I/O	M	P1[6]	
15	Input		XRES	Active high external reset with internal pull-down
16	I/O	I, M	P0[0]	Analog column mux input
17	I/O	I, M	P0[2]	Analog column mux input
18	I/O	I, M	P0[4]	Analog column mux input
19	I/O	I, M	P0[6]	Analog column mux input
20	Power		V_{DD}	Supply voltage

LEGEND A = Analog, I = Input, O = Output, and M = Analog Mux Input.

Figure 3. CY8C21312 20-pin PSoC Device



Note
4. These are the ISSP pins, which are not high Z when coming out of POR. See the *PSoC Technical Reference Manual* for details.

Table 4. Register Map 0 Table: User Space

Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access
PRT0DR	00	RW		40			80			C0	
PRT0IE	01	RW		41			81			C1	
PRT0GS	02	RW		42			82			C2	
PRT0DM2	03	RW		43			83			C3	
PRT1DR	04	RW		44		CSREF_CR1	84	RW		C4	
PRT1IE	05	RW		45			85			C5	
PRT1GS	06	RW		46			86			C6	
PRT1DM2	07	RW		47			87			C7	
PRT2DR	08	RW		48			88			C8	
PRT2IE	09	RW		49			89			C9	
PRT2GS	0A	RW		4A			8A			CA	
PRT2DM2	0B	RW		4B			8B			CB	
	0C			4C			8C			CC	
	0D			4D			8D			CD	
	0E			4E			8E			CE	
	0F			4F			8F			CF	
	10			50			90		CUR_PP	D0	RW
	11			51			91		STK_PP	D1	RW
	12			52			92			D2	
	13			53			93		IDX_PP	D3	RW
	14			54			94		MVR_PP	D4	RW
	15			55			95		MVW_PP	D5	RW
	16			56			96		I2C_CFG	D6	RW
	17			57			97		I2C_SCR	D7	#
	18			58			98		I2C_DR	D8	RW
	19			59			99		I2C_MSCR	D9	#
	1A			5A			9A		INT_CLR0	DA	RW
	1B			5B			9B		INT_CLR1	DB	RW
	1C			5C			9C			DC	
	1D			5D			9D		INT_CLR3	DD	RW
	1E			5E			9E		INT_MSK3	DE	RW
	1F			5F			9F			DF	
CSCNT_DR0	20	#		60			A0		INT_MSK0	E0	RW
CSCNT_DR1	21	W	AMUX_CFG	61	RW		A1		INT_MSK1	E1	RW
CSCNT_DR2	22	RW	CSCMP_CR0	62	RW		A2		INT_VC	E2	RC
CSCNT_CR0	23	#		63			A3		RES_WDT	E3	W
CSMOD0_DR0	24	#	CSCMP_CR1	64	#		A4			E4	
CSMOD0_DR1	25	W		65			A5			E5	
CSMOD0_DR2	26	RW	CSCMP_CR2	66	RW		A6		CSCMP_CR5	E6	RW
CSMOD0_CR0	27	#		67			A7		CSCMP_CR6	E7	RW
CSMOD1_DR0	28	#		68			A8			E8	
CSMOD1_DR1	29	W	CSREF_CR0	69	#		A9			E9	
CSMOD1_DR2	2A	RW		6A			AA			EA	
CSMOD1_CR0	2B	#		6B			AB			EB	
LDB0_DR0	2C	#	TMP_DR0	6C	RW		AC			EC	
LDB0_DR1	2D	W	TMP_DR1	6D	RW		AD			ED	
LDB0_DR2	2E	RW	TMP_DR2	6E	RW		AE			EE	
LDB0_CR0	2F	#	TMP_DR3	6F	RW		AF			EF	
	30			70		RDI0RI	B0	RW		F0	
	31			71		RDI0SYN	B1	RW		F1	
	32			72		RDI0IS	B2	RW		F2	
	33			73		RDI0LT0	B3	RW		F3	
	34			74		RDI0LT1	B4	RW		F4	
	35			75		RDI0RO0	B5	RW		F5	
	36		CSCMP_CR3	76	RW	RDI0RO1	B6	RW		F6	
	37		CSCMP_CR4	77	RW		B7		CPU_F	F7	RL
	38			78			B8			F8	
	39			79			B9			F9	
	3A			7A			BA			FA	
	3B			7B			BB			FB	
	3C			7C			BC			FC	
	3D			7D			BD			FD	
	3E			7E			BE		CPU_SCR1	FE	#
	3F			7F			BF		CPU_SCR0	FF	#

Blank fields are Reserved and must not be accessed. # Access is bit specific.

Electrical Specifications

This section presents the DC and AC electrical specifications of the automotive CY8C21x12 PSoC device. For the most up to date electrical specifications, confirm that you have the most recent datasheet by going to the web at http//www.cypress.com.

Specifications are valid for –40 °C ≤ T_A ≤ 125 °C and T_J ≤ 135 °C as specified, except where noted. Refer to Table 14 on page 18 for the electrical specifications for the IMO using slow IMO (SLIMO) mode.

Figure 5. Voltage versus CPU Frequency

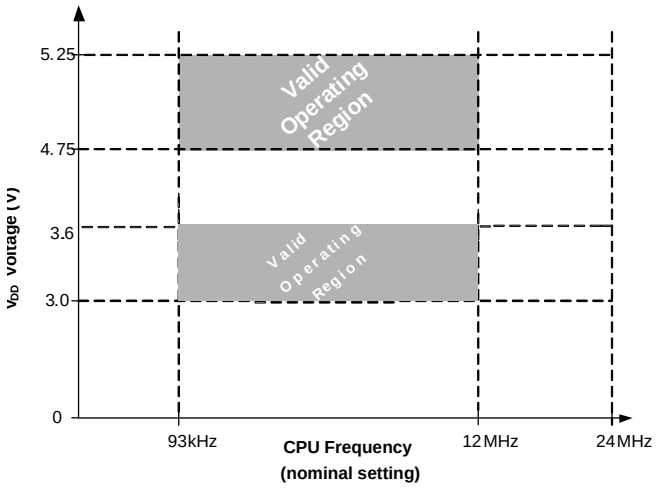
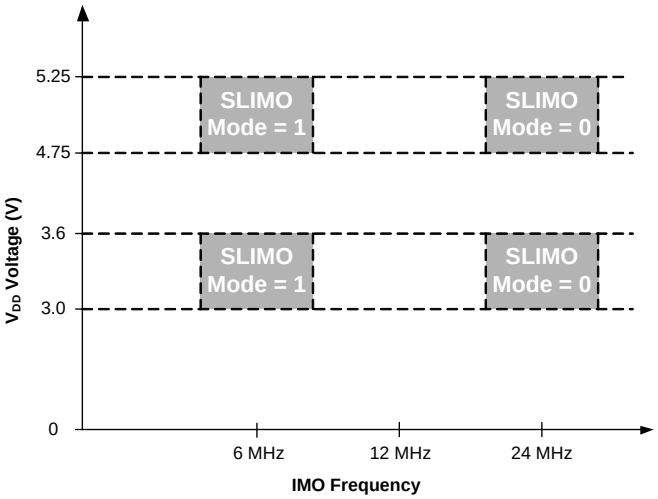


Figure 6. IMO Frequency Trim Options



DC Electrical Characteristics

DC Chip-Level Specifications

Table 8 lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 125 °C or 3.0 V to 3.6 V and –40 °C ≤ TA ≤ 125 °C, respectively. Typical parameters apply to 5 V or 3.3 V at 25 °C and are for design guidance only.

Table 8. DC Chip-Level Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{DD}	Supply voltage	3	–	5.25	V	See Table 12 on page 16.
I_{DD}	Supply current, IMO = 24 MHz	–	4	8	mA	Conditions are V_{DD} = 5.25 V, –40 °C ≤ T_A ≤ 125 °C, CPU = 3 MHz, 48 MHz disabled. VC1 = 1.5 MHz, VC2 = 93.75 kHz, VC3 = 0.366 kHz.
I_{DD3}	Supply current, IMO = 24 MHz	–	4	8	mA	Conditions are V_{DD} = 3.3 V, –40 °C ≤ TA ≤ 125 °C, CPU = 3 MHz, 48 MHz disabled. VC1 = 1.5 MHz, VC2 = 93.75 kHz, VC3 = 0.366 kHz.
I_{SB}	Sleep (mode) current with POR, LVD, sleep timer, WDT, and ILO active. Mid temperature range.	–	5	12	µA	V_{DD} = 5.25 V, –40 °C ≤ T_A ≤ 55 °C.
I_{SBH}	Sleep (mode) current with POR, LVD, sleep timer, WDT, and ILO active. High temperature range.	–	5	100	µA	V_{DD} = 5.25 V, 55 °C ≤ T_A ≤ 125 °C.
V_{REF}	Reference voltage (Bandgap)	1.25	1.30	1.35	V	

DC GPIO Specifications

Table 9 lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 125 °C or 3.0 V to 3.6 V and –40 °C ≤ TA ≤ 125 °C, respectively. Typical parameters apply to 5 V or 3.3 V at 25 °C and are for design guidance only.

Table 9. DC GPIO Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
R_{PU}	Pull-up resistor	4	5.6	8	kΩ	
R_{PD}	Pull-down resistor	4	5.6	8	kΩ	Also applies to the internal pull-down resistor on the XRES pin
V_{OH}	High output level	V_{DD} – 1.0	–	–	V	I_{OH} = 10 mA, V_{DD} = 4.75 to 5.25 V (8 total loads, 4 on even port pins (for example, P0[2], P1[4]), 4 on odd port pins (for example, P0[3], P1[5])).
V_{OL}	Low output level	–	–	0.75	V	I_{OL} = 25 mA, V_{DD} = 4.75 to 5.25 V (8 total loads, 4 on even port pins (for example, P0[2], P1[4]), 4 on odd port pins (for example, P0[3], P1[5])).
I_{OH}	High level source current	10	–	–	mA	V_{OH} ≥ V_{DD} – 1.0 V, see the limitations of the total current in the note for V_{OH}.
I_{OL}	Low level sink current	25	–	–	mA	V_{OL} ≤ 0.75 V, see the limitations of the total current in the note for V_{OL}.
V_{IL}	Input low level	–	–	0.8	V	
V_{IH}	Input high level	2.1	–		V	
V_H	Input hysteresis	–	60	–	mV	
I_{IL}	Input leakage (absolute value)	–	1	–	nA	Gross tested to 1 µA.
C_{IN}	Capacitive load on pins as input	–	3.5	10	pF	Package and pin dependent. T_A = 25 °C.
C_{OUT}	Capacitive load on pins as output	–	3.5	10	pF	Package and pin dependent. T_A = 25 °C.

DC Programming Specifications

Table 13 lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 125 °C or 3.0 V to 3.6 V and –40 °C ≤ TA ≤ 125 °C, respectively. Typical parameters apply to 5 V or 3.3 V at 25 °C and are for design guidance only.

Table 13. DC Programming Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{DDP}	V_{DD} for programming and erase	4.5	5	5.5	V	This specification applies to the functional requirements of external programmer tools
V_{DDLV}	Low V_{DD} for verify	3	3.1	3.2	V	This specification applies to the functional requirements of external programmer tools
V_{DDHV}	High V_{DD} for verify	5.1	5.2	5.3	V	This specification applies to the functional requirements of external programmer tools
$V_{DDIWRITE}$	Supply voltage for flash write operation	3	–	5.25	V	This specification applies to this device when it is executing internal flash writes
I_{DDP}	Supply current during programming or verify	–	5	25	mA	
V_{ILP}	Input low voltage during programming or verify	–	–	0.8	V	
V_{IHP}	Input high voltage during programming or verify	2.2	–	–	V	
I_{ILP}	Input current when applying V_{ILP} to P1[0] or P1[1] during programming or verify	–	–	0.2	mA	Driving internal pull-down resistor.
I_{IHP}	Input current when applying V_{IHP} to P1[0] or P1[1] during programming or verify	–	–	1.5	mA	Driving internal pull-down resistor.
V_{OLV}	Output low voltage during programming or verify	–	–	0.75	V	
V_{OHV}	Output high voltage during programming or verify	V_{DD} – 1	–	V_{DD}	V	
$Flash_{ENPB}$	Flash endurance (per block) [9]	100	–	–	–	Erase/write cycles per block.
$Flash_{ENT}$	Flash endurance (total) [9, 10]	12,800	–	–	–	Erase/write cycles.
$Flash_{DR}$	Flash data retention [11]	15	–	–	Years	

Notes
9. For the full temperature range, the user must employ a temperature sensor user module (FlashTemp) or other temperature sensor, and feed the result to the temperature argument before writing. Refer to the Flash APIs Application Note AN2015 for more information.
10. The maximum total number of allowed erase/write cycles is the minimum $Flash_{ENPB}$ value multiplied by the number of flash blocks in the device.
11. Flash data retention based on the use condition of ≤ 7000 hours at T_A ≤ 125 °C and the remaining time at T_A ≤ 65 °C.

AC Electrical Characteristics

AC Chip-Level Specifications

Table 14 lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 125 °C or 3.0 V to 3.6 V and –40 °C ≤ TA ≤ 125 °C, respectively. Typical parameters apply to 5 V or 3.3 V at 25 °C and are for design guidance only.

Table 14. AC Chip-Level Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{IMO24}	IMO frequency for 24 MHz	22.8 [12]	24	25.2 [12]	MHz	Trimmed using factory trim values. See Figure 6 on page 14. SLIMO mode = 0.
F_{IMO6}	IMO frequency for 6 MHz	5.5 [12]	6	6.5 [12]	MHz	Trimmed using factory trim values. See Figure 6 on page 14. SLIMO mode = 1.
F_{CPU1}	CPU frequency (5 V V_{DD} nominal)	0.09 [12]	12	12.6 [12]	MHz	SLIMO mode = 0.
F_{BLK5}	Digital PSoC block frequency (5 V V_{DD} nominal)	0	24	25.2 [12]	MHz	Refer to Table 17 on page 20.
F_{BLK33}	Digital PSoC block frequency (3.3 V V_{DD} nominal)	0	24	25.2 [12]	MHz	Refer to Table 17 on page 20.
F_{32K1}	ILO frequency	15	32	64	kHz	This specification applies when the ILO has been trimmed.
F_{32KU}	ILO untrimmed frequency	5	–	100	kHz	After a reset and before the M8C processor starts to execute, the ILO is not trimmed.
t_{XRST}	External reset pulse width	10	–	–	µs	
DC24M	24 MHz duty cycle	40	50	60	%	
DC_{ILO}	ILO duty cycle	20	50	80	%	
Step24M	24 MHz trim step size	–	50	–	kHz	
F_{MAX}	Maximum frequency of signal on row input or row output.	–	–	12.6 [12]	MHz	
$SR_{POWERUP}$	Power supply slew rate	–	–	250	V/ms	V_{DD} slew rate during power up.
$t_{POWERUP}$	Time between end of POR state and CPU code execution	–	16	100	ms	Power-up from 0 V.
t_{JIT_IMO} [13]	24 MHz IMO cycle-to-cycle jitter (RMS)	–	200	700	ps	
	24 MHz IMO long term N cycle-to-cycle jitter (RMS)	–	300	900		N = 32
	24 MHz IMO period jitter (RMS)	–	100	400		

Notes
12. Accuracy derived from Internal Main Oscillator with appropriate trim for V_{DD} range.
13. Refer to Cypress Jitter Specifications document, Understanding Datasheet Jitter Specifications for Cypress Timing Products, for more information.

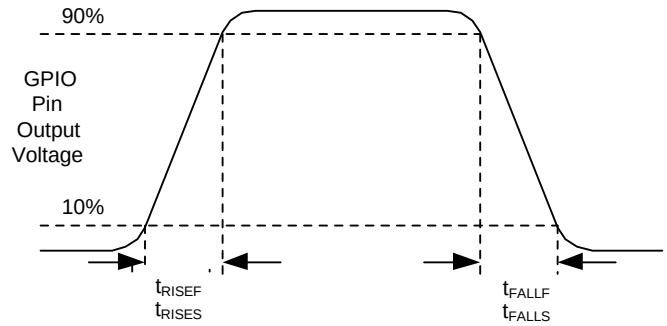
AC GPIO Specifications

Table 15 lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 125 °C or 3.0 V to 3.6 V and –40 °C ≤ TA ≤ 125 °C, respectively. Typical parameters apply to 5 V or 3.3 V at 25 °C and are for design guidance only.

Table 15. AC GPIO Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{GPIO}	GPIO operating frequency	0	–	12.6 [14]	MHz	Normal Strong Mode
$t_{RISEF33}$	Rise time, normal strong mode, Cload = 50 pF	2	–	30	ns	10% to 90%
t_{RISEF5}		2	–	22		
$t_{FALLF33}$	Fall time, normal strong mode, Cload = 50 pF	2	–	30	ns	10% to 90%
t_{FALLF5}		2	–	22		
t_{RISES}	Rise time, slow strong mode, Cload = 50 pF	7	27	–	ns	10% to 90%
t_{FALLS}	Fall time, slow strong mode, Cload = 50 pF	7	22	–	ns	10% to 90%

Figure 7. GPIO Timing Diagram



AC Operational Amplifier Specifications

Table 16 lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 125 °C or 3.0 V to 3.6 V and –40 °C ≤ TA ≤ 125 °C, respectively. Typical parameters apply to 5 V or 3.3 V at 25 °C and are for design guidance only.

Table 16. AC Operational Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
t_{COMP}	Comparator mode response time, 50 mV overdrive	–	–	150	ns	

Note
14. Accuracy derived from Internal Main Oscillator with appropriate trim for V_{DD} range.

AC Digital Block Specifications

Table 17 lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 125 °C or 3.0 V to 3.6 V and –40 °C ≤ TA ≤ 125 °C, respectively. Typical parameters apply to 5 V or 3.3 V at 25 °C and are for design guidance only.

Table 17. AC Digital Block Specifications

Function	Description	Min	Typ	Max	Units	Notes
All functions	Block input clock frequency	–	–	25.2 [15]	MHz	
Timer	Input clock frequency					
	No capture	–	–	25.2 [15]	MHz	
	With capture	–	–	25.2 [15]	MHz	
	Capture pulse width	50 [16]	–	–	ns	
Counter	Input clock frequency					
	No enable input	–	–	25.2 [15]	MHz	
	With enable input	–	–	25.2 [15]	MHz	
	Enable input pulse width	50 [16]	–	–	ns	
Dead Band	Kill pulse width					
	Asynchronous restart mode	20	–	–	ns	
	Synchronous restart mode	50 [16]	–	–	ns	
	Disable mode	50 [16]	–	–	ns	
	Input clock frequency	–	–	25.2 [15]	MHz	
CRCPRS (PRS Mode)	Input clock frequency	–	–	25.2 [15]	MHz	
CRCPRS (CRC Mode)	Input clock frequency	–	–	25.2 [15]	MHz	
SPIM	Input clock frequency	–	–	4.2 [15]	MHz	The SPI serial clock (SCLK) frequency is equal to the input clock frequency divided by 2.
SPIS	Input clock (SCLK) frequency	–	–	2.1 [15]	MHz	The input clock is the SPI SCLK in SPIS mode.
	Width of SS_ negated between transmissions	50 [16]	–	–	ns	
Transmitter	Input clock frequency	–	–	8.4 [15]	MHz	The baud rate is equal to the input clock frequency divided by 8.
Receiver	Input clock frequency	–	–	25.2 [15]	MHz	The baud rate is equal to the input clock frequency divided by 8.

Notes
15. Accuracy derived from IMO with appropriate trim for V_{DD} range.
16. 50 ns minimum input pulse width is based on the input synchronizers running at 24 MHz (42 ns nominal period).

AC External Clock Specifications

Table 18 lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 125 °C or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 125 °C, respectively. Typical parameters apply to 5 V or 3.3 V at 25 °C and are for design guidance only.

Table 18. AC External Clock Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{OSCEXT}	Frequency	0.093	–	24.24	MHz	
–	High period	20.6	–	5300	ns	
–	Low period	20.6	–	–	ns	
–	Power-up IMO to switch	150	–	–	µs	

AC Programming Specifications

Table 19 lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 125 °C or 3.0 V to 3.6 V and –40 °C ≤ TA ≤ 125 °C, respectively. Typical parameters apply to 5 V or 3.3 V at 25 °C and are for design guidance only.

Table 19. AC Programming Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
t_{RSCLK}	Rise time of SCLK	1	–	20	ns	
t_{FSCLK}	Fall time of SCLK	1	–	20	ns	
t_{SSCLK}	Data setup time to falling edge of SCLK	40	–	–	ns	
t_{HSCLK}	Data hold time from falling edge of SCLK	40	–	–	ns	
F_{SCLK}	Frequency of SCLK	0	–	8	MHz	
t_{ERASEB}	Flash erase time (block)	–	10	40 [17]	ms	
t_{WRITE}	Flash block write time	–	40	160 [17]	ms	
t_{DSCLK}	Data Out delay from falling edge of SCLK	–	–	50	ns	
t_{PRGH}	Total flash block program time (t_{ERASEB} + t_{WRITE}), hot	–	–	100 [17]	ms	$T_J \geq 0$ °C
t_{PRGC}	Total flash block program time (t_{ERASEB} + t_{WRITE}), cold	–	–	200 [17]	ms	$T_J < 0$ °C

Note
17. For the full temperature range, the user must employ a temperature sensor user module (FlashTemp) or other temperature sensor, and feed the result to the temperature argument before writing. Refer to the Flash APIs Application Note AN2015 for more information.

Accessories (Emulation and Programming)

Table 21. Emulation and Programming Accessories

Part Number	Pin Package	Pod Kit [20]	Foot Kit [21]	Adapter [22]
CY8C21312-12PVXE	20-pin SSOP	CY3250-21X34	CY3250-20SSOP-FK	Adapters are available at http://www.emulation.com.
CY8C21512-12PVXE	28-pin SSOP	CY3250-21X34	CY3250-28SSOP-FK	

Notes
20. Pod kit contains an emulation pod, a flex-cable (connects the pod to the ICE), two feet, and device samples.
21. Foot kit includes surface mount feet that can be soldered to the target PCB.
22. Programming adapter converts non-DIP package to DIP footprint. Specific details and ordering information for each of the adapters are available at http://www.emulation.com.

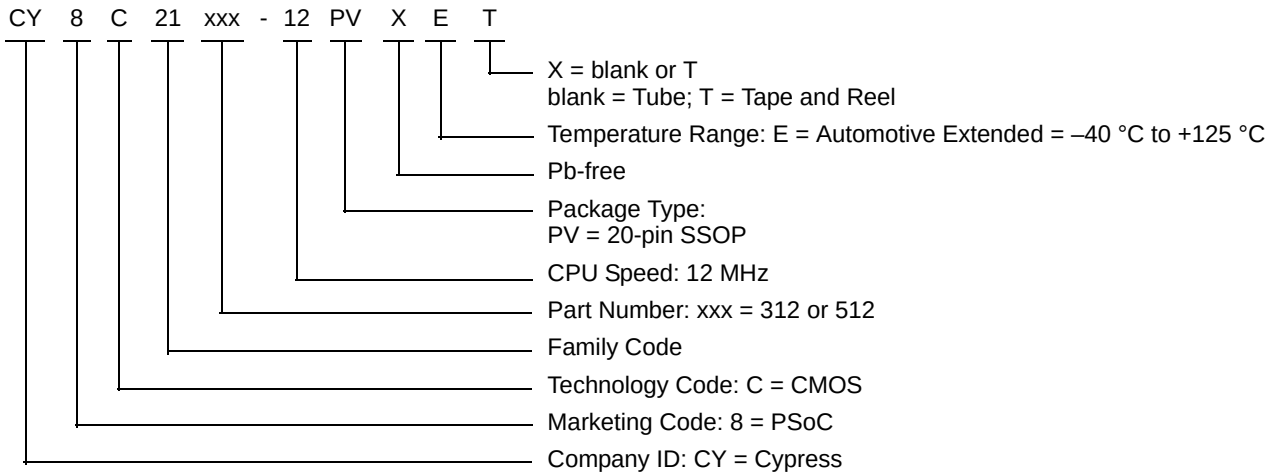
Ordering Information

The following table lists the CY8C21x12 PSoC device's key package features and ordering codes.

Table 22. PSoC Device Key Features and Ordering Information

Package	Ordering Code	Flash (Bytes)	SRAM (Bytes)	Temperature Range	Limited Digital Blocks	CapSense Blocks	Digital I/O Pins	Analog Inputs	Analog Outputs	XRES Pin
20-pin (210-Mil) SSOP	CY8C21312-12PVXE	8 K	512	–40 °C to +125 °C	1	1	16	16	0	Yes
20-pin (210-Mil) SSOP (Tape and Reel)	CY8C21312-12PVXET	8 K	512	–40 °C to +125 °C	1	1	16	16	0	Yes
28-pin (210-Mil) SSOP	CY8C21512-12PVXE	8 K	512	–40 °C to +125 °C	1	1	24	24	0	Yes
28-pin (210-Mil) SSOP (Tape and Reel)	CY8C21512-12PVXET	8 K	512	–40 °C to +125 °C	1	1	24	24	0	Yes

Ordering Code Definitions



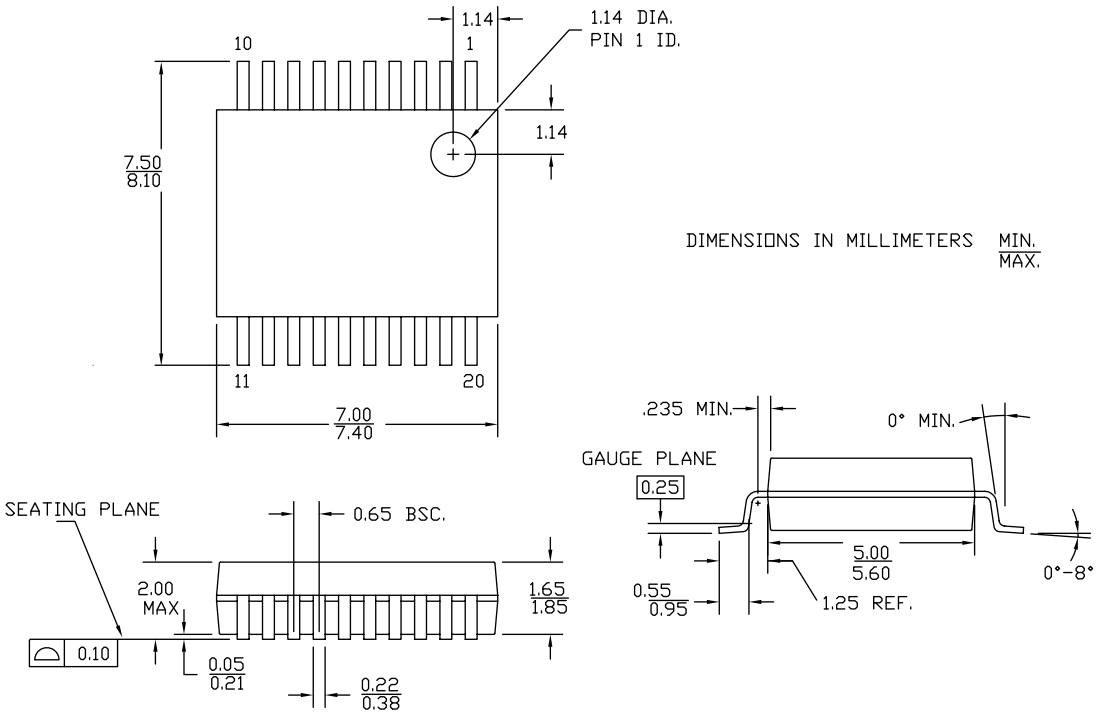
Packaging Information

This section illustrates the packaging specifications for the CY8C21x12 PSoC device, along with the thermal impedances for each package.

Important Note Emulation tools may require a larger area on the target PCB than the chip's footprint. For a detailed description of the emulator pod drawings at http://www.cypress.com.

Packaging Dimensions

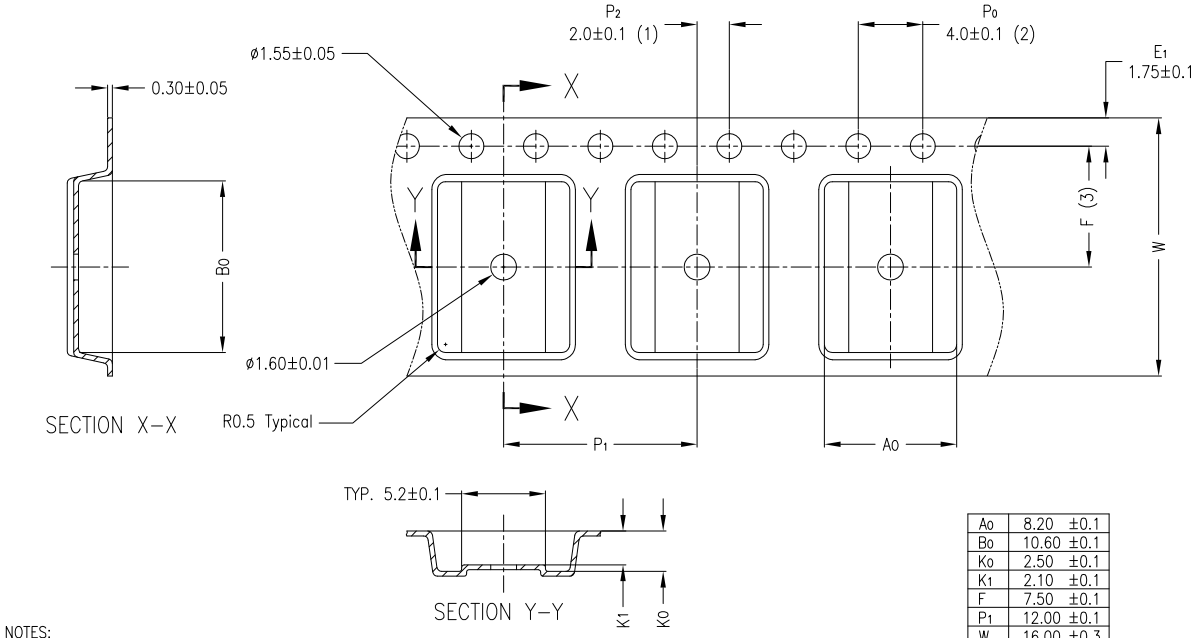
Figure 9. 20-pin SSOP (210 Mils) O20.21 Package Outline, 51-85077



51-85077 *E

Packaging Information *(continued)*

Figure 12. 28-pin SSOP (209 Mils) (C-Pak) Carrier Tape Drawing, 51-51100



A0	8.20 ±0.1
B0	10.60 ±0.1
K0	2.50 ±0.1
K1	2.10 ±0.1
F	7.50 ±0.1
P1	12.00 ±0.1
W	16.00 ±0.3

NOTES:
(1) Measured from centerline of sprocket hole to centerline of pocket.
(2) Cumulative tolerance of 10 sprocket holes is ± 0.10.
(3) Measured from centerline of sprocket hole to centerline of pocket
4 Material: Conductive Polystyrene
5 Camber not to exceed 1mm in 100mm
6 Supplier P/N: SSOP28–3 CL3 22B3 Lxx W16

51-51100 *C

Table 23. Tape and Reel Specifications

Package	Cover Tape Width (mm)	Hub Size (inches)	Minimum Leading Empty Pockets	Minimum Trailing Empty Pockets	Standard Full Reel Quantity
20-pin SSOP	13.3	4	42	25	2000
28-pin SSOP	13.3	7	42	25	1000

Glossary

active high	1. A logic signal having its asserted state as the logic 1 state. 2. A logic signal having the logic 1 state as the higher voltage of the two states.
analog blocks	The basic programmable opamp circuits. These are SC (switched capacitor) and CT (continuous time) blocks. These blocks can be interconnected to provide ADCs, DACs, multi-pole filters, gain stages, and much more.
analog-to-digital converter (ADC)	A device that changes an analog signal to a digital signal of corresponding magnitude. Typically, an ADC converts a voltage to a digital number. The digital-to-analog converter (DAC) performs the reverse operation.
Application programming interface (API)	A series of software routines that comprise an interface between a computer application and lower level services and functions (for example, user modules and libraries). APIs serve as building blocks for programmers that create software applications.
asynchronous	A signal whose data is acknowledged or acted upon immediately, irrespective of any clock signal.
bandgap reference	A stable voltage reference design that matches the positive temperature coefficient of VT with the negative temperature coefficient of VBE, to produce a zero temperature coefficient (ideally) reference.
bandwidth	1. The frequency range of a message or information processing system measured in hertz. 2. The width of the spectral region over which an amplifier (or absorber) has substantial gain (or loss); it is sometimes represented more specifically as, for example, full width at half maximum.
bias	1. A systematic deviation of a value from a reference value. 2. The amount by which the average of a set of values departs from a reference value. 3. The electrical, mechanical, magnetic, or other force (field) applied to a device to establish a reference level to operate the device.
block	1. A functional unit that performs a single function, such as an oscillator. 2. A functional unit that may be configured to perform one of several functions, such as a digital PSoC block or an analog PSoC block.
buffer	1. A storage area for data that is used to compensate for a speed difference, when transferring data from one device to another. Usually refers to an area reserved for I/O operations, into which data is read, or from which data is written. 2. A portion of memory set aside to store data, often before it is sent to an external device or as it is received from an external device. 3. An amplifier used to lower the output impedance of a system.
bus	1. A named connection of nets. Bundling nets together in a bus makes it easier to route nets with similar routing patterns. 2. A set of signals performing a common function and carrying similar data. Typically represented using vector notation; for example, address[7:0]. 3. One or more conductors that serve as a common connection for a group of related devices.
clock	The device that generates a periodic signal with a fixed frequency and duty cycle. A clock is sometimes used to synchronize different logic blocks.
comparator	An electronic circuit that produces an output voltage or current whenever two input levels simultaneously satisfy predetermined amplitude requirements.
compiler	A program that translates a high level language, such as C, into machine language.
configuration space	In PSoC devices, the register space accessed when the XIO bit, in the CPU_F register, is set to ‘1’.

jitter	1. A misplacement of the timing of a transition from its ideal position. A typical form of corruption that occurs on serial data streams. 2. The abrupt and unwanted variations of one or more signal characteristics, such as the interval between successive pulses, the amplitude of successive cycles, or the frequency or phase of successive cycles.
low voltage detect (LVD)	A circuit that senses V_{DD} and provides an interrupt to the system when V_{DD} falls below a selected threshold.
M8C	An 8-bit Harvard-architecture microprocessor. The microprocessor coordinates all activity inside a PSoC by interfacing to the flash, SRAM, and register space.
master device	A device that controls the timing for data exchanges between two devices. Or when devices are cascaded in width, the master device is the one that controls the timing for data exchanges between the cascaded devices and an external interface. The controlled device is called the *slave device*.
microcontroller	An integrated circuit chip that is designed primarily for control systems and products. In addition to a CPU, a microcontroller typically includes memory, timing circuits, and I/O circuitry. The reason for this is to permit the realization of a controller with a minimal quantity of chips, thus achieving maximal possible miniaturization. This in turn, reduces the volume and the cost of the controller. The microcontroller is normally not used for general-purpose computation as is a microprocessor.
mixed-signal	The reference to a circuit containing both analog and digital techniques and components.
modulator	A device that imposes a signal on a carrier.
noise	1. A disturbance that affects a signal and that may distort the information carried by the signal. 2. The random variations of one or more characteristics of any entity such as voltage, current, or data.
oscillator	A circuit that may be crystal controlled and is used to generate a clock frequency.
parity	A technique for testing transmitted data. Typically, a binary digit is added to the data to make the sum of all the digits of the binary data either always even (even parity) or always odd (odd parity).
phase-locked loop (PLL)	An electronic circuit that controls an *oscillator* so that it maintains a constant phase angle relative to a reference signal.
pinouts	The pin number assignment: the relation between the logical inputs and outputs of the PSoC device and their physical counterparts in the printed circuit board (PCB) package. Pinouts involve pin numbers as a link between schematic and PCB design (both being computer generated files) and may also involve pin names.
port	A group of pins, usually eight.
power-on reset (POR)	A circuit that forces the PSoC device to reset when the voltage is below a pre-set level. This is one type of hardware reset.
PSoC®	Cypress Semiconductor's PSoC® is a registered trademark and Programmable System-on-Chip™ is a trademark of Cypress.
PSoC Designer™	The software for Cypress' Programmable System-on-Chip technology.
pulse width modulator (PWM)	An output in the form of duty cycle which varies as a function of the applied value.
RAM	An acronym for random access memory. A data-storage device from which data can be read out and new data can be written in.
register	A storage device with a specific capacity, such as a bit or byte.

reset	A means of bringing a system back to a known state. See hardware reset and software reset.
ROM	An acronym for read only memory. A data-storage device from which data can be read out, but new data cannot be written in.
serial	1. Pertaining to a process in which all events occur one after the other. 2. Pertaining to the sequential or consecutive occurrence of two or more related activities in a single device or channel.
settling time	The time it takes for an output signal or value to stabilize after the input has changed from one value to another.
shift register	A memory storage device that sequentially shifts a word either left or right to output a stream of serial data.
slave device	A device that allows another device to control the timing for data exchanges between two devices. Or when devices are cascaded in width, the slave device is the one that allows another device to control the timing of data exchanges between the cascaded devices and an external interface. The controlling device is called the master device.
SRAM	An acronym for static random access memory. A memory device where you can store and retrieve data at a high rate of speed. The term static is used because, after a value is loaded into an SRAM cell, it remains unchanged until it is explicitly altered or until power is removed from the device.
SROM	An acronym for supervisory read only memory. The SROM holds code that is used to boot the device, calibrate circuitry, and perform flash operations. The functions of the SROM may be accessed in normal user code, operating from flash.
stop bit	A signal following a character or block that prepares the receiving device to receive the next character or block.
synchronous	1. A signal whose data is not acknowledged or acted upon until the next active edge of a clock signal. 2. A system whose operation is synchronized by a clock signal.
tristate	A function whose output can adopt three states: 0, 1, and Z (high-impedance). The function does not drive any value in the Z state and, in many respects, may be considered to be disconnected from the rest of the circuit, allowing another output to drive the same net.
UART	A UART or universal asynchronous receiver-transmitter translates between parallel bits of data and serial bits.
user modules	Pre-built, pre-tested hardware/firmware peripheral functions that take care of managing and configuring the lower level analog and digital PSoC blocks. User modules also provide high level *API (Application Programming Interface)* for the peripheral function.
user space	The bank 0 space of the register map. The registers in this bank are more likely to be modified during normal program execution and not just during initialization. Registers in bank 1 are most likely to be modified only during the initialization phase of the program.
V_{DD}	A name for a power net meaning "voltage drain". The most positive power supply signal. Usually 5 V or 3.3 V.
V_{SS}	A name for a power net meaning "voltage source." The most negative power supply signal.
watchdog timer	A timer that must be serviced periodically. If it is not serviced, the CPU resets after a specified period of time.

Document History Page

Document Title: CY8C21312/CY8C21512, Automotive Extended PSoC® Programmable System-on-Chip™ Document Number: 001-81890				
Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	3705964	MASJ	08/09/2012	New data sheet.
*A	4008934	KAUL	05/23/2013	Updated Features. Updated PSoC Functional Overview (Updated The Digital System). Updated Electrical Specifications (Updated DC Electrical Characteristics (Updated DC Chip-Level Specifications (Updated Table 8), updated DC GPIO Specifications (Updated Table 9), updated DC Operational Amplifier Specifications, updated DC Analog Mux Bus Specifications, updated DC POR and LVD Specifications, updated DC Programming Specifications (Updated Table 13)), updated AC Electrical Characteristics (Updated AC Chip-Level Specifications (Updated Table 14), updated AC GPIO Specifications (Updated Table 15), updated AC Operational Amplifier Specifications, updated AC Digital Block Specifications (Updated Table 17), updated AC External Clock Specifications, updated AC Programming Specifications, updated AC I2C Specifications)). Updated Packaging Information: Updated Tape and Reel Information: spec 51-51101 – Changed revision from *B to *C.
*B	4265204	JICG	01/28/2014	Removed ‘CY3207ISSP In-System Serial Programmer (ISSP)’ section.

Sales, Solutions, and Legal Information

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at Cypress Locations.

Products

Automotive	cypress.com/go/automotive
Clocks & Buffers	cypress.com/go/clocks
Interface	cypress.com/go/interface
Lighting & Power Control	cypress.com/go/powerpsoc cypress.com/go/plc
Memory	cypress.com/go/memory
PSoC	cypress.com/go/psoc
Touch Sensing	cypress.com/go/touch
USB Controllers	cypress.com/go/USB
Wireless/RF	cypress.com/go/wireless

PSoC Solutions

psoc.cypress.com/solutions

PSoC 1 | PSoC 3 | PSoC 5