Renesas Electronics America Inc - UPD70F3801GA-GAM-AX Datasheet

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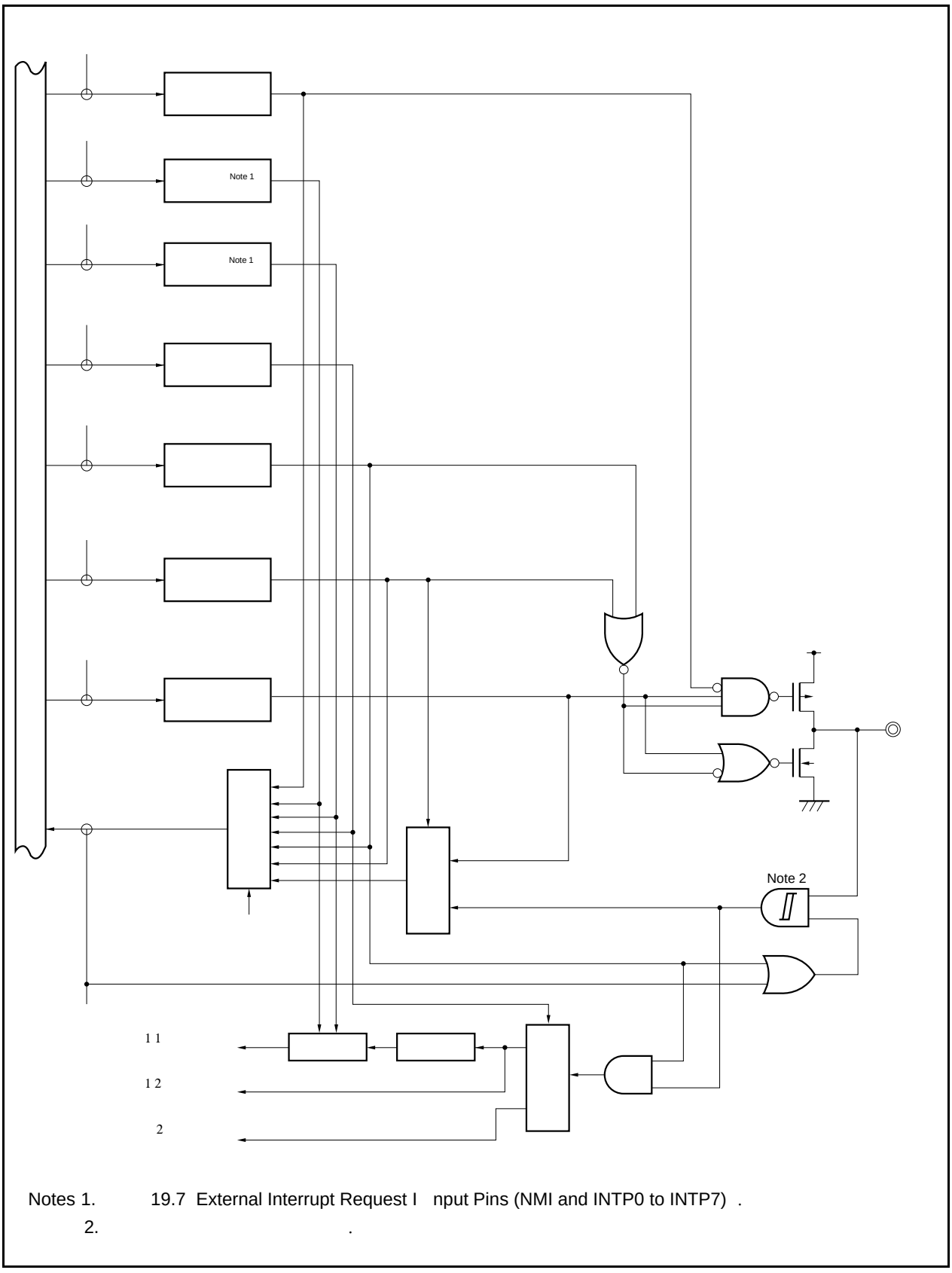
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	V850ES
Core Size	32-Bit Single-Core
Speed	20MHz
Connectivity	CSI, EBI/EMI, I²C, UART/USART
Peripherals	DMA, LVD, PWM, WDT
Number of I/O	34
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 3.6V
Data Converters	A/D 6x10b; D/A 1x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP Exposed Pad
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd70f3801ga-gam-ax

Table 1-2. V850ES/JE3-L Product List

Generic Name		V850ES/JE3-L				
Part Number		μPD70F3805	μPD70F3806	μPD70F3807	μPD70F3808	μPD70F3840
Internal memory	Flash memory	16 KB	32 KB	64 KB	128 KB	256 KB
	RAM	8 KB	8 KB	8 KB	8 KB	16 KB
Memory space		64 MB				
General-purpose register		32 bits × 32 registers				
Clock	Main clock (oscillation frequency)	Ceramic/crystal (in PLL mode: f_X = 2.5 to 5 MHz (multiplied by 4), in clock through mode: f_X = 2.5 to 10 MHz) External clock (in PLL mode: f_X = 2.5 to 5 MHz (multiplied by 4), in clock through mode: f_X = 2.5 to 5 MHz)				
	Subclock (oscillation frequency)	Crystal (f_{XT} = 32.768 kHz)				
	Internal oscillator	f_R = 220 kHz (TYP.)				
	Minimum instruction execution time	50 ns (main clock (f_{XX}) = 20 MHz)				
I/O port		I/O: 50 (5 V tolerant/N-ch open-drain output selectable: 28)				
Timer	16-bit TMP	6 channels				
	16-bit TMQ	1 channel				
	16-bit TMM	1 channel				
	Watch timer	1 channel				
	RTC	1 channel				
	WDT	1 channel				
Real-time output port		4 bits × 1 channel, 2 bits × 1 channel, or 6 bits × 1 channel				
10-bit A/D converter		10 channels				
8-bit D/A converter		1 channel				
Serial interface	CSIB	3 channels				
	UARTA/CSIB	1 channel				
	CSIB/I^2C bus	1 channel				
	UARTA/I^2C bus	2 channels				
	UARTA	-				
DMA controller		4 channels (transfer target: on-chip peripheral I/O, internal RAM)				
Interrupt source	External	9 (9)[Note]				
	Internal	48				
Power save function		HALT/IDLE1/IDLE2/STOP/subclock/sub-IDLE/ low-voltage STOP/low-voltage subclock/low-voltage sub-IDLE mode				
Reset source		RESET pin input, watchdog timer 2 (WDT2), clock monitor (CLM), low-voltage detector (LVI)				
CRC function		16-bit error detection code generated for 8-bit unit data				

Figure 4-19. Block Diagram of Type N-3



Notes 1. 19.7 External Interrupt Request I nput Pins (NMI and INTP0 to INTP7) .

2. .

(3) V850ES/JE3-L

Channel	Register name	Bit position							
		7	6	5	4	3	2	1	0
TMP0	TP0CTL0	TP0CE	0	0	0	0	TP0CKS2	TP0CKS1	TP0CKS0
	TP0CTL1	0	TP0EST	TP0EEE	0	0	TP0MD2	TP0MD1	TP0MD0
	TP0IOC0	0	0	0	0	TP0OL1	TP0OE1	TP0OL0	TP0OE0
	TP0IOC1	0	0	0	0	TP0IS3	TP0IS2	TP0IS1	TP0IS0
	TP0IOC2	0	0	0	0	TP0EES1	TP0EES0	TP0ETS1	TP0ETS0
	TP0OPT0	0	0	TP0CCS1	TP0CCS0	0	0	0	TP0OVF
TMP1	TP1CTL0	TP1CE	0	0	0	0	TP1CKS2	TP1CKS1	TP1CKS0
	TP1CTL1	0	TP1EST	TP1EEE	0	0	TP1MD2	TP1MD1	TP1MD0
	TP1IOC0	0	0	0	0	TP1OL1	TP1OE1	TP1OL0	TP1OE0
	TP1IOC1	0	0	0	0	TP1IS3	TP1IS2	TP1IS1	TP1IS0
	TP1IOC2	0	0	0	0	TP1EES1	TP1EES0	TP1ETS1	TP1ETS0
	TP1OPT0	0	0	TP1CCS1	TP1CCS0	0	0	0	TP1OVF
TMP2	TP2CTL0	TP2CE	0	0	0	0	TP2CKS2	TP2CKS1	TP2CKS0
	TP2CTL1	0	TP2EST	TP2EEE	0	0	TP2MD2	TP2MD1	TP2MD0
	TP2IOC0	0	0	0	0	TP2OL1	TP2OE1	TP2OL0	TP2OE0
	TP2IOC1	0	0	0	0	TP2IS3	TP2IS2	TP2IS1	TP2IS0
	TP2IOC2	0	0	0	0	TP2EES1	TP2EES0	TP2ETS1	TP2ETS0
	TP2OPT0	0	0	TP2CCS1	TP2CCS0	0	0	0	TP2OVF
TMP3	TP3CTL0	TP3CE	0	0	0	0	TP3CKS2	TP3CKS1	TP3CKS0
	TP3CTL1	0	TP3EST	0	0	0	TP3MD2	TP3MD1	TP3MD0
	TP3IOC0	0	0	0	0	TP3OL1	TP3OE1	0	0
	TP3IOC1	0	0	0	0	TP3IS3	TP3IS2	0	0
	TP3OPT0	0	0	TP3CCS1	TP3CCS0	0	0	0	TP3OVF
TMP4	TP4CTL0	TP4CE	0	0	0	0	TP4CKS2	TP4CKS1	TP4CKS0
	TP4CTL1	0	TP4EST	TP4EEE	0	0	TP4MD2	TP4MD1	TP4MD0
	TP4IOC0	0	0	0	0	TP4OL1	TP4OE1	TP4OL0	TP4OE0
	TP4IOC1	0	0	0	0	TP4IS3	TP4IS2	TP4IS1	TP4IS0
	TP4IOC2	0	0	0	0	TP4EES1	TP4EES0	TP4ETS1	TP4ETS0
	TP4OPT0	0	0	TP4CCS1	TP4CCS0	0	0	0	TP4OVF
TMP5	TP5CTL0	TP5CE	0	0	0	0	TP5CKS2	TP5CKS1	TP5CKS0
	TP5CTL1	0	TP5EST	TP5EEE	0	0	TP5MD2	TP5MD1	TP5MD0
	TP5IOC0	0	0	0	0	TP5OL1	TP5OE1	TP5OL0	TP5OE0
	TP5IOC1	0	0	0	0	TP5IS3	TP5IS2	TP5IS1	TP5IS0
	TP5IOC2	0	0	0	0	TP5EES1	TP5EES0	TP5ETS1	TP5ETS0
	TP5OPT0	0	0	TP5CCS1	TP5CCS0	0	0	0	TP5OVF

Remark **The TPnCCR0, TPnCCR1, and TPnCNT registers are available for all channels.**

(2) TMPn control register 1 (TPnCTL1)

The TPnCTL1 register is an 8-bit register that controls the operation of TMPn.

This register can be read or written in 8-bit or 1-bit units.

Reset sets this register to 00H.

After reset: 00H R/W Address: TP0CTL1 FFFFF591H, TP1CTL1 FFFFF5A1H, TP2CTL1 FFFFF5B1H, TP3CTL1 FFFFF5C1H, TP4CTL1 FFFFF5D1H, TP5CTL1 FFFFF5E1H

TPnCTL1 (n = 0 to 5)

7	<6>	<5>	4	3	2	1	0
0	TPnEST	TPnEEE	0	0	TPnMD2	TPnMD1	TPnMD0

TPnEST	Software trigger control
0	–
1	Generate a valid signal for external trigger input. • In one-shot pulse output mode: A one-shot pulse is output with writing 1 to the TPnEST bit as the trigger. • In external trigger pulse output mode: A PWM waveform is output with writing 1 to the TPnEST bit as the trigger.

TPnEEE	Count clock selection
0	Disable operation with external event count input. (Perform counting with the internal count clock selected by the TPnCTL0.TPnCK0 to TPnCK2 bits.)
1	Enable operation with external event count input. (Perform counting at the valid edge of the external event count input signal.)

TPnMD2	TPnMD1	TPnMD0	Timer mode selection
0	0	0	Interval timer mode
0	0	1	External event count mode
0	1	0	External trigger pulse output mode
0	1	1	One-shot pulse output mode
1	0	0	PWM output mode
1	0	1	Free-running timer mode
1	1	0	Pulse width measurement mode
1	1	1	Setting prohibited

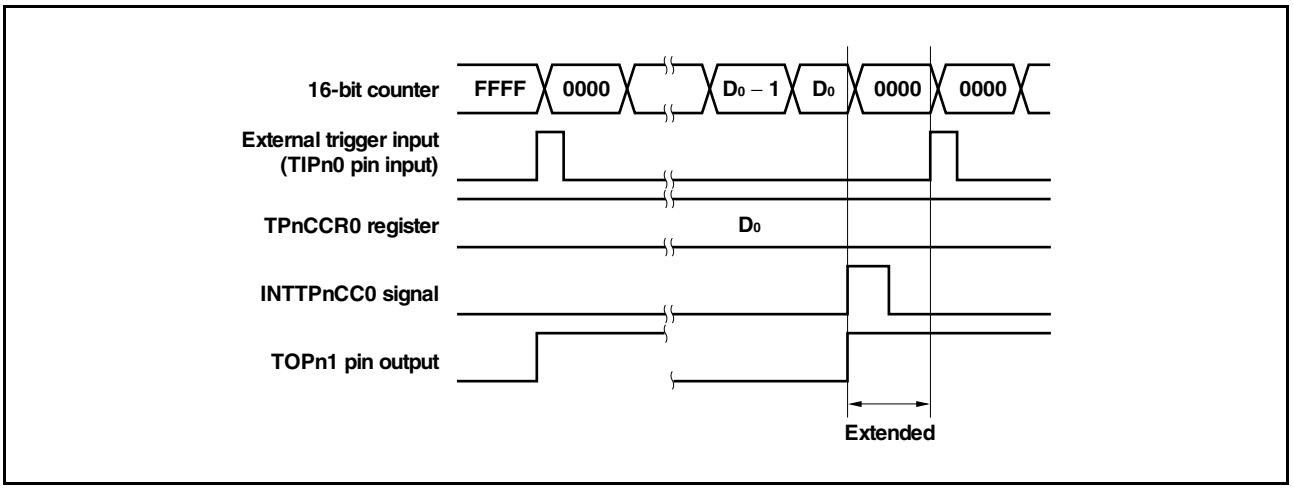
Cautions 1. The TPnEST bit is valid only in the external trigger pulse output mode or the one-shot pulse output mode. In any other mode, writing 1 to this bit is ignored.

2. External event count input is selected in the external event count mode regardless of the value of the TPnEEE bit.
3. Set the TPnEEE and TPnMD2 to TPnMD0 bits when the timer operation is stopped (TPnCTL0.TPnCE bit = 0). (The same value can be written when the TPnCE bit = 1.) The operation is not guaranteed when rewriting is performed with the TPnCE bit = 1. If rewriting was mistakenly performed, clear the TPnCE bit to 0 and then set the bits again.
4. Be sure to clear bits 3, 4, and 7 to "0".

(d) Detection of trigger immediately before or after INTTPnCC0 generation

If the trigger is detected immediately after the INTTPnCC0 signal is generated, the 16-bit counter is cleared to 0000H and continues incrementing. Therefore, the active period of the TOPn1 pin is extended by the amount of time between the generation of the INTTPnCC0 signal and the detection of the trigger.

Figure 6-35. Detection of Trigger Immediately After INTTPnCC0 Signal Was Generated



If the trigger is detected immediately before the INTTPnCC0 signal is generated, the INTTPnCC0 signal is not generated. The 16-bit counter is cleared to 0000H, the TOPn1 pin is set to the active level, and the counter continues incrementing. Consequently, the inactive period of the PWM waveform is shortened.

Figure 6-36. Detection of Trigger Immediately Before INTTPnCC0 Signal Is Generated

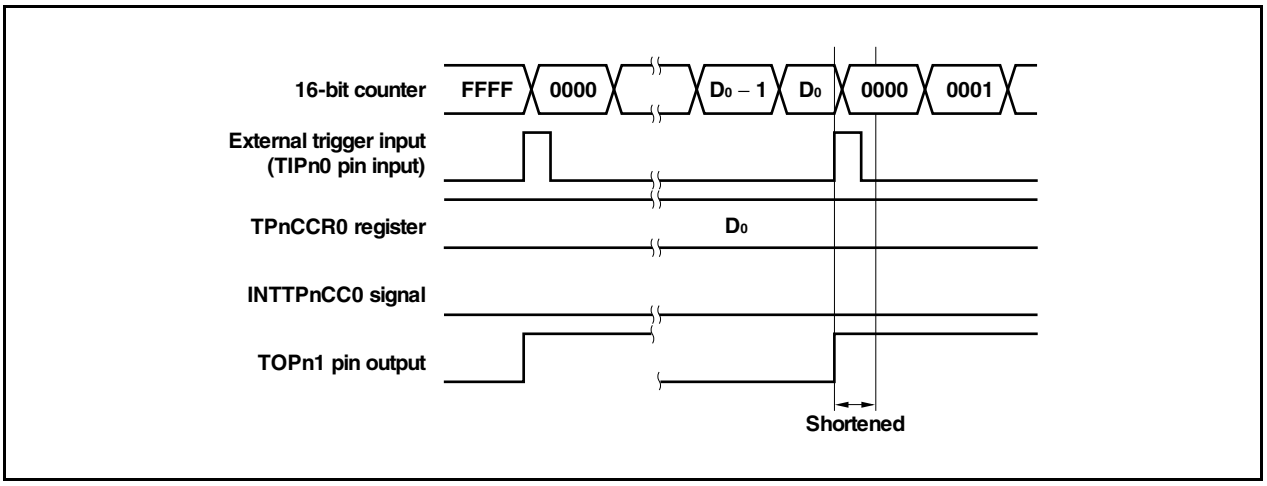
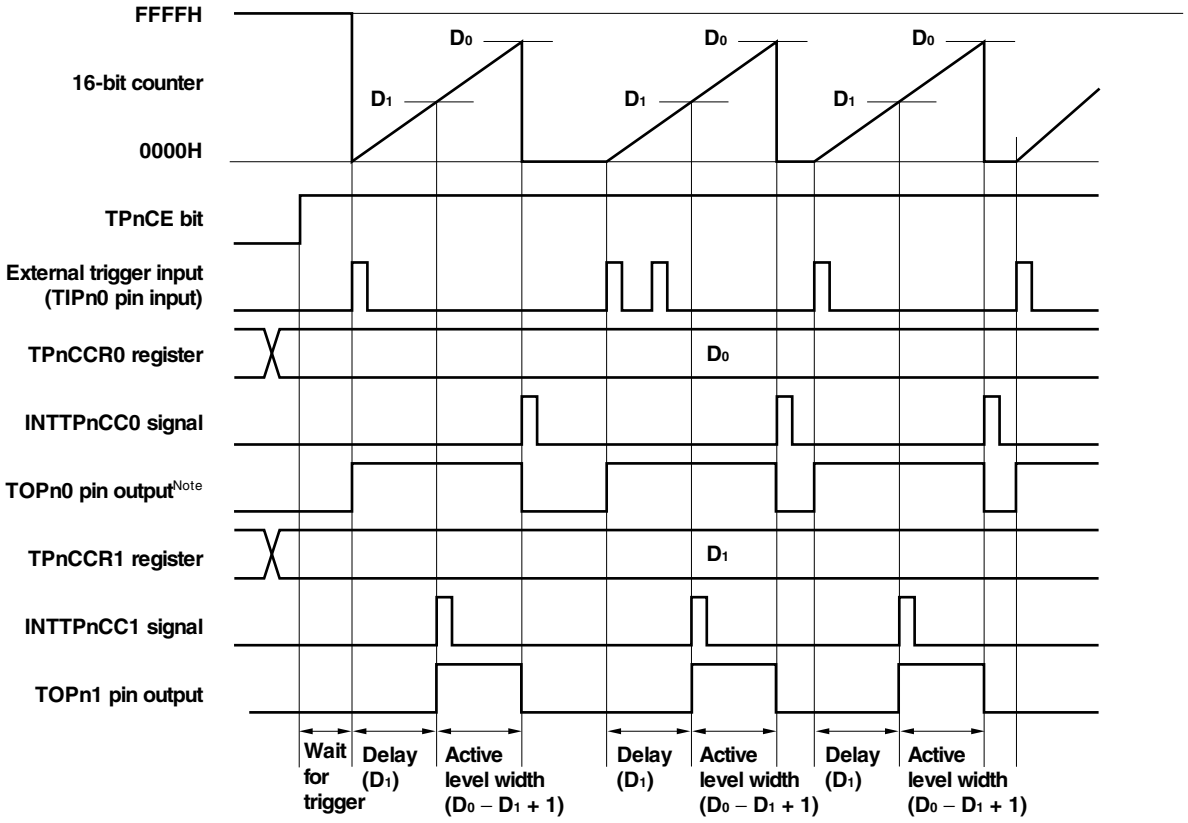


Figure 6-39. Basic Timing of Operations in One-Shot Pulse Output Mode



Note The output from the TOPn0 pin can also be used as the input to the TIPn0 pin. When using the output from the TOPn0 pin as the input to the TIPn0 pin, use a software trigger instead of an external trigger.

When the TPnCE bit is set to 1, TMPn waits for a trigger. When the trigger is generated, the 16-bit counter is cleared from FFFFH to 0000H, starts incrementing, and outputs a one-shot pulse from the TOPn1 pin. After the one-shot pulse is output, the 16-bit counter is set to 0000H, stops incrementing, and waits for a trigger. If a trigger is generated again while the one-shot pulse is being output, it is ignored.

The output delay period and active level width of the one-shot pulse can be calculated as follows:

Output delay period = (Set value of TPnCCR1 register) × Count clock cycle

Active level width = (Set value of TPnCCR0 register − Set value of TPnCCR1 register + 1) × Count clock cycle

The INTTPnCC0 compare match interrupt request signal is generated when the 16-bit counter increments next time after its value matches the value of the CCR0 buffer register. The INTTPnCC1 compare match interrupt request signal is generated when the value of the 16-bit counter matches the value of the CCR1 buffer register.

Either the valid edge of the external trigger input signal or setting the software trigger (TPnCTL1.TPnEST bit) to 1 is used as the trigger.

7.2.2 Interrupts

The following five types of interrupt signals are used by TMQ0:

(1) INTTQ0CC0

This signal is generated when the value of the 16-bit counter matches the value of the CCR0 buffer register, or when a capture signal is input from the TIQ00 pin.

(2) INTTQ0CC1

This signal is generated when the value of the 16-bit counter matches the value of the CCR1 buffer register, or when a capture signal is input from the TIQ01 pin.

(3) INTTQ0CC2

This signal is generated when the value of the 16-bit counter matches the value of the CCR2 buffer register, or when a capture signal is input from the TIQ02 pin.

(4) INTTQ0CC3

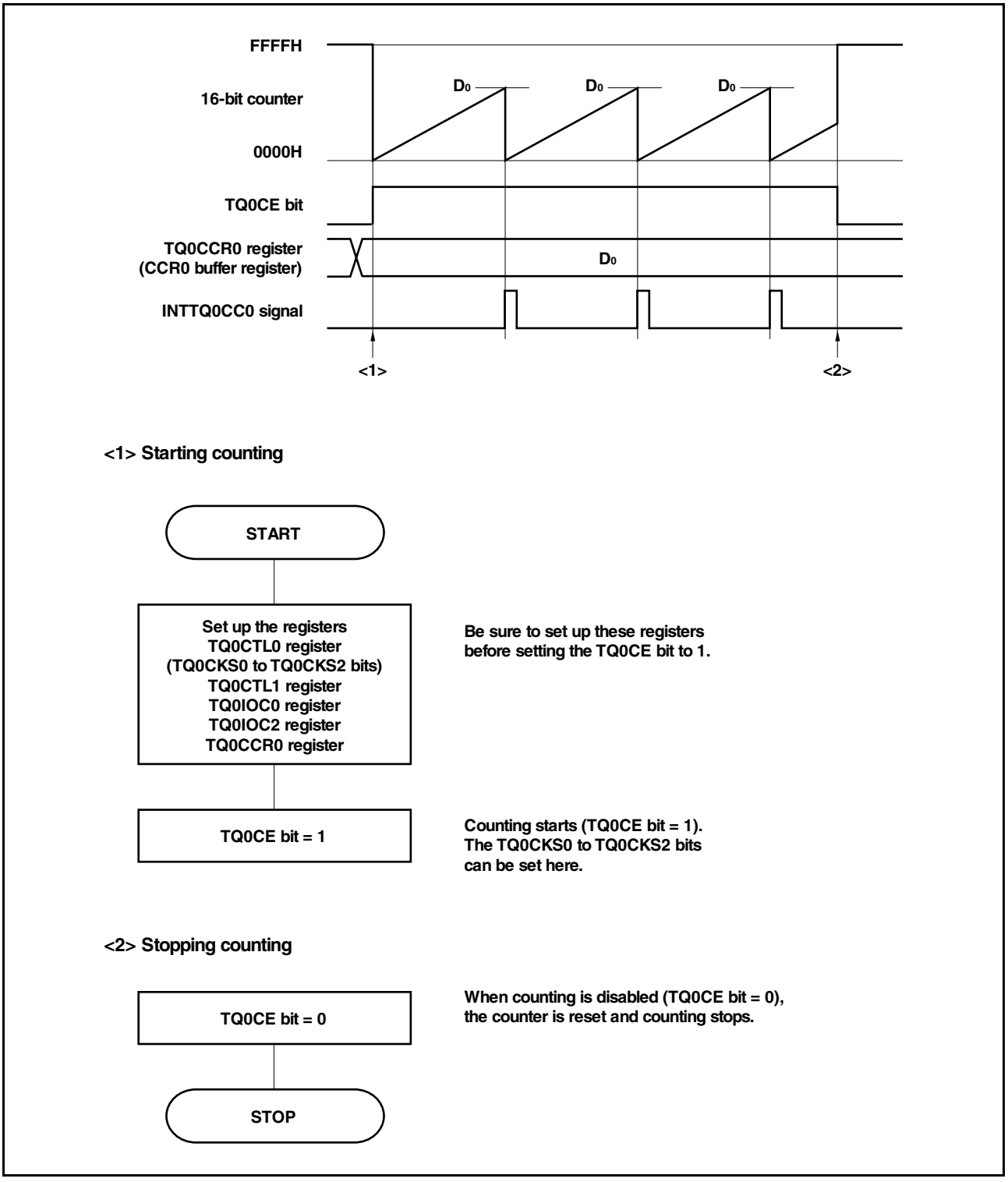
This signal is generated when the value of the 16-bit counter matches the value of the CCR3 buffer register, or when a capture signal is input from the TIQ03 pin.

(5) INTTQ0OV

This signal is generated when the 16-bit counter overflows after incrementing up to FFFFH.

(1) Operations in external event count mode

Figure 7-20. Timing and Processing of Operations in External Event Count Mode



(13) Watch error correction register (RC1SUBU)

The RC1SUBU register is an 8-bit register that can be used to correct the watch with high accuracy when the watch is early or late, by changing the value (reference value: 7FFFH) overflowing from the sub-count register (RSUBC) to the second counter register.

This register can be read or written in 8-bit or 1-bit units.

Reset sets this register to 00H.

Remarks 1. **The RC1SUBU register can be rewritten only when the real-time counter is set to its initial values. Be sure to see** 10.4.1 Initial settings**.**

2. **See** 10.4.9 Watch error correction example of real-time counter **for details of watch error correction.**

After reset: 00H R/W Address: FFFFFAD9H

	7	6	5	4	3	2	1	0
RC1SUBU	DEV	F6	F5	F4	F3	F2	F1	F0

DEV	Setting of watch error correction timing
0	Corrects watch errors when RC1SEC (second counter) is at 00, 20, or 40 seconds (every 20 seconds).
1	Corrects watch errors when RC1SEC (second counter) is at 00 seconds (every 60 seconds).

F6	Setting of watch error correction value
0	Increments the RC1SUBC count value by the value set using the F5 to F0 bits (positive correction). Expression for calculating increment value: (Setting value of F5 to F0 bits − 1) × 2
1	Decrements the RC1SUBC count value by the value set using the F5 to F0 bits (negative correction). Expression for calculating decrement value: (Inverted value of setting value of F5 to F0 bits + 1) × 2
If the F6 to F0 bit values are 1/0, 0, 0, 0, 0, 0, 1/0 , watch error correction is not performed.	

11.3 Registers

(1) Watchdog timer mode register 2 (WDTM2)

The WDTM2 register sets the overflow time and operation clock of watchdog timer 2.

This register can be read or written in 8-bit units. This register can be read any number of times, but it can be written only once following reset release.

Reset sets this register to 67H.

Caution Accessing the WDTM2 register is prohibited in the following statuses. Moreover, if the system is in the wait status, the only way to cancel the wait status is to execute a reset. For details, see 3.4.9 (1) Accessing specific on-chip peripheral I/O registers.

- When the CPU operates on the subclock and main clock oscillation is stopped
- When the CPU operates on the internal oscillator clock

After reset: 67H R/W Address: FFFFF6D0H

	7	6	5	4				
WDTM2	**0**	**WDM21**	**WDM20**	**WDCS24**	**WDCS23**	**WDCS22**	**WDCS21**	**WDCS20**

WDM21	WDM20	Selection of operation mode of watchdog timer 2
0	0	Stops operation
0	1	Non-maskable interrupt request mode (generation of INTWDT2 signal)
1	-	Reset mode (generation of WDT2RES signal)

(2) UARTAn control register 1 (UAnCTL1)

The UAnCTL1 register is an 8-bit register that selects the UARTAn base clock.

This register can be read or written in 8-bit units.

Reset sets this register to 00H.

Caution Clear the UAnCTL0.UAnPWR bit to 0 before rewriting the UAnCTL1 register.

After reset: 00H R/W Address: UA0CTL1 FFFFFA01H, UA1CTL1 FFFFFA11H, UA2CTL1 FFFFFA21H

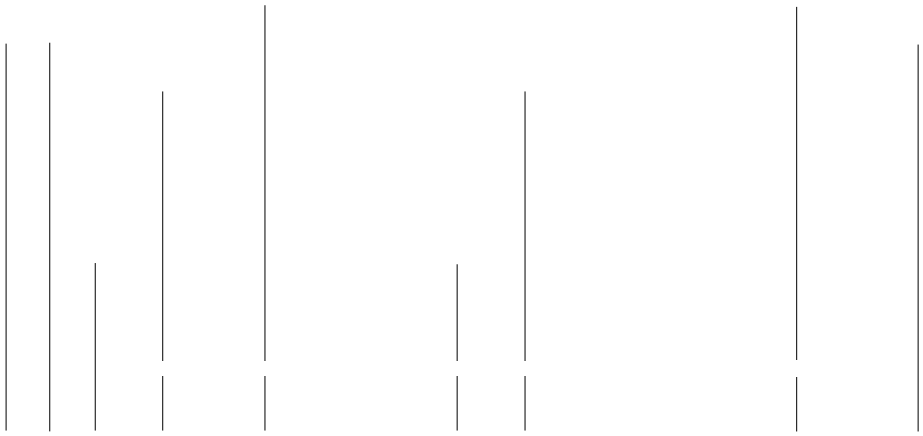
	7	6	5	4	3	2	1	0
UAnCTL1	0	0	0	0	UAnCKS3	UAnCKS2	UAnCKS1	UAnCKS0

UAnCKS3	UAnCKS2	UAnCKS1	UAnCKS0	Base clock (f_{UCLK}) selection
0	0	0	0	fxx
0	0	0	1	fxx/2
0	0	1	0	fxx/4
0	0	1	1	fxx/8
0	1	0	0	fxx/16
0	1	0	1	fxx/32
0	1	1	0	fxx/64
0	1	1	1	fxx/128
1	0	0	0	fxx/256
1	0	0	1	fxx/512
1	0	1	0	fxx/1,024
1	0	1	1	External clock[Note] (ASCKA0 pin)
Other than above				Setting prohibited

Note **Only UARTA0 is valid; setting UARTA1, UART2, V850ES/JC3-L (40-pin) are prohibited.**

Remark **fxx: Main clock frequency**

Figure 16-18. Continuous Transfer Mode Operation Timing (Master Mode, Transmission Mode)



(4) Start Address Data Start Address Data Stop

<1> When WTIMn bit = 0 (after restart, address mismatch (= not extension code))

ST	AD6 to AD0	R/$\overline{W}$	$\overline{ACK}$	D7 to D0	$\overline{ACK}$	ST	AD6 to AD0	R/$\overline{W}$	$\overline{ACK}$	D7 to D0	$\overline{ACK}$	SP
			S 1		**S** 2				**S** 3			'4

S 1: IICSn register = 0001X110B

S 2: IICSn register = 0001X000B

S 3: IICSn register = 00000X10B

' 4: IICSn register = 00000001B

Remark **S** :Always generated

': Generated only when SPIEn bit = 1

X: don't care

<2> When WTIMn bit = 1 (after restart, address mismatch (= not extension code))

ST	AD6 to AD0	R/$\overline{W}$	$\overline{ACK}$	D7 to D0	$\overline{ACK}$	ST	AD6 to AD0	R/$\overline{W}$	$\overline{ACK}$	D7 to D0	$\overline{ACK}$	SP
			S 1		**S** 2				**S** 3			'4

S 1: IICSn register = 0001X110B

S 2: IICSn register = 0001XX00B

S 3: IICSn register = 00000X10B

' 4: IICSn register = 00000001B

Remark **S** :Always generated

': Generated only when SPIEn bit = 1

X: don't care

29.2.2 Mask function

Only reset signals can be masked.

The maskable signals in the debugger (ID850QB) and the corresponding V850ES/JC3-L and V850ES/JE3-L functions are listed below.

Table 29-5. Mask Functions

Maskable Signals in ID850QB	Corresponding V850ES/JC3-L and V850ES/JE3-L Functions
NMI0	–
NMI1	–
NMI2	–
STOP	–
HOLD	–
RESET	Reset signal generation by $\overline{\text{RESET}}$ pin input
WAIT	–

31.8.4 UART timing

(T_A = –40 to +85°C, V_{DD} = EV_{DD} = AV_{REF0} = AV_{REF1}, V_{SS} = EV_{SS} = AV_{SS} = 0 V, C_L = 50 pF)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Transmit rate		V_{DD} = 2.2 to 3.6 V		625	kbps
ASCK0 frequency		V_{DD} = 2.2 to 3.6 V		5	MHz
		V_{DD} = 2.7 to 3.6 V		10	MHz

31.8.5 CSIB timing

(1) Master mode

(T_A = –40 to +85°C, V_{DD} = EV_{DD} = AV_{REF0} = AV_{REF1}, V_{SS} = EV_{SS} = AV_{SS} = 0 V, C_L = 50 pF)

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
$\overline{SCKBn}$ cycle time	t_{KCY1}	<60>	2.7 V ≤ V_{DD} ≤ 3.6 V	125		ns
			2.2 V ≤ V_{DD} < 2.7 V	800		ns
$\overline{SCKBn}$ high-level width	t_{KH1}	<61>	2.7 V ≤ V_{DD} ≤ 3.6 V	$t_{KCY1}/2 - 8$		ns
			2.2 V ≤ V_{DD} < 2.7 V	$t_{KCY1}/2 - 80$		ns
$\overline{SCKBn}$ low-level width	t_{KL1}	<62>	2.7 V ≤ V_{DD} ≤ 3.6 V	$t_{KCY1}/2 - 8$		ns
			2.2 V ≤ V_{DD} < 2.7 V	$t_{KCY1}/2 - 80$		ns
SIBn setup time (to $\overline{SCKBn}$↑)	t_{SIK1}	<63>	2.7 V ≤ V_{DD} ≤ 3.6 V	27		ns
			2.2 V ≤ V_{DD} < 2.7 V	100		ns
SIBn hold time (from $\overline{SCKBn}$↑)	t_{KSI1}	<64>	2.7 V ≤ V_{DD} ≤ 3.6 V	27		ns
			2.2 V ≤ V_{DD} < 2.7 V	100		ns
Delay time from $\overline{SCKBn}$↓ to SOBn output	t_{KSO1}	<65>	2.7 V ≤ V_{DD} ≤ 3.6 V		27	ns
			2.2 V ≤ V_{DD} < 2.7 V		95	ns

Remark **n = 0 to 2, 4**