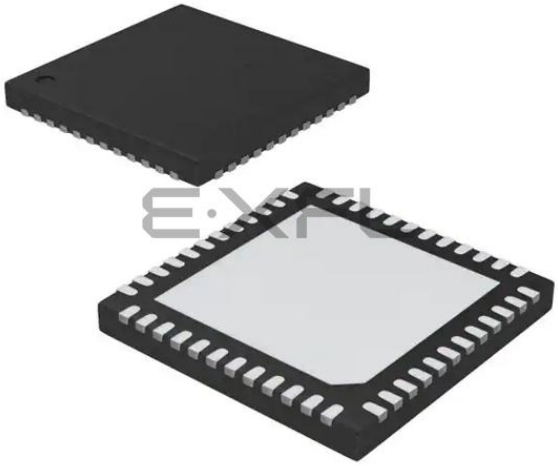
Renesas Electronics America Inc - UPD70F3802GA-GAM-AX Datasheet



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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	V850ES
Core Size	32-Bit Single-Core
Speed	20MHz
Connectivity	CSI, EBI/EMI, I²C, UART/USART
Peripherals	DMA, LVD, PWM, WDT
Number of I/O	34
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 3.6V
Data Converters	A/D 6x10b; D/A 1x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-WFQFN Exposed Pad
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd70f3802ga-gam-ax

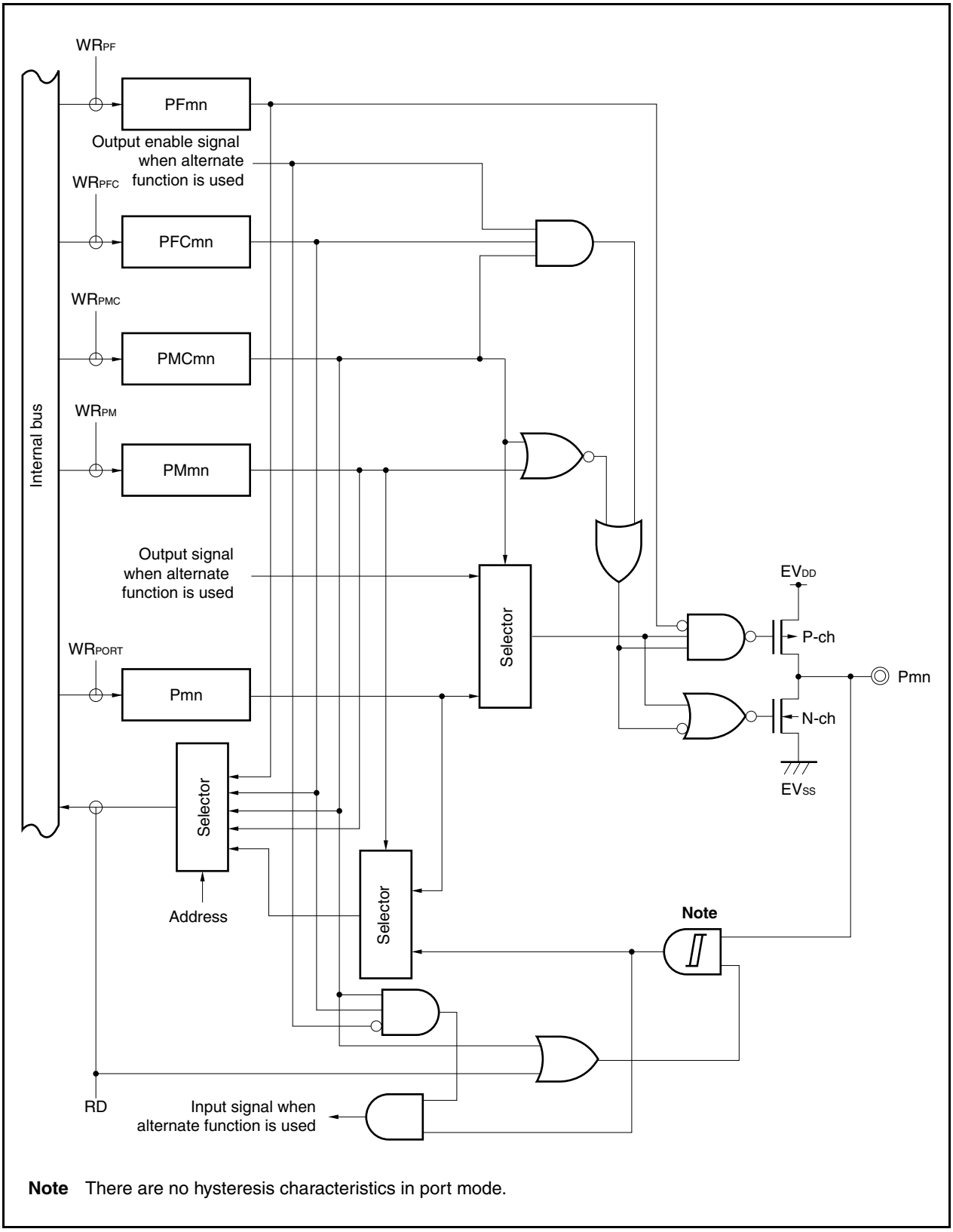
2.3 Pin I/O Circuit Types, I/O Buffer Power Supplies, and Connection of Unused Pins

(1/2)

Pin	Alternate Function	Pin No.			I/O Circuit Type	Recommended Connection of Unused Pin
		JC3L (40)	JC3L (48)	JE3L		
P02	NMI	11	13	17	10-D	Input: Independently connect to EV_{DD} or EV_{SS} via a resistor. Output: Leave open.
P03	INTP0/ADTRG/RTC1HZ	12	14	18		
P04	INTP1/RTCDIV/RTCCL	–	–	19		
P05	INTP2/$\overline{DRST}$	27	31	41	10-N	Input: Independently connect to EV_{SS} via a resistor. Fixing to V_{DD} level is prohibited. Output: Leave open. Internally pull-down after reset by $\overline{RESET}$ pin.
P06	INTP3	–	–	20	10-D	Input: Independently connect to EV_{DD} or EV_{SS} via a resistor. Output: Leave open.
P10	ANO0	–	3	3	12-D	Input: Independently connect to AV_{REF1} or AV_{SS} via a resistor. Output: Leave open.
P30	TXDA0/SOB4	–	33	45	10-G	Input: Independently connect to EV_{DD} or EV_{SS} via a resistor. Output: Leave open.
	TXDA0	29	–	–		
P31	RXDA0/INTP7/SIB4	–	34	46	10-D	
	RXDA0/INTP7	30	–	–		
P32	ASCKA0/$\overline{SCKB4}$/TIP00	–	35	47		
P33	TIP01/TOP01	–	–	43		
P34	TIP10/TOP10	–	–	44		
P35	TIP11/TOP11	–	–	23		
P38	TXDA2/SDA00	–	18	26		
P39	RXDA2/SCL00	–	19	27		
P40	SIB0/SDA01	16	20	28		
P41	SOB0/SCL01	17	21	29		
P42	$\overline{SCKB0}$	18	22	30		
P50	TIQ01/KR0/TOQ01/RTP00	21	25	35	10-D	
P51	TIQ02/KR1/TOQ02/RTP01	22	26	36		
P52	TIQ03/KR2/TOQ03/RTP02/DDI	23	27	37		
P53	SIB2/KR3/TIQ00/TOQ00 /RTP03/DDO	24	28	38		
P54	SOB2/KR4/RTP04/DCK	25	29	39		
P55	$\overline{SCKB2}$/KR5/RTP05/DMS	26	30	40		

Remark JC3L (40): V850ES/JC3-L (40-pin products)
JC3L (48): V850ES/JC3-L (48-pin products)
JE3L : V850ES/JE3-L

Figure 4-15. Block Diagram of Type G-15



Note There are no hysteresis characteristics in port mode.

(a) Function as compare register

The TPnCCR1 register can be rewritten even when the TPnCTL0.TPnCE bit = 1.

The set value of the TPnCCR1 register is transferred to the CCR1 buffer register. When the value of the 16-bit counter matches the value of the CCR1 buffer register, a compare match interrupt request signal (INTTPnCC1) is generated. If TOPn1 pin output is enabled at this time, the output of the TOPn1 pin is inverted (For details, see the descriptions of each operating mode.).

(b) Function as capture register

When the TPnCCR1 register is used as a capture register in the free-running timer mode, the count value of the 16-bit counter is stored in the TPnCCR1 register if the valid edge of the capture trigger input pin (TIPn1 pin) is detected. In the pulse-width measurement mode, the count value of the 16-bit counter is stored in the TPnCCR1 register and the 16-bit counter is cleared (0000H) if the valid edge of the capture trigger input pin (TIPn1) is detected.

Even if the capture operation and reading the TPnCCR1 register conflict, the correct value of the TPnCCR1 register can be read.

The following table shows the functions of the capture/compare register in each mode, and how to write data to the compare register.

Table 6-4. Function of Capture/Compare Register in Each Mode and How to Write Compare Register

Operation Mode	Capture/Compare Register	How to Write Compare Register
Interval timer	Compare register	Anytime write
External event counter	Compare register	Anytime write
External trigger pulse output	Compare register	Batch write
One-shot pulse output	Compare register	Anytime write
PWM output	Compare register	Batch write
Free-running timer	Capture/compare register	Anytime write
Pulse width measurement	Capture register	–

Remark For details about anytime write and batch write, see **6.4 (2) Anytime write and batch write**.

(b) Batch write

This writing method is used to transfer data from the TQ0CCR0 to TQ0CCR3 registers to the CCR0 to CCR3 buffer registers all at once while TMQ0 is operating. The data is transferred when the value of the 16-bit counter matches the value of the CCR0 buffer register. Transfer is enabled by writing to the TQ0CCR1 register. Whether transfer of the next data is enabled or not depends on whether the TQ0CCR1 register has been written.

To specify the value of the rewritten TQ0CCR0 to TQ0CCR3 registers as the 16-bit counter compare value (that is, the value to be transferred to the CCR0 to CCR3 buffer registers), the TQ0CCR0 register must be rewritten before the value of the 16-bit counter matches the value of the CCR0 buffer register, and then the TQ0CCR1 register must be written. The value of the TQ0CCR0 to TQ0CCR3 registers is then transferred to the CCR0 to CCR3 buffer registers when the value of the 16-bit counter matches the value of the CCR0 buffer register. Note that even if you wish to rewrite one of the TQ0CCR0, TQ0CCR2 and TQ0CCR3 register values, you must also write the same value to the TQ0CCR1 register (that is, the same value as the value already specified for the TQ0CCR1 register).

(2) Using pulse width measurement mode

(a) Clearing the overflow flag (TQ0OVF)

The overflow flag (TQ0OVF) can be cleared to 0 by reading the TQ0OVF bit and, if its value is 1, either clearing the bit to 0 by using the CLR1 instruction or by writing 8-bit data (with bit 0 as “0”) to the TQ0OPT0 register.

7.4.8 Timer output operations

The following table shows the operations and output levels of the TOQ00 to TOQ03 pins.

Table 7-8. Timer Output Control in Each Mode

Operation Mode	TOQ00 Pin	TOQ01 Pin	TOQ02 Pin	TOQ03 Pin
Interval timer mode	Square wave output			
External event count mode	–			
External trigger pulse output mode	Square wave output	External trigger pulse output	External trigger pulse output	External trigger pulse output
One-shot pulse output mode		One-shot pulse output	One-shot pulse output	One-shot pulse output
PWM output mode		PWM output	PWM output	PWM output
Free-running timer mode	Square wave output (only when compare function is used)			
Pulse width measurement mode	–			

Table 7-9. Truth Table of TOQ00 to TOQ03 Pins Under Control of Timer Output Control Bits

TQ0IOC0.TQ0OLm Bit	TQ0IOC0.TQ0OEm Bit	TQ0CTL0.TQ0CE Bit	Level of TOQ0m Pin
0	0	×	Low-level output
	1	0	Low-level output
		1	Low level immediately before counting, high level after counting is started
1	0	×	High-level output
	1	0	High-level output
		1	High level immediately before counting, low level after counting is started

Remark m = 0 to 3

10.2 Configuration

The real-time counter includes the following hardware.

Table 10-1. Configuration of Real-Time Counter

Item	Configuration
Control registers	Real-time counter control register 0 (RC1CC0) Real-time counter control register 1 (RC1CC1) Real-time counter control register 2 (RC1CC2) Real-time counter control register 3 (RC1CC3) Sub-count register (RC1SUBC) Second count register (RC1SEC) Minute count register (RC1MIN) Hour count register (RC1HOUR) Day count register (RC1DAY) Day-of-week count register (RC1WEEK) Month count register (RC1MONTH) Year count register (RC1YEAR) Watch error correction register (RC1SUBU) Alarm minute register (RC1ALM) Alarm hour register (RC1ALH) Alarm week register (RC1ALW) Prescaler mode register 0 (PRSM0) Prescaler compare register 0 (PRSCM0)

CHAPTER 13 A/D CONVERTER

13.1 Overview

The A/D converter of the V850ES/JC3-L and V850ES/JE3-L have a resolution of 10 bits and converts an input analog signal into a digital value.

The number of A/D converter in the V850ES/JC3-L and V850ES/JE3-L are shown below.

Product Name	V850ESJC3-L (40-pin)	V850ES/JC3-L (48-pin)	V850ES/JE3-L
Number of ANI channels (m)	5 channels (m = 5)	6 channels (m = 6)	10 channels (m =10)
Number of mounted (n)	ANI0 to ANI4 (n = 0 to 4)	ANI0 to ANI5 (n = 0 to 5)	ANI0 to ANI9 (n = 0 to 9)

In this chapter, the number of ANI channels is expressed as m and the number of ANI pins (analog input function pins) is expressed as n.

The A/D converter has the following features.

- 10-bit resolution
- Successive approximation method
- Operating voltage: AV_{REF0} = 2.7 to 3.6 V
- Analog input voltage: 0 V to AV_{REF0}
- The following functions are provided as operation modes.
  - Continuous select mode
  - Continuous scan mode
  - One-shot select mode
  - One-shot scan mode
- The following functions are provided as trigger modes.
  - Software trigger mode
  - External trigger mode (external, 1)
  - Timer trigger mode
- Conversion time
  2.6 to 24 μs@3.0 V $\leq AV_{REF0} \leq$ 3.6 V
  3.9 to 24 μs@2.7 V $\leq AV_{REF0} <$ 3.0 V
- Power-fail monitor function (conversion result compare function)

13.2 Functions

(1) 10-bit resolution A/D conversion

A/D conversion is repeated at a resolution of 10 bits for an analog signal that is input to a channel selected from ANIn. Each time A/D conversion is completed, an interrupt request signal (INTAD) is generated.

(2) Power-fail detection

This function is used to detect a drop in the battery voltage. The result of A/D conversion (the value of the ADA0CRnH register) is compared with the value of the ADA0PFT register, and the INTAD signal is generated only when the comparison condition specified by the ADA0PFM register is satisfied.

CHAPTER 15 ASYNCHRONOUS SERIAL INTERFACE A (UARTA)

The number of UARTA channels in the V850ES/JC3-L, V850ES/JE3-L are shown below.

Product Name	V850ESJC3-L (40-pin)	V850ES/JC3-L (48-pin)	V850ES/JE3-L
Number of channels	2 channels UARTA0, UARTA1	3 channels UARTA0 to UARTA2	3 channels UARTA0 to UARTA2

In this chapter, the number of channels is expressed as n.

15.1 Features

- On-chip dedicated baud rate generator
- Transfer rate: 300 bps to 625 kbps (using dedicated baud rate generator)
- Full-duplex communication
- Double buffer configuration Internal UARTAn receive data register (UAnRX)
  Internal UARTAn transmit data register (UAnTX)
- Reception error detection function
  - Parity error
  - Framing error
  - Overrun error
- Interrupt sources: 2
  - Reception complete interrupt (INTUAnR): This interrupt occurs upon transfer of receive data from the receive shift register to the receive data register after serial transfer completion, in the reception enabled status.
  - Transmission enable interrupt (INTUAnT): This interrupt occurs upon transfer of transmit data from the transmit data register to the transmit shift register in the transmission enabled status. (Continuous transmission is possible.)
- Character length: 7, 8 bits
- Parity function: Odd, even, 0, none
- Transmission stop bit: 1, 2 bits
- MSB-/LSB-first transfer selectable
- Internal digital noise filter
- Inverted input/output of transmit/receive data possible
- SBF (Sync Break Field) transmission/reception in the LIN (Local Interconnect Network) communication format
  - 13 to 20 bits selectable for SBF transmission
  - Recognition of 11 bits or more possible for SBF reception
  - SBF reception flag provided

15.4 Registers

(1) UARTAn control register 0 (UAnCTL0)

The UAnCTL0 register is an 8-bit register that controls the UARTAn serial transfer operation.

This register can be read or written in 8-bit or 1-bit units.

Reset sets this register to 10H.

(1/2)

After reset: 10H R/W Address: UA0CTL0 FFFFFA00H, UA1CTL0 FFFFFA10H, UA2CTL0 FFFFFA20H

	<7>	<6>	<5>	<4>	3	2	1	0
UAnCTL0	UAnPWR	UAnTXE	UAnRXE	UAnDIR	UAnPS1	UAnPS0	UAnCL	UAnSL

UAnPWR	UARTAn operation control
0	Disable UARTAn operation (UARTAn reset asynchronously)
1	Enable UARTAn operation
The UARTAn operation is controlled by the UAnPWR bit. The TXDAn pin output is fixed to high level by clearing the UAnPWR bit to 0 (fixed to low level if UAnOPT0.UAnTDL bit = 1).	

UAnTXE	Transmission operation enable
0	Disable transmission operation
1	Enable transmission operation
• To start transmission, set the UAnPWR bit to 1 and then set the UAnTXE bit to 1. To stop transmission, clear the UAnTXE bit to 0 and then UAnPWR bit to 0. • To initialize the transmission unit, clear the UAnTXE bit to 0, wait for two cycles of the base clock, and then set the UAnTXE bit to 1 again. Otherwise, initialization may not be executed (for the base clock, see **15.7 (1) (a) Base clock**). • When UARTAn operation is enabled (UAnPWR bit = 1) and the UAnTXE bit is set to 1, transmission is enabled after at least two cycles of the base clock (f_{UCLK}) have elapsed.	

UAnRXE	Reception operation enable
0	Disable reception operation
1	Enable reception operation
• To start reception, set the UAnPWR bit to 1 and then set the UAnRXE bit to 1. To stop reception, clear the UAnRXE bit to 0 and then UAnPWR bit to 0. • To initialize the reception unit, clear the UAnRXE bit to 0, wait for two cycles of the base clock, and then set the UAnRXE bit to 1 again. Otherwise, initialization may not be executed (for the base clock, see **15.7 (1) (a) Base clock**). • When UARTAn operation is enabled (UAnPWR bit = 1) and the UAnRXE bit is set to 1, reception is enabled after at least two cycles of the base clock (f_{UCLK}) have elapsed. If a start bit is received before reception is enabled, the start bit is ignored.	

15.6 Operation

15.6.1 Data format

As shown in Figure 15-5, one frame of transmit/receive data consists of a start bit, character bits, parity bit, and stop bit(s).

Specification of the character bit length within 1 data frame, parity selection, specification of the stop bit length, and specification of MSB-first/LSB-first transfer are performed using the UAnCTL0 register.

The UAnOPT0.UAnTDL bit is used to specify normal output/inverted output for the data to be transferred via the TXDAn pin.

The UAnOPT0.UAnRDL bit is used to specify normal input/inverted input for the data to be received via the RXDAn pin.

- Start bit ..... 1 bit
- Character bits ..... 7 bits/8 bits
- Parity bit ..... Even parity/odd parity/0 parity/no parity
- Stop bit ..... 1 bit/2 bits
- Input logic ..... Normal input/inverted input
- Output logic ..... Normal output/inverted output
- Communication direction ..... MSB/LSB

15.6.2 UART transmission

Transmission is enabled by setting the UAnCTL0.UAnPWR and UAnCTL0.UAnTXE bits to 1, and transmission is started by writing transmit data to the UAnTX register. The start bit, parity bit, and stop bit are automatically added.

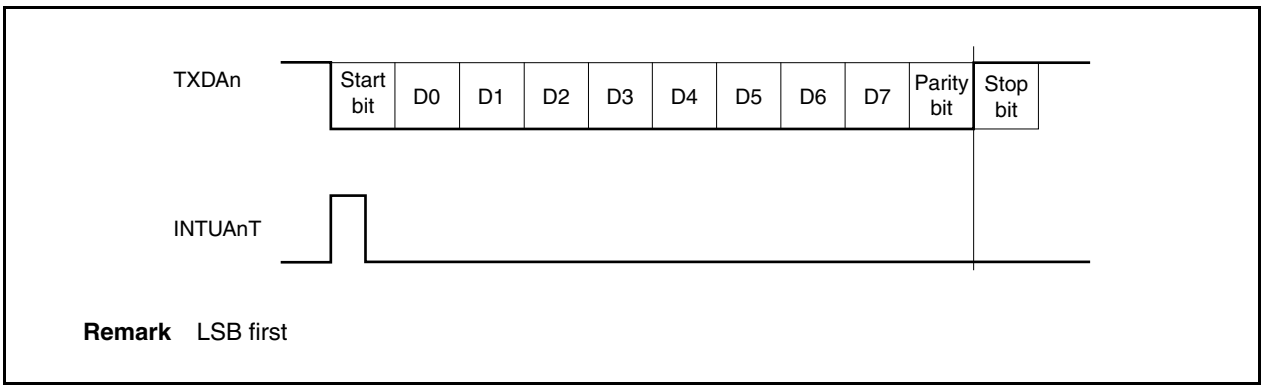
Since the CTS (transmit enable signal) input pin is not provided in UARTAn, use a port to check that reception is enabled at the transmit destination.

The data in the UAnTX register is transferred to the UARTAn transmit shift register upon the start of transmission.

A transmission enable interrupt request signal (INTUAnT) is generated upon completion of transmission of the data of the UAnTX register to the UARTAn transmit shift register, and the contents of the UARTAn transmit shift register are output to the TXDAn pin.

Writing the next transmit data to the UAnTX register is enabled after the INTUAnT signal is generated.

Figure 15-6. UART Transmission



Remark LSB first

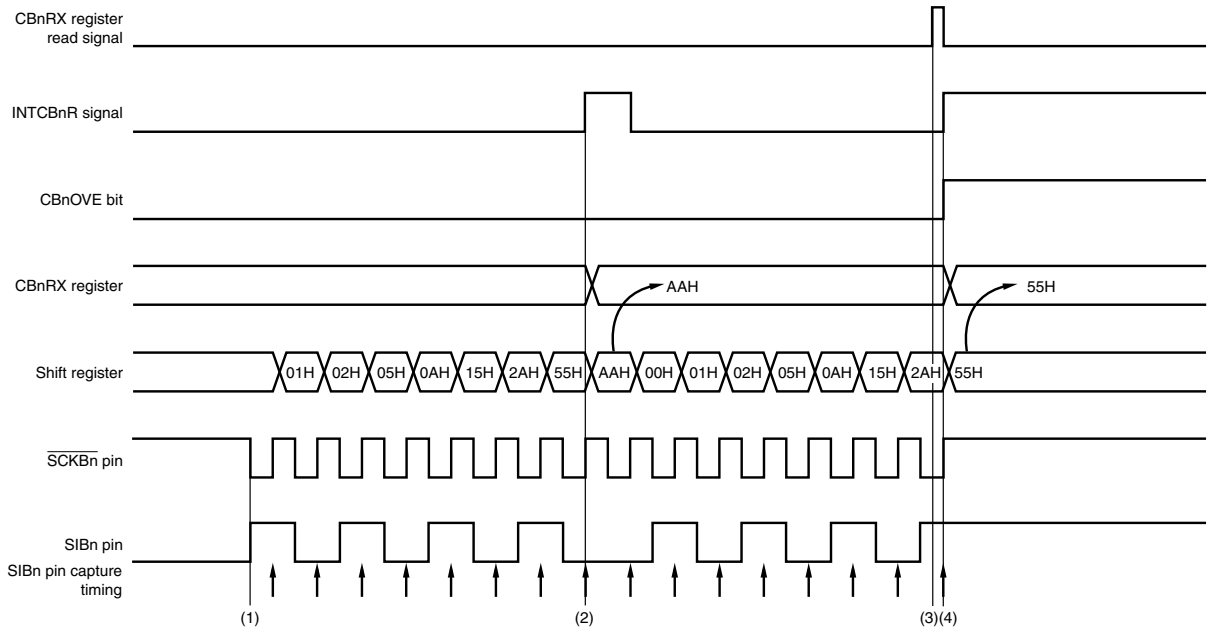
16.6.13 Reception errors

When transfer is performed with reception enabled (CBnCTL0.CBnRXE bit = 1) in the continuous transfer mode, the reception complete interrupt request signal (INTCBnR) is generated again if the next receive operation is completed before the CBnRX register is read after the INTCBnR signal is generated, and the overrun error flag (CBnSTR.CBnOVE) is set to 1.

If an overrun error occurs, the previous receive data is lost because the CBnRX register is updated. Even if a reception error occurs, the INTCBnR signal is generated again upon completion of the next reception if the CBnRX register is not read.

An overrun error occurs if reading the CBnRX register has not been completed half a clock cycle before the last bit of the next receive data is sampled after the INTCBnR signal is generated.

Figure 16-29. Overrun Error Timing



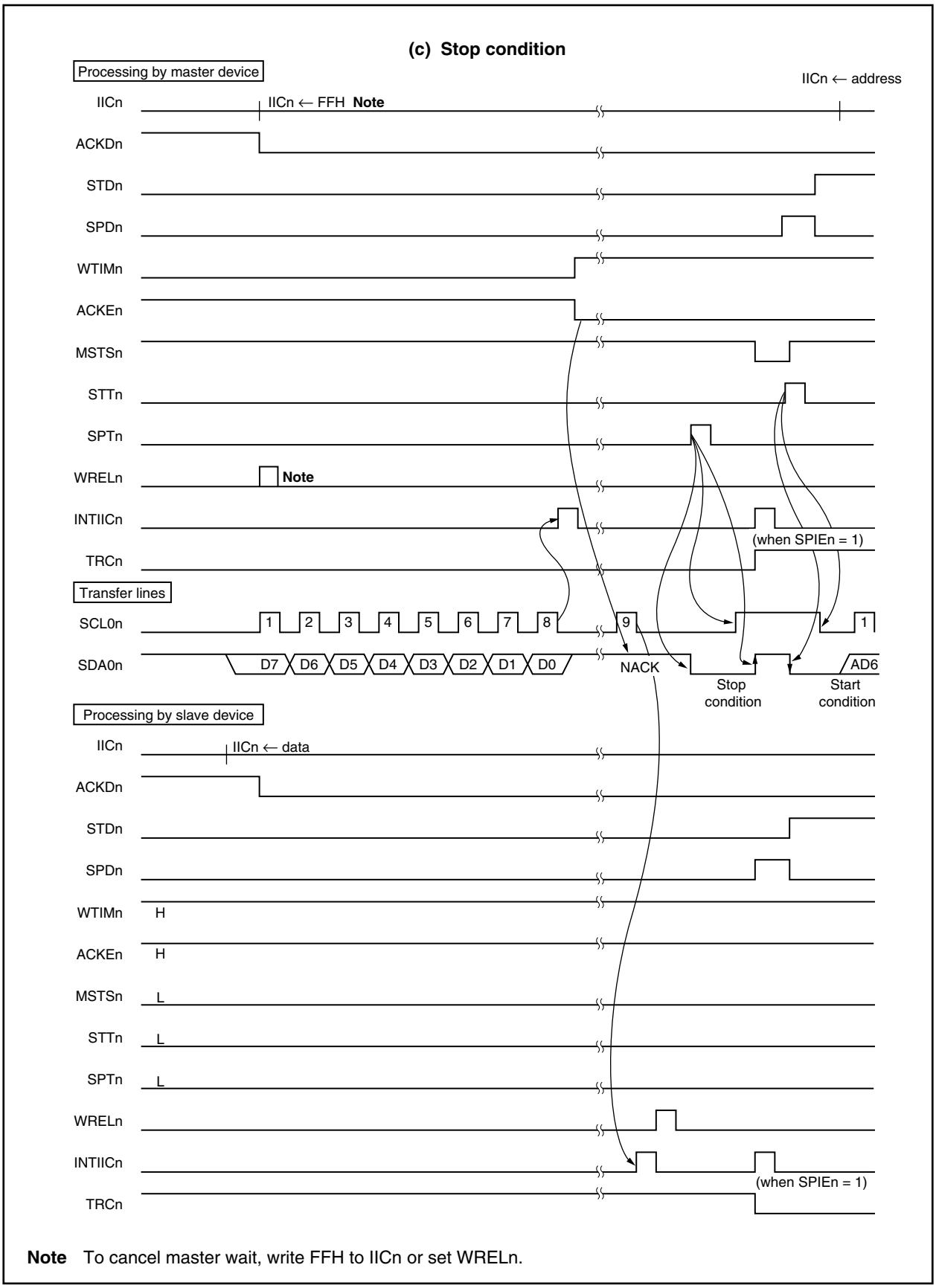
(1) Start of continuous transfer

(2) Completion of the first transfer

(3) The CBnRX register cannot be read until half a clock cycle before the completion of the second transfer.

(4) An overrun error occurs, the reception complete interrupt request signal (INTCBnR) is generated, and the overrun error flag (CBnSTR.CBnOVE) is set to 1. The receive data is overwritten.

Figure 17-24. Example of Slave to Master Communication
(When Wait Is Changed from 8 Clocks to 9 Clocks for Master and 9-Clock Wait Is Selected for Slave) (3/3)



Note To cancel master wait, write FFH to IICn or set WRELn.

18.8 Time Related to DMA Transfer

The time required to respond to a DMA request, and the minimum number of clocks required for DMA transfer are shown below.

Single transfer: DMA response time (<1>) + Transfer source memory access (<2>) + 1[Note 1] + Transfer destination memory access (<2>)

Table 18-4. Number of Execution Clocks During DMA Cycle

DMA Cycle		Number of Execution Clocks
<1> DMA request response time		4 clocks (MIN.) + Noise elimination time[Note 2]
<2> Memory access	Internal RAM access	2 clocks
	Peripheral I/O register access	3 clocks + Number of wait cycles specified by VSWC register[Note 3]

Notes 1. One clock is always inserted between a read cycle and a write cycle in DMA transfer.

2. If an external interrupt (INTPn) is specified as the trigger to start DMA transfer, noise elimination time is added (n = 0 to 7).

3. More wait cycles may be necessary for accessing a special register described in **3.4.9 (1)**.

(2) Restoration

Execution is returned from a debug trap by using the DBRET instruction.

When the DBRET instruction is executed, the CPU performs the following processing and transfers control to the address of the restored PC.

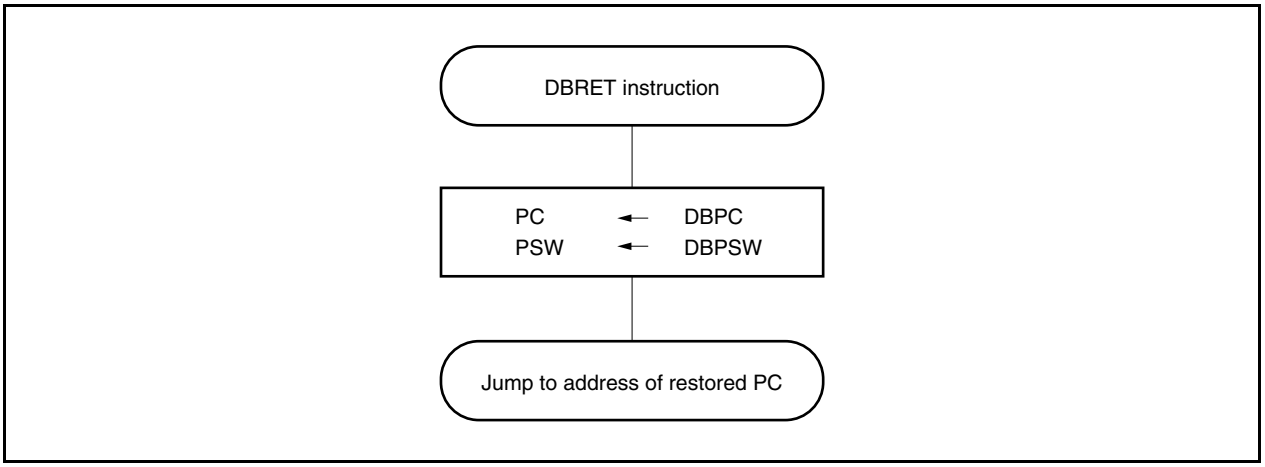
<1> Loads the saved PC and PSW from DBPC and DBPSW.

<2> Transfers control back to address of the restored PC and PSW.

Caution DBPC and DBPSW can be accessed only during the interval between the execution of the DBTRAP instruction and the DBRET instruction.

The processing for returning from a debug trap is shown below.

Figure 19-14. Returning from Debug Trap



(4) Regulator protection register (REGPR)

The REGPR register is used to protect the regulator output voltage level control register 0 (REGOVL0) so that illegal data is not written to REGOVL0. Data cannot be written to the REGOVL0 register unless enabling data (C9H) is written to the REGPR register. Only two types of data, C9H (enabling data) and 00H (protection data), can be written to the REGPR register. Writing any other value is prohibited. (If a value other than C9H or 00H is written to the REGPR register, the written value is set to prohibit a write access to the REGOVL0 register, but the operation is not guaranteed.)

This register can be read or written only in 8-bit units (accessing it in 1-bit units is prohibited).

Reset sets this register to 00H (protection data status).

After reset: 00H R/W Address: FFFFF331H

	7	6	5	4	3	2	1	0
REGPR	PR7	PR6	PR5	PR4	PR3	PR2	PR1	PR0

- **Protection data status: REGPR = 00H**

  In this status, the REGOVL0 register is protected from an illegal write access. In the protection data status, a value is not written to the REGOVL0 register even if an attempt is made to write it, and the REGOVL0 register holds the previous value.

  Be sure to set REGPR to 00H, except when changing the value of the REGOVL0 register, in order to avoid unexpected malfunction.

- **Enabling data status: REGPR = C9H**

  In this status, a write access to the REGOVL0 register is enabled.

  - Transition from normal mode → low-voltage STOP mode

    See **21.6.1 Setting and operation status.**
  - Transition of subclock operation mode → low-voltage subclock operation mode

    See **21.7.1 Setting and operation status.**
  - Transition of subclock operation mode → low-voltage sub-IDLE mode

    See **21.8.1 Setting and operation status.**

CHAPTER 31 ELECTRICAL SPECIFICATIONS (V850ES/JC3-L (48-pin))

31.1 Absolute Maximum Ratings

Absolute Maximum Ratings (T_A = 25°C) (1/2)

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{DD}	$V_{DD} = EV_{DD} = AV_{REF0} = AV_{REF1}$	−0.5 to +4.6	V
	EV_{DD}	$V_{DD} = EV_{DD} = AV_{REF0} = AV_{REF1}$	−0.5 to +4.6	V
	AV_{REF0}	$V_{DD} = EV_{DD} = AV_{REF0} = AV_{REF1}$	−0.5 to +4.6	V
	AV_{REF1}	$V_{DD} = EV_{DD} = AV_{REF0} = AV_{REF1}$	−0.5 to +4.6	V
	V_{SS}	$V_{SS} = EV_{SS} = AV_{SS}$	−0.5 to +0.5	V
	AV_{SS}	$V_{SS} = EV_{SS} = AV_{SS}$	−0.5 to +0.5	V
	EV_{SS}	$V_{SS} = EV_{SS} = AV_{SS}$	−0.5 to +0.5	V
Input voltage	V_{I1}	P97 to P99, P914, P915, PCM0, PDL5, $\overline{\text{RESET}}$, FLMD0	−0.5 to EV_{DD} + 0.5 Note 1	V
	V_{I2}	P10	−0.5 to AV_{REF1} + 0.5 Note 1	V
	V_{I3}	X1	−0.5 to V_{DD} + 0.5 Note 1	V
		X2	−0.5 to V_{RO} Note 2 + 0.5 Note 1	
	V_{I4}	P02, P03, P05, P30 to P32, P38, P39, P40 to P42, P50 to P55, P90, P91, P96	−0.5 to +6.0	V
	V_{I5}	XT1, XT2	−0.5 to V_{RO} Note 2 + 0.5	V
Analog input voltage	V_{IAN}	P70 to P75	−0.5 to AV_{REF0} + 0.5 Note 1	V

Notes 1. Be sure not to exceed the absolute maximum ratings (MAX. value) of each supply voltage.

2. On-chip regulator output voltage

Cautions 1. Do not directly connect the output (or I/O) pins of IC products to each other, or to V_{DD}, V_{CC}, and GND. Open-drain pins or open-collector pins, however, can be directly connected to each other. Direct connection of the output pins between an IC product and an external circuit is possible, if the output pins can be set to the high-impedance state and the output timing of the external circuit is designed to avoid output conflict.

2. Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

The ratings and conditions indicated for DC characteristics, AC characteristics, and operating conditions represent the quality assurance range during normal operation.

Remark Unless specified otherwise, the ratings of alternate-function pins are the same as those of port pins.

CHAPTER 33 RECOMMENDED SOLDERING CONDITIONS

The V850ES/JC3-L should be soldered and mounted under the following recommended conditions.
For technical information, see the following website.

Semiconductor Device Mount Manual (http://www.renesas.com/prod/package/manual/)

Table 33-1. Surface Mounting Type Soldering Conditions (1/2)

(1) μPD70F3797K8-4B4-AX: 40-pin plastic WQFN (6 × 6)
μPD70F3798K8-4B4-AX: 40-pin plastic WQFN (6 × 6)
μPD70F3799K8-4B4-AX: 40-pin plastic WQFN (6 × 6)
μPD70F3800K8-4B4-AX: 40-pin plastic WQFN (6 × 6)
μPD70F3838K8-4B4-AX: 40-pin plastic WQFN (6 × 6)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 260°C, Time: 60 seconds max. (at 220°C or higher), Count: Three times or less, Exposure limit: 7 days[Note] (after that, prebake at 125°C for 10 to 72 hours)	IR60-107-3

Note After opening the dry pack, store it at 25°C or less and 65% RH or less for the allowable storage period.

Caution Do not use different soldering methods together (except for partial heating).

Remarks 1. The V850ES/JC3-L is a lead-free product.
2. For soldering methods and conditions other than those recommended above, please contact a Renesas Electronics sales representative.

(2) μPD70F3801GA-GAM-AX: 48-pin plastic LQFP (fine pitch) (7 × 7)
μPD70F3802GA-GAM-AX: 48-pin plastic LQFP (fine pitch) (7 × 7)
μPD70F3803GA-GAM-AX: 48-pin plastic LQFP (fine pitch) (7 × 7)
μPD70F3804GA-GAM-AX: 48-pin plastic LQFP (fine pitch) (7 × 7)
μPD70F3839GA-GAM-AX: 48-pin plastic LQFP (fine pitch) (7 × 7)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 260°C, Time: 60 seconds max. (at 220°C or higher), Count: Three times or less, Exposure limit: 7 days[Note] (after that, prebake at 125°C for 10 to 72 hours)	IR60-107-3
Partial heating	Pin temperature: 350°C max., Time: 3 seconds max. (per pin row)	–

Note After opening the dry pack, store it at 25°C or less and 65% RH or less for the allowable storage period.

Caution Do not use different soldering methods together (except for partial heating).

Remarks 1. The V850ES/JC3-L is a lead-free product.
2. For soldering methods and conditions other than those recommended above, please contact a Renesas Electronics sales representative.

(6/6)

Mnemonic	Operand	Opcode	Operation	Execution Clock			Flags				
				i	r	l	CY	OV	S	Z	SAT
SUB	reg1,reg2	rrrrr001101RRRRR	GR[reg2]←GR[reg2]–GR[reg1]	1	1	1	×	×	×	×	
SUBR	reg1,reg2	rrrrr001100RRRRR	GR[reg2]←GR[reg1]–GR[reg2]	1	1	1	×	×	×	×	
SWITCH	reg1	00000000010RRRRR	adr←(PC+2) + (GR [reg1] logically shift left by 1) PC←(PC+2) + (sign-extend (Load-memory (adr,Halfword)) logically shift left by 1	5	5	5					
SXB	reg1	00000000101RRRRR	GR[reg1]←sign-extend (GR[reg1] (7 : 0))	1	1	1					
SXH	reg1	00000000111RRRRR	GR[reg1]←sign-extend (GR[reg1] (15 : 0))	1	1	1					
TRAP	vector	0000011111iiiii 0000000100000000	EIPC ←PC+4 (Restored PC) EIPSW ←PSW ECR.EICC ←Interrupt code PSW.EP ←1 PSW.ID ←1 PC ←00000040H (when vector is 00H to 0FH) 00000050H (when vector is 10H to 1FH)	3	3	3					
TST	reg1,reg2	rrrrr001011RRRRR	result←GR[reg2] AND GR[reg1]	1	1	1		0	×	×	
TST1	bit#3,disp16[reg1]	11bbb111110RRRRR ddddddddddddddd	adr←GR[reg1]+sign-extend(disp16) Z flag←Not (Load-memory-bit (adr,bit#3))	3 Note 3	3 Note 3	3 Note 3				×	
	reg2, [reg1]	rrrrr111111RRRRR 0000000011100110	adr←GR[reg1] Z flag←Not (Load-memory-bit (adr,reg2))	3 Note 3	3 Note 3	3 Note 3				×	
XOR	reg1,reg2	rrrrr001001RRRRR	GR[reg2]←GR[reg2] XOR GR[reg1]	1	1	1		0	×	×	
XORI	imm16,reg1,reg2	rrrrr110101RRRRR iiiiiiiiiiiiiiii	GR[reg2]←GR[reg1] XOR zero-extend (imm16)	1	1	1		0	×	×	
ZXB	reg1	00000000100RRRRR	GR[reg1]←zero-extend (GR[reg1] (7 : 0))	1	1	1					
ZXH	reg1	00000000110RRRRR	GR[reg1]←zero-extend (GR[reg1] (15 : 0))	1	1	1					

Notes 1. ddddddddd: Higher 8 bits of disp9.

2. 3 if there is an instruction that rewrites the contents of the PSW immediately before.

3. If there is no wait state (3 + the number of read access wait states).

4. n is the total number of list12 load registers. (According to the number of wait states. Also, if there are no wait states, n is the total number of list12 registers. If n = 0, same operation as when n = 1)

5. RRRRR: other than 00000.

6. The lower halfword data only are valid.

7. ddddddddddddddddddddd: The higher 21 bits of disp22.

8. ddddddddddddddd: The higher 15 bits of disp16.

9. According to the number of wait states (1 if there are no wait states).

10. b: bit 0 of disp16.

11. According to the number of wait states (2 if there are no wait states).