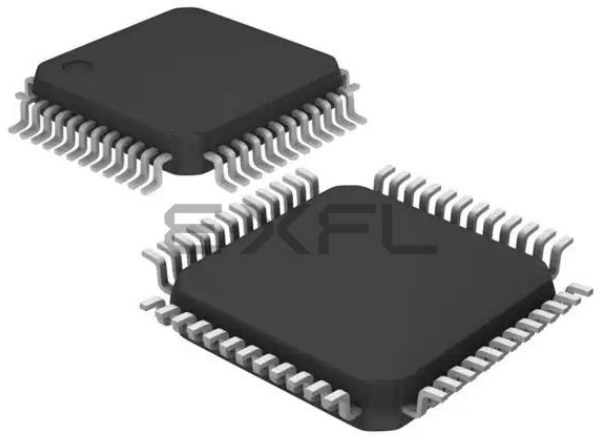
Renesas Electronics America Inc - UPD70F3803GA-GAM-AX Datasheet



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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	V850ES
Core Size	32-Bit Single-Core
Speed	20MHz
Connectivity	CSI, EBI/EMI, I²C, UART/USART
Peripherals	DMA, LVD, PWM, WDT
Number of I/O	34
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 3.6V
Data Converters	A/D 6x10b; D/A 1x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd70f3803ga-gam-ax

Conventions

Data significance:	Higher digits on the left and lower digits on the right
Active low representation:	$\overline{xxx}$ (overscore over pin or signal name)
Memory map address:	Higher addresses on the top and lower addresses on the bottom
Note:	Footnote for item marked with **Note** in the text
Caution:	Information requiring particular attention
Remark:	Supplementary information
Numeric representation:	Binary ... xxxx or xxxxB
	Decimal ... xxxx
	Hexadecimal ... xxxxH

Prefix indicating power of 2 (address space, memory capacity):

K (kilo): $2^{10} = 1,024$

M (mega): $2^{20} = 1,024^2$

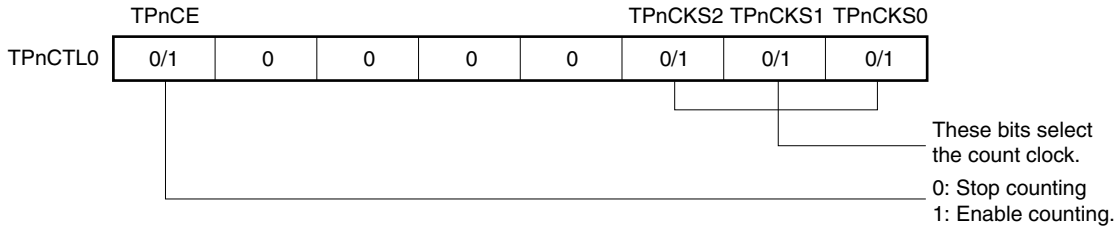
G (giga): $2^{30} = 1,024^3$

(6/10)

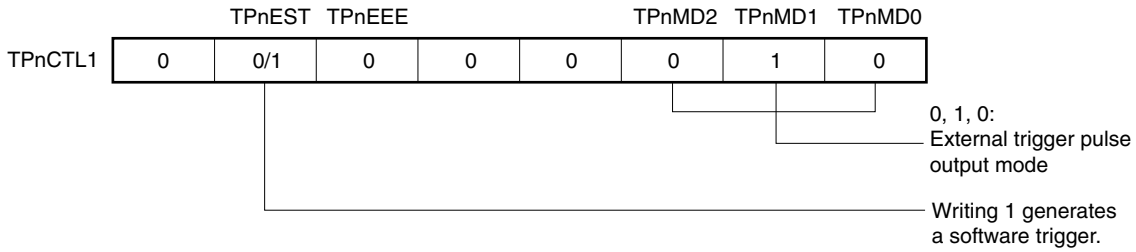
Address	Function Register Name	Symbol	R/W	Manipulatable Bits			Default Value
				1	8	16	
FFFFF590H	TMP0 control register 0	TP0CTL0	R/W	√	√		00H
FFFFF591H	TMP0 control register 1	TP0CTL1		√	√		00H
FFFFF592H	TMP0 I/O control register 0	TP0IOC0		√	√		00H
FFFFF593H	TMP0 I/O control register 1	TP0IOC1		√	√		00H
FFFFF594H	TMP0 I/O control register 2	TP0IOC2		√	√		00H
FFFFF595H	TMP0 option register 0	TP0OPT0		√	√		00H
FFFFF596H	TMP0 capture/compare register 0	TP0CCR0				√	0000H
FFFFF598H	TMP0 capture/compare register 1	TP0CCR1				√	0000H
FFFFF59AH	TMP0 counter read buffer register	TP0CNT	R			√	0000H
FFFFF5A0H	TMP1 control register 0	TP1CTL0	R/W	√	√		00H
FFFFF5A1H	TMP1 control register 1	TP1CTL1		√	√		00H
FFFFF5A2H	TMP1 I/O control register 0	TP1IOC0		√	√		00H
FFFFF5A3H	TMP1 I/O control register 1	TP1IOC1		√	√		00H
FFFFF5A4H	TMP1 I/O control register 2	TP1IOC2		√	√		00H
FFFFF5A5H	TMP1 option register 0	TP1OPT0		√	√		00H
FFFFF5A6H	TMP1 capture/compare register 0	TP1CCR0				√	0000H
FFFFF5A8H	TMP1 capture/compare register 1	TP1CCR1				√	0000H
FFFFF5AAH	TMP1 counter read buffer register	TP1CNT	R			√	0000H
FFFFF5B0H	TMP2 control register 0	TP2CTL0	R/W	√	√		00H
FFFFF5B1H	TMP2 control register 1	TP2CTL1		√	√		00H
FFFFF5B2H	TMP2 I/O control register 0	TP2IOC0		√	√		00H
FFFFF5B3H	TMP2 I/O control register 1	TP2IOC1		√	√		00H
FFFFF5B4H	TMP2 I/O control register 2	TP2IOC2		√	√		00H
FFFFF5B5H	TMP2 option register 0	TP2OPT0		√	√		00H
FFFFF5B6H	TMP2 capture/compare register 0	TP2CCR0				√	0000H
FFFFF5B8H	TMP2 capture/compare register 1	TP2CCR1				√	0000H
FFFFF5BAH	TMP2 counter read buffer register	TP2CNT	R			√	0000H
FFFFF5C0H	TMP3 control register 0	TP3CTL0	R/W	√	√		00H
FFFFF5C1H	TMP3 control register 1	TP3CTL1		√	√		00H
FFFFF5C2H	TMP3 I/O control register 0	TP3IOC0		√	√		00H
FFFFF5C3H	TMP3 I/O control register 1	TP3IOC1		√	√		00H
FFFFF5C5H	TMP3 option register 0	TP3OPT0		√	√		00H
FFFFF5C6H	TMP3 capture/compare register 0	TP3CCR0				√	0000H
FFFFF5C8H	TMP3 capture/compare register 1	TP3CCR1				√	0000H
FFFFF5CAH	TMP3 counter read buffer register	TP3CNT	R			√	0000H
FFFFF5D0H	TMP4 control register 0	TP4CTL0	R/W	√	√		00H
FFFFF5D1H	TMP4 control register 1	TP4CTL1		√	√		00H
FFFFF5D2H	TMP4 I/O control register 0	TP4IOC0		√	√		00H
FFFFF5D3H	TMP4 I/O control register 1	TP4IOC1		√	√		00H
FFFFF5D4H	TMP4 I/O control register 2	TP4IOC2		√	√		00H
FFFFF5D5H	TMP4 option register 0	TP4OPT0		√	√		00H

Figure 6-28. Register Settings in External Trigger Pulse Output Mode (1/2)

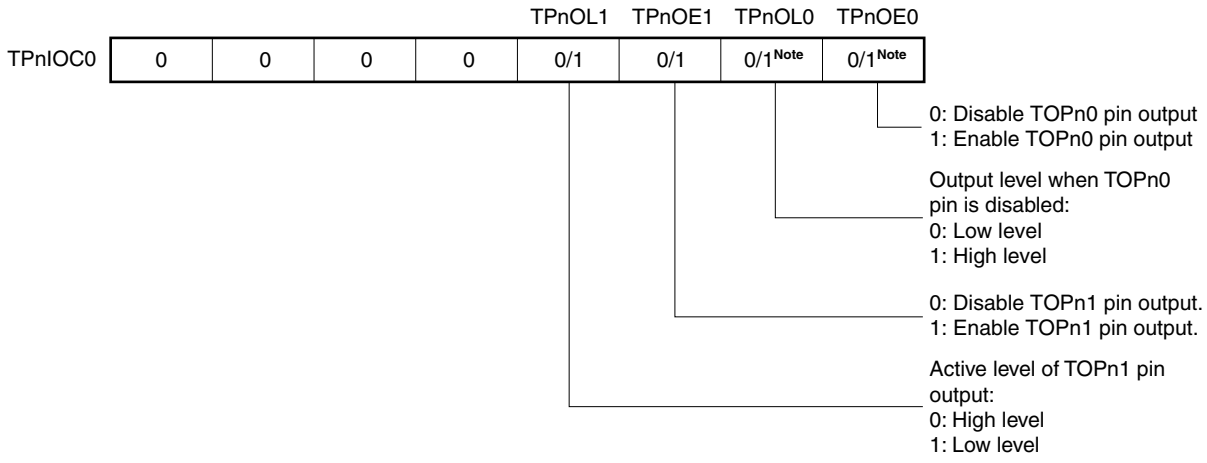
(a) TMPn control register 0 (TPnCTL0)



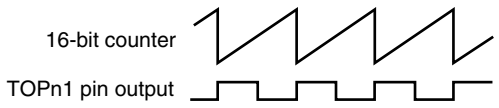
(b) TMPn control register 1 (TPnCTL1)



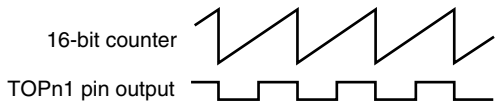
(c) TMPn I/O control register 0 (TPnIOC0)



- When TPnOL1 bit is 0:



- When TPnOL1 bit is 1:

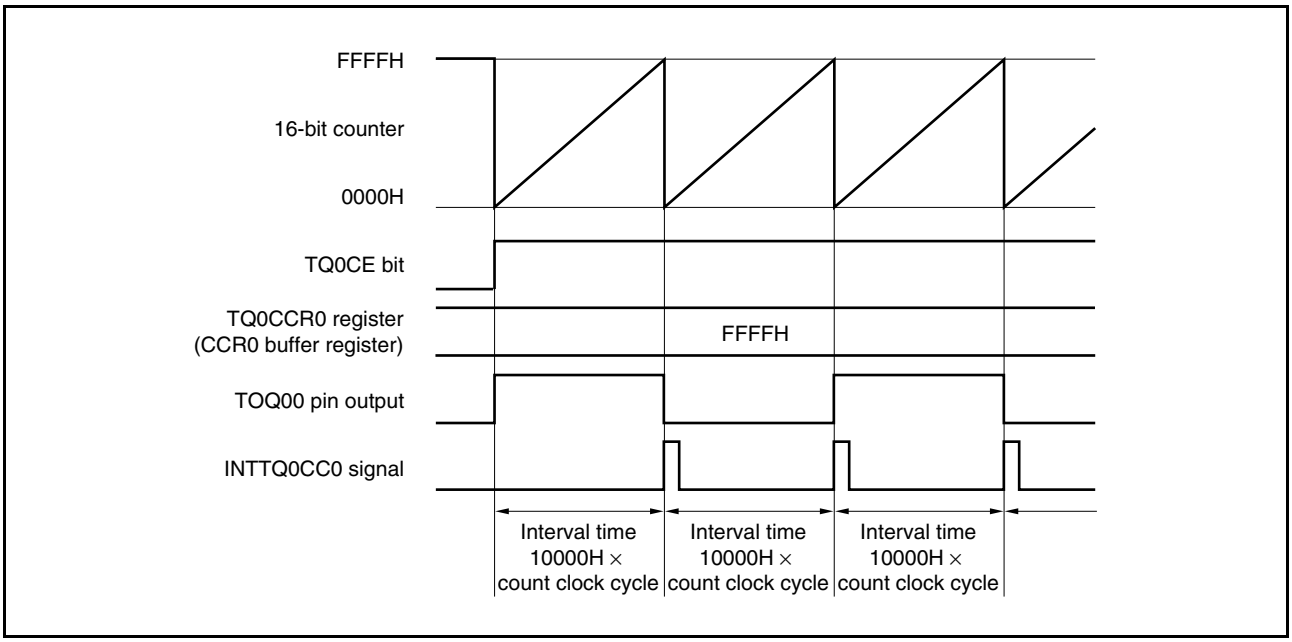


Note Set this bit to 0 when not using the TOPn0 pin in external trigger pulse output mode.

(b) Operation when TQ0CCR0 register is set to FFFFH

When the TQ0CCR0 register is set to FFFFH, the 16-bit counter increments up to FFFFH and is reset to 0000H in synchronization with the next increment timing. The INTTQ0CC0 signal is then generated and the output of the TOQ00 pin is inverted. At this time, an overflow interrupt request signal (INTTQ0OV) is not generated, nor is the overflow flag (TQ0OPT0.TQ0OVF bit) set to 1.

Figure 7-11. Operation of Interval Timer When TQ0CCR0 Register Is Set to FFFFH



If the value of the TQ0CCRk register is greater than the value of the TQ0CCR0 register, the value of the 16-bit counter will not match the value of the TQ0CCRk register. Consequently, the INTTQ0CCk signal is not generated, nor is the output of the TOQ0k pin changed.

A chart showing the timing of operations when the value of the TQ0CCRk register (D_{k1}) is greater than the value of the TQ0CCR0 register (D_{01}) is shown below.

Remark k = 1 to 3

Figure 7-15. Timing of Operations When $D_{01} < D_{k1}$

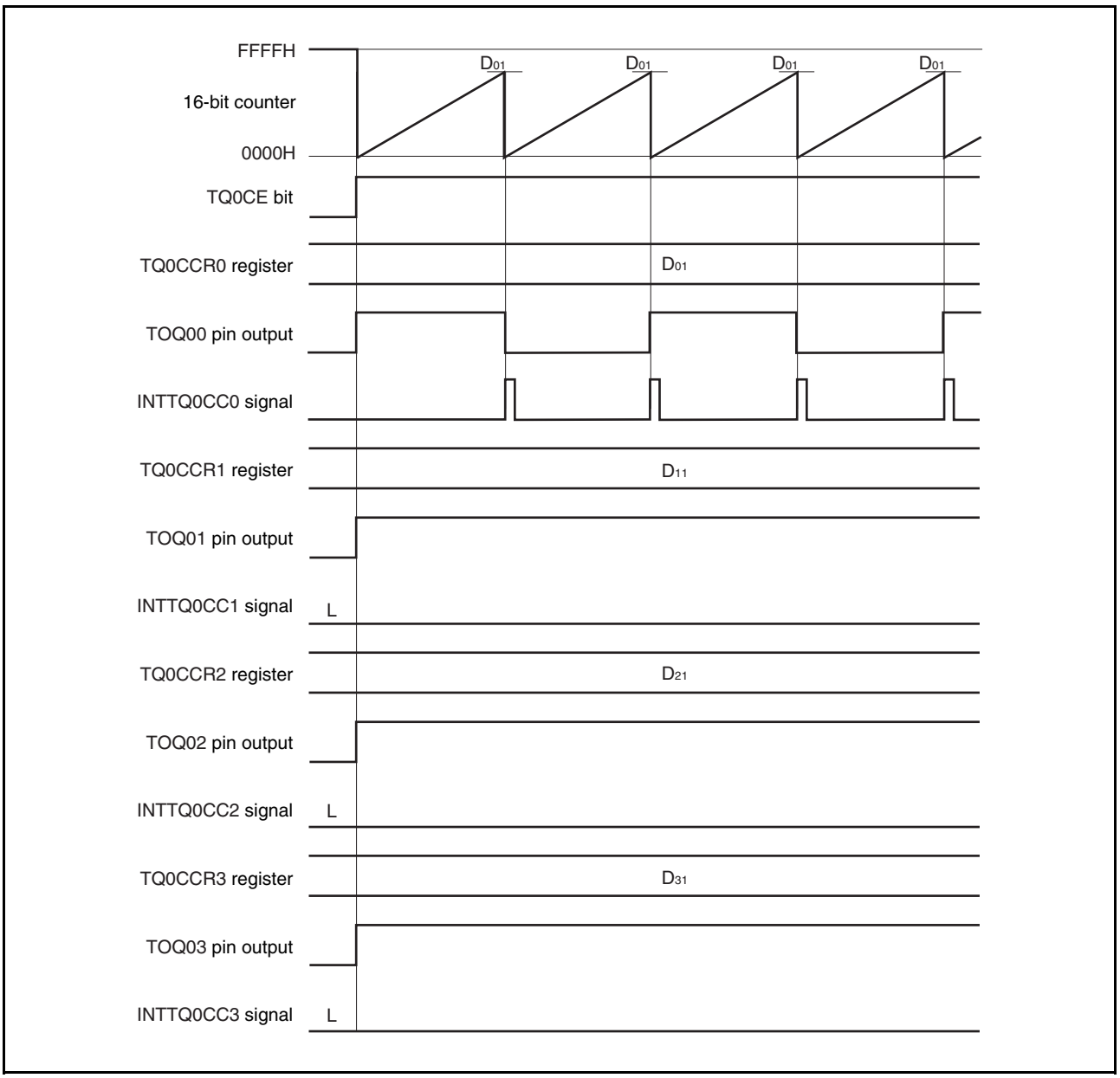
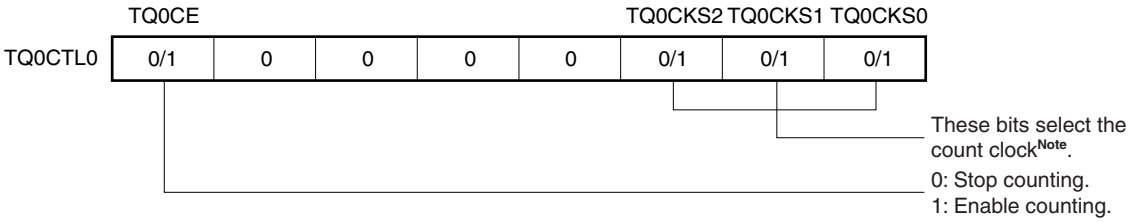


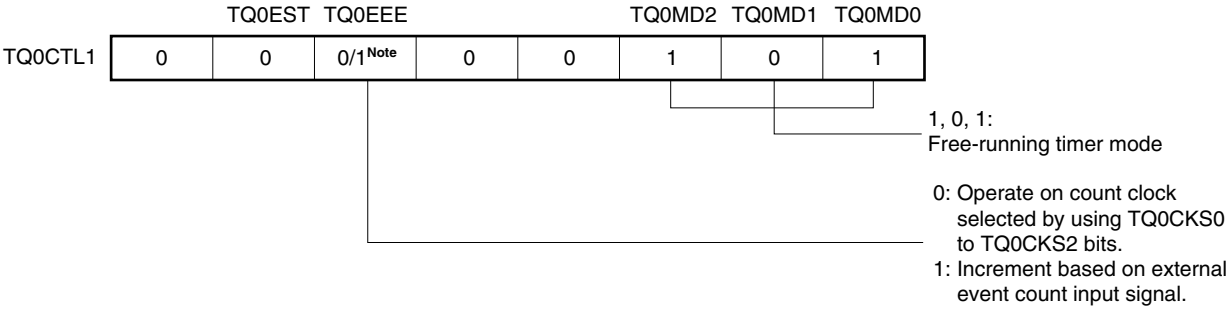
Figure 7-55. Register Settings in Free-Running Timer Mode (1/3)

(a) TMQ0 control register 0 (TQ0CTL0)



Note The setting of these bits is invalid when the TQ0CTL1.TQ0EEE bit is 1.

(b) TMQ0 control register 1 (TQ0CTL1)

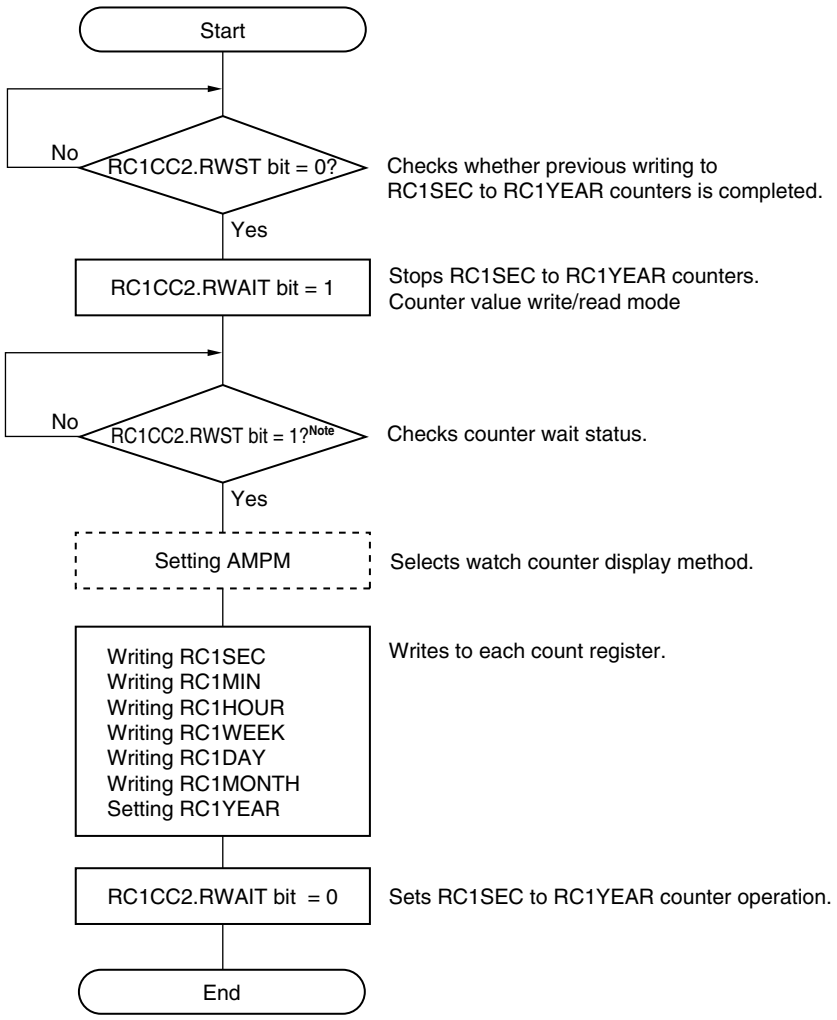


Note The TIQ00 pin cannot be used for capture operations when the TQ0CTL1.TQ0EEE bit is 1.

10.4.2 Rewriting each counter during real-time counter operation

Set as follows when rewriting each counter (RC1SEC, RC1MIN, RC1HOUR, RC1WEEK, RC1DAY, RC1MONTH, RC1YEAR) during real-time counter operation (RC1PWR = 1).

Figure 10-3. Rewriting Each Counter During Real-time Counter Operation



Note Be sure to confirm that RWST = 0 before setting STOP mode.

Caution Complete the series of operations for setting RWAIT to 1 to clearing RWAIT to 0 within 1 second.
If RWAIT = 1 is set, the operation of RC1SEC to RC1YEAR is stopped. If a carry occurs from RC1SUBC while RWAIT = 1, one carry can be internally retained. However, if two or more carries occur, the number of carries cannot be retained.

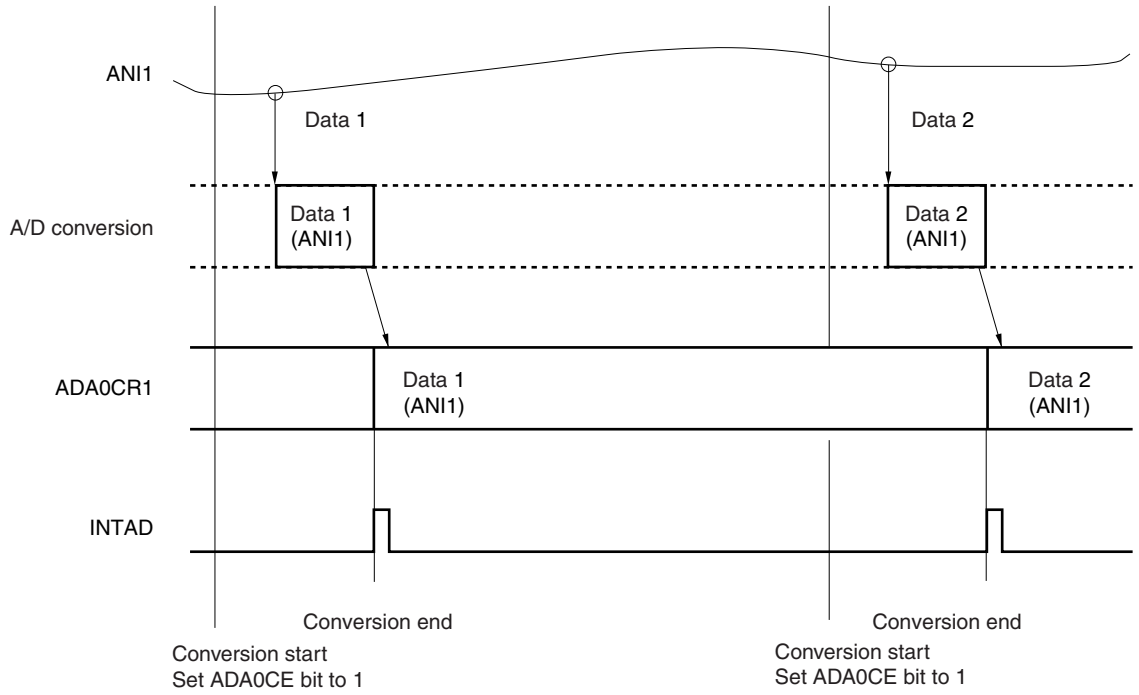
Remark RC1SEC, RC1MIN, RC1HOUR, RC1WEEK, RC1DAY, RC1MONTH, and RC1YEAR may berewrite in any sequence.
All the registers do not have to be set and only some registers may be read.

(3) One-shot select mode

In this mode, the voltage of the analog input pin specified by the ADA0S register is converted into a digital value only once.

The conversion result is stored in the ADA0CRn register corresponding to the analog input pin. In this mode, an analog input pin and an ADA0CRn register correspond on a one-to-one basis. When A/D conversion has been completed once, the INTAD signal is generated. A/D conversion is stopped after it has been completed.

Figure 13-6. Example of Timing in One-Shot Select Mode (ADA0S Register = 01H)



Remark The above timing applies to the software trigger mode (ADA0M0.AD0TMD bit = 0) or the high-speed conversion mode (ADA0M1.ADA0HS1 bit = 1).

(4) One-shot scan mode

In this mode, analog input pins are sequentially selected, from the ANI0 pin to the pin specified by the ADA0S register, and their values are converted into digital values .

Each conversion result is stored in the ADA0CRn register corresponding to the analog input pin. When conversion of the analog input pin specified by the ADA0S register is complete, the INTAD signal is generated. A/D conversion is stopped after it has been completed.

15.3.2 UARTA1 and I²C02 mode switching

In the V850ES/JC3-L (48-pin), V850ES/JE3-L, UARTA1 and I²C02 share pins and therefore cannot be used simultaneously. To use the UARTA1 function, specify the UARTA1 mode in advance by using the PMC9, PFC9, and PFCE9 registers.

Switching the operation mode between UARTA1 and I²C02 are described below.

Caution Transmission and reception by UARTA1 and I²C02 are not guaranteed if these operation modes are switched during transmission or reception. Be sure to stop the serial interface that is not being used.

Figure 15-3. Switching UARTA1 and I²C02 Operation Modes

After reset: 0000H R/W Address: FFFFF452H, FFFFF453H

PMC9

15	14	13	12	11	10	9	8
PMC915	PMC914	PMC913	PMC912	PMC911	PMC910	PMC99	PMC98

7	6	5	4	3	2	1	0
PMC97	PMC96	0	PMC94	PMC93	PMC92	PMC91	PMC90

After reset: 0000H R/W Address: FFFFF472H, FFFFF473H

PFC9

15	14	13	12	11	10	9	8
PFC915	PFC914	PFC913	PFC912	PFC911	PFC910	PFC99	PFC98

7	6	5	4	3	2	1	0
PFC97	PFC96	0	PFC94	PFC93	PFC92	PFC91	PFC90

After reset: 0000H R/W Address: FFFFF712H, FFFFF713H

PFCE9

15	14	13	12	11	10	9	8
PFCE915	PFCE914	0	0	0	0	0	0

7	6	5	4	3	2	1	0
PFCE97	PFCE96	0	PFCE94	PFCE93	PFCE92	PFCE91	PFCE90

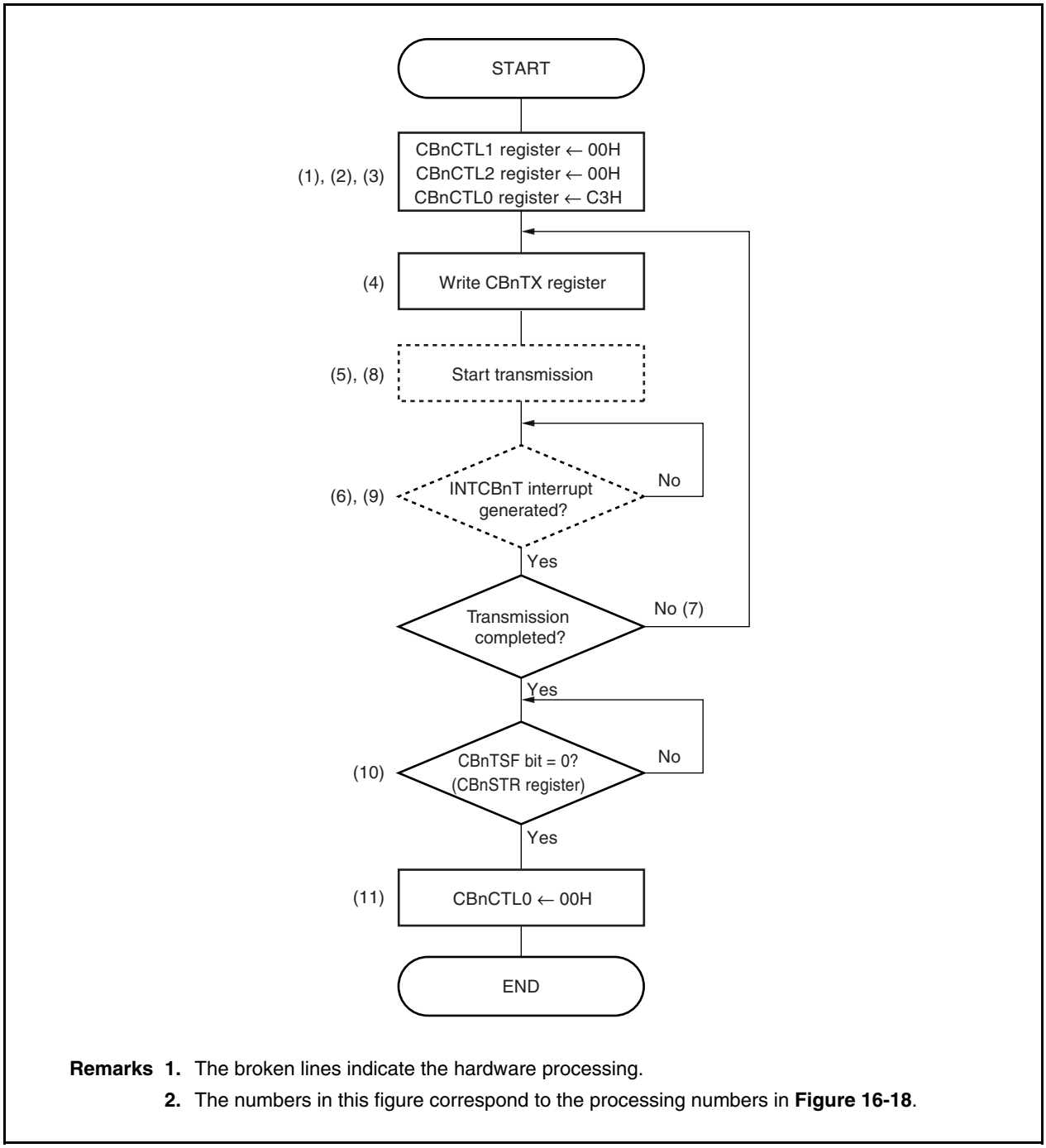
PMC9m	PFCE9m	PFC9m	Operation mode
1	1	0	UARTA1 mode
1	1	1	I²C02 mode

Remark m = 0, 1

16.6.7 Continuous transfer mode (master mode, transmission mode)

MSB first (CBnCTL0.CBnDIR bit = 0), communication type 1 (CBnCTL1.CBnCKP and CBnCTL1.CBnDAP bits = 00), communication clock (f_{CCLK}) = f_{XX}/2 (CBnCTL1.CBnCKS2 to CBnCTL1.CBnCKS0 bits = 000), transfer data length = 8 bits (CBnCTL2.CBnCL3 to CBnCTL2.CBnCL0 bits = 0000)

Figure 16-17. Continuous Transfer Mode Operation (Master Mode, Transmission Mode)



Remarks 1. The broken lines indicate the hardware processing.

2. The numbers in this figure correspond to the processing numbers in **Figure 16-18**.

(2) Start ~ Code ~ Data ~ Start ~ Address ~ Data ~ Stop

<1> When WTIMn bit = 0 (after restart, address match)

ST	AD6 to AD0	R/$\overline{W}$	$\overline{ACK}$	D7 to D0	$\overline{ACK}$	ST	AD6 to AD0	R/$\overline{W}$	$\overline{ACK}$	D7 to D0	$\overline{ACK}$	SP
			▲1		▲2					▲3	▲4	Δ5

▲1: IICSn register = 0010X010B

▲2: IICSn register = 0010X000B

▲3: IICSn register = 0001X110B

▲4: IICSn register = 0001X000B

Δ 5: IICSn register = 00000001B

Remark ▲:Always generated

Δ: Generated only when SPIEn bit = 1

X: don't care

<2> When WTIMn bit = 1 (after restart, address match)

ST	AD6 to AD0	R/$\overline{W}$	$\overline{ACK}$	D7 to D0	$\overline{ACK}$	ST	AD6 to AD0	R/$\overline{W}$	$\overline{ACK}$	D7 to D0	$\overline{ACK}$	SP
			▲1	▲2		▲3				▲4		▲5 Δ6

▲1: IICSn register = 0010X010B

▲2: IICSn register = 0010X110B

▲3: IICSn register = 0010XX00B

▲4: IICSn register = 0001X110B

▲5: IICSn register = 0001XX00B

Δ 6: IICSn register = 00000001B

Remark ▲: Always generated

Δ: Generated only when SPIEn bit = 1

X: don't care

19.4.3 EP flag

The EP flag is a status flag that indicates that exception processing is in progress. This flag is set when an exception occurs.

PSW

31 to 8	7	6	5	4	3	2	1	0
0	NP	**EP**	ID	SAT	CY	OV	S	Z

EP	Exception processing status
0	Exception processing not in progress (initial value).
1	Exception processing in progress.

CHAPTER 24 LOW-VOLTAGE DETECTOR (LVI)

24.1 Functions

The low-voltage detector (LVI) has the following functions.

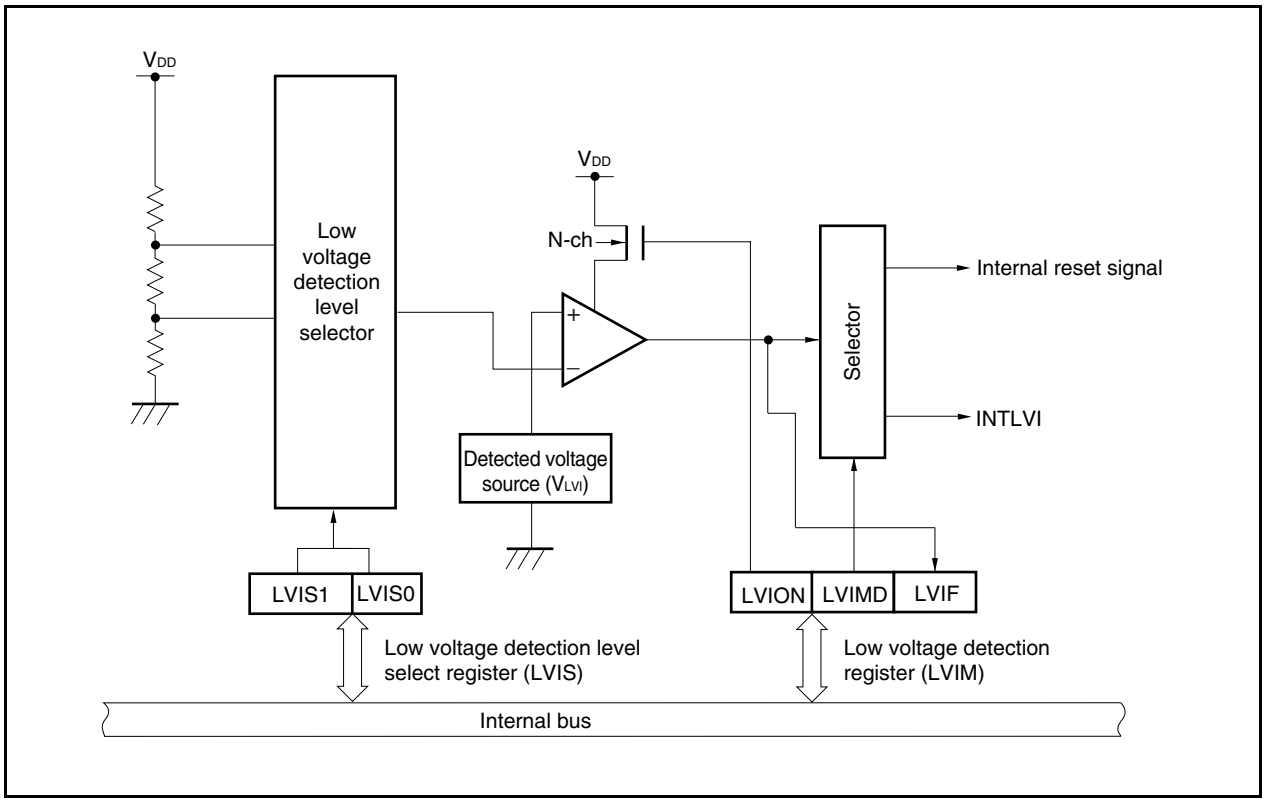
- If interrupt occurrence at low-voltage detection is selected as the operation mode, the low-voltage detector compares the supply voltage (V_{DD}) and the detection voltage (V_{LVI}), and generates an internal interrupt signal when the supply voltage drops below or rises above the detection voltage.
- If reset occurrence at low-voltage detection is selected as the operation mode, the low-voltage detector generates an internal reset signal when the supply voltage (V_{DD}) drops below the detection voltage (V_{LVI}).
- The level of the supply voltage to be detected can be changed by software.
- Interrupt or reset signal can be selected by software.
- The low-voltage detector is operable in the standby mode.

If a reset occurs when the low-voltage detector is selected to generate a reset signal, the RESF.LVIRF bit is set to 1. For details about the RESF register, see **22.3 Register to Check Reset Source**.

24.2 Configuration

The block diagram of the low-voltage detector is shown below.

Figure 24-1. Block Diagram of Low-Voltage Detector



Absolute Maximum Ratings (T_A = 25°C) (2/2)

Parameter	Symbol	Conditions		Ratings	Unit
Output current, low	I_{OL}	P02, P03, P05, P30, P31, P40 to P42, P50 to P55, P90, P91, P96, P97, P914, P915	Per pin	4	mA
			Total of all pins	50	mA
		PCM0, PDL5	Per pin	4	mA
			Total of all pins	8	mA
		P70 to P74	Per pin	4	mA
			Total of all pins	20	mA
Output current, high	I_{OH}	P02, P03, P05, P30, P31, P40 to P42, P50 to P55, P90, P91, P96, P97, P914, P915	Per pin	−4	mA
			Total of all pins	−50	mA
		PCM0, PDL5	Per pin	−4	mA
			Total of all pins	−8	mA
		P70 to P74	Per pin	−4	mA
			Total of all pins	−20	mA
Operating ambient temperature	T_A	Normal operation mode		−40 to +85	°C
		Flash memory programming mode		−40 to +85	°C
Storage temperature	T_{stg}			−40 to +125	°C

Cautions 1. Do not directly connect the output (or I/O) pins of IC products to each other, or to V_{DD}, V_{CC}, and GND. Open-drain pins or open-collector pins, however, can be directly connected to each other. Direct connection of the output pins between an IC product and an external circuit is possible, if the output pins can be set to the high-impedance state and the output timing of the external circuit is designed to avoid output conflict.

2. Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.
The ratings and conditions indicated for DC characteristics, AC characteristics, and operating conditions represent the quality assurance range during normal operation.

Remark Unless specified otherwise, the ratings of alternate-function pins are the same as those of port pins.

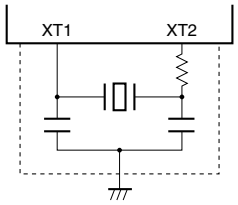
30.2 Capacitance

Capacitance (T_A = 25°C, V_{DD} = EV_{DD} = AV_{REF0} = V_{SS} = EV_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
I/O capacitance	C_{IO}	f_X = 1 MHz Unmeasured pins returned to 0 V			10	pF

30.4.2 Subclock oscillator characteristics

(T_A = –40 to +85°C, V_{DD} = EV_{DD} = AV_{REF0} = 2.2 to 3.6 V, V_{SS} = EV_{SS} = AV_{SS} = 0 V)

Resonator	Circuit Example	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Crystal resonator		Oscillation frequency (f_{XT})Note 1		32	32.768	35	kHz
		Oscillation stabilization timeNote 2				10	s

Notes 1. The oscillation frequency shown above indicates only oscillator characteristics. Use the V850ES/JC3-L (40-pin) so that the internal operation conditions do not exceed the ratings shown in **AC Characteristics**, **DC Characteristics**, and operating conditions.

2. Time required from when V_{DD} reaches the oscillation voltage range (2.2 V (MIN.)) to when the crystal resonator stabilizes.

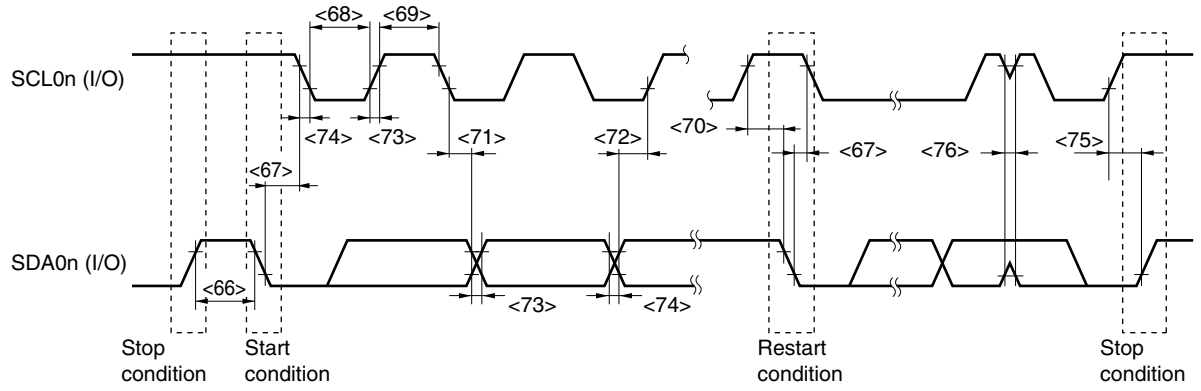
Cautions 1. When using the subclock oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as V_{SS}.**
- **Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

2. The subclock oscillator is designed as a low-amplitude circuit for reducing power consumption, and is more prone to malfunction due to noise than the main clock oscillator.
Particular care is therefore required with the wiring method when the subclock is used.

3. For the resonator selection and oscillator constant, customers are requested to either evaluate the oscillation themselves or apply to the resonator manufacturer for evaluation.

I²C Bus Timing



Remark n = 1, 2

30.8.7 A/D converter

(T_A = –40 to +85°C, V_{DD} = EV_{DD} = AV_{REF0}, 2.7 V ≤ AV_{REF0} ≤ 3.6 V, V_{SS} = EV_{SS} = AV_{SS} = 0 V, C_L = 50 pF)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution					10	bit
Overall error[Note]		2.7 V ≤ AV_{REF0} ≤ 3.6 V			±0.6	%FSR
A/D conversion time	t_{CONV}	3.0 V ≤ AV_{REF0} ≤ 3.6 V	2.6		24	μs
		2.7 V ≤ AV_{REF0} ≤ 3.0 V	3.9		24	μs
Zero scale error					±0.5	%FSR
Full scale error					±0.5	%FSR
Non-linearity error					±4.0	LSB
Differential linearity error					±4.0	LSB
Analog input voltage	V_{IAN}		AV_{SS}		AV_{REF0}	V
Reference voltage	AV_{REF0}		2.7		3.6	V
AV_{REF0} current	AI_{REF0}	Normal conversion mode		3	6.5	mA
		High-speed conversion mode		4	10	mA
		When A/D converter unused			5	μA

Note Excluding quantization error (±0.05 %FSR).

Caution Do not set (read/write) alternate-function ports during A/D conversion; otherwise the conversion resolution may be degraded.

Remark LSB: Least Significant Bit
FSR: Full Scale Range

(T_A = −40 to +85°C, V_{DD} = EV_{DD} = AV_{REF0} = AV_{REF1}, V_{SS} = EV_{SS} = AV_{SS} = 0 V) (2/2)

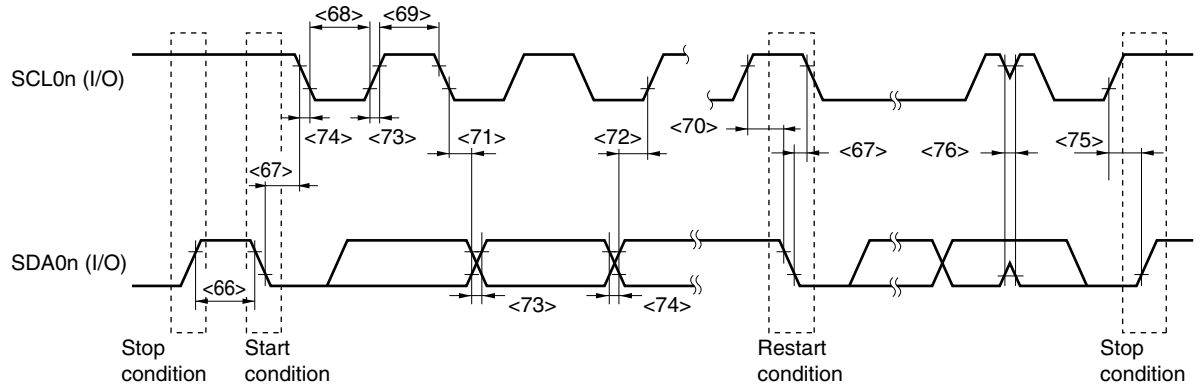
Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Output voltage, high	V_{OH1}	P02, P03, P05, P30 to P32, P38, P39, P40 to P42, P50 to P55, P90, P91, P96 to P99, P914, P915	Per pin I_{OH} = −1.0 mA	Total of all pins −20 mA	EV_{DD} − 1.0		EV_{DD}	V
			Per pin I_{OH} = −100 μA	Total of all pins −2.5 mA	EV_{DD} − 0.5		EV_{DD}	V
	V_{OH2}	PCM0, PDL5	Per pin I_{OH} = −1.0 mA	Total of all pins −2 mA	EV_{DD} − 1.0		EV_{DD}	V
			Per pin I_{OH} = −100 μA	Total of all pins −0.2 mA	EV_{DD} − 0.5		EV_{DD}	V
	V_{OH3}	P70 to P75	Per pin I_{OH} = −0.4 mA	Total of all pins −2.4 mA	AV_{REF0} − 1.0		AV_{REF0}	V
			Per pin I_{OH} = −100 μA	Total of all pins −0.6 mA	AV_{REF0} − 0.5		AV_{REF0}	V
	V_{OH4}	P10	I_{OH} = −0.4 mA		AV_{REF1} − 1.0		AV_{REF1}	V
			I_{OH} = −100 μA		AV_{REF1} − 0.5		AV_{REF1}	V
Output voltage, low	V_{OL1}	P02, P03, P05, P30 to P32, P42, P50 to P55, P96 to P99, P914, P915	Per pin I_{OL} = 1.0 mA	Total of all pins 20 mA	0		0.4	V
	V_{OL2}	P38, P39, P40, P41, P90, P91	Per pin I_{OL} = 3.0 mA		0		0.4	V
	V_{OL3}	PCM0, PDL5	Per pin I_{OL} = 1.0 mA	Total of all pins 2 mA	0		0.4	V
	V_{OL4}	P10, P70 to P75	Per pin I_{OL} = 0.4 mA	Total of all pins 2.8 mA	0		0.4	V
Software pull-down resistor[Note]	R_1	P05	V_I = V_{DD}		10	20	100	kΩ

Note $\overline{\text{DRST}}$ pin only (controlled by OCDM register)

Remarks 1. Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

2. When the I_{OH} and I_{OL} conditions are not satisfied for a pin but the total value of all pins is satisfied, only that pin does not satisfy the DC characteristics.

I²C Bus Timing



Remark **n = 0 to 2**

32.8.7 A/D converter

(T_A = –40 to +85°C, V_{DD} = EV_{DD} = AV_{REF0} = AV_{REF1}, 2.7 V ≤ AV_{REF0} = AV_{REF1} ≤ 3.6 V, V_{SS} = EV_{SS} = AV_{SS} = 0 V, C_L = 50 pF)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution					10	bit
Overall error[Note]		2.7 V ≤ AV_{REF0} ≤ 3.6 V			±0.6	%FSR
A/D conversion time	t_{CONV}	3.0 V ≤ AV_{REF0} ≤ 3.6 V	2.6		24	μs
		2.7 V ≤ AV_{REF0} ≤ 3.0 V	3.9		24	μs
Zero scale error					±0.5	%FSR
Full scale error					±0.5	%FSR
Non-linearity error					±4.0	LSB
Differential linearity error					±4.0	LSB
Analog input voltage	V_{IAN}		AV_{SS}		AV_{REF0}	V
Reference voltage	AV_{REF0}		2.7		3.6	V
AV_{REF0} current	AI_{REF0}	Normal conversion mode		3	6.5	mA
		High-speed conversion mode		4	10	mA
		When A/D converter unused			5	μA

Note Excluding quantization error (±0.05 %FSR).

Caution Do not set (read/write) alternate-function ports during A/D conversion; otherwise the conversion resolution may be degraded.

Remark LSB: Least Significant Bit
FSR: Full Scale Range

(5/6)

Mnemonic	Operand	Opcode	Operation	Execution Clock			Flags				
				i	r	l	CY	OV	S	Z	SAT
SET1	bit#3,disp16[reg1]	00bbb111110RRRRR ddddddddddddddd	adr←GR[reg1]+sign-extend(disp16) Z flag←Not (Load-memory-bit(adr,bit#3)) Store-memory-bit(adr,bit#3,1)	3 Note 3	3 Note 3	3 Note 3				×	
	reg2,[reg1]	rrrrr111111RRRRR 0000000011100000	adr←GR[reg1] Z flag←Not(Load-memory-bit(adr,reg2)) Store-memory-bit(adr,reg2,1)	3 Note 3	3 Note 3	3 Note 3				×	
SHL	reg1,reg2	rrrrr111111RRRRR 0000000011000000	GR[reg2]←GR[reg2] logically shift left by GR[reg1]	1	1	1	×	0	×	×	
	imm5,reg2	rrrrr010110iiiii	GR[reg2]←GR[reg2] logically shift left by zero-extend(imm5)	1	1	1	×	0	×	×	
SHR	reg1,reg2	rrrrr111111RRRRR 0000000010000000	GR[reg2]←GR[reg2] logically shift right by GR[reg1]	1	1	1	×	0	×	×	
	imm5,reg2	rrrrr010100iiiii	GR[reg2]←GR[reg2] logically shift right by zero-extend(imm5)	1	1	1	×	0	×	×	
SLD.B	disp7[ep],reg2	rrrrr0110ddddddd	adr←ep+zero-extend(disp7) GR[reg2]←sign-extend(Load-memory(adr,Byte))	1	1	Note 9					
SLD.BU	disp4[ep],reg2	rrrrr0000110dddd **Note 18**	adr←ep+zero-extend(disp4) GR[reg2]←zero-extend(Load-memory(adr,Byte))	1	1	Note 9					
SLD.H	disp8[ep],reg2	rrrrr1000ddddddd **Note 19**	adr←ep+zero-extend(disp8) GR[reg2]←sign-extend(Load-memory(adr,Halfword))	1	1	Note 9					
SLD.HU	disp5[ep],reg2	rrrrr0000111dddd **Notes 18, 20**	adr←ep+zero-extend(disp5) GR[reg2]←zero-extend(Load-memory(adr,Halfword))	1	1	Note 9					
SLD.W	disp8[ep],reg2	rrrrr1010ddddddd0 **Note 21**	adr←ep+zero-extend(disp8) GR[reg2]←Load-memory(adr,Word)	1	1	Note 9					
SST.B	reg2,disp7[ep]	rrrrr0111ddddddd	adr←ep+zero-extend(disp7) Store-memory(adr,GR[reg2],Byte)	1	1	1					
SST.H	reg2,disp8[ep]	rrrrr1001ddddddd **Note 19**	adr←ep+zero-extend(disp8) Store-memory(adr,GR[reg2],Halfword)	1	1	1					
SST.W	reg2,disp8[ep]	rrrrr1010ddddddd1 **Note 21**	adr←ep+zero-extend(disp8) Store-memory(adr,GR[reg2],Word)	1	1	1					
ST.B	reg2,disp16[reg1]	rrrrr111010RRRRR ddddddddddddddd	adr←GR[reg1]+sign-extend(disp16) Store-memory(adr,GR[reg2],Byte)	1	1	1					
ST.H	reg2,disp16[reg1]	rrrrr111011RRRRR ddddddddddddddd0 **Note 8**	adr←GR[reg1]+sign-extend(disp16) Store-memory (adr,GR[reg2], Halfword)	1	1	1					
ST.W	reg2,disp16[reg1]	rrrrr111011RRRRR ddddddddddddddd1 **Note 8**	adr←GR[reg1]+sign-extend(disp16) Store-memory (adr,GR[reg2], Word)	1	1	1					
STSR	regID,reg2	rrrrr111111RRRRR 0000000001000000	GR[reg2]←SR[regID]	1	1	1					

REVISION HISTORY	V850ES/JC3-L, V850ES/JE3-L User's Manual: Hardware

Rev.	Date	Description	
		Page	Summary
0.01	Jul 23, 2010	—	First Edition issued
1.00	Mar 29, 2011	Throughout	Addition of products to V850ES/JE3-L •μ PD70F3807F1-AN9-A •μ PD70F3808F1-AN9-A •μ PD70F3840F1-AN9-A
		p.195	Modification of **5.5.2(4) PLL lockup time specification register (PLLS)**
		p.196	Modification of **5.5.3 Usage**
		p.722	Modification of **19.2.2 (2) From INTWDT2 signal**
		p.866	Modification of **30. 4. 1 (1) Main clock oscillator characteristics**
		p.867	Addition of **30. 4. 1 (1) (a) KYOCERA KINSEKI CORPORATION: Crystal resonator (TA = –10 to +70°C)**
		p.867	Addition of **30. 4. 1 (1) (b) Murata Mfg. Co. Ltd.: Ceramic resonator (TA = –20 to +80°C)**
		p 868	Addition of **30. 4. 1 (1) (c) KYOCERA CORPORATION: Ceramic resonator (TA = –40 to +85 °C)**
		p.870	Addition of **30. 4. 2 (a) Seiko Instruments Inc.: Crystal resonator (TA = –40 to +85°C)**
		p.870	Addition of **30. 4. 2 (b) Citizen Miyota Co., Ltd.: Crystal resonator (TA = –40 to +85°C)**
		p.871	Modification of **30. 4. 3 PLL characteristics**
		p.874	Modification of **30. 6. 2 Supply current characteristics**
		p.889	Modification of **31. 4. 1 (1) Main clock oscillator characteristics**
		p.890	Addition of **31. 4. 1 (1) (a) KYOCERA KINSEKI CORPORATION: Crystal resonator (TA = –10 to +70°C)**
		p.890	Addition of **31. 4. 1 (1) (b) Murata Mfg. Co. Ltd.: Ceramic resonator (TA = –20 to +80°C)**
		p 891	Addition of **31. 4. 1 (1) (c) KYOCERA CORPORATION: Ceramic resonator (TA = –40 to +85 °C)**
		p.893	Addition of **31. 4. 2 (a) Seiko Instruments Inc.: Crystal resonator (TA = –40 to +85°C)**
		p.893	Addition of **31. 4. 2 (b) Citizen Miyota Co., Ltd.: Crystal resonator (TA = –40 to +85°C)**
		p.894	Modification of **31. 4. 3 PLL characteristics**
		p.897	Modification of **31. 6. 2 Supply current characteristics**
		p.912	Modification of **32. 4. 1 (1) Main clock oscillator characteristics**
		p.913	Addition of **32. 4. 1 (1) (a) KYOCERA KINSEKI CORPORATION: Crystal resonator (TA = –10 to +70°C)**
		p.913	Addition of **32. 4. 1 (1) (b) Murata Mfg. Co. Ltd.: Ceramic resonator (TA = –20 to +80°C)**
		p 914	Addition of **31. 4. 1 (1) (c) KYOCERA CORPORATION: Ceramic resonator (TA = –40 to +85 °C)**
		p.916	Addition of **32. 4. 2 (a) Seiko Instruments Inc.: Crystal resonator (TA = –40 to +85°C)**
		p.916	Addition of **32. 4. 2 (b) Citizen Miyota Co., Ltd.: Crystal resonator (TA = –40 to +85°C)**
		p.917	Modification of **32. 4. 3 PLL characteristics**
		p.920	Modification of **32. 6. 2 Supply current characteristics**
		p.932	Addition of **CHAPTER 33 RECOMMENDED SOLDERING CONDITIONS**
1.01	Aug 25, 2011	p.28	Modification of **1.5 Pin Configuration (Top View) V850ES/JC3-L**
2.00	Mar 25, 2014	Throughout	Deletion of all products of V850ES/JF3-L
			• Under development → mass production μ UPD70F3805GB-GAH-AX, 70F3806GB-GAH-AX, 70F3807GB-GAH-AX, 70F3808GB-GAH-AX, 70F3840GB-GAH-AX