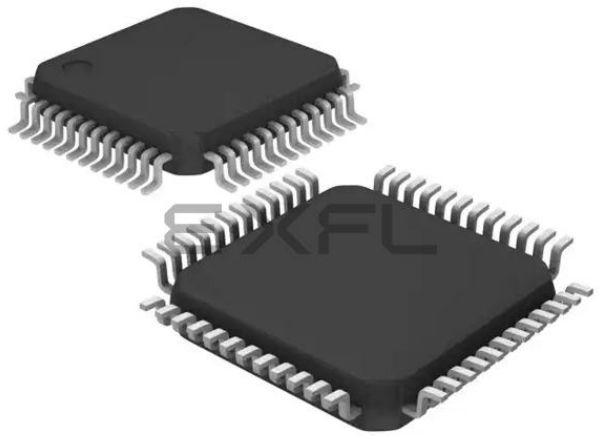

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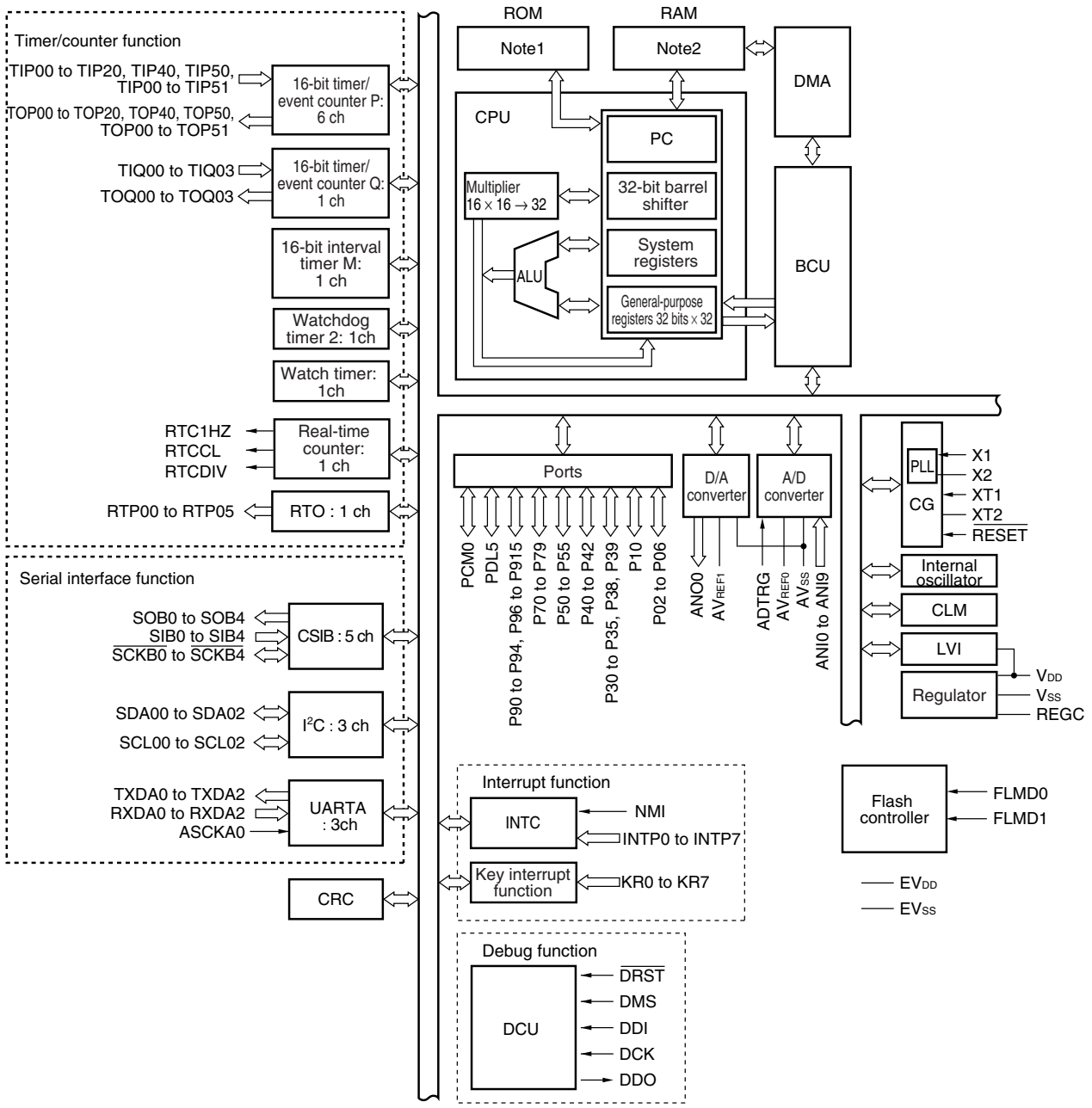
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	V850ES
Core Size	32-Bit Single-Core
Speed	20MHz
Connectivity	CSI, EBI/EMI, I²C, UART/USART
Peripherals	DMA, LVD, PWM, WDT
Number of I/O	34
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 3.6V
Data Converters	A/D 6x10b; D/A 1x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd70f3804ga-gam-ax

(3) V850ES/JE3-L



Notes1. μPD70F3805: 16 KB, μPD70F3806: 32 KB, μPD70F3807: 64 KB, μPD70F3808: 128 KB, μPD70F3840: 256 KB

2. μPD70F3805, 70F3806, 70F3807, 70F3808: 8 KB, μPD70F3840: 16 KB

1.6.2 Internal units

(1) CPU

The CPU uses five-stage pipeline control to enable single-clock execution of address calculations, arithmetic logic operations, data transfers, and almost all other instruction processing.

Other dedicated on-chip hardware, such as a multiplier (16 bits × 16 bits → 32 bits) and a barrel shifter (32 bits) contribute to faster complex processing.

(2) Bus control unit (BCU)

The BCU controls the internal bus.

(3) Flash memory (ROM)

This is a 256/128/64/32/16 KB flash memory mapped to addresses 0000000H to 003FFFFH/0000000H to 001FFFFH/0000000H to 000FFFFH/0000000H-0007FFFH/0000000H-0003FFFH.

It can be accessed from the CPU in one clock during instruction fetch.

(4) RAM

This is a 16/8 KB RAM mapped to addresses 3FFB000H to 3FFEFFFH/3FFD000H to 3FFEFFFH. It can be accessed from the CPU in one clock during data access.

(5) Interrupt controller (INTC)

This controller handles hardware interrupt requests (NMI, INTP0 to INTP7) from on-chip peripheral hardware and external hardware. Eight levels of interrupt priorities can be specified for these interrupt requests, and multiplexed interrupt servicing control can be performed.

(6) Clock generator (CG)

A main clock oscillator and subclock oscillator are provided and generate the main clock oscillation frequency (f_X) and subclock frequency (f_{XT}), respectively. There are two modes: In the clock-through mode, f_X is used as the main clock frequency (f_{XX}) as is. In the PLL mode, f_X is used multiplied by 4.

The CPU clock frequency (f_{CPU}) can be selected from among f_{XX}, $f_{XX}/2$, $f_{XX}/4$, $f_{XX}/8$, $f_{XX}/16$, $f_{XX}/32$, and f_{XT}.

(7) Internal oscillator

An internal oscillator is provided on chip. The oscillation frequency is 220 kHz (TYP). The internal oscillator supplies the clock for watchdog timer 2 and timer M.

(8) Timer/counter

Six-channel 16-bit timer/event counter P (TMP), one-channel 16-bit timer/event counter Q (TMQ), and one-channel 16-bit interval timer M (TMM), are provided on chip.

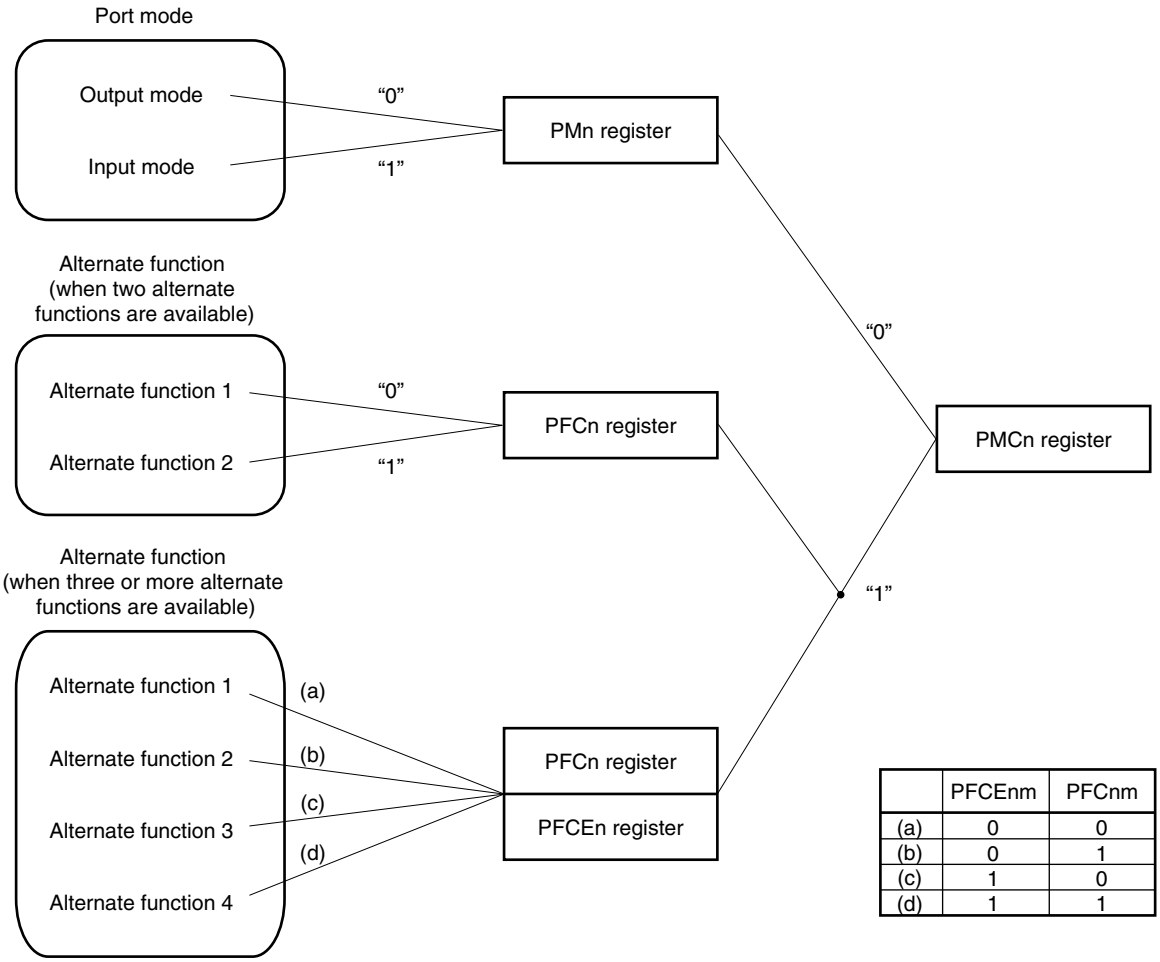
(9) Watch timer

This timer counts the reference time period (0.5 s) for counting the clock (the 32.768 kHz subclock or the 32.768 kHz f_{BRG} clock from the prescaler). The watch timer can also be used as an interval timer based on the main clock.

(7) Port setting

Set a port as illustrated below.

Figure 4-4. Setting of Each Register and Pin Function



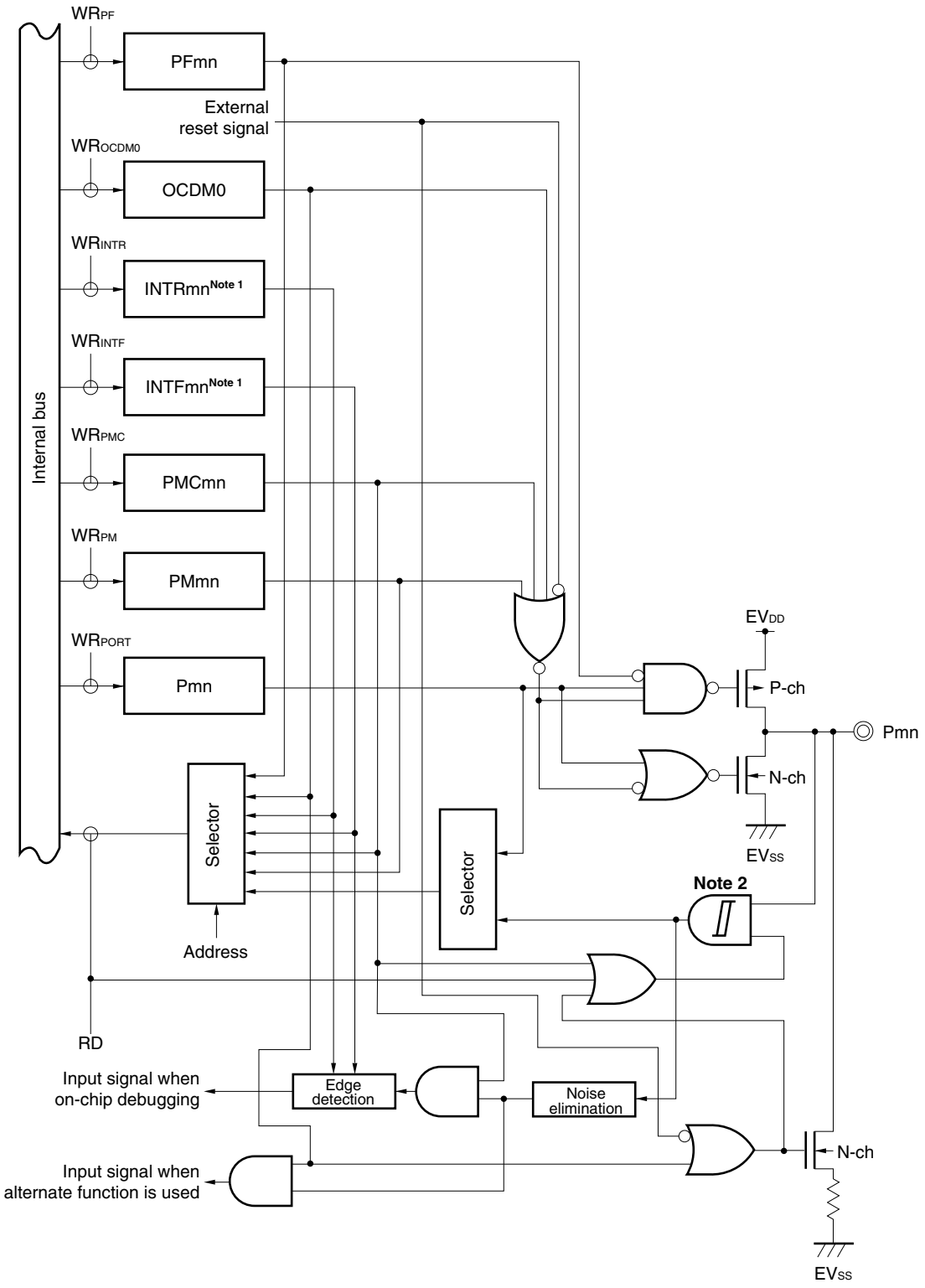
	PFCEnm	PFCnm
(a)	0	0
(b)	0	1
(c)	1	0
(d)	1	1

Remark Set the alternate functions in the following sequence.

<1> Set the PFCn and PFCEn registers.
<2> Set the PMCn register.
<3> Set the INTRn or INTFn register (to specify an external interrupt pin).

If the PMCn register is set first, an unintended function may be set while the PFCn and PFCEn registers are being set.

Figure 4-36. Block Diagram of Type AA-1



Notes 1. See **19.7 External Interrupt Request Input Pins (NMI and INTP0 to INTP7)**.

2. There are no hysteresis characteristics in port mode.

(2) TMPn control register 1 (TPnCTL1)

The TPnCTL1 register is an 8-bit register that controls the operation of TMPn.

This register can be read or written in 8-bit or 1-bit units.

Reset sets this register to 00H.

After reset: 00H R/W Address: TP0CTL1 FFFFF591H, TP1CTL1 FFFFF5A1H, TP2CTL1 FFFFF5B1H, TP3CTL1 FFFFF5C1H, TP4CTL1 FFFFF5D1H, TP5CTL1 FFFFF5E1H

TPnCTL1 (n = 0 to 5)

7	<6>	<5>	4	3	2	1	0
0	TPnEST	TPnEEE	0	0	TPnMD2	TPnMD1	TPnMD0

TPnEST	Software trigger control
0	–
1	Generate a valid signal for external trigger input. • In one-shot pulse output mode: A one-shot pulse is output with writing 1 to the TPnEST bit as the trigger. • In external trigger pulse output mode: A PWM waveform is output with writing 1 to the TPnEST bit as the trigger.

TPnEEE	Count clock selection
0	Disable operation with external event count input. (Perform counting with the internal count clock selected by the TPnCTL0.TPnCK0 to TPnCK2 bits.)
1	Enable operation with external event count input. (Perform counting at the valid edge of the external event count input signal.)

TPnMD2	TPnMD1	TPnMD0	Timer mode selection
0	0	0	Interval timer mode
0	0	1	External event count mode
0	1	0	External trigger pulse output mode
0	1	1	One-shot pulse output mode
1	0	0	PWM output mode
1	0	1	Free-running timer mode
1	1	0	Pulse width measurement mode
1	1	1	Setting prohibited

Cautions 1. The TPnEST bit is valid only in the external trigger pulse output mode or the one-shot pulse output mode. In any other mode, writing 1 to this bit is ignored.

2. External event count input is selected in the external event count mode regardless of the value of the TPnEEE bit.

3. Set the TPnEEE and TPnMD2 to TPnMD0 bits when the timer operation is stopped (TPnCTL0.TPnCE bit = 0). (The same value can be written when the TPnCE bit = 1.) The operation is not guaranteed when rewriting is performed with the TPnCE bit = 1. If rewriting was mistakenly performed, clear the TPnCE bit to 0 and then set the bits again.

4. Be sure to clear bits 3, 4, and 7 to "0".

(9) TMQ0 capture/compare register 2 (TQ0CCR2)

The TQ0CCR2 register can be used as a capture register or a compare register depending on the mode.

This register can be selected as a capture register or a compare register only in the free-running timer mode, according to the setting of the TQ0OPT0.TQ0CCS2 bit. In the pulse width measurement mode, the TQ0CCR2 register can be used only as a capture register. In any other mode, this register can be used only as a compare register.

The TQ0CCR2 register can be read or written during operation.

This register can be read or written in 16-bit units.

Reset sets this register to 0000H.

Caution Accessing the TQ0CCR2 register is prohibited in the following statuses. Moreover, if the system is in the wait status, the only way to cancel the wait status is to execute a reset. For details, see 3.4.9 (1) Accessing specific on-chip peripheral I/O registers.

- **When the CPU operates on the subclock and main clock oscillation is stopped**
- **When the CPU operates on the internal oscillator clock**

After reset: 0000H R/W Address: FFFFF54AH

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TQ0CCR2																

(a) Function as compare register

The TQ0CCR2 register can be rewritten even when the TQ0CTL0.TQ0CE bit = 1.

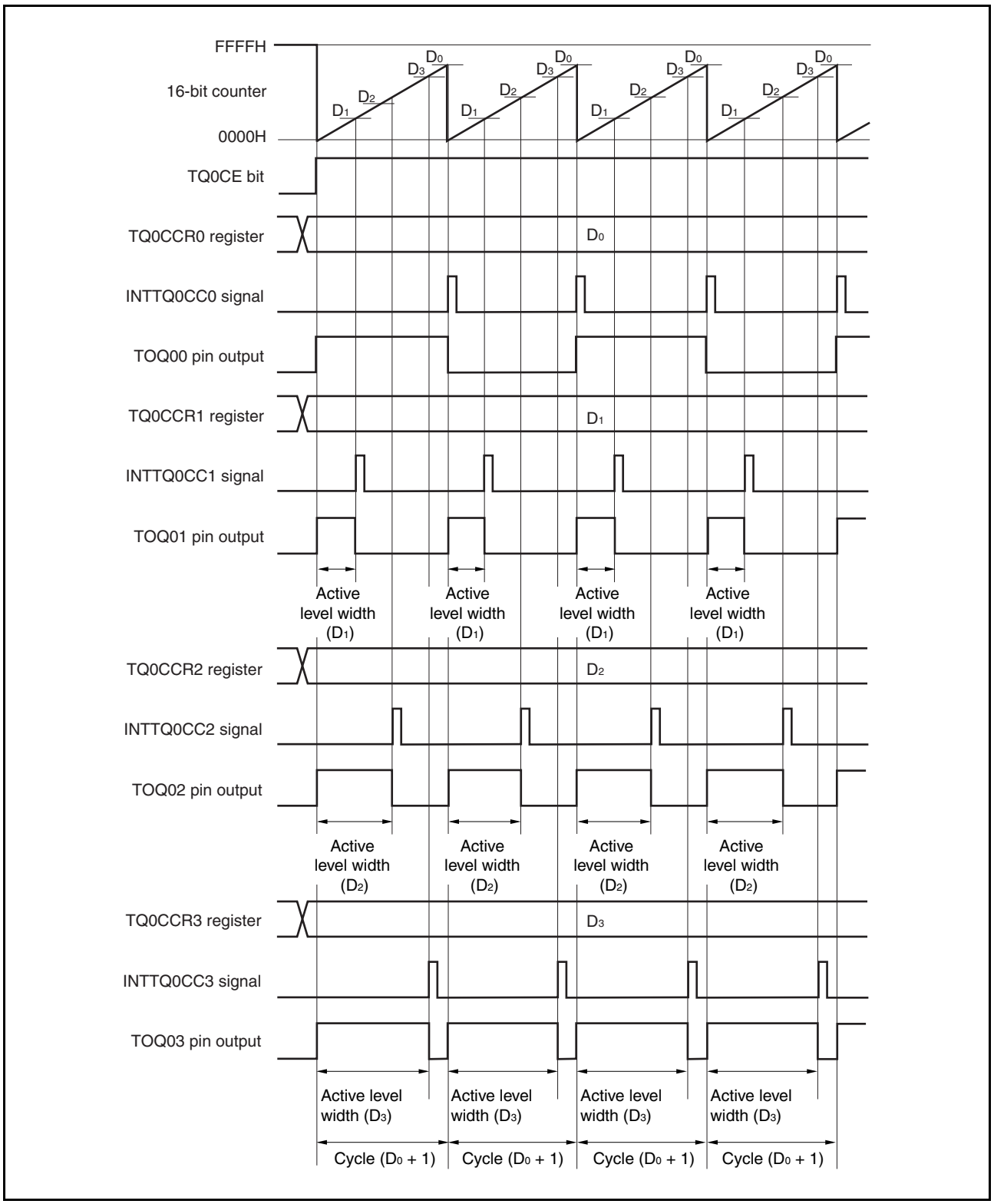
The set value of the TQ0CCR2 register is transferred to the CCR2 buffer register. When the value of the 16-bit counter matches the value of the CCR2 buffer register, a compare match interrupt request signal (INTTQ0CC2) is generated. If TOQ02 pin output is enabled at this time, the output of the TOQ02 pin is inverted (For details, see the descriptions of each operating mode.).

(b) Function as capture register

When the TQ0CCR2 register is used as a capture register in the free-running timer mode, the count value of the 16-bit counter is stored in the TQ0CCR2 register if the valid edge of the capture trigger input pin (TIQ02 pin) is detected. In the pulse-width measurement mode, the count value of the 16-bit counter is stored in the TQ0CCR2 register and the 16-bit counter is cleared (0000H) if the valid edge of the capture trigger input pin (TIQ02 pin) is detected.

Even if the capture operation and reading the TQ0CCR2 register conflict, the correct value of the TQ0CCR2 register can be read.

Figure 7-45. Basic Timing of Operations in PWM Output Mode



14.2 Configuration

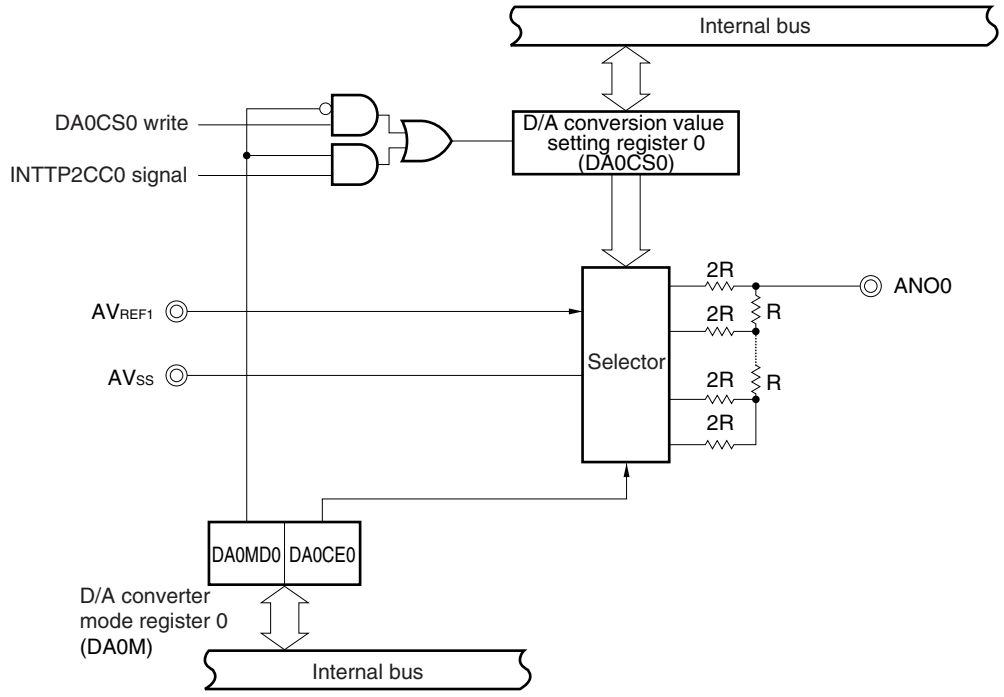
The D/A converter includes the following hardware.

Table 14-1. D/A Converter Registers Used by Software

Item	Configuration
Control registers	D/A converter mode register (DA0M) D/A conversion value setting registers 0 (DA0CS0)

The block diagram of the D/A converter is shown below.

Figure 14-1. Block Diagram of D/A Converter

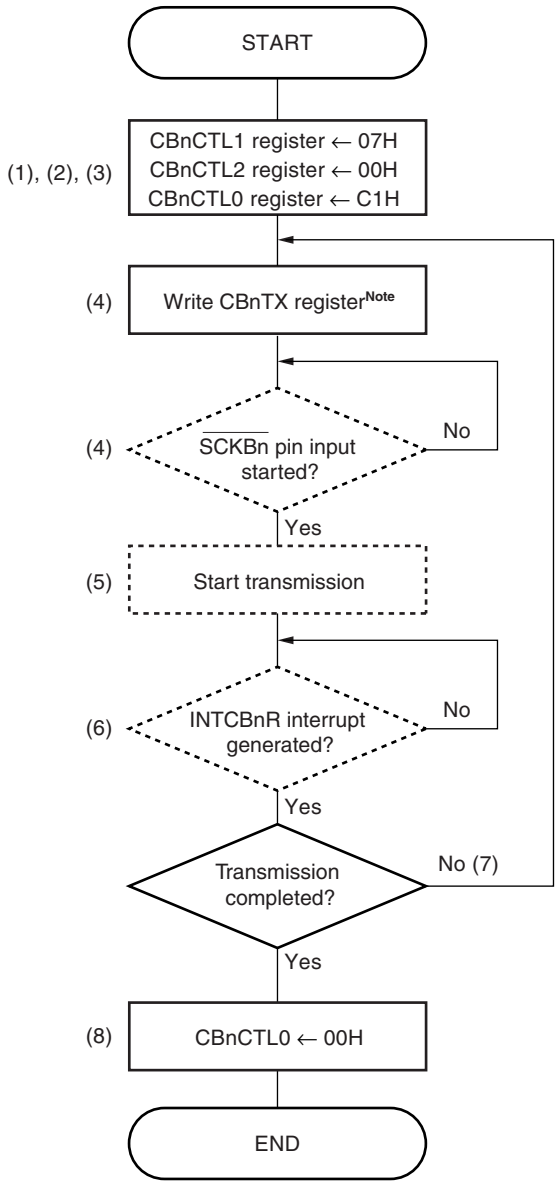


Caution DA0CS0 is also used as the AV_{REF1} and AV_{SS} pins. The AV_{SS} pin is also used by the A/D converter.

16.6.4 Single transfer mode (slave mode, transmission mode)

MSB first (CBnCTL0.CBnDIR bit = 0), communication type 1 (CBnCTL1.CBnCKP and CBnCTL1.CBnDAP bits = 00), communication clock (f_{CCLK}) = external clock ($\overline{SCKBn}$) (CBnCTL1.CBnCKS2 to CBnCTL1.CBnCKS0 bits = 111), transfer data length = 8 bits (CBnCTL2.CBnCL3 to CBnCTL2.CBnCL0 bits = 0000)

Figure 16-11. Single Transfer Mode Operation (Slave Mode, Transmission Mode)



Note If the serial clock is input via the $\overline{SCKBn}$ pin of the master before the CBnTX register is written, data cannot be transmitted normally. In this case, initialize both the master and the slave.

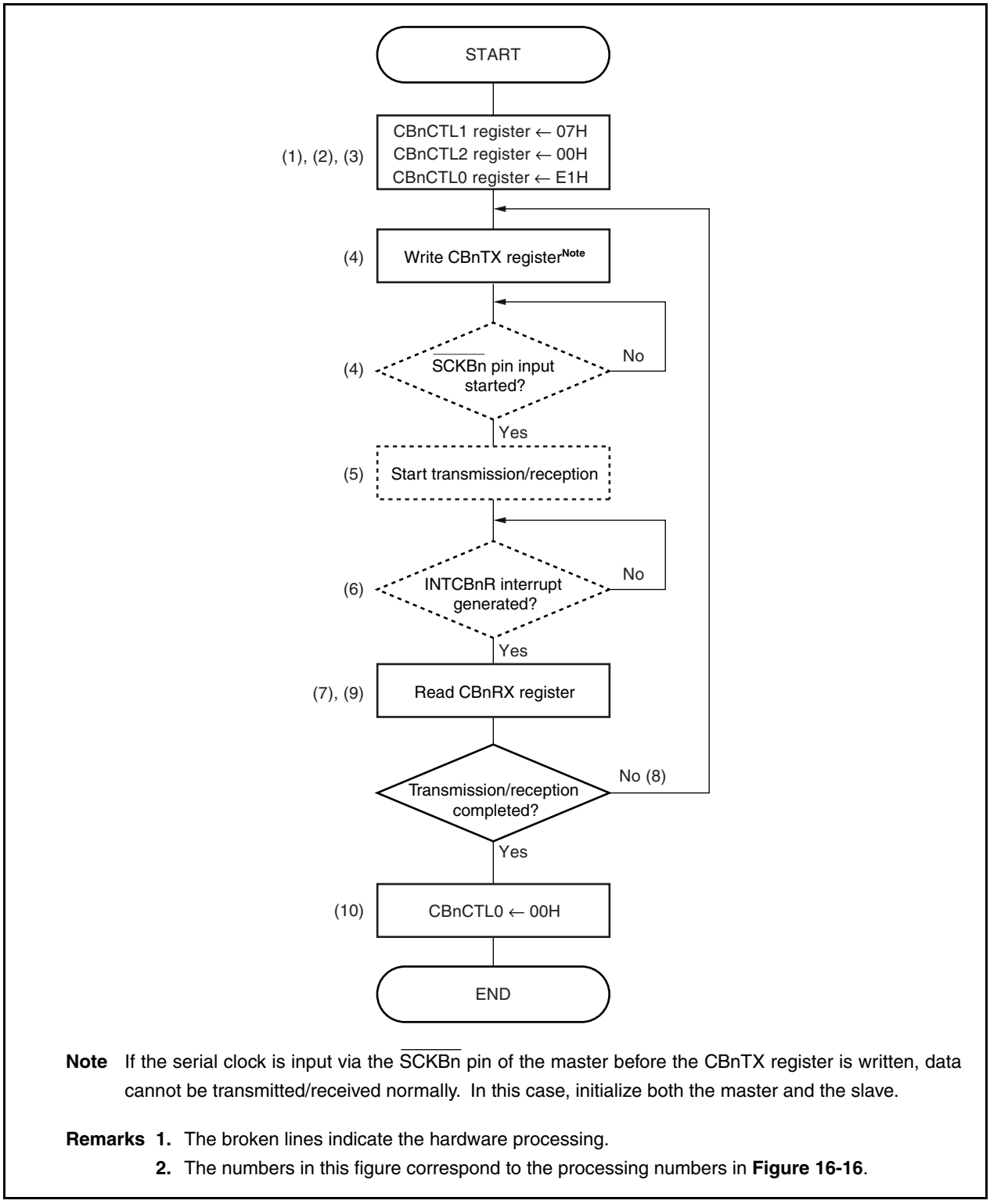
Remarks 1. The broken lines indicate the hardware processing.

2. The numbers in this figure correspond to the processing numbers in **Figure 16-12**.

16.6.6 Single transfer mode (slave mode, transmission/reception mode)

MSB first (CBnCTL0.CBnDIR bit = 0), communication type 1 (CBnCTL1.CBnCKP and CBnCTL1.CBnDAP bits = 00), communication clock (f_{CCLK}) = external clock ($\overline{SCKBn}$) (CBnCTL1.CBnCKS2 to CBnCTL1.CBnCKS0 bits = 111), transfer data length = 8 bits (CBnCTL2.CBnCL3 to CBnCTL2.CBnCL0 bits = 0000)

Figure 16-15. Single Transfer Mode Operation (Slave Mode, Transmission/Reception Mode)



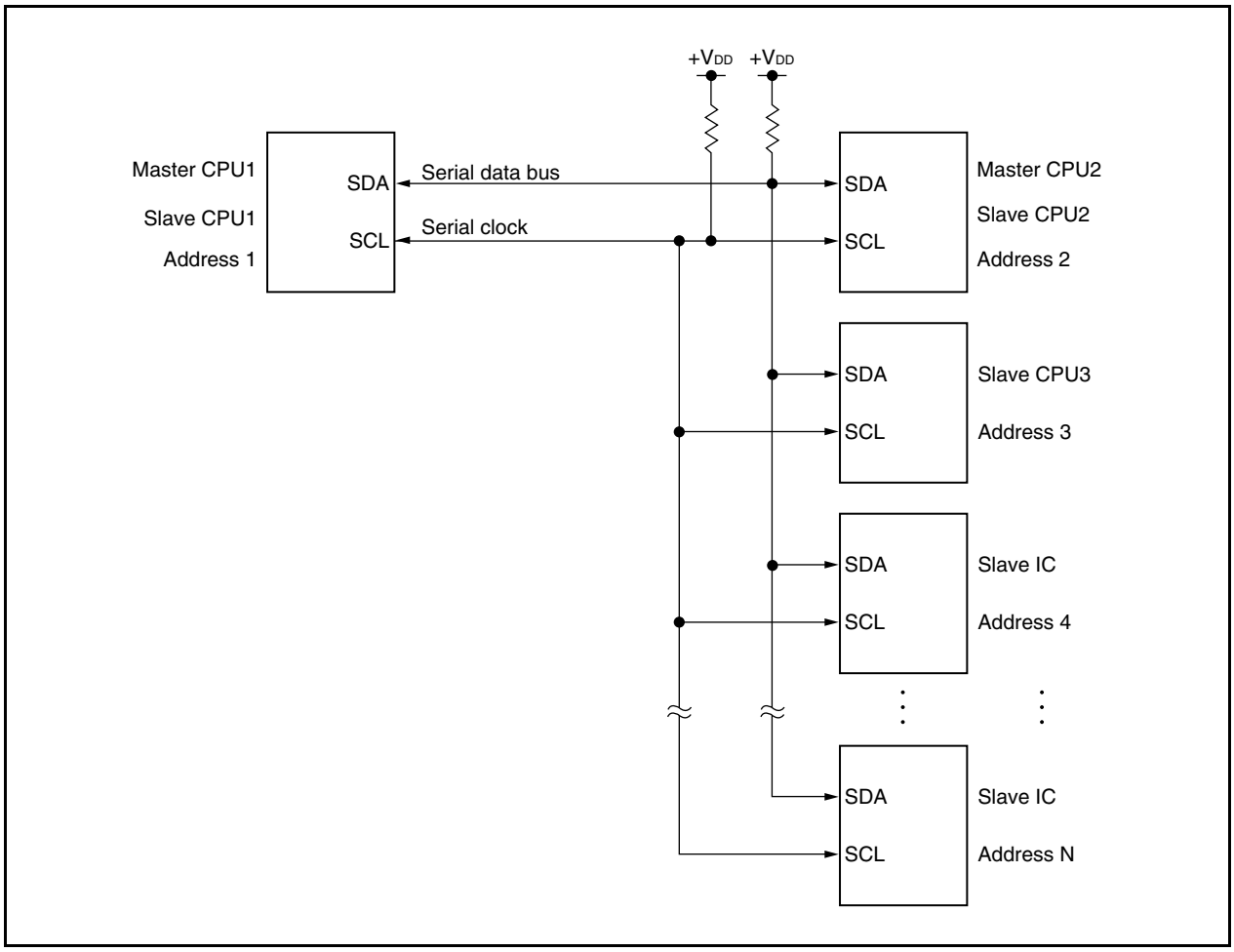
Note If the serial clock is input via the $\overline{SCKBn}$ pin of the master before the CBnTX register is written, data cannot be transmitted/received normally. In this case, initialize both the master and the slave.

Remarks 1. The broken lines indicate the hardware processing.

2. The numbers in this figure correspond to the processing numbers in **Figure 16-16**.

A serial bus configuration example is shown below.

Figure 17-5. Serial Bus Configuration Example Using I²C Bus



17.4 Registers

I²C0n is controlled by the following registers.

- IIC control registers n (IICCn)
- IIC status registers n (IICSn)
- IIC flag registers n (IICFn)
- IIC clock select registers n (IICCLn)
- IIC function expansion registers n (IICXn)
- IIC division clock select registers 0, 1 (OCKS0, OCKS1)

The following registers are also used.

- IIC shift registers n (IICn)
- Slave address registers n (SVAn)

Remark For the alternate-function pin settings, see **Table 4-17 Settings When Pins Are Used for Alternate Functions**.

(1) IIC control registers n (IICCn)

The IICCn register enables/stops I²C0n operations, sets the wait timing, and sets other I²C operations.

These registers can be read or written in 8-bit or 1-bit units. However, set the SPIEn, WTIMn, and ACKEn bits when the IICEn bit is 0 or during the wait period. When setting the IICEn bit from “0” to “1”, these bits can also be set at the same time.

Reset sets these registers to 00H.

17.6.7 Wait state cancellation method

In the case of I²C0n, a wait state can be canceled normally in the following ways.

- By writing data to the IICn register
- By setting the IICCn.WRELn bit to 1 (wait state cancellation)
- By setting the IICCn.STTn bit to 1 (start condition generation)
- By setting the IICCn.SPTn bit to 1 (stop condition generation)

If any of these wait state cancellation actions is performed, I²C0n will cancel the wait state and restart communication.

When canceling the wait state and sending data (including addresses), write data to the IICn register.

To receive data after canceling the wait state, or to complete data transmission, set the WRELn bit to 1.

To generate a restart condition after canceling the wait state, set the STTn bit to 1.

To generate a stop condition after canceling the wait state, set the SPTn bit to 1.

Cancel each wait state only once.

For example, if data is written to the IICn register following wait state cancellation by setting the WRELn bit to 1, a conflict between the SDA0n line change timing and the IICn register write timing may result in the data output to the SDA0n line being incorrect.

Even in other operations, if communication is stopped halfway, clearing the IICCn.IICEn bit to 0 will stop communication, enabling the wait state to be cancelled.

If the I²C bus deadlocks due to noise, etc., setting the IICCn.LRELn bit to 1 causes the communication to stop, enabling the wait state to be cancelled.

21.5.2 Releasing IDLE2 mode

The IDLE2 mode is released by a non-maskable interrupt request signal (NMI pin input, INTWDT2 signal), unmasked external interrupt request signal (INTP0 to INTP7 pin input), unmasked internal interrupt request signal from the peripheral functions operable in the IDLE2 mode, or reset signal (reset by RESET pin input, WDT2$\overline{\text{RES}}$ signal, low-voltage detector (LVI), or clock monitor (CLM)). The PLL returns to the operating status it was in before the IDLE2 mode was set.

After the IDLE2 mode has been released, the normal operation mode is restored.

(1) Releasing IDLE2 mode by non-maskable interrupt request signal or unmasked maskable interrupt request signal

The IDLE mode is released by a non-maskable interrupt request signal or an unmasked maskable interrupt request signal, regardless of the priority of the interrupt request. If the IDLE2 mode is set in an interrupt servicing routine, however, an interrupt request that is issued later is processed as follows.

Table 21-6. Operation After Releasing IDLE2 Mode by Interrupt Request Signal

Release Source	Interrupt Acknowledgment Status	Status After Release	Operation After Release
Reset	Disabled (DI)	–	Normal reset operation
	Enabled (EI)		
Non-maskable interrupt request signal (excluding multiple interrupts)	Disabled (DI)	–	The IDLE2 mode is released, and after securing the specified setup time, the interrupt request is acknowledged.
	Enabled (EI)		
Maskable interrupt request signal	Disabled (DI)	–	The IDLE2 mode is released but the interrupt request that is the release source is not acknowledged. The interrupt request itself is retained. After securing the specified setup time, the interrupt that was being serviced before shifting to the IDLE2 mode is serviced.
	Enabled (EI)	• An interrupt request with a priority higher than that of the release source is being serviced.	The IDLE2 mode is released but the interrupt request that is the release source, is not acknowledged. The interrupt request itself is retained. After securing the specified setup time, the processing that was being executed before shifting to the IDLE2 mode is executed.
		• An interrupt request with a priority lower than that of the release source is being serviced.	The IDLE2 mode is released, and after securing the specified setup time, the interrupt request is acknowledged.

Caution An interrupt request signal that is disabled by setting the PSC.NMI2M, PSC.NMI0M, and PSC.INTM bits to 1 (interrupt disabled) is invalid and cannot release the IDLE2 mode.

29.3.2 Setting

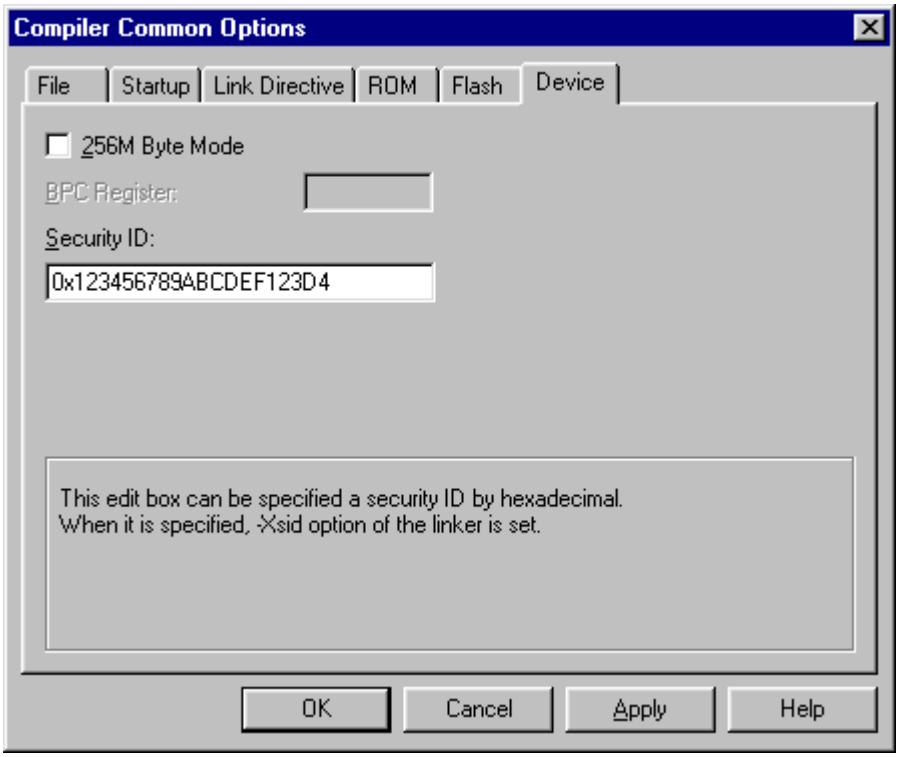
The following shows how to set the ID code as shown in Table 29-6.

When the ID code is set as shown in Table 29-6, the ID code input in the configuration dialog box of the ID850QB is “123456789ABCDEF123D4” (the ID code is not case-sensitive).

Table 29-6. ID Code

Address	Value
0x70	0x12
0x71	0x34
0x72	0x56
0x73	0x78
0x74	0x9A
0x75	0xBC
0x76	0xDE
0x77	0XF1
0x78	0x23
0x79	0xD4

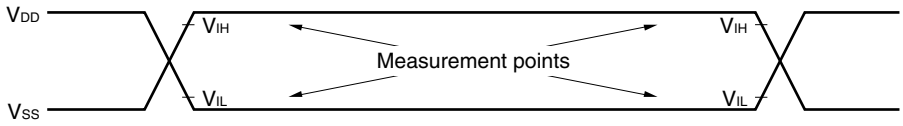
The ID code can be specified in the Compiler Common Options dialog box in PM+.



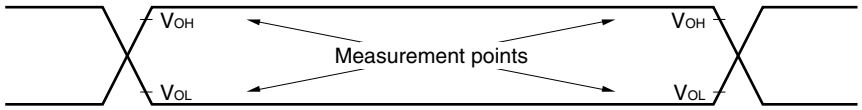
30.7 AC Characteristics

30.7.1 Measurement conditions

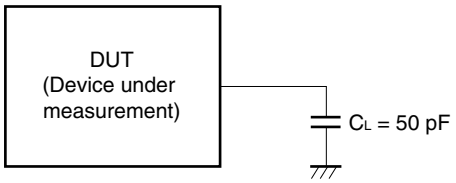
(1) AC test input measurement points



(2) AC test output measurement points

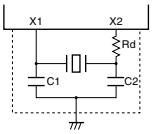


(3) Load conditions



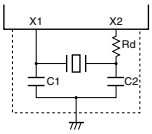
Caution If the load capacitance exceeds 50 pF due to the circuit configuration, bring the load capacitance of the device to 50 pF or less by inserting a buffer or by some other means.

(a) KYOCERA KINSEKI CORPORATION: Crystal resonator (T_A = −10 to +70°C)

Type	Circuit Example	Part Number	Oscillation Frequency f_X (MHz)	Recommended Circuit Constant			Oscillation Voltage Range		Oscillation Stabilization Time
				C1 (pF)	C2 (pF)	Rd (Ω)	MIN. (V)	MAX. (V)	MAX. (ms)
Surface mounting		CX49GFWB04000H0PESZZ	4.000	10	10	1000	2.2	3.6	10.45
		CX49GFWB05000H0PESZZ	5.000	10	10	1000	2.2	3.6	10.08
		CX49GFWB06000H0PESZZ	6.000	10	10	1000	2.2	3.6	9.26
		CX49GFWB08000H0PESZZ	8.000	10	10	0	2.2	3.6	8.98
		CX49GFWB10000H0PESZZ	10.000	10	10	0	2.2	3.6	8.59

Caution This oscillator constant is a reference value based on evaluation under a specific environment by the resonator manufacturer.
If optimization of oscillator characteristics is necessary in the actual application, apply to the resonator manufacturer for evaluation on the implementation circuit.
The oscillation voltage and oscillation frequency indicate only oscillator characteristics. Use the V850ES/JC3-L so that the internal operating conditions are within the specifications of the AC Characteristics, DC Characteristics, and Operating Conditions.

(b) Murata Mfg. Co. Ltd.: Ceramic resonator (T_A = −20 to +80°C)

Type	Circuit Example	Part Number	Oscillation Frequency f_X (MHz)	Recommended Circuit Constant			Oscillation Voltage Range		Oscillation Stabilization Time
				C1 (pF)	C2 (pF)	Rd (Ω)	MIN. (V)	MAX. (V)	MAX. (ms)
Surface mounting		CSTCC2M50G56-R0	2.500	(47)	(47)	2200	2.2	3.6	0.09
		CSTCR4M00G55-R0	4.000	(39)	(39)	680	2.2	3.6	0.09
		CSTCR5M00G55-R0	5.000	(39)	(39)	680	2.2	3.6	0.11
		CSTCR6M00G55-R0	6.000	(39)	(39)	470	2.2	3.6	0.11
		CSTCE8M00G55-R0	8.000	(33)	(33)	0	2.2	3.6	0.10
		CSTCE10M0G55-R0	10.000	(33)	(33)	0	2.2	3.6	0.10
Lead		CSTLS4M00G56-B0	4.000	(47)	(47)	680	2.2	3.6	0.11
		CSTLS5M00G56-B0	5.000	(47)	(47)	680	2.2	3.6	0.13
		CSTLS6M00G56-B0	6.000	(47)	(47)	470	2.2	3.6	0.11
		CSTLS8M00G56-B0	8.000	(47)	(47)	100	2.2	3.6	0.10
		CSTLS10M0G56-B0	10.000	(47)	(47)	100	2.2	3.6	0.10

Caution This oscillator constant is a reference value based on evaluation under a specific environment by the resonator manufacturer.
If optimization of oscillator characteristics is necessary in the actual application, apply to the resonator manufacturer for evaluation on the implementation circuit.
The oscillation voltage and oscillation frequency indicate only oscillator characteristics. Use the V850ES/JC3-L so that the internal operating conditions are within the specifications of the AC characteristics, DC characteristics, and operating conditions.

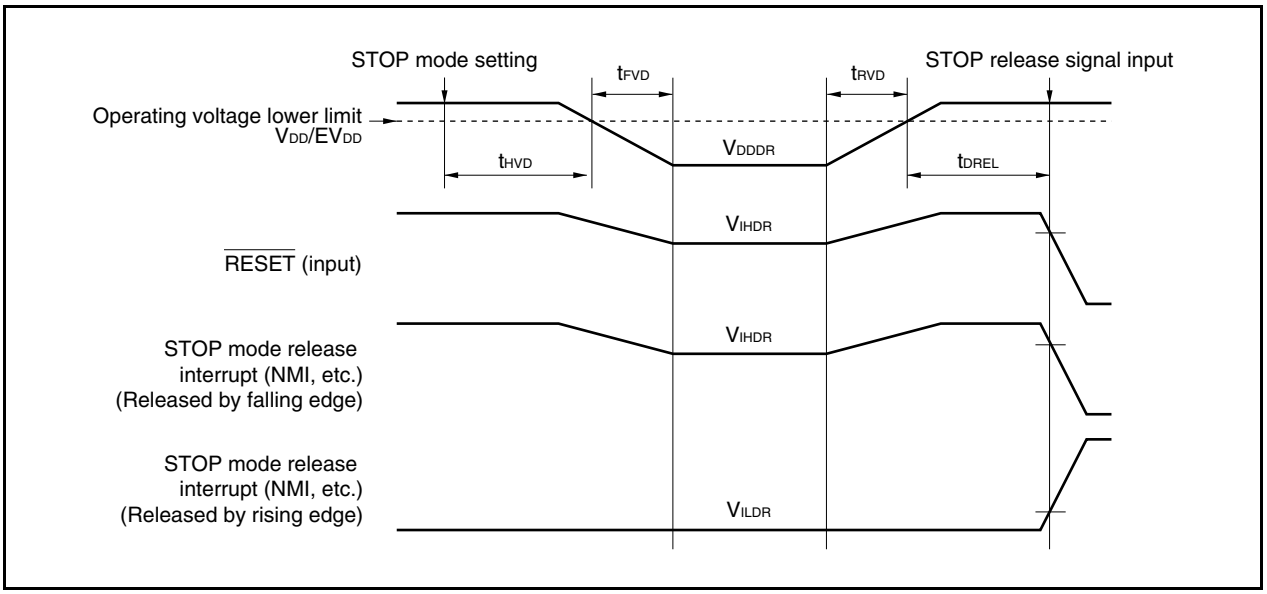
Remark Figures in parentheses in columns C1 and C2 indicate the capacitance incorporated in the resonator.

31.6.3 Data retention characteristics (in STOP mode)

(T_A = –40 to +85°C, V_{DD} = EV_{DD} = AV_{REF0} = AV_{REF1}, V_{SS} = EV_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention voltage	V_{DDDR}	STOP mode (all functions stopped)	1.9		3.6	V
Data retention current	I_{DDDR}	Subclock stopped, internal oscillator stopped T_A = 85°C			45	μA
Supply voltage rise time	t_{RVD}		200			μs
Supply voltage fall time	t_{FVD}		200			μs
Supply voltage retention time	t_{HVD}	After STOP mode setting	0			ms
STOP release signal input time	t_{DREL}	After V_{DD} reaches the operating voltage MIN. (see **31.3 Operating Conditions**)	0			ms
Data retention input voltage, high	V_{IHDR}	V_{DD} = EV_{DD} = V_{DDDR}	0.9V_{DDDR}		V_{DDDR}	V
Data retention input voltage, low	V_{ILDR}	V_{DD} = EV_{DD} = V_{DDDR}	0		0.1V_{DDDR}	V

Caution Shifting to STOP mode and restoring from STOP mode must be performed within the rated operating range.

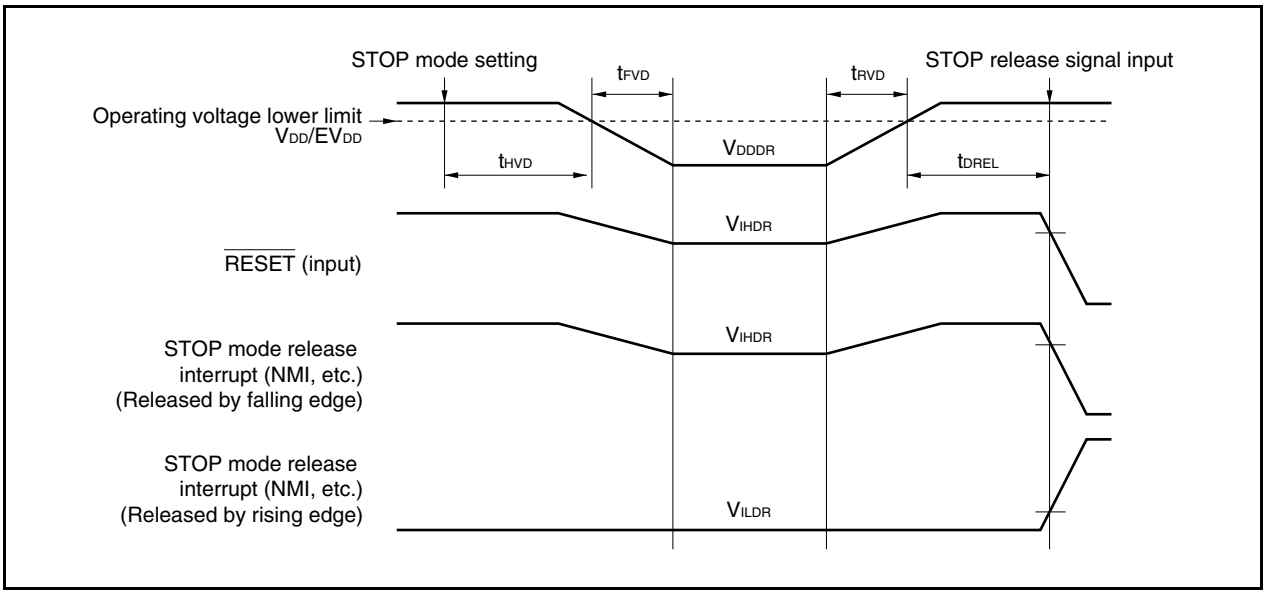


32.6.3 Data retention characteristics (in STOP mode)

(T_A = –40 to +85°C, V_{DD} = EV_{DD} = AV_{REF0} = AV_{REF1}, V_{SS} = EV_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention voltage	V_{DDDR}	STOP mode (all functions stopped)	1.9		3.6	V
Data retention current	I_{DDDR}	Subclock stopped, internal oscillator stopped T_A = 85°C			45	μA
Supply voltage rise time	t_{RVD}		200			μs
Supply voltage fall time	t_{FVD}		200			μs
Supply voltage retention time	t_{HVD}	After STOP mode setting	0			ms
STOP release signal input time	t_{DREL}	After V_{DD} reaches the operating voltage MIN. (see **32.3 Operating Conditions**)	0			ms
Data retention input voltage, high	V_{IHDR}	V_{DD} = EV_{DD} = V_{DDDR}	0.9V_{DDDR}		V_{DDDR}	V
Data retention input voltage, low	V_{ILDR}	V_{DD} = EV_{DD} = V_{DDDR}	0		0.1V_{DDDR}	V

Caution Shifting to STOP mode and restoring from STOP mode must be performed within the rated operating range.

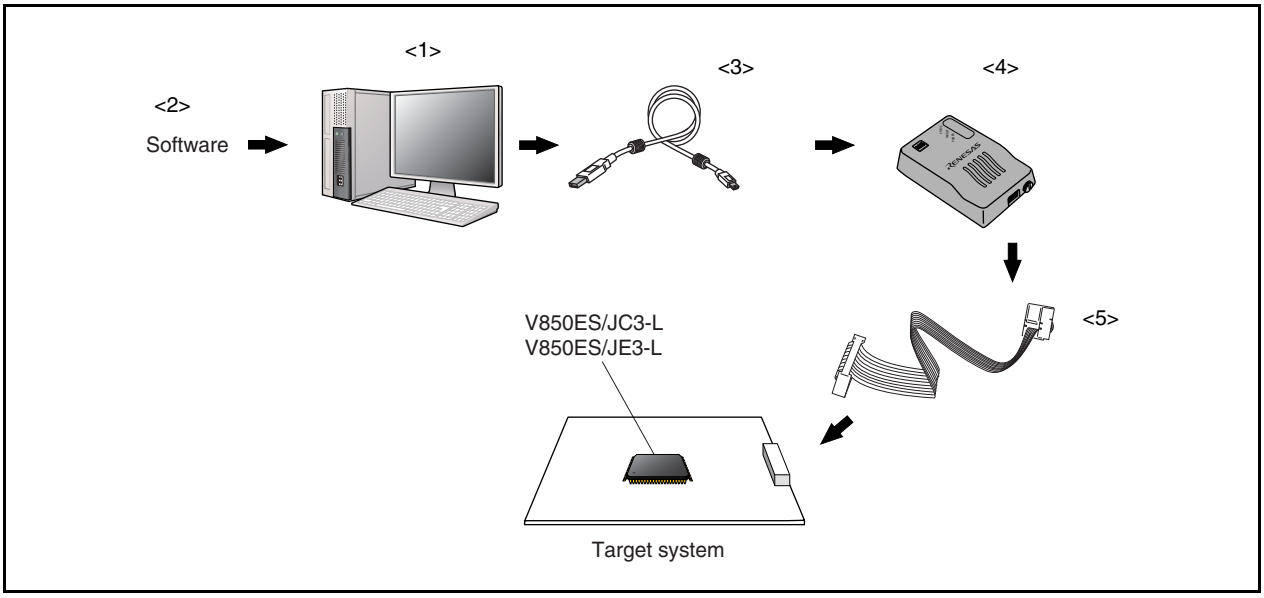


A.4.2 When using MINICUBE QB-V850MINIL

(1) On-chip emulation using MINICUBE

The system configuration when connecting MINICUBE to the host machine (PC-9821 series, PC/AT compatible) is shown below.

Figure A-3. On-Chip Emulation System Configuration



<1> Host machine	PC with USB ports
<2> Software	The integrated debugger ID850QB, device file, etc. Download the device file from the Renesas Electronics website. http://www2.renesas.com/micro/en/ods/index.html
<3> USB interface cable	USB cable to connect the host machine and MINICUBE. It is supplied with MINICUBE. The cable length is approximately 2 m.
<4> MINICUBE On-chip debug emulator	This on-chip debug emulator serves to debug hardware and software when developing application systems using the V850ES/JC3-L, V850ES/JE3-L. It supports integrated debugger ID850QB.
<5> OCD cable	Cable to connect MINICUBE and the target system. It is supplied with MINICUBE. The cable length is approximately 20 cm.

Remark The numbers in the angular brackets correspond to the numbers in Figure A-3.