Renesas Electronics America Inc - UPD70F3805GB(R)-GAH-AX Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	V850ES
Core Size	32-Bit Single-Core
Speed	20MHz
Connectivity	CSI, EBI/EMI, I²C, UART/USART
Peripherals	DMA, LVD, PWM, WDT
Number of I/O	50
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 3.6V
Data Converters	A/D 10x10b; D/A 1x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd70f3805gb-r-gah-ax

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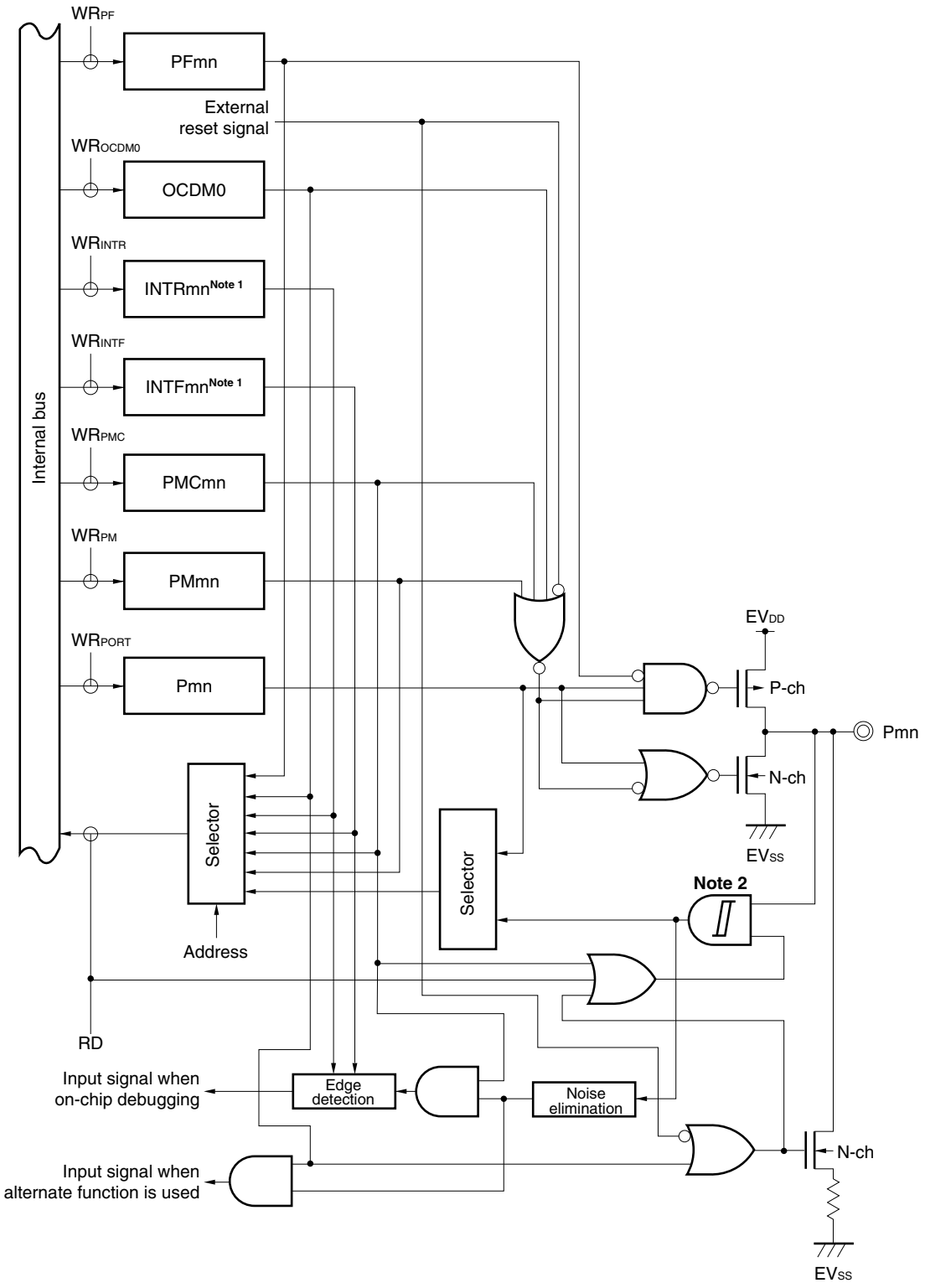
Figure 4-36. Block Diagram of Type AA-1



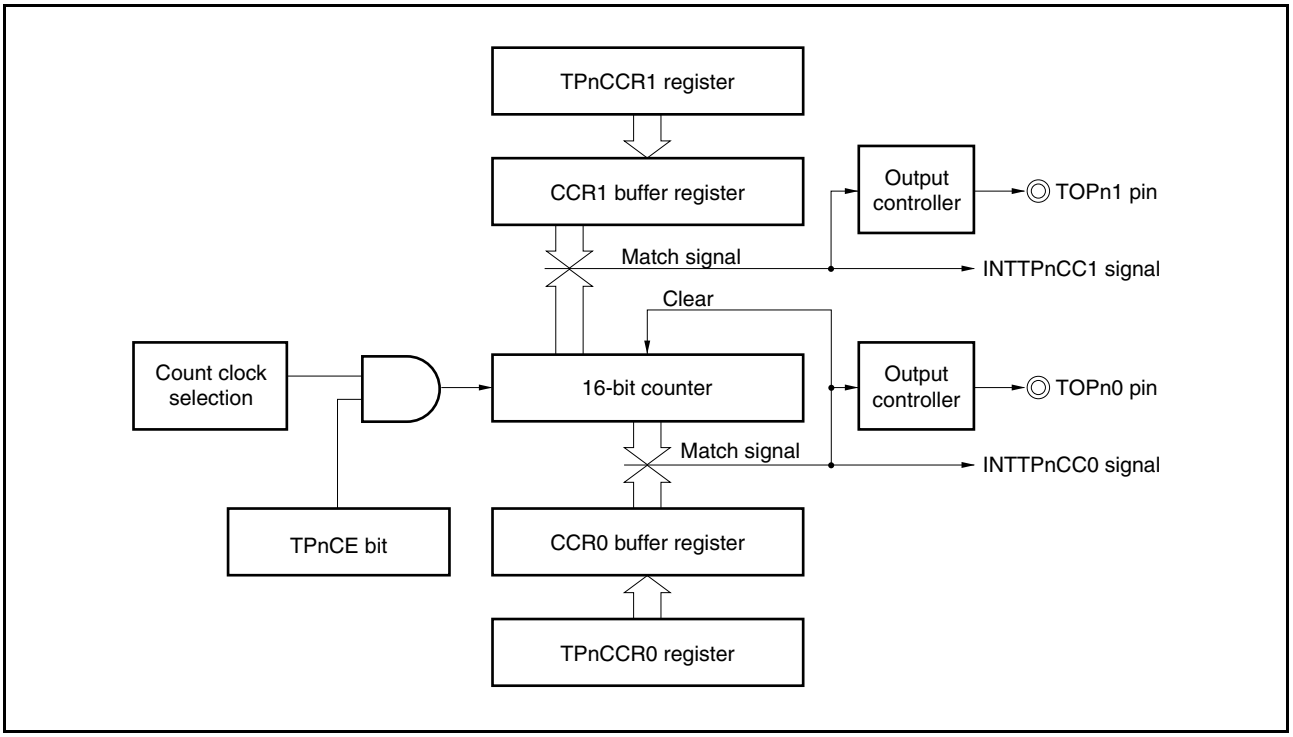
Notes 1. See **19.7 External Interrupt Request Input Pins (NMI and INTP0 to INTP7)**.

2. There are no hysteresis characteristics in port mode.

(d) Operation of TPnCCR1 register

The TPnCCR1 register is configured as follows in the interval timer mode.

Figure 6-13. Configuration of TPnCCR1 Register



(1) Operations in external trigger pulse output mode

Figure 6-29. Timing and Processing of Operations in External Trigger Pulse Output Mode (1/2)

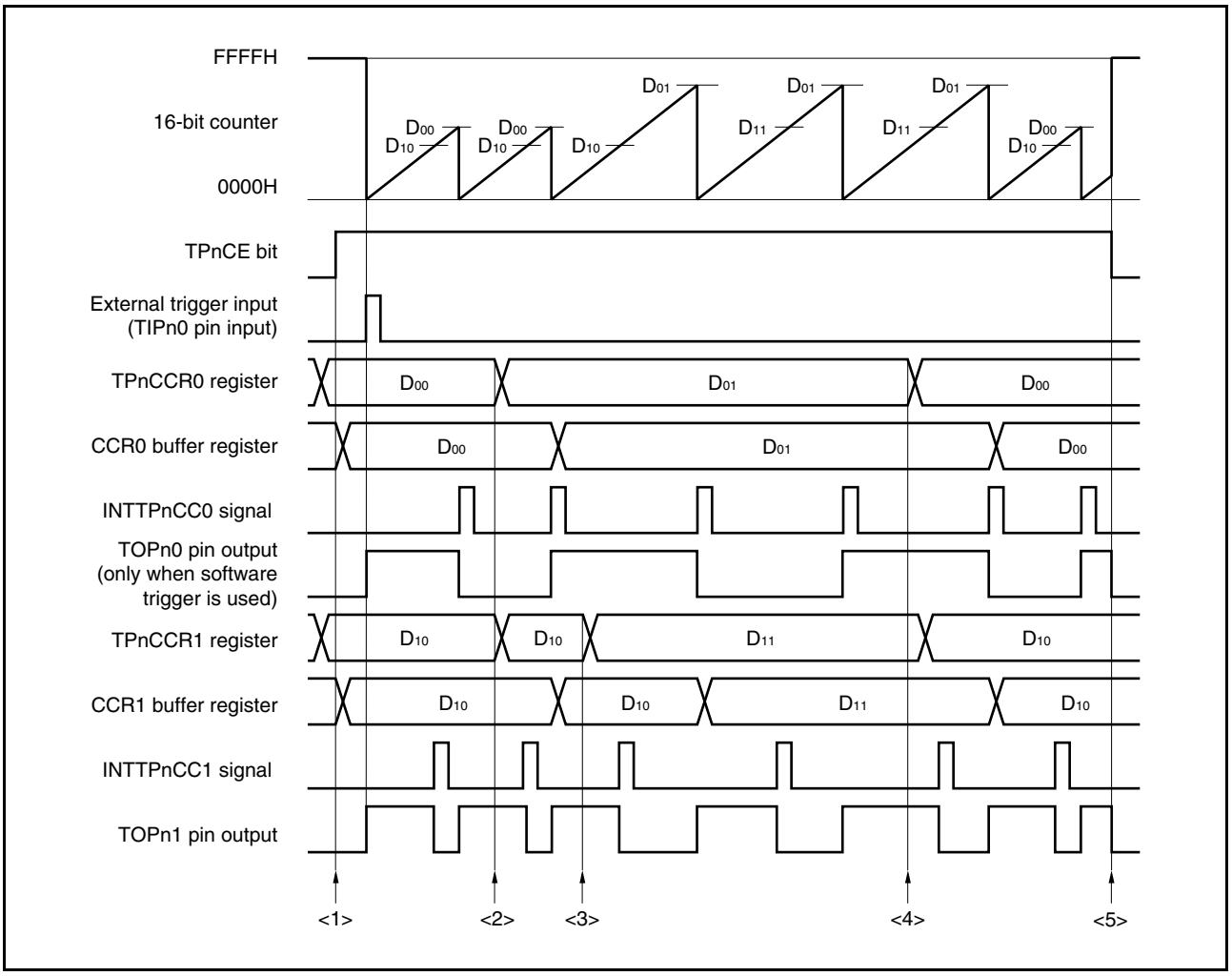
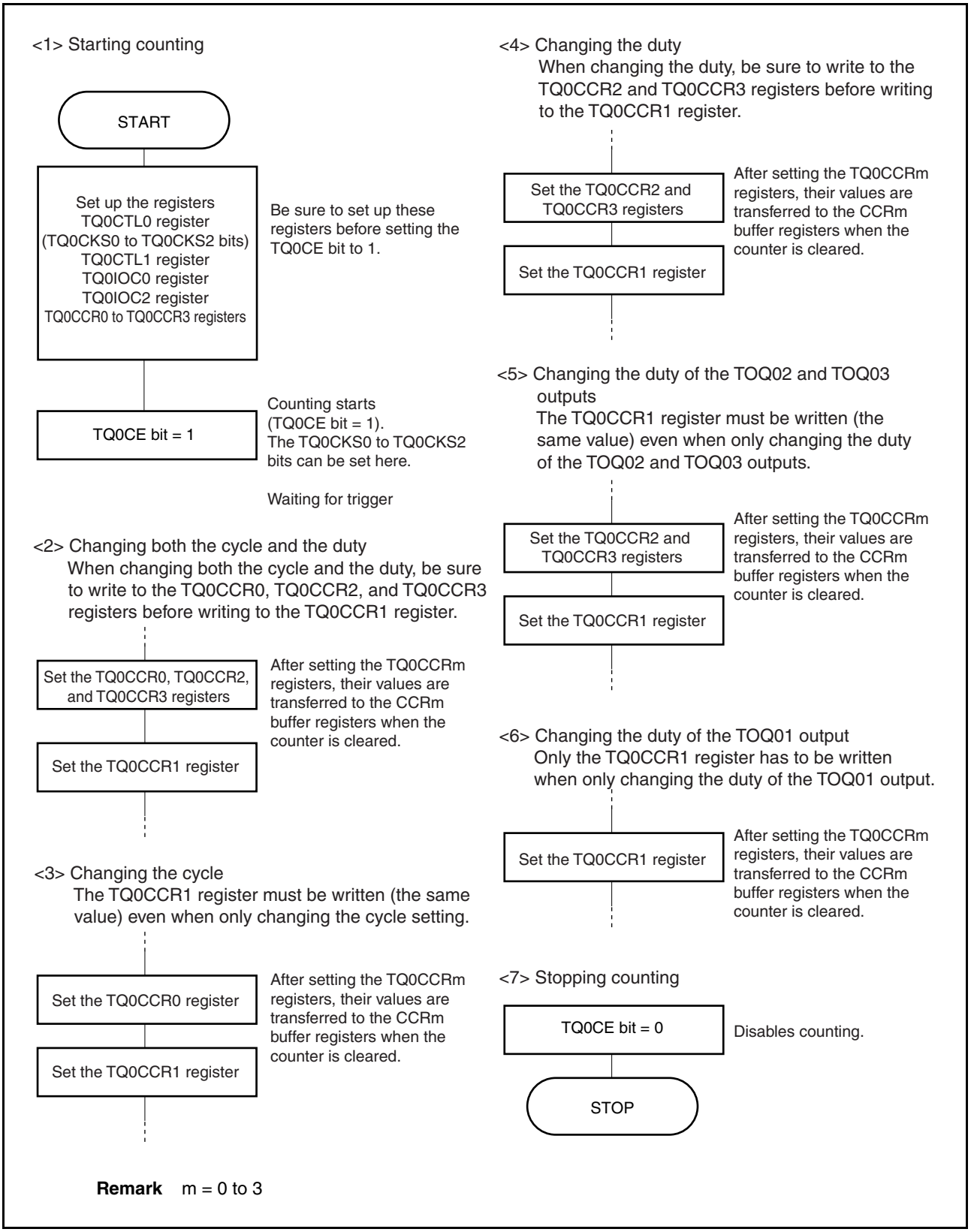


Figure 7-29. Timing and Processing of Operations in External Trigger Pulse Output Mode (2/2)



Remark m = 0 to 3

Figure 7-40. Register Settings in One-Shot Pulse Output Mode (3/3)

(f) TMQ0 capture/compare registers 0 to 3 (TQ0CCR0 to TQ0CCR3)

If the TQ0CCR0 register is set to D_0 and the TQ0CCRk register is set to D_k, the one-shot pulse is as follows:

One-shot pulse active level width = $(D_0 - D_k + 1) \times$ Count clock cycle
One-shot pulse output delay period = $D_k \times$ Count clock cycle

Caution One-shot pulses are not output from the TOQ0k pin in the one-shot pulse output mode if the value of the TQ0CCRk register is greater than the value of the TQ0CCR0 register.

Remarks 1. TMQ0 I/O control register 1 (TQ0IOC1) and TMQ0 option register 0 (TQ0OPT0) are not used in the one-shot pulse output mode.

2. k = 1 to 3

10.2.1 Pin configuration

The RTC outputs included in the real-time counter are alternatively used as shown in Table 10-2. The port function must be set when using each pin (see **Table 4-17 Settings When Pins Are Used for Alternate Functions**).

Table 10-2. Pin Configuration

Pin Number			Port	RTC Output	Other Alternate Function
JC3L(40)	JC3L(48)	JE3L			
12	14	18	P03	RTC1HZ	INTP0/ADTRG
–	–	19	P04	RTCDIV	INTP1/RTCCL
–	–	19	P04	RTCCL	INTP1/RTCDIV

Remark JC3L (40): V850ES/JC3-L (40-pin products)
JC3L (48): V850ES/JC3-L (48-pin products)
JE3L : V850ES/JE3-L

10.2.2 Interrupt functions

The RTC includes the following three types of interrupt signals.

(1) INTRTC0

A fixed-cycle interrupt signal is generated every 0.5 second, second, minute, hour, day, or month.

(2) INTRTC1

Alarm interrupt signal

(3) INTRTC2

An interval interrupt signal of a cycle of $f_{XT}/2^6$, $f_{XT}/2^7$, $f_{XT}/2^8$, $f_{XT}/2^9$, $f_{XT}/2^{10}$, $f_{XT}/2^{11}$, or $f_{XT}/2^{12}$ is generated.

(2) D/A conversion value setting registers 0 (DA0CS0)

The DA0CS0 register sets the analog voltage value output to the ANO0 pin.

These register can be read or written in 8-bit units.

Reset sets these registers to 00H.

After reset: 00H R/W Address: DA0CS0 FFFFF280H, DA0CS1 FFFFF281H

	7	6	5	4	3	2	1	0
DA0CSn	DA0CSn7	DA0CSn6	DA0CSn5	DA0CSn4	DA0CSn3	DA0CSn2	DA0CSn1	DA0CSn0

Caution In the real-time output mode (DA0M.DA0MD0 bit = 1), set the DA0CS0 register before the INTTP2CC0 signal is generated. D/A conversion starts when the INTTP2CC0 signal is generated.

15.2 Configuration

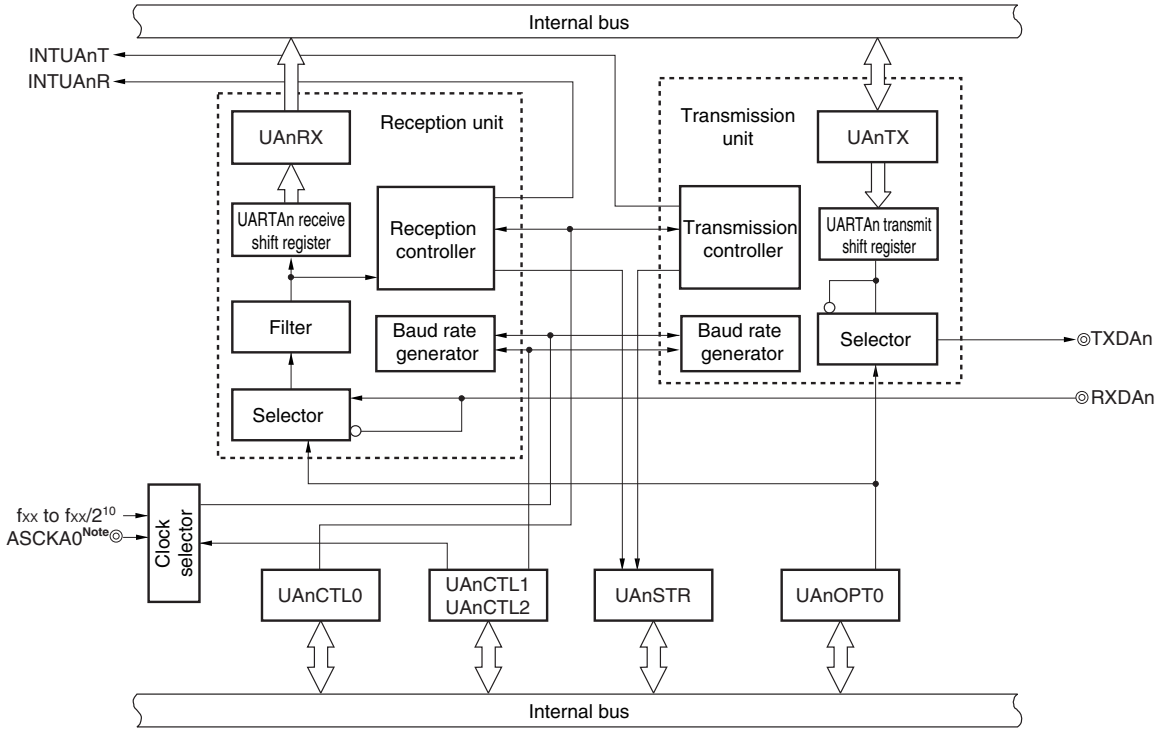
UARTAn includes the following hardware.

Table 15-1. Configuration of UARTAn

Item	Configuration
Registers	UARTAn control register 0 (UAnCTL0) UARTAn control register 1 (UAnCTL1) UARTAn control register 2 (UAnCTL2) UARTAn option control register 0 (UAnOPT0) UARTAn status register (UAnSTR) UARTAn receive shift register UARTAn receive data register (UAnRX) UARTAn transmit shift register UARTAn transmit data register (UAnTX)

The block diagram of the UARTAn is shown below.

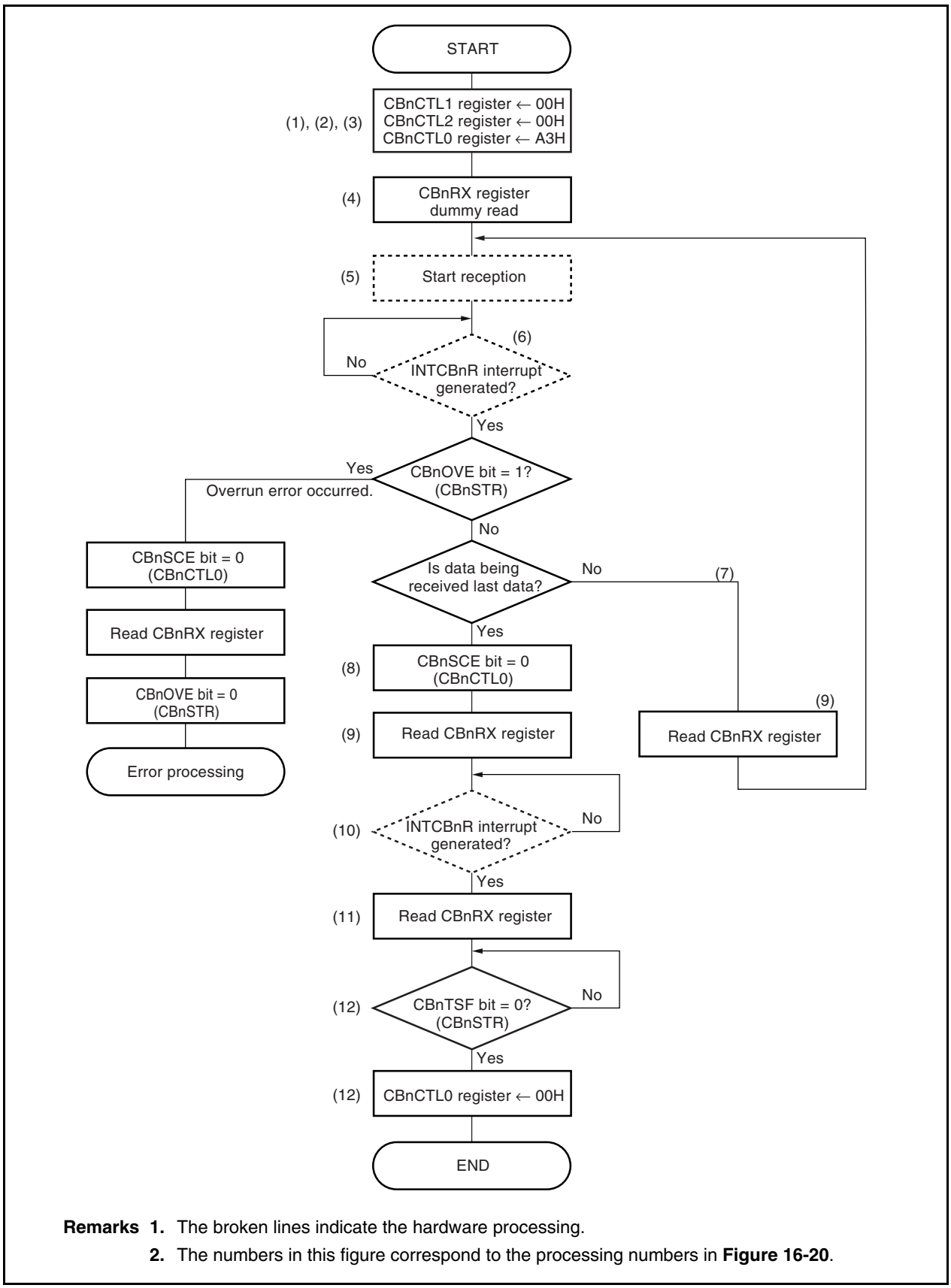
Figure 15-1. Block Diagram of UARTAn



Note UARTA0 only (V850ES/JC3-L (48-pin), V850ES/JE3-L only)

Remark For the configuration of the baud rate generator, see **Figure 15-17**.

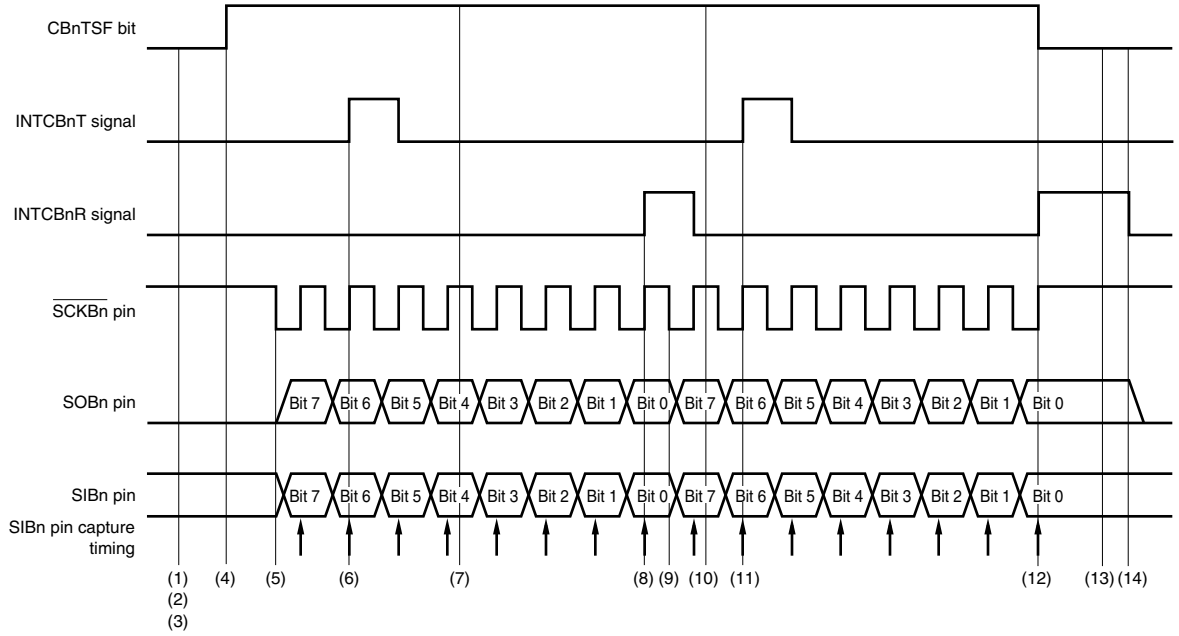
Figure 16-19. Continuous Transfer Mode Operation (Master Mode, Reception Mode)



Remarks 1. The broken lines indicate the hardware processing.

2. The numbers in this figure correspond to the processing numbers in **Figure 16-20**.

Figure 16-22. Continuous Transfer Mode Operation Timing (Master Mode, Transmission/Reception Mode) (1/2)



(1) Write 00H to the CBnCTL1 register, and select communication type 1, communication clock (f_{CCLK}) = f_{XX}/2, and master mode.

(2) Write 00H to the CBnCTL2 register, and set the transfer data length to 8 bits.

(3) Write E3H to the CBnCTL0 register, and select the transmission/reception mode, MSB first, and continuous transfer mode at the same time as enabling the operation of the communication clock (f_{CCLK}).

(4) The CBnSTR.CBnTSF bit is set to 1 by writing the transmit data to the CBnTX register, and transmission/reception is started.

(5) When transmission/reception is started, output the serial clock to the $\overline{\text{SCKBn}}$ pin, output the transmit data to the SOBn pin in synchronization with the serial clock, and capture the receive data of the SIBn pin.

(6) When transfer of the transmit data from the CBnTX register to the shift register is completed and writing to the CBnTX register is enabled, the transmission enable interrupt request signal (INTCBnT) is generated.

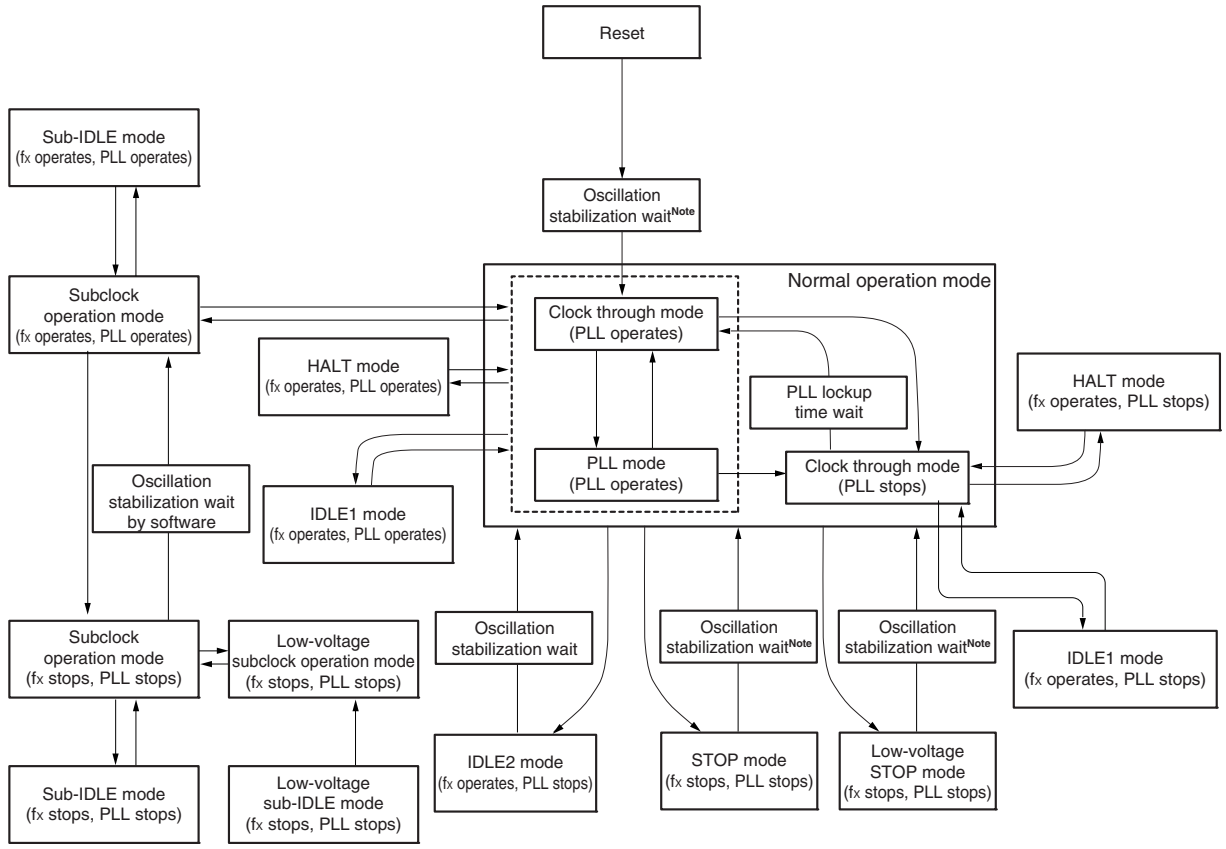
(7) To continue transmission/reception, write the transmit data to the CBnRX register again after the INTCBnT signal is generated.

(8) When one transmission/reception is completed, the reception complete interrupt request signal (INTCBnR) is generated, and reading of the CBnRX register is enabled.

(9) When new transmit data is written to the CBnTX register before communication is complete, the next communication is started following completion of communication.

(10) Read the CBnRX register.

Figure 21-1. Status Transition



Note If a WDT overflow occurs during an oscillation stabilization time, the CPU operates on the internal oscillator clock.

Remark fx: Main clock oscillation

(5) Allocation of communication serial interface

UARTA0, CSIB0, or CSIB3 is used for communication between MINICUBE2 and the target system. The settings related to the serial interface modes are performed by the debug monitor program, but if the setting is changed by the user program, a communication error may occur.

To prevent such a problem from occurring, the communication serial interface must be secured in the user program.

[How to secure the communication serial interface]

- On-chip debug mode register (OCDM)

  For the on-chip debug function using the UARTA0, CSIB0, or CSIB3, set the OCDM register to normal mode. Be sure to set as follows.

  - Input low level to the P05/INTP2/$\overline{\text{DRST}}$ pin.
  - Set the OCDM0 bit as shown below.

    <1> Clear the OCDM0 bit to 0.

    <2> Fix the P05/INTP2/$\overline{\text{DRST}}$ pin input to low level until the processing of <1> is complete.

- Serial interface registers

  Do not set the registers related to CSIB0, CSIB3, or UARTA0 in the user program.

- Interrupt mask register

  When CSIB0 is used, do not mask the transmit end interrupt (INTCB0R). When CSIB3 is used, do not mask the transmit end interrupt (INTCB3R). When UARTA0 is used, do not mask the reception complete interrupt (INTUA0R).

(a) When CSIB0 is used

	7	6	5	4	3	2	1	0
CB0RIC	×	0	×	×	×	×	×	×

(b) When CSIB3 is used

	7	6	5	4	3	2	1	0
CB3RIC	×	0	×	×	×	×	×	×

(C) When UARTA0 is used

	7	6	5	4	3	2	1	0
UA0RIC	×	0	×	×	×	×	×	×

Remark ×: don't care

- Port registers when CSIB3 is used

  When CSIB3 is used, port registers are set by the debug monitor program to make the SIB3, SOB3, $\overline{\text{SCKB3}}$, and HS (PCM0) pins valid. Do not change the following register settings in the user program during debugging. (The same value can be written again.)

(a) SIB3, SOB3, and $\overline{\text{SCKB3}}$ settings

	7	6	5	4	3	2	1	0
PFC9H	×	×	×	1	1	1	×	×

	7	6	5	4	3	2	1	0
PMC9H	×	×	×	1	1	1	×	×

(b) HS (PCM0 pin) settings

	7	6	5	4	3	2	1	0
PMCM	×	×	×	×	×	×	×	0

	7	6	5	4	3	2	1	0
PCM	×	×	×	×	×	×	×	**Note**

Note Writing to this bit is prohibited.
The port values corresponding to the HS pin are changed by the monitor program according to the debugger status. To specify port register settings in 8-bit units, read-modify-write can usually be used in the user program. If an interrupt for debugging occurs before writing, however, an unexpected operation may be performed.

Remark ×: don't care

29.3 ROM Security Function

29.3.1 Security ID

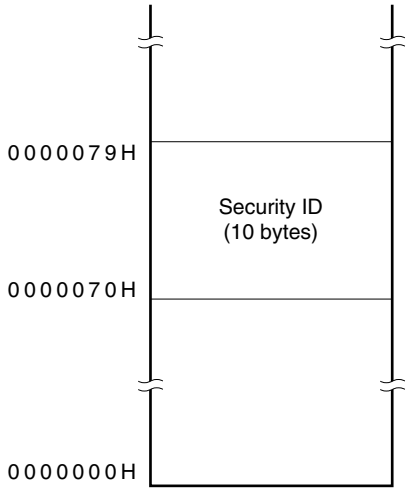
The flash memory versions of the V850ES/JC3-L and V850ES/JE3-L perform authentication using a 10-byte ID code to prevent the contents of the flash memory from being read by an unauthorized person during on-chip debugging by the on-chip debug emulator.

Set the ID code in the 10-byte internal flash memory area from 0000070H to 0000079H to allow the debugger perform ID authentication.

If the IDs match, the security is released and reading the flash memory and using the on-chip debug emulator are enabled.

- Set the 10-byte ID code to 0000070H to 0000079H.
- Bit 7 of 0000079H is the on-chip debug emulator enable flag.
  (0: Disable, 1: Enable)
- When the on-chip debug emulator is started, the debugger requests ID input. When the ID code input to the debugger and the ID code set in 0000070H to 0000079H match, the debugger starts.
- Debugging cannot be performed if the on-chip debug emulator enable flag is 0, even if the ID codes match.

Figure 29-6. Security ID Area



Caution After the flash memory is erased, 1 is written to the entire area.

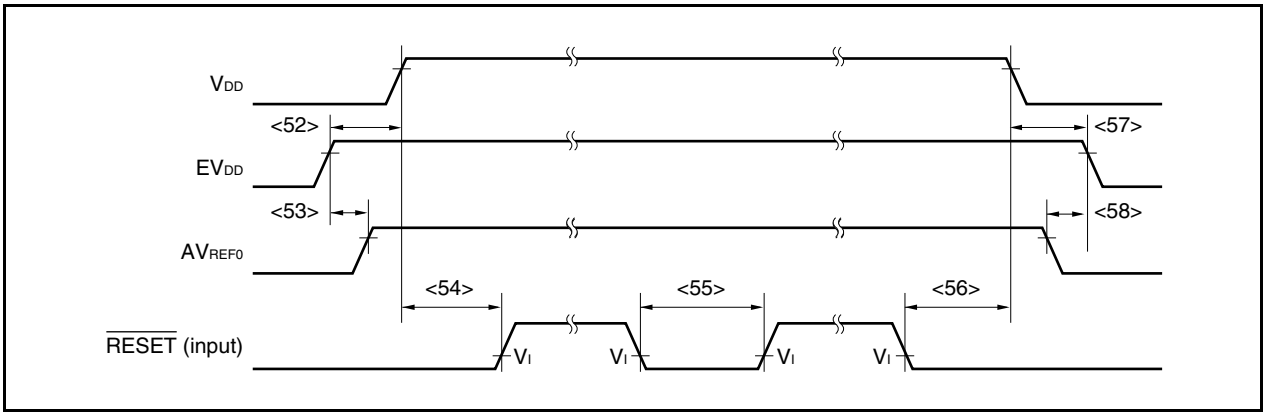
31.7.2 Power on/power off/reset timing

(T_A = –40 to +85°C, V_{DD} = EV_{DD} = AV_{REF0} = AV_{REF1} = 2.2 to 3.6 V, V_{SS} = EV_{SS} = AV_{SS} = 0 V, C_L = 50 pF)

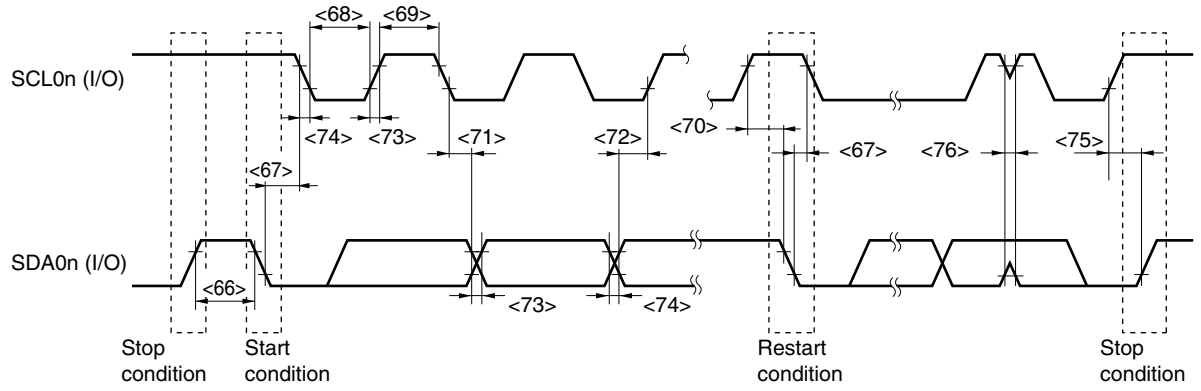
Parameter	Symbol		Conditions	MIN.	MAX.	Unit
$EV_{DD}\uparrow \rightarrow V_{DD}\uparrow$	t_{REL}	<52>		0		ns
$EV_{DD}\uparrow \rightarrow AV_{REF0}$, $AV_{REF1}\uparrow$	t_{REA}	<53>		0	t_{REL}	ns
$V_{DD}\uparrow \rightarrow \overline{RESET}\uparrow$	t_{RER}	<54>		500 + t_{REG} Note		ns
$\overline{RESET}$ low-level width	t_{WRSL}	<55>		500		ns
$\overline{RESET}\downarrow \rightarrow V_{DD}\downarrow$	t_{FRE}	<56>		500		ns
$V_{DD}\downarrow \rightarrow EV_{DD}\downarrow$	t_{FEL}	<57>		0		ns
$AV_{REF0}\downarrow \rightarrow EV_{DD}\downarrow$	t_{FEA}	<58>		0	t_{FEL}	ns

Note See **31.5 Regulator Characteristics**.

Remark The $\overline{RESET}$ pin has an analog noise elimination function.



I²C Bus Timing



Remark **n = 0 to 2**

31.8.7 A/D converter

(T_A = –40 to +85°C, V_{DD} = EV_{DD} = AV_{REF0} = AV_{REF1}, 2.7 V ≤ AV_{REF0} = AV_{REF1} ≤ 3.6 V, V_{SS} = EV_{SS} = AV_{SS} = 0 V, C_L = 50 pF)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution					10	bit
Overall error[Note]		2.7 V ≤ AV_{REF0} ≤ 3.6 V			±0.6	%FSR
A/D conversion time	t_{CONV}	3.0 V ≤ AV_{REF0} ≤ 3.6 V	2.6		24	μs
		2.7 V ≤ AV_{REF0} ≤ 3.0 V	3.9		24	μs
Zero scale error					±0.5	%FSR
Full scale error					±0.5	%FSR
Non-linearity error					±4.0	LSB
Differential linearity error					±4.0	LSB
Analog input voltage	V_{IAN}		AV_{SS}		AV_{REF0}	V
Reference voltage	AV_{REF0}		2.7		3.6	V
AV_{REF0} current	AI_{REF0}	Normal conversion mode		3	6.5	mA
		High-speed conversion mode		4	10	mA
		When A/D converter unused			5	μA

Note Excluding quantization error (±0.05 %FSR).

Caution Do not set (read/write) alternate-function ports during A/D conversion; otherwise the conversion resolution may be degraded.

Remark LSB: Least Significant Bit
FSR: Full Scale Range

(3) Programming characteristics

(T_A = –40 to +85°C, V_{DD} = EV_{DD} = AV_{REF0} = AV_{REF1} = 2.7 to 3.6 V, V_{SS} = EV_{SS} = AV_{SS} = 0 V, C_L = 50 pF)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Chip erase time		f_{XX} = 20 MHz (when the chip erase command is executed)		105		ms
Write time per 256 bytes		f_{XX} = 20 MHz		2.0		ms
Block internal verify time		f_{XX} = 20 MHz		10		ms
Block blank check time		f_{XX} = 20 MHz		0.5		ms
Flash memory information setting time		f_{XX} = 20 MHz		30		ms

Remark Block size = 2 KB

APPENDIX B MAJOR DIFFERENCES BETWEEN PRODUCTS

Table B-1. Major Differences between V850ES/Jx3-L products

Major Differences		V850ES/JC3-L		V850ES/JE3-L	V850ES/JF3-L	V850ES/JG3-L		
Device name		μPD70F3797, 70F3798, 70F3799, 70F3800, 70F3838	μPD70F3801, 70F3802, 70F3803, 70F3804, 70F3839	μPD70F3805, 70F3806, 70F3807, 70F3808, 70F3840	μPD70F3735, 70F3736	μPD70F3737, 70F3738	μPD70F3792, 70F3793/ 70F3841/ 70F3842	μPD70F3794, 70F3795, 70F3796
Pin		40	48	64	80	100/121	100/121	100/121
memory	Internal flash memory	16/32/64/128/ 256 KB	16/32/64/128/ 256 KB	16/32/64/128/ 256 KB	128/256 KB	128/256 KB	384/512/768/ 1024 KB	256/384/512 KB
	Internal RAM	8/16 KB	8/16 KB	8/16 KB	8/16 KB	8/16 KB	32/40/80 KB	40 KB
External bus	Bus type	–	–	–	Multiplexed bus	Separate bus /multiplexed bus	Separate bus /multiplexed bus[Note]	Separate bus /multiplexed bus[Note]
	Address bus	–	–	–	18	22	22	22
	Address data bus	–	–	–	16	16	16	16
I/O port		27	34	50	66	84	83	80
Timer	16-bit TMP	6 ch	6 ch	6 ch	4 ch	6 ch	6 ch	6 ch
	16-bit TMQ	1 ch	1 ch	1 ch	1 ch	1 ch	1 ch	1 ch
	16-bit TMM	1 ch	1 ch	1 ch	1 ch	1 ch	1 ch	1 ch
	Watch timer	1 ch	1 ch	1 ch	1 ch	1 ch	1 ch	1 ch
	RTC	1 ch	1 ch	1 ch	–	–	1 ch	1 ch
	WDT	1 ch	1 ch	1 ch	1 ch	1 ch	1 ch	1 ch
10-bit A/D converter		5 ch	6 ch	10 ch	8 ch	12 ch	12 ch	12 ch
8-bit D/A converter		–	1 ch	1 ch	1 ch	2 ch	2 ch	2 ch
Serial interface	CSIB	2 ch	4 ch	5 ch	3 ch	5 ch	5 ch	5 ch
	UARTA	2 ch	3 ch	3 ch	3 ch	3 ch	6 ch	6 ch
	UARTC	–	–	–	–	–	1 ch	1 ch
	I^2C	2 ch	3 ch	3 ch	2 ch	3 ch	3 ch	3 ch
	USBF	–	–	–	–	–	–	1 ch
DMA controller		4 ch	4 ch	4 ch	4 ch	4 ch	4 ch	4 ch
Interrupt source	External	6	6	9	9	9	9	9
	Internal	42	46	48	40	48	55	55
RTC backup mode		None	None	None	None	None	Available	Available
Operating power supply voltage		2.2 to 3.6V	2.2 to 3.6V	2.2 to 3.6V	2.2 to 3.6V	2.2 to 3.6V	2.0 to 3.6V	2.0 to 3.6V
Package		40-pinWQFN (6×6 mm)	48-pinWQFN (7×7 mm), 48-pinLQFP (7×7 mm)	64-pinLQFP (10×10 mm)	80-pinLQFP (14×14 mm), 80-pinLQFP (12×12 mm)	100-pinLQFP (14×14 mm), 121-pinFBGA (8×8 mm)	100-pinLQFP (14×14 mm), 121-pinFBGA (8×8 mm)	100-pinLQFP (14×14 mm), 121-pinFBGA (8×8 mm)

Note μPD70F3794, 70F3975, 70F3796, 70F3841, and 70F3842 are Multiplexed bus mode (capable of separate output)

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Symbol	Name	Unit	Page
ECR	Interrupt source register	CPU	55
EIPC	Interrupt status saving register	CPU	54
EIPSW	Interrupt status saving register	CPU	54
FEPC	NMI status saving register	CPU	55
FEPSW	NMI status saving register	CPU	55
IIC0	IIC shift register 0	I^2C	635
IIC1	IIC shift register 1	I^2C	635
IIC2	IIC shift register 2	I^2C	635
IICC0	IIC control register 0	I^2C	621
IICC1	IIC control register 1	I^2C	621
IICC2	IIC control register 2	I^2C	621
IICCL0	IIC clock select register 0	I^2C	631
IICCL1	IIC clock select register 1	I^2C	631
IICCL2	IIC clock select register 2	I^2C	631
IICF0	IIC flag register 0	I^2C	629
IICF1	IIC flag register 1	I^2C	629
IICF2	IIC flag register 2	I^2C	629
IICIC0	Interrupt control register	INTC	729
IICIC1	Interrupt control register	INTC	729
IICIC2	Interrupt control register	INTC	729
IICS0	IIC status register 0	I^2C	626
IICS1	IIC status register 1	I^2C	626
IICS2	IIC status register 2	I^2C	626
IICX0	IIC function expansion register 0	I^2C	632
IICX1	IIC function expansion register 1	I^2C	632
IICX2	IIC function expansion register 2	I^2C	632
IMR0	Interrupt mask register 0	INTC	731
IMR0H	Interrupt mask register 0H	INTC	731
IMR0L	Interrupt mask register 0L	INTC	731
IMR1	Interrupt mask register 1	INTC	731
IMR1H	Interrupt mask register 1H	INTC	731
IMR1L	Interrupt mask register 1L	INTC	731
IMR2	Interrupt mask register 2	INTC	731
IMR2H	Interrupt mask register 2H	INTC	731
IMR2L	Interrupt mask register 2L	INTC	731
IMR3	Interrupt mask register 3	INTC	731
IMR3H	Interrupt mask register 3H	INTC	731
IMR3L	Interrupt mask register 3L	INTC	731
INTF0	External interrupt falling edge specification register 0	INTC	744
INTF3	External interrupt falling edge specification register 3	INTC	745
INTF9H	External interrupt falling edge specification register 9H	INTC	746
INTR0	External interrupt rising edge specification register 0	INTC	744
INTR3	External interrupt rising edge specification register 3	INTC	745