Renesas Electronics America Inc - UPD70F3807GB(R)-GAH-AX Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	V850ES
Core Size	32-Bit Single-Core
Speed	20MHz
Connectivity	CSI, EBI/EMI, I²C, UART/USART
Peripherals	DMA, LVD, PWM, WDT
Number of I/O	50
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 3.6V
Data Converters	A/D 10x10b; D/A 1x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd70f3807gb-r-gah-ax

1.3 Application Fields

Digital cameras, electrical power meters, mobile terminals, digital home electronics, other consumer devices

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1.4 Ordering Information

1.4.1 V850ES/JC3-L

Part Number	Package	Internal Flash Memory
μPD70F3797K8-4B4-AX	40-pin plastic WQFN (6 × 6)	16 KB
μPD70F3798K8-4B4-AX	40-pin plastic WQFN (6 × 6)	32 KB
μPD70F3799K8-4B4-AX	40-pin plastic WQFN (6 × 6)	64 KB
μPD70F3800K8-4B4-AX	40-pin plastic WQFN (6 × 6)	128 KB
μPD70F3838K8-4B4-AX	40-pin plastic WQFN (6 × 6)	256 KB
μPD70F3801GA-GAM-AX	48-pin plastic LQFP (fine pitch) (7 × 7)	16 KB
μPD70F3802GA-GAM-AX	48-pin plastic LQFP (fine pitch) (7 × 7)	32 KB
μPD70F3803GA-GAM-AX	48-pin plastic LQFP (fine pitch) (7 × 7)	64 KB
μPD70F3804GA-GAM-AX	48-pin plastic LQFP (fine pitch) (7 × 7)	128 KB
μPD70F3839GA-GAM-AX	48-pin plastic LQFP (fine pitch) (7 × 7)	256 KB
μPD70F3801K8-5B4-AX	48-pin plastic WQFN (7 × 7)	16 KB
μPD70F3802K8-5B4-AX	48-pin plastic WQFN (7 × 7)	32 KB
μPD70F3803K8-5B4-AX	48-pin plastic WQFN (7 × 7)	64 KB
μPD70F3804K8-5B4-AX	48-pin plastic WQFN (7 × 7)	128 KB
μPD70F3839K8-5B4-AX	48-pin plastic WQFN (7 × 7)	256 KB

Remark The V850ES/JC3-L is a lead-free product.

1.4.2 V850ES/JE3-L

Part Number	Package	Internal Flash Memory
μPD70F3805GB-GAH-AX	64-pin plastic LQFP (fine pitch) (10 × 10)	16 KB
μPD70F3806GB-GAH-AX	64-pin plastic LQFP (fine pitch) (10 × 10)	32 KB
μPD70F3807GB-GAH-AX	64-pin plastic LQFP (fine pitch) (10 × 10)	64 KB
μPD70F3808GB-GAH-AX	64-pin plastic LQFP (fine pitch) (10 × 10)	128 KB
μPD70F3840GB-GAH-AX	64-pin plastic LQFP (fine pitch) (10 × 10)	256 KB

Remark The V850ES/JE3-L is a lead-free product.

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Address	Function Register Name	Symbol	R/W	Manipulatable Bits			Default Value
				1	8	16	
FFFFF590H	TMP0 control register 0	TP0CTL0	R/W	√	√		00H
FFFFF591H	TMP0 control register 1	TP0CTL1		√	√		00H
FFFFF592H	TMP0 I/O control register 0	TP0IOC0		√	√		00H
FFFFF593H	TMP0 I/O control register 1	TP0IOC1		√	√		00H
FFFFF594H	TMP0 I/O control register 2	TP0IOC2		√	√		00H
FFFFF595H	TMP0 option register 0	TP0OPT0		√	√		00H
FFFFF596H	TMP0 capture/compare register 0	TP0CCR0				√	0000H
FFFFF598H	TMP0 capture/compare register 1	TP0CCR1				√	0000H
FFFFF59AH	TMP0 counter read buffer register	TP0CNT	R			√	0000H
FFFFF5A0H	TMP1 control register 0	TP1CTL0	R/W	√	√		00H
FFFFF5A1H	TMP1 control register 1	TP1CTL1		√	√		00H
FFFFF5A2H	TMP1 I/O control register 0	TP1IOC0		√	√		00H
FFFFF5A3H	TMP1 I/O control register 1	TP1IOC1		√	√		00H
FFFFF5A4H	TMP1 I/O control register 2	TP1IOC2		√	√		00H
FFFFF5A5H	TMP1 option register 0	TP1OPT0		√	√		00H
FFFFF5A6H	TMP1 capture/compare register 0	TP1CCR0				√	0000H
FFFFF5A8H	TMP1 capture/compare register 1	TP1CCR1				√	0000H
FFFFF5AAH	TMP1 counter read buffer register	TP1CNT	R			√	0000H
FFFFF5B0H	TMP2 control register 0	TP2CTL0	R/W	√	√		00H
FFFFF5B1H	TMP2 control register 1	TP2CTL1		√	√		00H
FFFFF5B2H	TMP2 I/O control register 0	TP2IOC0		√	√		00H
FFFFF5B3H	TMP2 I/O control register 1	TP2IOC1		√	√		00H
FFFFF5B4H	TMP2 I/O control register 2	TP2IOC2		√	√		00H
FFFFF5B5H	TMP2 option register 0	TP2OPT0		√	√		00H
FFFFF5B6H	TMP2 capture/compare register 0	TP2CCR0				√	0000H
FFFFF5B8H	TMP2 capture/compare register 1	TP2CCR1				√	0000H
FFFFF5BAH	TMP2 counter read buffer register	TP2CNT	R			√	0000H
FFFFF5C0H	TMP3 control register 0	TP3CTL0	R/W	√	√		00H
FFFFF5C1H	TMP3 control register 1	TP3CTL1		√	√		00H
FFFFF5C2H	TMP3 I/O control register 0	TP3IOC0		√	√		00H
FFFFF5C3H	TMP3 I/O control register 1	TP3IOC1		√	√		00H
FFFFF5C5H	TMP3 option register 0	TP3OPT0		√	√		00H
FFFFF5C6H	TMP3 capture/compare register 0	TP3CCR0				√	0000H
FFFFF5C8H	TMP3 capture/compare register 1	TP3CCR1				√	0000H
FFFFF5CAH	TMP3 counter read buffer register	TP3CNT	R			√	0000H
FFFFF5D0H	TMP4 control register 0	TP4CTL0	R/W	√	√		00H
FFFFF5D1H	TMP4 control register 1	TP4CTL1		√	√		00H
FFFFF5D2H	TMP4 I/O control register 0	TP4IOC0		√	√		00H
FFFFF5D3H	TMP4 I/O control register 1	TP4IOC1		√	√		00H
FFFFF5D4H	TMP4 I/O control register 2	TP4IOC2		√	√		00H
FFFFF5D5H	TMP4 option register 0	TP4OPT0		√	√		00H

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(c) V850ES/JE3-L (2/2)

PMC97	Specification of pin operation
0	I/O port (P97)
1	SIB1 input/TIP20 input/TOP20 output

PMC96	Specification of pin operation
0	I/O port (P96)
1	TIP21 input/TOP21 output

PMC94	Specification of pin operation
0	I/O port (P94)
1	TIP31 input/TOP31 output

PMC93	Specification of pin operation
0	I/O port (P93)
1	TIP40 input/TOP40 output

PMC92	Specification of pin operation
0	I/O port (P92)
1	TIP41 input/TOP41 output

PMC91	Specification of pin operation
0	I/O port (P91)
1	KR7 input/RXDA1 input/SCL02 I/O

PMC90	Specification of pin operation
0	I/O port (P90)
1	KR6 input/TXDA1 output/SDA02 I/O

Remarks 1. The PMC9 register can be read or written in 16-bit units.
However, when using the higher 8 bits of the PMC9 register as the PMC9H register and the lower 8 bits as the PMC9L register, PMC9 can be read or written in 8-bit or 1-bit units.

2. To read/write bits 8 to 15 of the PMC9 register in 8-bit or 1-bit units, specify them as bits 0 to 7 of the PMC9H register.

PFCE96	PFC96	Specification of P96 pin alternate function
0	0	Setting prohibited
0	1	Setting prohibited
1	0	TIP21 input
1	1	TOP21 output

PFCE94 Note1	PFC94 Note1	Specification of P94 pin alternate function
0	0	Setting prohibited
0	1	TIP31 input
1	0	TOP31 output
1	1	Setting prohibited

PFCE93 Note1	PFC93 Note1	Specification of P93 pin alternate function
0	0	Setting prohibited
0	1	TIP40 input
1	0	TOP40 output
1	1	Setting prohibited

PFCE92 Note1	PFC92 Note1	Specification of P92 pin alternate function
0	0	Setting prohibited
0	1	TIP41 input
1	0	TOP41 output
1	1	Setting prohibited

PFCE91	PFC91	Specification of P91 pin alternate function
0	0	Setting prohibited
0	1	KR7 input
1	0	RXDA1 input/KR7 input Note2
1	1	SCL02 I/O

PFCE90	PFC90	Specification of P90 pin alternate function
0	0	Setting prohibited
0	1	KR6 input
1	0	TXDA1 output
1	1	SDA02 I/O

Notes1. V850ES/JE3-L only

2. The RXDA1 and KR7 functions cannot be used at the same time. When using the pin for RXDA1, do not use the KR7 function. When using the pin for KR7, do not use the RXDA1 function. (It is recommended to set the PFC91 bit to 1 and clear the PFCE91 bit to 0.)

Figure 4-6. Block Diagram of Type A-2

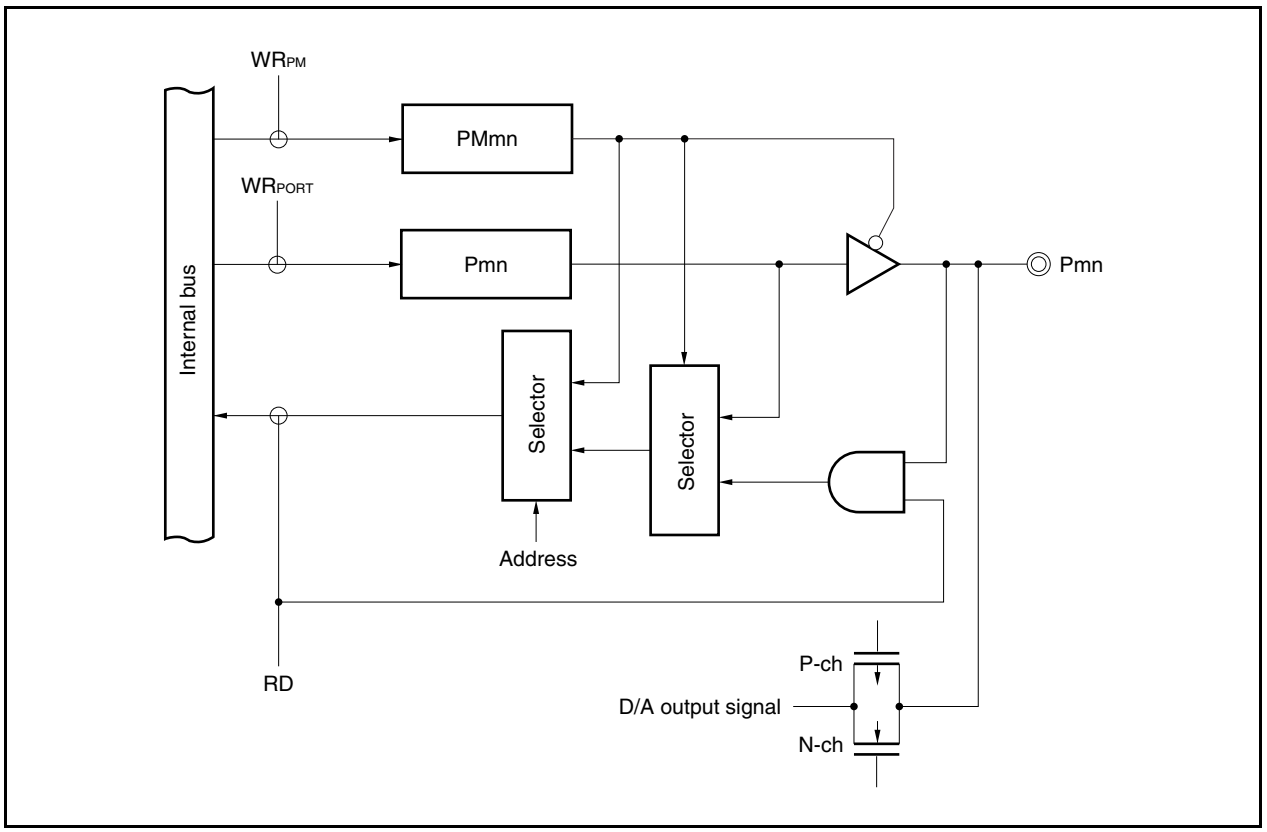
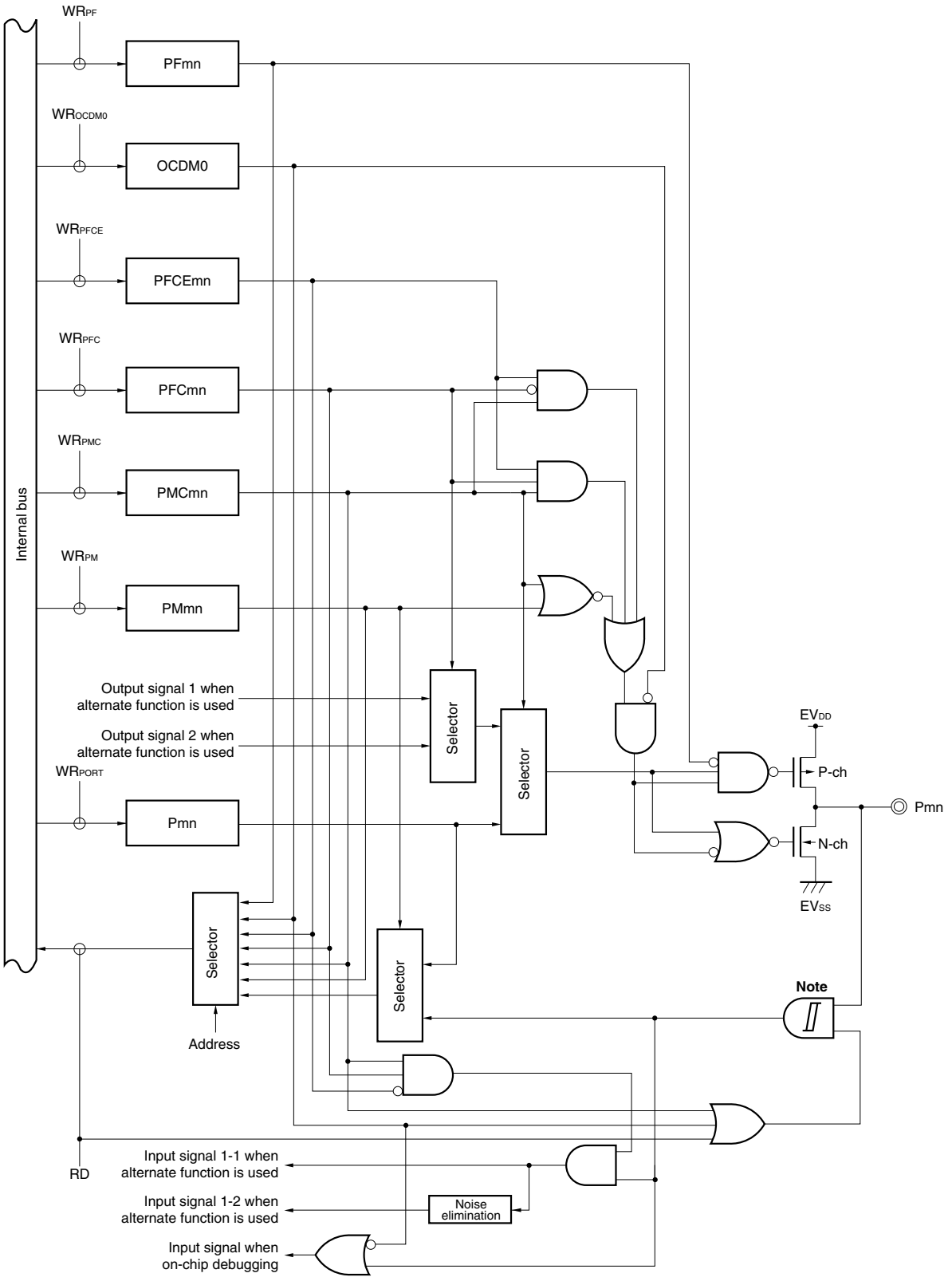


Figure 4-24. Block Diagram of Type U-6



Note There are no hysteresis characteristics in port mode.

5.5.3 Usage

(1) When PLL is used

- After the reset signal has been released, the PLL operates (PLLCTL.PLLON bit = 1), but because the default mode is the clock-through mode (PLLCTL.SELPLL bit = 0), select the PLL mode (SELPLL bit = 1).
- To enable PLL operation, first set the PLLON bit to 1, and then set the SELPLL bit to 1 after the LOCKR.LOCK bit becomes 0. To stop the PLL, first select the clock-through mode (SELPLL bit = 0), wait for 8 clocks or more, and then stop the PLL (PLLON bit = 0).
- The PLL stops during transition to the IDLE2 or STOP mode regardless of the setting and is restored from the IDLE2 or STOP mode to the status before transition. The time required for restoration is as follows.

(a) When transitioning to the IDLE2 or STOP mode from the clock through mode

- STOP mode: Set the OSTS register so that the oscillation stabilization time is at least 400 μs.
- IDLE2 mode: Set the OSTS register so that the setup time is at least 200 μs.

(b) When transitioning to the IDLE 2 or STOP mode while remaining in the PLL operation mode

- STOP mode: Set the OSTS register so that the oscillation stabilization time is at least 400 μs.
- IDLE2 mode: Set the OSTS register so that the setup time is at least 400 μs.

When transitioning to the IDLE1 mode, the PLL does not stop. Stop the PLL if necessary.

(2) When PLL is not used

- The clock-through mode (SELPLL bit = 0) is selected after the reset signal has been released, but the PLL is operating (PLLON bit = 1) and must therefore be stopped (PLLON bit = 0).
  The time required for restoration from the IDLE2 and STOP modes is as follows.

- STOP mode: Set the OSTS register so that the oscillation stabilization time is at least 400 μs.
- IDLE2 mode: Set the OSTS register so that the setup time is at least 200 μs.

(2) TMQ0 control register 1 (TQ0CTL1)

The TQ0CTL1 register is an 8-bit register that controls the operation of TMQ0.

This register can be read or written in 8-bit or 1-bit units.

Reset sets this register to 00H.

After reset: 00H R/W Address: FFFFF541H

	7	<6>	<5>	4	3	2	1	0
TQ0CTL1	0	TQ0EST	TQ0EEE	0	0	TQ0MD2	TQ0MD1	TQ0MD0

TQ0EST	Software trigger control
0	–
1	Generate a valid signal for external trigger input. • In one-shot pulse output mode: A one-shot pulse is output with writing 1 to the TQ0EST bit as the trigger. • In external trigger pulse output mode: A PWM waveform is output with writing 1 to the TQ0EST bit as the trigger.

TQ0EEE	Count clock selection
0	Disable operation with external event count input. (Perform counting using the internal count clock selected by the TQ0CLT0.TQ0CK0 to TQ0CK2 bits.)
1	Enable operation with external event count input. (Perform counting at the valid edge of the external event count input signal.)

TQ0MD2	TQ0MD1	TQ0MD0	Timer mode selection
0	0	0	Interval timer mode
0	0	1	External event count mode
0	1	0	External trigger pulse output mode
0	1	1	One-shot pulse output mode
1	0	0	PWM output mode
1	0	1	Free-running timer mode
1	1	0	Pulse width measurement mode
1	1	1	Setting prohibited

Cautions 1. The TQ0EST bit is valid only in the external trigger pulse output mode or one-shot pulse output mode. In any other mode, writing 1 to this bit is ignored.

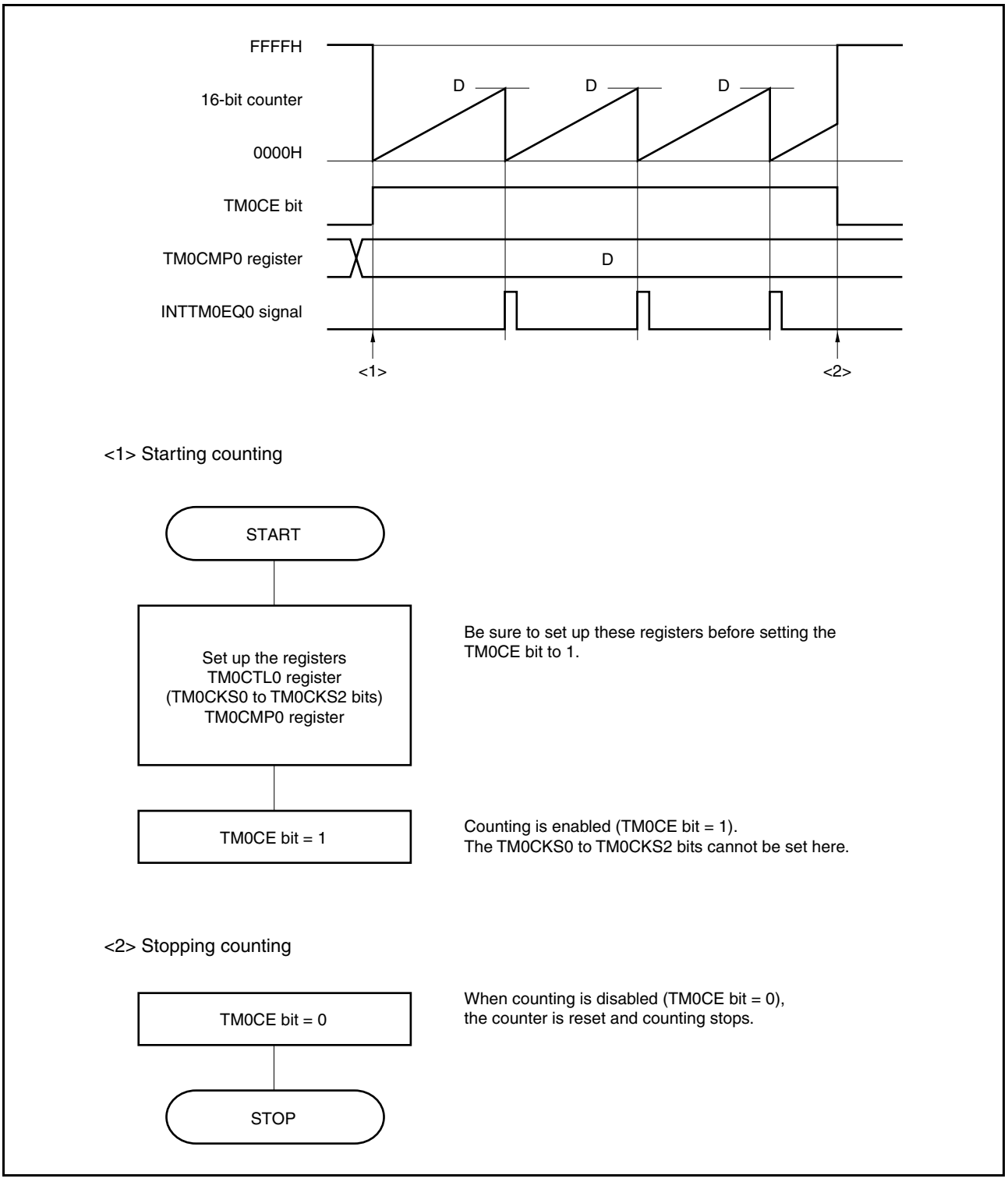
2. External event count input is selected in the external event count mode regardless of the value of the TQ0EEE bit.

3. Set the TQ0EEE and TQ0MD2 to TQ0MD0 bits after stopping the timer (by setting the TQ0CTL0.TQ0CE bit to 0). (However, if the same value is being written, this can be done while the TQ0CE bit is 1.) The operation is not guaranteed if the TQ0EEE and TQ0MD2 to TQ0MD0 bits are rewritten while the TQ0CE bit is 1. If the TQ0EEE and TQ0MD2 to TQ0MD0 bits were mistakenly rewritten while the TQ0CE bit was 1, clear the TQ0CE bit to 0 and then write the bits again.

4. Be sure to clear bits 3, 4, and 7 to "0".

(1) Operations in interval timer mode

Figure 8-5. Timing and Processing of Operations in Interval Timer Mode



10.2 Configuration

The real-time counter includes the following hardware.

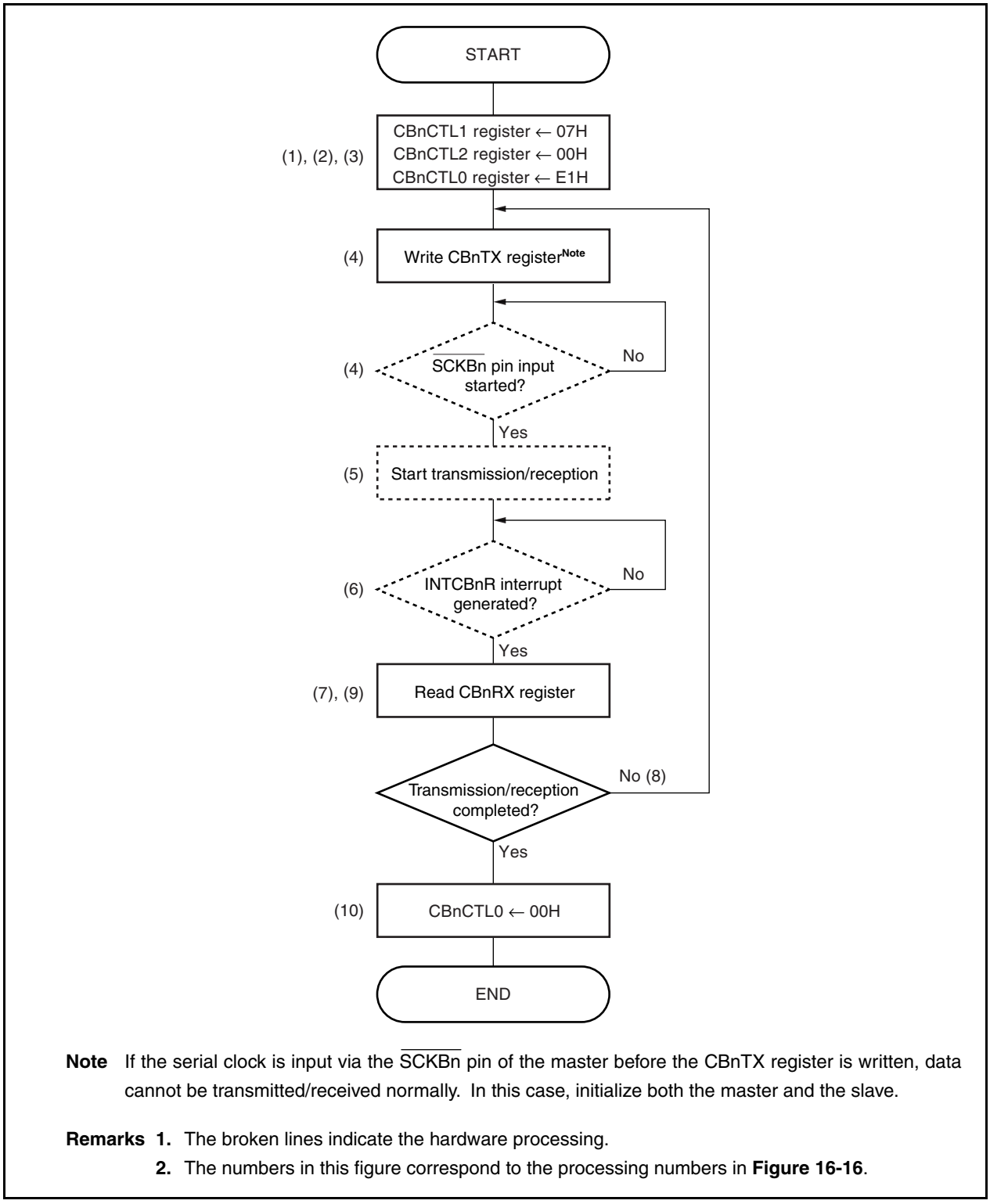
Table 10-1. Configuration of Real-Time Counter

Item	Configuration
Control registers	Real-time counter control register 0 (RC1CC0) Real-time counter control register 1 (RC1CC1) Real-time counter control register 2 (RC1CC2) Real-time counter control register 3 (RC1CC3) Sub-count register (RC1SUBC) Second count register (RC1SEC) Minute count register (RC1MIN) Hour count register (RC1HOUR) Day count register (RC1DAY) Day-of-week count register (RC1WEEK) Month count register (RC1MONTH) Year count register (RC1YEAR) Watch error correction register (RC1SUBU) Alarm minute register (RC1ALM) Alarm hour register (RC1ALH) Alarm week register (RC1ALW) Prescaler mode register 0 (PRSM0) Prescaler compare register 0 (PRSCM0)

16.6.6 Single transfer mode (slave mode, transmission/reception mode)

MSB first (CBnCTL0.CBnDIR bit = 0), communication type 1 (CBnCTL1.CBnCKP and CBnCTL1.CBnDAP bits = 00), communication clock (f_{CCLK}) = external clock ($\overline{SCKBn}$) (CBnCTL1.CBnCKS2 to CBnCTL1.CBnCKS0 bits = 111), transfer data length = 8 bits (CBnCTL2.CBnCL3 to CBnCTL2.CBnCL0 bits = 0000)

Figure 16-15. Single Transfer Mode Operation (Slave Mode, Transmission/Reception Mode)



Note If the serial clock is input via the $\overline{SCKBn}$ pin of the master before the CBnTX register is written, data cannot be transmitted/received normally. In this case, initialize both the master and the slave.

Remarks 1. The broken lines indicate the hardware processing.

2. The numbers in this figure correspond to the processing numbers in **Figure 16-16**.

16.7 Output Pins

(1) $\overline{\text{SCKBn}}$ pin

When CSIBn is disabled (CBnCTL0.CBnPWR bit = 0), the $\overline{\text{SCKBn}}$ pin output status is as follows.

Table 16-4. $\overline{\text{SCKBn}}$ Pin Output Status with CSIBn Disabled

CBnCKP	CBnCKS2	CBnCKS1	CBnCKS0	$\overline{\text{SCKBn}}$ Pin Output
0	1	1	1	High impedance
	Other than above			High level
1	1	1	1	High impedance
	Other than above			Low level

Remark The output level of the $\overline{\text{SCKBn}}$ pin changes if any of the CBnCTL1.CBnCKP and CBnCKS2 to CBnCKS0 bits is rewritten.

(2) SOBn pin

When CSIBn is disabled (CBnPWR bit = 0), the SOBn pin output status is as follows.

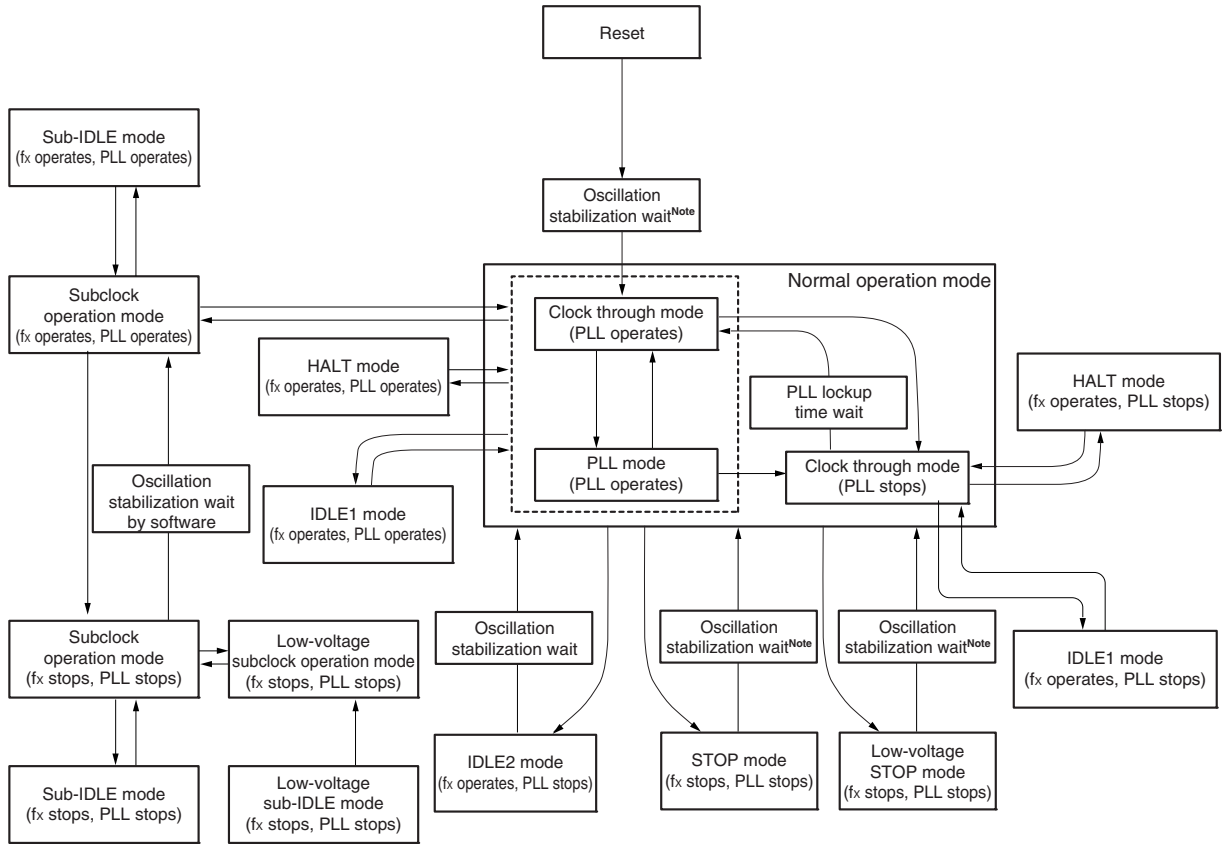
Table 16-5. SOBn Pin Output Status with CSIBn Disabled

CBnTXE	CBnDAP	CBnDIR	SOBn Pin Output
0	×	×	Low level
1	0	×	Low level
	1	0	CBnTX0 value (MSB)
		1	CBnTX0 value (LSB)

Remarks 1. The SOBn pin output changes when any one of the CBnCTL0.CBnTXE, CBnCTL0.CBnDIR, and CBnCTL1.CBnDAP bits is rewritten.

2. ×: Don't care

Figure 21-1. Status Transition



Note If a WDT overflow occurs during an oscillation stabilization time, the CPU operates on the internal oscillator clock.

Remark fx: Main clock oscillation

CHAPTER 24 LOW-VOLTAGE DETECTOR (LVI)

24.1 Functions

The low-voltage detector (LVI) has the following functions.

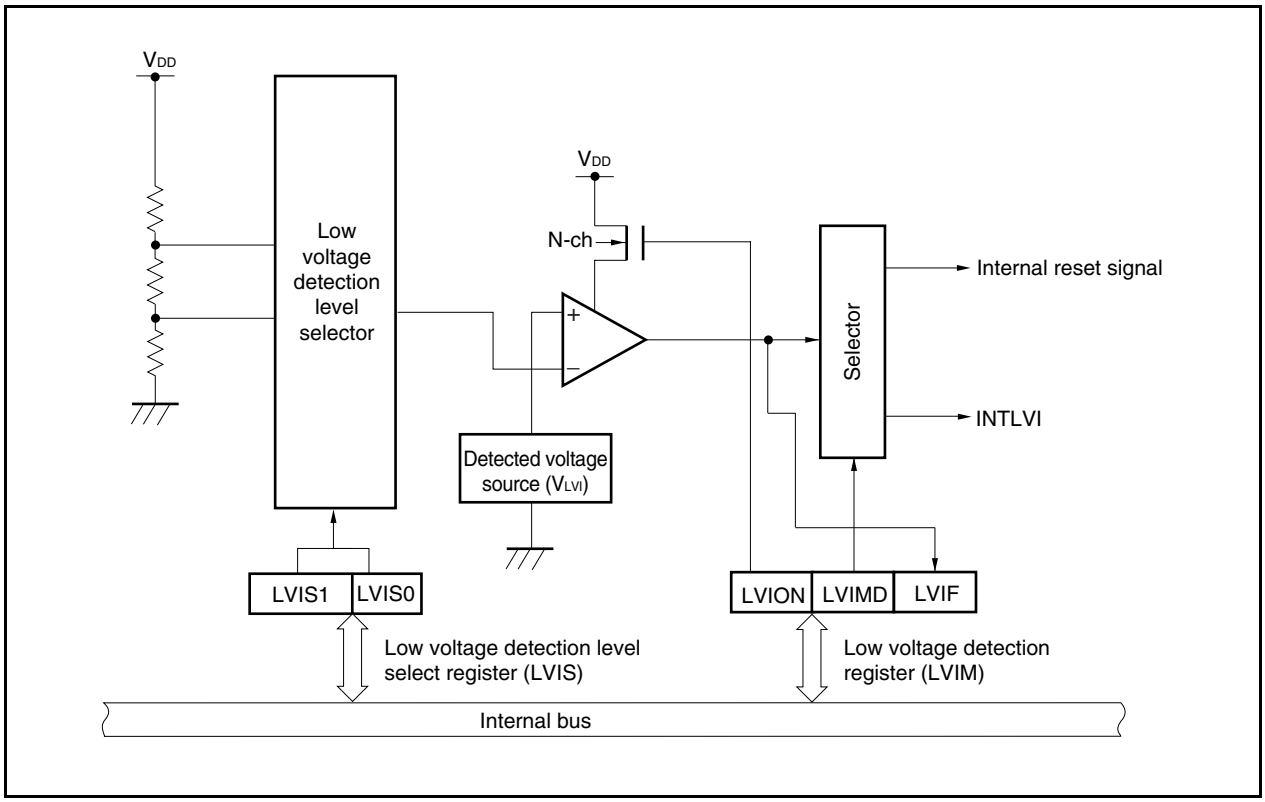
- If interrupt occurrence at low-voltage detection is selected as the operation mode, the low-voltage detector compares the supply voltage (V_{DD}) and the detection voltage (V_{LVI}), and generates an internal interrupt signal when the supply voltage drops below or rises above the detection voltage.
- If reset occurrence at low-voltage detection is selected as the operation mode, the low-voltage detector generates an internal reset signal when the supply voltage (V_{DD}) drops below the detection voltage (V_{LVI}).
- The level of the supply voltage to be detected can be changed by software.
- Interrupt or reset signal can be selected by software.
- The low-voltage detector is operable in the standby mode.

If a reset occurs when the low-voltage detector is selected to generate a reset signal, the RESF.LVIRF bit is set to 1. For details about the RESF register, see **22.3 Register to Check Reset Source**.

24.2 Configuration

The block diagram of the low-voltage detector is shown below.

Figure 24-1. Block Diagram of Low-Voltage Detector



29.1.5 Operation

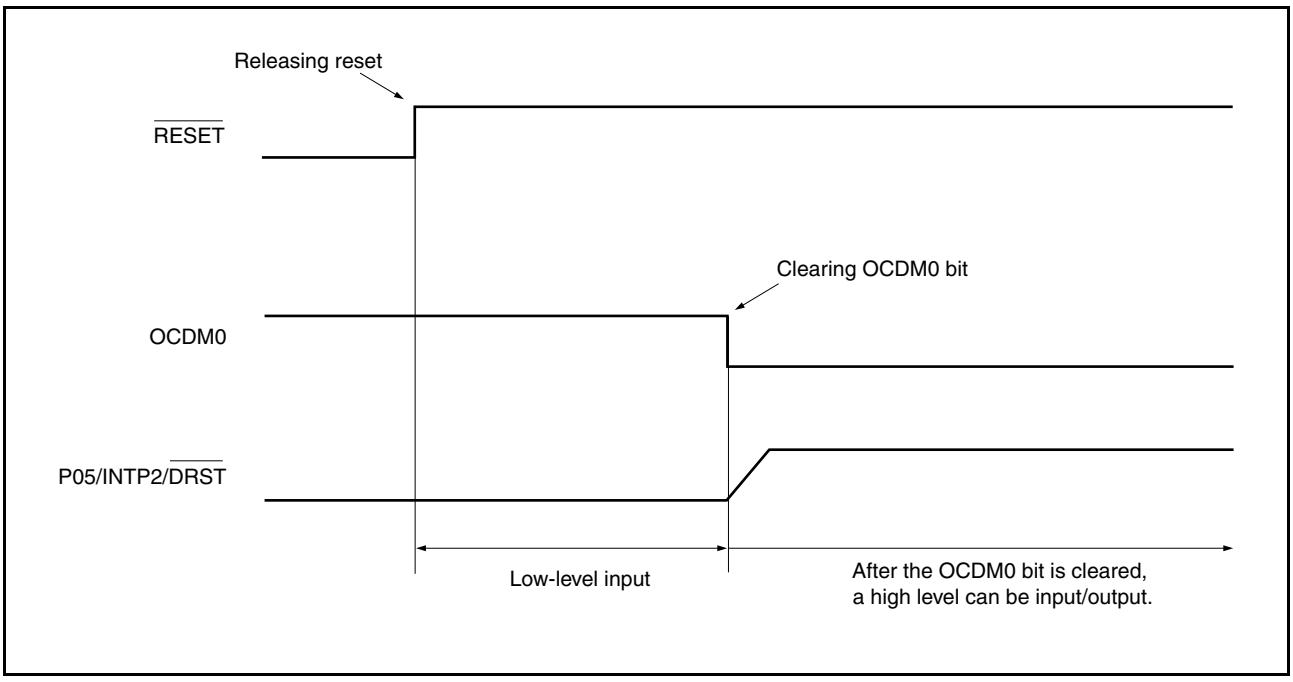
The on-chip debug function is made invalid under the conditions shown in the table below.

When this function is not used, keep the $\overline{\text{DRST}}$ pin low until the OCDM.OCDM0 flag is cleared to 0.

$\overline{\text{DRST}}$ Pin \ OCDM0 Flag	0	1
L	Invalid	Invalid
H	Invalid	Valid

Remark L: Low-level input
H: High-level input

Figure 29-3. Timing When On-Chip Debug Function Is Not Used

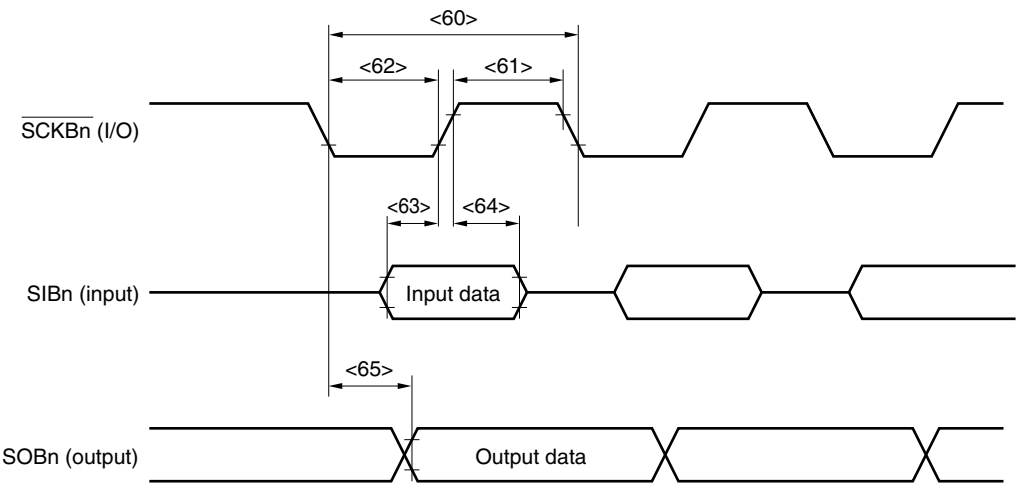


(2) Slave mode

(T_A = –40 to +85°C, V_{DD} = EV_{DD} = AV_{REF0} = AV_{REF1}, V_{SS} = EV_{SS} = AV_{SS} = 0 V, C_L = 50 pF)

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
$\overline{SCKBn}$ cycle time	t_{KCY2}	<60>	2.7 V ≤ V_{DD} ≤ 3.6 V	125		ns
			2.2 V ≤ V_{DD} < 2.7 V	800		ns
$\overline{SCKBn}$ high-level width	t_{KH2}	<61>	2.2 V ≤ V_{DD} ≤ 3.6 V	54.5		ns
$\overline{SCKBn}$ low-level width	t_{KL2}	<62>	2.2 V ≤ V_{DD} ≤ 3.6 V	54.5		ns
SIBn setup time (to $\overline{SCKBn}$↑)	t_{SIK2}	<63>	2.7 V ≤ V_{DD} ≤ 3.6 V	27		ns
			2.2 V ≤ V_{DD} < 2.7 V	100		ns
SIBn hold time (from $\overline{SCKBn}$↑)	t_{KSI2}	<64>	2.7 V ≤ V_{DD} ≤ 3.6 V	27		ns
			2.2 V ≤ V_{DD} < 2.7 V	100		ns
Delay time from $\overline{SCKBn}$↓ to SOBn output	t_{KSO2}	<65>	2.7 V ≤ V_{DD} ≤ 3.6 V		27	ns
			2.2 V ≤ V_{DD} < 2.7 V		95	ns

Remark n = 0 to 2, 4



Remark n = 0 to 2, 4

31.8.6 I²C bus mode

(T_A = –40 to +85°C, V_{DD} = EV_{DD} = AV_{REF0} = AV_{REF1} = 2.2 to 3.6 V, V_{SS} = EV_{SS} = AV_{SS} = 0 V)

Parameter		Symbol		Normal Mode		High-Speed Mode		Unit
				MIN.	MAX.	MIN.	MAX.	
SCL0n clock frequency		f_{CLK}		0	100	0	400	kHz
Bus free time (Between start and stop conditions)		t_{BUF}	<66>	4.7	–	1.3	–	μs
Hold time[Note 1]		$t_{HD:STA}$	<67>	4.0	–	0.6	–	μs
SCL0n clock low-level width		t_{LOW}	<68>	4.7	–	1.3	–	μs
SCL0n clock high-level width		t_{HIGH}	<69>	4.0	–	0.6	–	μs
Setup time for start/restart conditions		$t_{SU:STA}$	<70>	4.7	–	0.6	–	μs
Data hold time	CBUS compatible master	$t_{HD:DAT}$	<71>	5.0	–	–	–	μs
	I²C mode			0[Note 2]	–	0[Note 2]	0.9[Note 3]	μs
Data setup time		$t_{SU:DAT}$	<72>	250	–	100[Note 4]	–	ns
SDA0n and SCL0n signal rise time		t_R	<73>	–	1000	20 + 0.1Cb[Note 5]	300	ns
SDA0n and SCL0n signal fall time		t_F	<74>	–	300	20 + 0.1Cb[Note 5]	300	ns
Stop condition setup time		$t_{SU:STO}$	<75>	4.0	–	0.6	–	μs
Pulse width of spike suppressed by input filter		t_{SP}	<76>	–	–	0	50	ns
Capacitance load of each bus line		Cb		–	400	–	400	pF

Notes 1. At the start condition, the first clock pulse is generated after the hold time.

2. The system requires a minimum of 300 ns hold time internally for the SDA0n signal (at $V_{IHmin.}$ of SCL0n signal) in order to occupy the undefined area at the falling edge of SCL0n.

3. If the system does not extend the SCL0n signal low hold time (t_{LOW}), only the maximum data hold time ($t_{HD:DAT}$) needs to be satisfied.

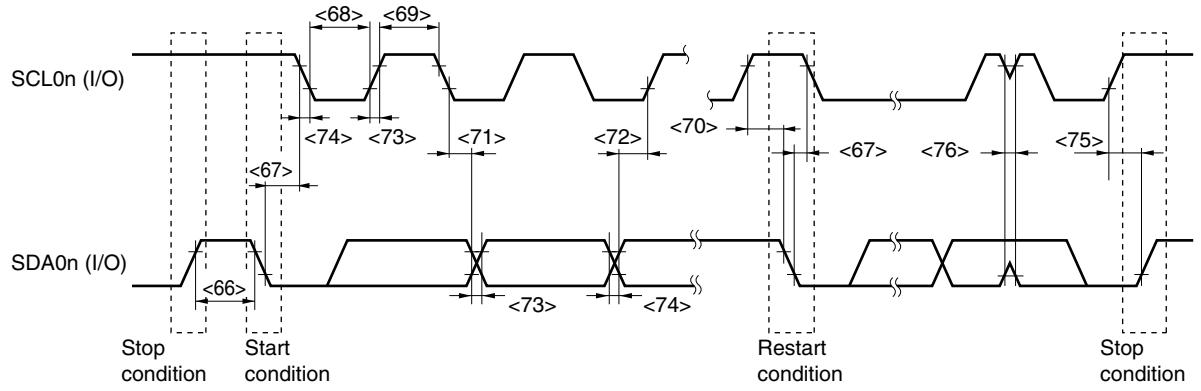
4. The high-speed mode I²C bus can be used in the normal-mode I²C bus system. In this case, set the high-speed mode I²C bus so that it meets the following conditions.

- If the system does not extend the SCL0n signal's low state hold time:
  $t_{SU:DAT} \geq 250$ ns
- If the system extends the SCL0n signal's low state hold time:
  Transmit the following data bit to the SDA0n line prior to the SCL0n line release ($t_{Rmax.} + t_{SU:DAT}$ = 1,000 + 250 = 1,250 ns: Normal mode I²C bus specification).

5. Cb: Total capacitance of one bus line (unit: pF)

Remark n = 0 to 2

I²C Bus Timing



Remark **n = 0 to 2**

31.8.7 A/D converter

(T_A = –40 to +85°C, V_{DD} = EV_{DD} = AV_{REF0} = AV_{REF1}, 2.7 V ≤ AV_{REF0} = AV_{REF1} ≤ 3.6 V, V_{SS} = EV_{SS} = AV_{SS} = 0 V, C_L = 50 pF)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution					10	bit
Overall error[Note]		2.7 V ≤ AV_{REF0} ≤ 3.6 V			±0.6	%FSR
A/D conversion time	t_{CONV}	3.0 V ≤ AV_{REF0} ≤ 3.6 V	2.6		24	μs
		2.7 V ≤ AV_{REF0} ≤ 3.0 V	3.9		24	μs
Zero scale error					±0.5	%FSR
Full scale error					±0.5	%FSR
Non-linearity error					±4.0	LSB
Differential linearity error					±4.0	LSB
Analog input voltage	V_{IAN}		AV_{SS}		AV_{REF0}	V
Reference voltage	AV_{REF0}		2.7		3.6	V
AV_{REF0} current	AI_{REF0}	Normal conversion mode		3	6.5	mA
		High-speed conversion mode		4	10	mA
		When A/D converter unused			5	μA

Note Excluding quantization error (±0.05 %FSR).

Caution Do not set (read/write) alternate-function ports during A/D conversion; otherwise the conversion resolution may be degraded.

Remark LSB: Least Significant Bit
FSR: Full Scale Range

(3) Programming characteristics

(T_A = –40 to +85°C, V_{DD} = EV_{DD} = AV_{REF0} = AV_{REF1} = 2.7 to 3.6 V, V_{SS} = EV_{SS} = AV_{SS} = 0 V, C_L = 50 pF)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Chip erase time		f_{XX} = 20 MHz (when the chip erase command is executed)		105		ms
Write time per 256 bytes		f_{XX} = 20 MHz		2.0		ms
Block internal verify time		f_{XX} = 20 MHz		10		ms
Block blank check time		f_{XX} = 20 MHz		0.5		ms
Flash memory information setting time		f_{XX} = 20 MHz		30		ms

Remark Block size = 2 KB