Renesas Electronics America Inc - UPD70F3808GB(R)-GAH-AX Datasheet

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Applications of "Embedded - Microcontrollers"

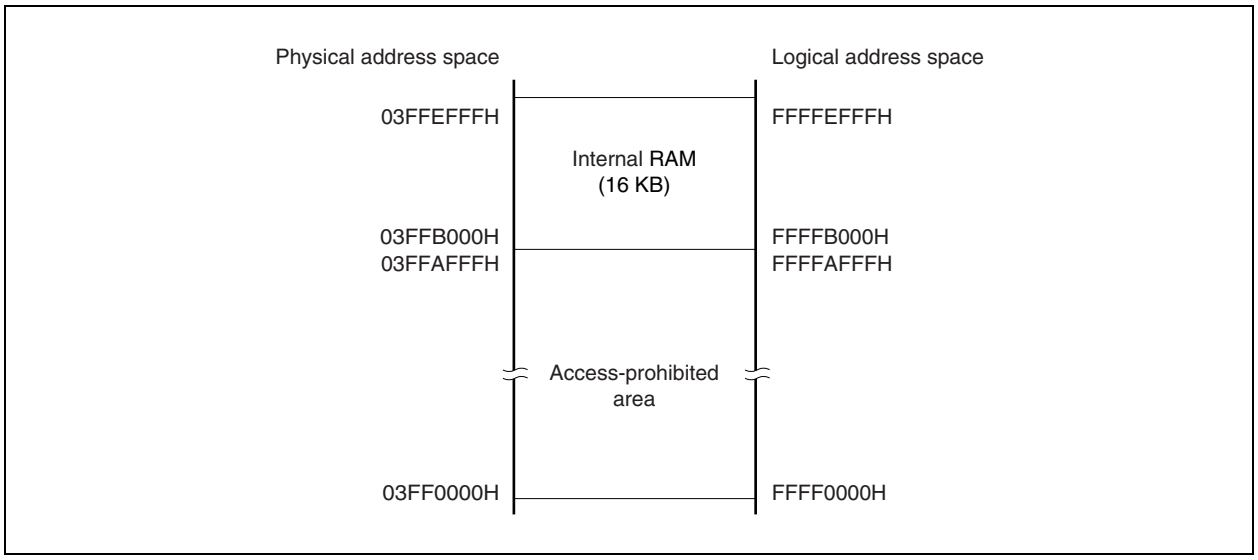
Details	
Product Status	Obsolete
Core Processor	V850ES
Core Size	32-Bit Single-Core
Speed	20MHz
Connectivity	CSI, EBI/EMI, I²C, UART/USART
Peripherals	DMA, LVD, PWM, WDT
Number of I/O	50
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 3.6V
Data Converters	A/D 10x10b; D/A 1x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd70f3808gb-r-gah-ax

(b) Internal RAM (16 KB)

16 KB are allocated to addresses 03FFB000H to 03FFEFFFH in the following versions.
Accessing addresses 03FF0000H to 03FFAFFFH is prohibited.

- μPD70F3838, 70F3839, 70F3840

Figure 3-10. Internal RAM Area (16 KB)



(6) Port 3 alternate function specifications

PFC39[Note1]	Specification of P39 pin alternate function
0	RXDA2 input
1	SCL00 I/O

PFC38[Note1]	Specification of P38 pin alternate function
0	TXDA2 output
1	SDA00 I/O

PFC35[Note2]	Specification of P35 pin alternate function
0	TIP11 input
1	TOP11 output

PFC34[Note2]	Specification of P34 pin alternate function
0	TIP10 input
1	TOP10 output

PFC33[Note2]	Specification of P33 pin alternate function
0	TIP01 input
1	TOP01 output

PFCE32[Note1]	PFC32[Note1]	Specification of P32 pin alternate function
0	0	ASCKA0 input
0	1	$\overline{\text{SCKB4}}$ I/O
1	0	TIP00 input
1	1	TOP00 output

PFC31	Specification of P31 pin alternate function
0	RXDA0 input/INTP7[Note3] input
1	SIB4 input[Note1]

PFC30	Specification of P30 pin alternate function
0	TXDA0 output
1	SOB4 output[Note1]

Notes1. V850ES/JC3-L (48-pin), V850/JE3-L only

2. V850ES/JE3-L only

3. INTP7 and RXDA0 are alternate functions. When using the pin for RXDA0, disable edge detection for INTP7 (clear the INTF3.INTF31 bit and the INTR3.INTR31 bit to 0). When using the pin for INTP7, stop UARTA0 reception (clear the UA0CTL0.UA0RXE bit to 0).

(4) Port 9 function control register (PFC9)

Caution When performing separate address bus output (A0 to A15), set the PMC9 register to FFFFH for all 16 bits at once after clearing the PFC9 and PFCE9 registers to 0000H.

(a) V850ES/JC3-L (40-pin)

After reset: 0000H R/W Address: PFC9 FFFFF472H,
PFC9L FFFFF472H, PFC9H FFFFF473H

	15	14	13	12	11	10	9	8
PFC9 (PFC9H)	PFC915	PFC914	0	0	0	0	0	0

	7	6	5	4	3	2	1	0
(PFC9L)	PFC97	PFC96	0	0	0	0	PFC91	PFC90

(b) V850ES/JC3-L (48-pin)

After reset: 0000H R/W Address: PFC9 FFFFF472H,
PFC9L FFFFF472H, PFC9H FFFFF473H

	15	14	13	12	11	10	9	8
PFC9 (PFC9H)	PFC915	PFC914	0	0	0	0	PFC99	PFC98

	7	6	5	4	3	2	1	0
(PFC9L)	PFC97	PFC96	0	0	0	0	PFC91	PFC90

(c) V850ES/JE3-L

After reset: 0000H R/W Address: PFC9 FFFFF472H,
PFC9L FFFFF472H, PFC9H FFFFF473H

	15	14	13	12	11	10	9	8
PFC9 (PFC9H)	PFC915	PFC914	PFC913	PFC912	PFC911	PFC910	PFC99	PFC98

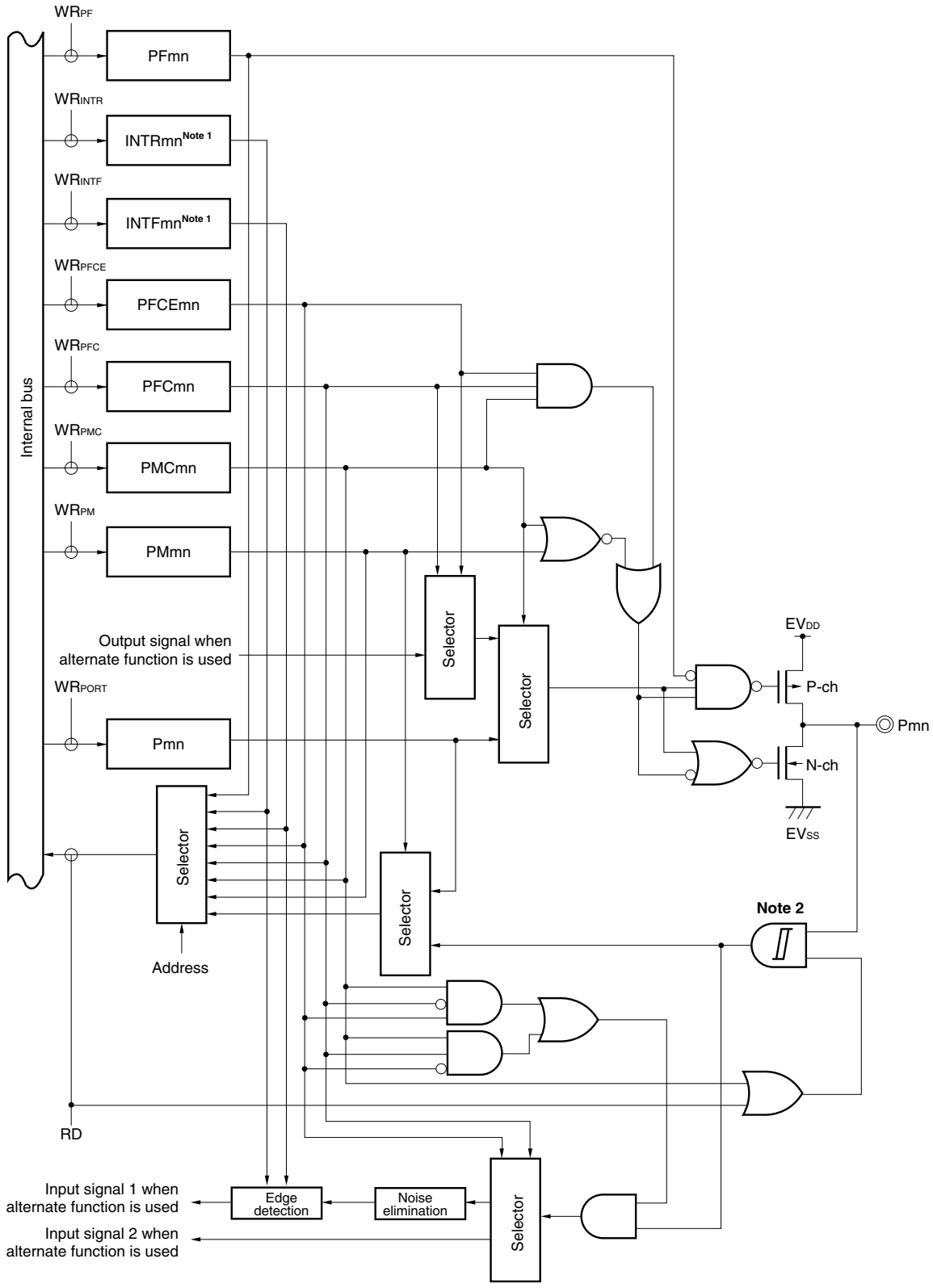
	7	6	5	4	3	2	1	0
(PFC9L)	PFC97	PFC96	0	PFC94	PFC93	PFC92	PFC91	PFC90

Remarks 1. For details of alternate function specification, see **4.3.7 (6) Port 9 alternate function specifications**.

2. The PFC9 register can be read or written in 16-bit units.
However, when using the higher 8 bits of the PFC9 register as the PFC9H register and the lower 8 bits as the PFC9L register, PFC9 can be read or written in 8-bit or 1-bit units.

3. To read/write bits 8 to 15 of the PFC9 register in 8-bit or 1-bit units, specify them as bits 0 to 7 of the PFC9H register.

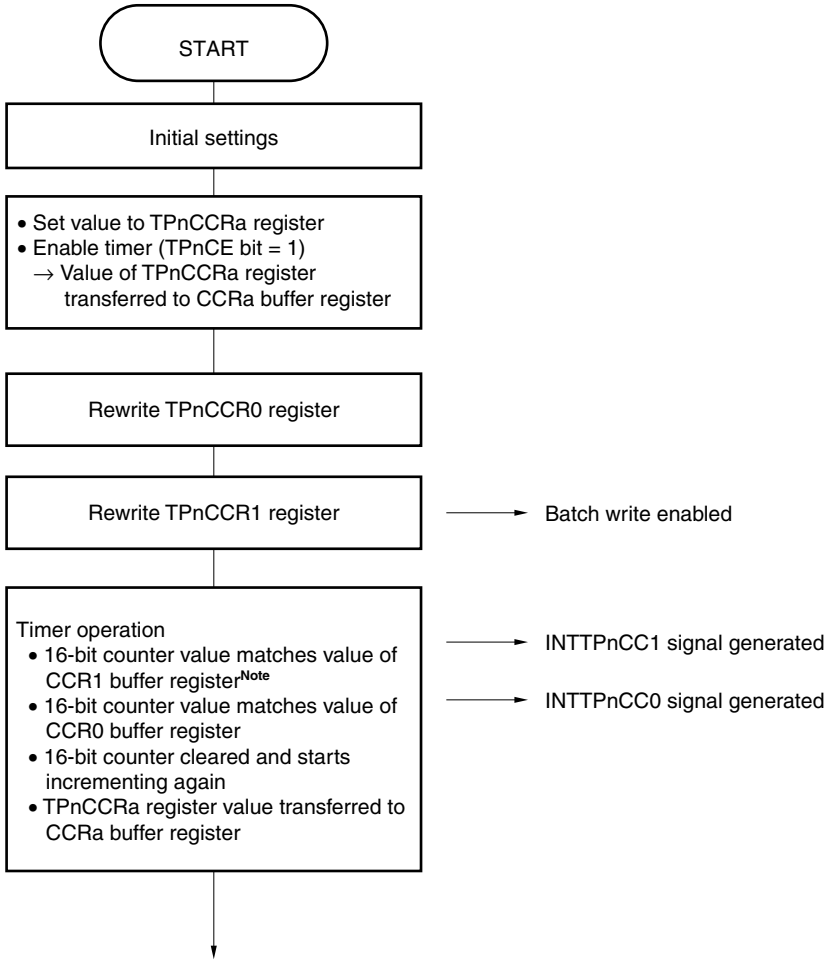
Figure 4-35. Block Diagram of Type U-24



Notes 1. See **19.7 External Interrupt Request Input Pins (NMI and INTP0 to INTP7)**.

2. There are no hysteresis characteristics in port mode.

Figure 6-4. Flowchart Showing Basic Batch Write Operation



Note The 16-bit counter is only cleared when its value matches the value of the CCR0 buffer register, not the CCR1 buffer register.

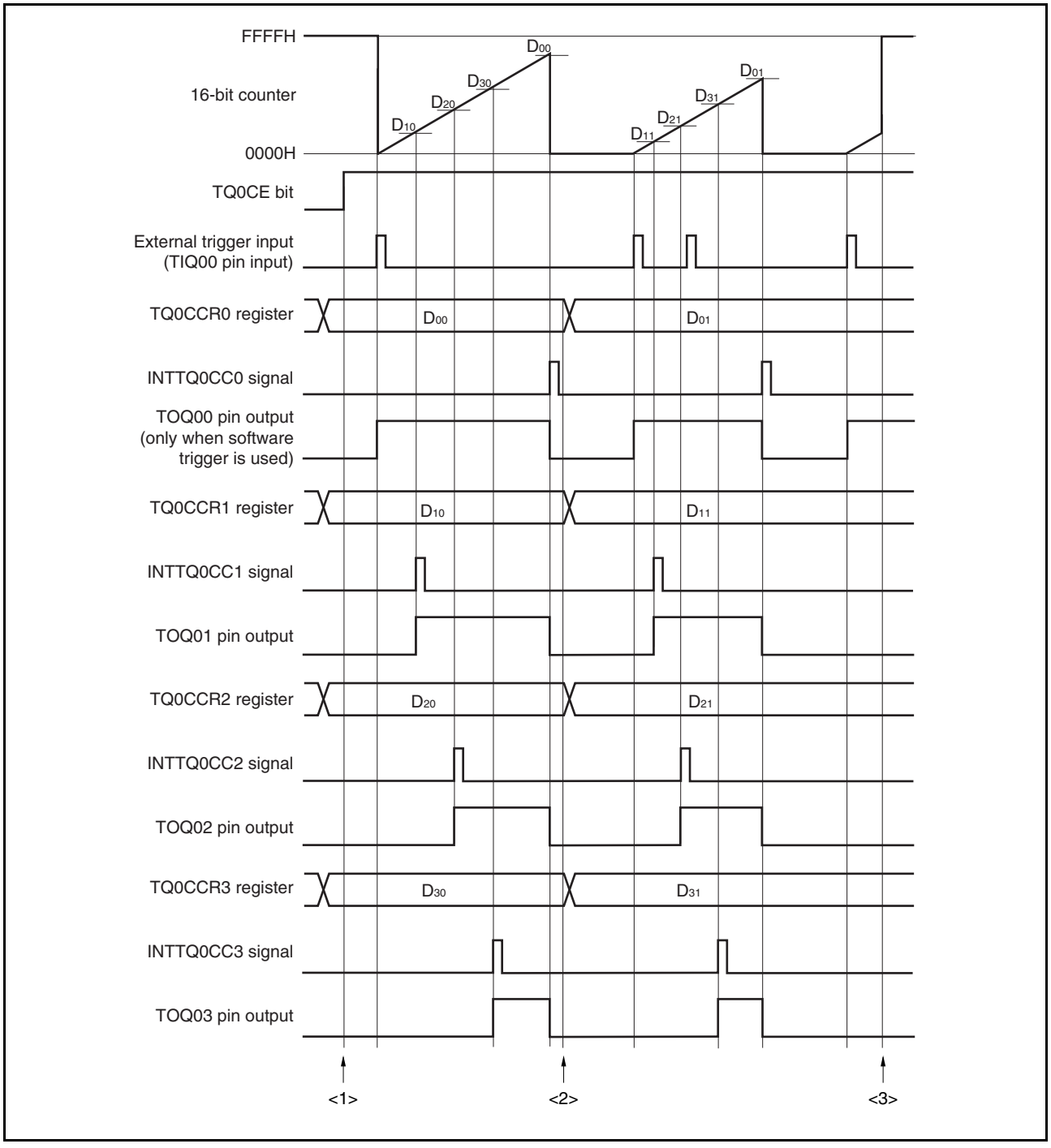
Caution The process of writing to the TPnCCR1 register includes enabling batch write. It is therefore necessary to rewrite the TPnCCR1 register after rewriting the TPnCCR0 register.

Remarks 1. The flowchart applies to the case when TMPn is being used in the PWM output mode.

2. a = 0, 1

(1) Operations in one-shot pulse output mode

Figure 7-41. Timing and Processing of Operations in One-Shot Pulse Output Mode (1/2)



(2) Using one-shot pulse mode

(a) Rewriting the TQ0CCRm register

When rewriting the value of the TQ0CCRm register to a smaller value, stop counting first and then change the set value.

When changing the value of the TQ0CCR0 register from D_{00} to D_{01} and the value of the TQ0CCRk register from D_{k0} to D_{k1}, if the registers are rewritten under any of the following conditions, a one-shot pulse will not be output as expected.

Condition 1 When rewriting the TQ0CCR0 register, if:

$D_{00} > D_{01}$ or,

$D_{00} <$ 16-bit counter value $< D_{01}$

In the case of condition 1, the 16-bit counter will not be cleared and will overflow in the cycle in which the new value is being written. The counter will be cleared for the first time at the newly written value (D_{01}).

Condition 2 When rewriting the TQ0CCRk register, if:

$D_{k0} > D_{k1}$ or,

$D_{k0} <$ 16-bit counter value $< D_{k1}$

In the case of condition 2, the TOQ0k pin output cannot be inverted to the active level in the cycle in which the new value is being written.

An example of what happens when condition 1 and condition 2 are satisfied in the same cycle is shown in Figure 7-42.

The 16-bit counter increments up to FFFFH, overflows, and starts incrementing again from 0000H.

When the 16-bit counter value matches D_{k1}, the INTTQ0CCk signal is generated and the TOQ0k pin output is set to the active level. Subsequently, when the 16-bit counter value matches D_{01}, the INTTQ0CC0 signal is generated, the TOQ0k pin output is set to the inactive level, and the counter stops incrementing.

Remark m = 0 to 3
K = 1 to 3

(2) Using pulse width measurement mode

(a) Clearing the overflow flag (TQ0OVF)

The overflow flag (TQ0OVF) can be cleared to 0 by reading the TQ0OVF bit and, if its value is 1, either clearing the bit to 0 by using the CLR1 instruction or by writing 8-bit data (with bit 0 as “0”) to the TQ0OPT0 register.

7.4.8 Timer output operations

The following table shows the operations and output levels of the TOQ00 to TOQ03 pins.

Table 7-8. Timer Output Control in Each Mode

Operation Mode	TOQ00 Pin	TOQ01 Pin	TOQ02 Pin	TOQ03 Pin
Interval timer mode	Square wave output			
External event count mode	–			
External trigger pulse output mode	Square wave output	External trigger pulse output	External trigger pulse output	External trigger pulse output
One-shot pulse output mode		One-shot pulse output	One-shot pulse output	One-shot pulse output
PWM output mode		PWM output	PWM output	PWM output
Free-running timer mode	Square wave output (only when compare function is used)			
Pulse width measurement mode	–			

Table 7-9. Truth Table of TOQ00 to TOQ03 Pins Under Control of Timer Output Control Bits

TQ0IOC0.TQ0OLm Bit	TQ0IOC0.TQ0OEm Bit	TQ0CTL0.TQ0CE Bit	Level of TOQ0m Pin
0	0	×	Low-level output
	1	0	Low-level output
		1	Low level immediately before counting, high level after counting is started
1	0	×	High-level output
	1	0	High-level output
		1	High level immediately before counting, low level after counting is started

Remark m = 0 to 3

(13) Watch error correction register (RC1SUBU)

The RC1SUBU register is an 8-bit register that can be used to correct the watch with high accuracy when the watch is early or late, by changing the value (reference value: 7FFFH) overflowing from the sub-count register (RSUBC) to the second counter register.

This register can be read or written in 8-bit or 1-bit units.

Reset sets this register to 00H.

Remarks 1. The RC1SUBU register can be rewritten only when the real-time counter is set to its initial values. Be sure to see **10.4.1 Initial settings**.

2. See **10.4.9 Watch error correction example of real-time counter** for details of watch error correction.

After reset: 00H R/W Address: FFFFFAD9H

	7	6	5	4	3	2	1	0
RC1SUBU	DEV	F6	F5	F4	F3	F2	F1	F0

DEV	Setting of watch error correction timing
0	Corrects watch errors when RC1SEC (second counter) is at 00, 20, or 40 seconds (every 20 seconds).
1	Corrects watch errors when RC1SEC (second counter) is at 00 seconds (every 60 seconds).

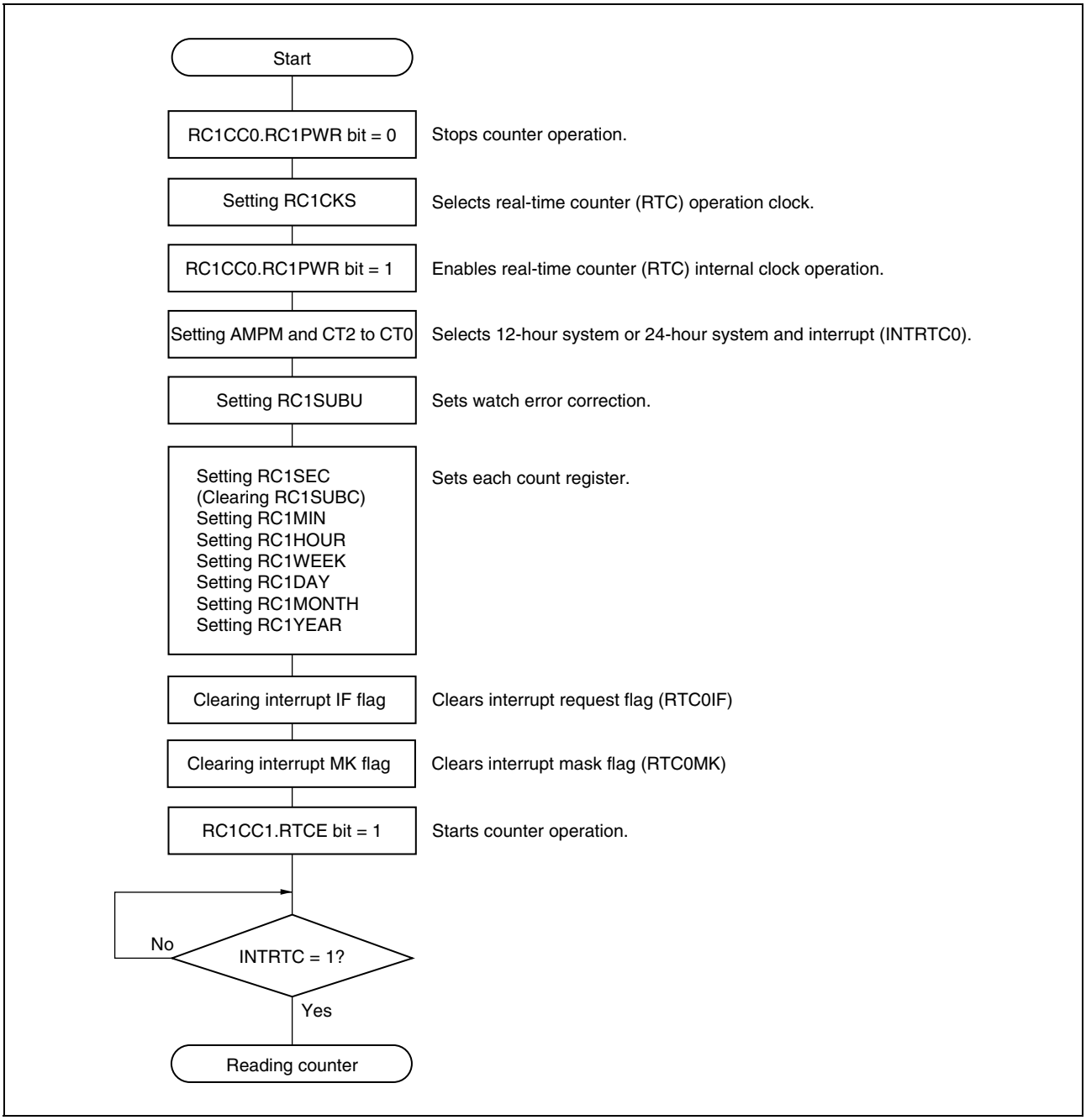
F6	Setting of watch error correction value
0	Increments the RC1SUBC count value by the value set using the F5 to F0 bits (positive correction). Expression for calculating increment value: (Setting value of F5 to F0 bits − 1) × 2
1	Decrements the RC1SUBC count value by the value set using the F5 to F0 bits (negative correction). Expression for calculating decrement value: (Inverted value of setting value of F5 to F0 bits + 1) × 2
If the F6 to F0 bit values are {1/0, 0, 0, 0, 0, 0, 1/0}, watch error correction is not performed.	

10.4 Operation

10.4.1 Initial settings

The initial settings are set when operating the watch function and performing a fixed-cycle interrupt operation.

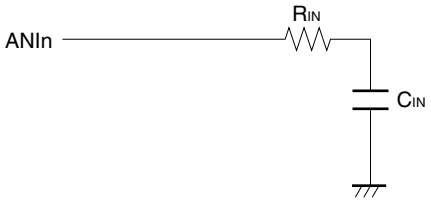
Figure 10-2. Initial Setting Procedure



(6) Internal equivalent circuit

The following shows the equivalent circuit of the analog input block.

Figure 13-14. Internal Equivalent Circuit of ANIn Pin



R_{IN}	C_{IN}
14 kΩ	8.0 pF

Remark The above values are reference values.

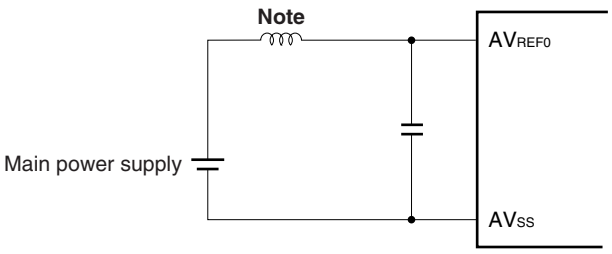
(7) AV_{REF0} pin

(a) The AV_{REF0} pin is used as the power supply pin of the A/D converter and also supplies power to the alternate-function ports. In an application where a backup power supply is used, be sure to supply the same voltage as V_{DD} to the AV_{REF0} pin as shown in Figure 13-15.

(b) The AV_{REF0} pin is also used as the reference voltage pin of the A/D converter. If the source supplying power to the AV_{REF0} pin has a high impedance or if the power supply has a low current supply capability, the reference voltage may fluctuate due to the current that flows during conversion (especially, immediately after the conversion enable bit ADA0CE has been set to 1). As a result, the conversion accuracy may drop. To avoid this, it is recommended to connect a capacitor across the AV_{REF0} and AV_{SS} pins to suppress the reference voltage fluctuation as shown in Figure 13-15.

(c) If the source supplying power to the AV_{REF0} pin has a high DC resistance, the voltage when conversion is enabled may be lower than the voltage when conversion is stopped, because of a voltage drop caused by the A/D conversion current.

Figure 13-15. Example of Handling AV_{REF0} Pin



Note Parasitic inductance

15.2.1 Pin functions of each channel

The RXDAn, TXDAn, and ASCKA0 pins used by UARTA in the V850ES/JC3-L, V850ES/JE3-L are used for other functions as shown in Table 15-2. To use these pins for UARTA, set the related registers as described in **Table 4-17 Settings When Pins Are Used for Alternate Functions**.

Table 15-2. Pins Used by UARTA

Channel	Pin No.			Port	UARTA Reception Input	UARTA Transmission Output	UARTA Clock I/O[Note]	Other Functions
	JC3L (40)	JC3L (48)	JE3L					
UARTA0	–	34	46	P31	RXDA0	–	–	INTP7/SIB4
	30	–	–					INTP7
	–	33	45	P30	–	TXDA0	–	SOB4
	29	–	–					–
	–	35	47	P32	–	–	ASCKA0[Note]	$\overline{\text{SCKB4}}$/TIP00/TOP00
UARTA1	20	24	32	P91	RXDA1	–	–	KR7/SCL02
	19	23	31	P90	–	TXDA1	–	KR6/SDA02
UARTA2	–	19	27	P39	RXDA2	–	–	SCL00
	–	18	26	P38	–	TXDA2	–	SDA00

Note The ASCKA0 function is provided only for UARTA0 (V850ES/JC3-L (48-pin), V850ES/JE3-L only).

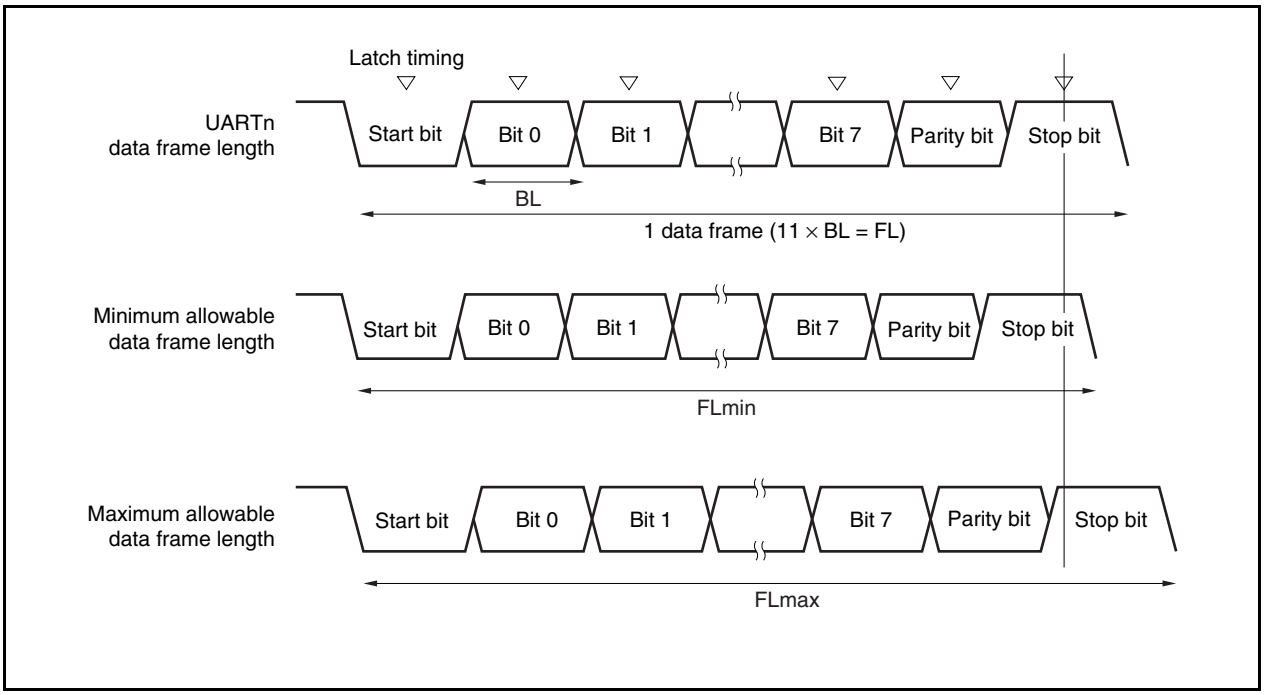
Remark JC3L (40): V850ES/JC3-L (40-pin products)
JC3L (48): V850ES/JC3-L (48-pin products)
JE3L : V850ES/JE3-L

(5) Allowable baud rate range during reception

The baud rate error range at the destination that is allowable during reception is shown below.

Caution The baud rate error indicated below is a theoretical value. In practice, the signal might be distorted, or communication might not be performed normally even if the error is within the allowable range. Therefore, the error must be minimized.

Figure 15-18. Allowable Baud Rate Range During Reception



As shown in Figure 15-18, the receive data latch timing is determined by the counter set using the UAnCTL2 register following start bit detection. The transmit data can be received normally if up to the last data (stop bit) can be received in time for this latch timing.

When this is applied to 11-bit reception, the following is the theoretical result.

$BL = (Brate)^{-1}$

Brate: UARTAn baud rate (n = 0 to 2)

k: Setting value of UAnCTL2.UAnBRS7 to UAnCTL2.UAnBRS0 bits (n = 0 to 2)

BL: 1-bit data length

FL: Length of 1 data frame

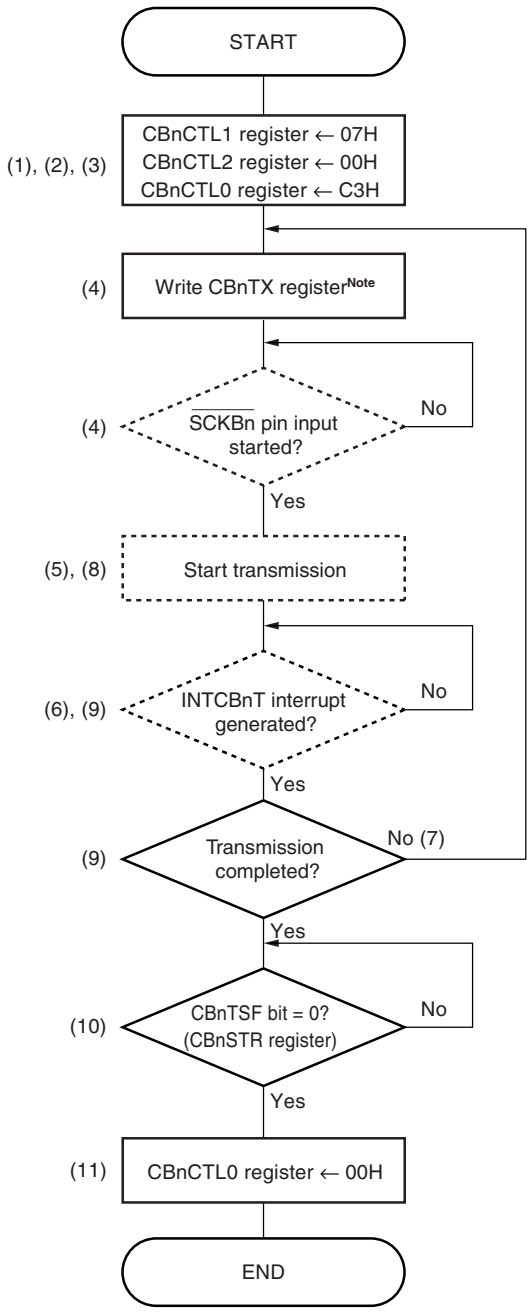
Latch timing margin: 2 clock cycles

Minimum allowable data frame length: $FLmin = 11 \times BL - \frac{k-2}{2k} \times BL = \frac{21k+2}{2k} BL$

16.6.10 Continuous transfer mode (slave mode, transmission mode)

MSB first (CBnCTL0.CBnDIR bit = 0), communication type 1 (CBnCTL1.CBnCKP and CBnCTL1.CBnDAP bits = 00), communication clock (f_{CCLK}) = external clock ($\overline{SCKBn}$) (CBnCTL1.CBnCKS2 to CBnCTL1.CBnCKS0 bits = 111), transfer data length = 8 bits (CBnCTL2.CBnCL3 to CBnCTL2.CBnCL0 bits = 0000)

Figure 16-23. Continuous Transfer Mode Operation (Slave Mode, Transmission Mode)

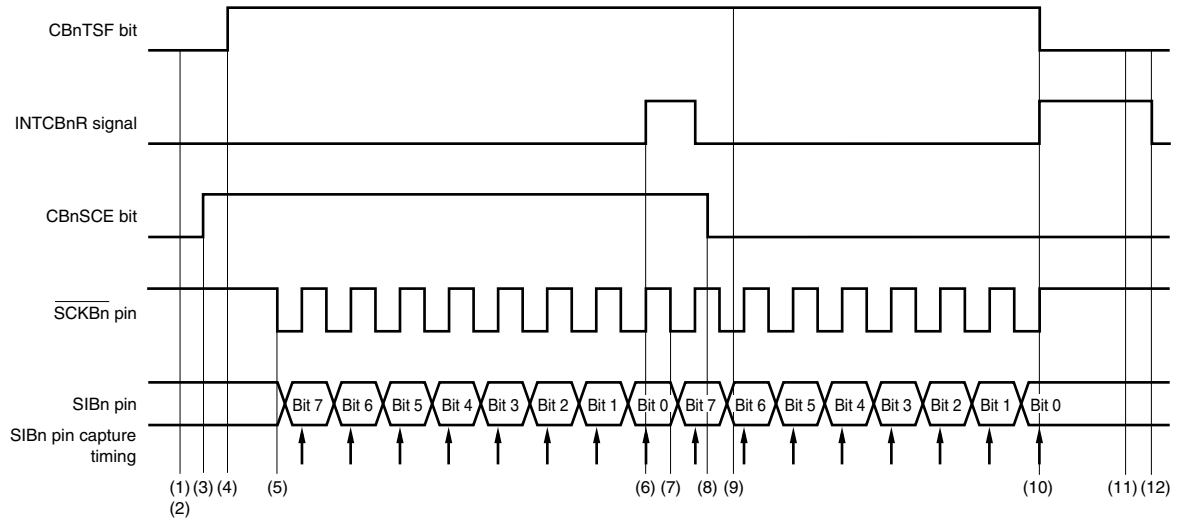


Note If the serial clock is input via the $\overline{SCKBn}$ pin of the master before the CBnTX register is written, data cannot be transmitted normally. In this case, initialize both the master and the slave.

Remarks 1. The broken lines indicate the hardware processing.

2. The numbers in this figure correspond to the processing numbers in **Figure 16-24**.

Figure 16-26. Continuous Transfer Mode Operation Timing (Slave Mode, Reception Mode)



(1) Write 07H to the CBnCTL1 register, and select communication type 1, communication clock (f_{CCLK}) = external clock ($\overline{SCKBn}$), and slave mode.
(2) Write 00H to the CBnCTL2 register, and set the transfer data length to 8 bits.
(3) Write A3H to the CBnCTL0 register, and select the reception mode, MSB first, and continuous transfer mode at the same time as enabling the operation of the communication clock (f_{CCLK}).
(4) The CBnSTR.CBnTSF bit is set to 1 by performing a dummy read of the CBnRX register, and the device waits for serial clock input.
(5) When the serial clock is input, capture the receive data of the SIBn pin in synchronization with the serial clock.
(6) When reception is completed, the reception complete interrupt request signal (INTCBnR) is generated, and reading receive data from the CBnRX register is enabled.
(7) When the serial clock is input with the CBnCTL0.CBnSCE bit set to 1, continuous reception is started.
(8) To end continuous reception with the current reception, clear the CBnSCE bit to 0.
(9) Read the CBnRX register.
(10) When reception is completed, the INTCBnR signal is generated, and reading receive data from the CBnRX register is enabled. If the CBnSCE bit is set to 0 before communication is complete, clear the CBnTSF bit to 0 to end the receive operation.
(11) Read the CBnRX register.
(12) To disable reception, clear the CBnCTL0.CBnPWR and CBnCTL0.CBnRXE bits to 0 after confirming that the CBnTSF bit is 0.

(4) Wait cancellation method

The following four wait cancellation methods are available.

- By setting the IICCn.WRELn bit to 1
- By writing to the IICn register
- By setting start condition (IICCn.STTn bit = 1)[Note]
- By setting stop condition (IICCn.SPTn bit = 1)[Note]

Note Master only

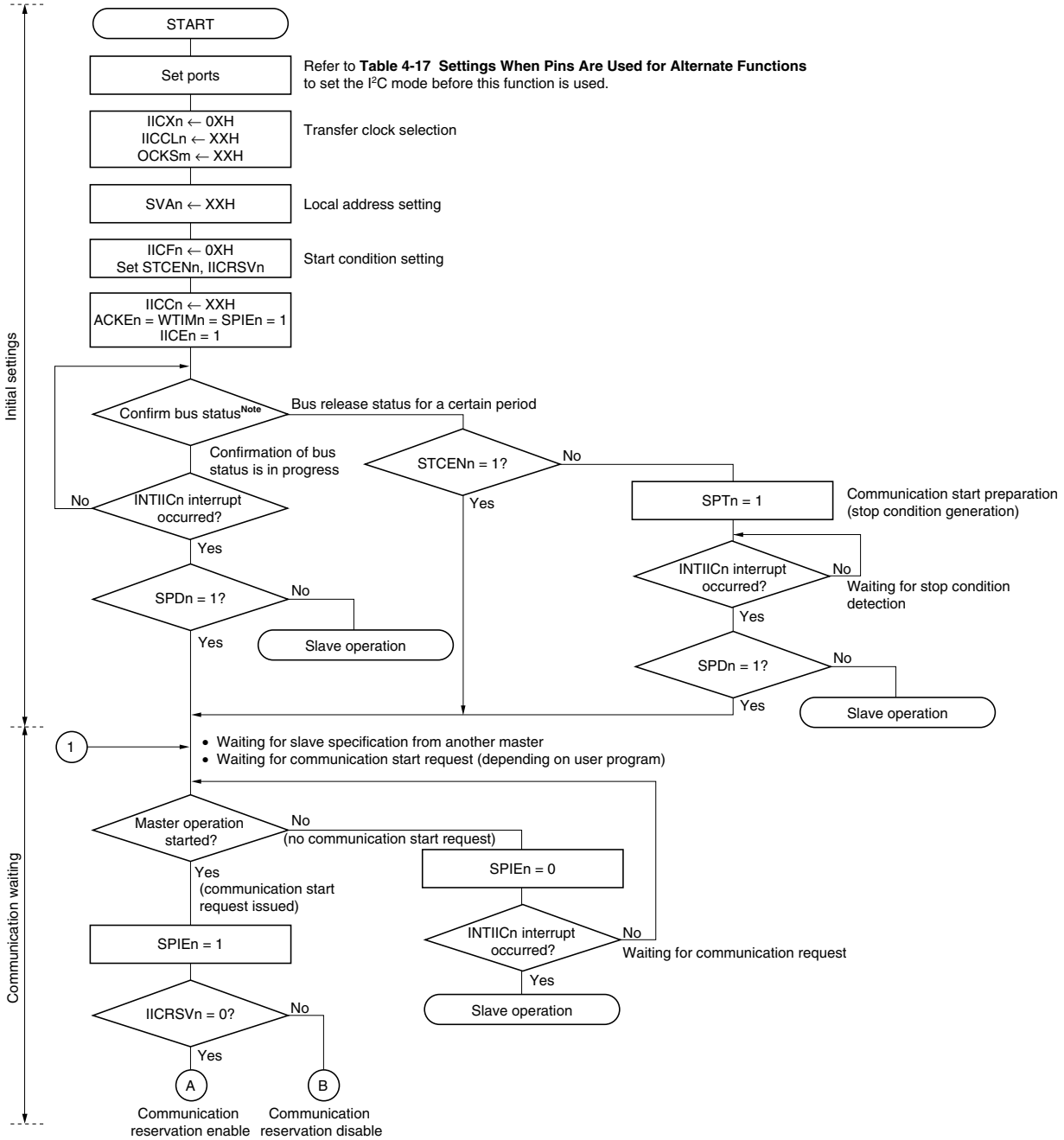
When an 8-clock wait has been selected (WTIMn bit = 0), whether or not $\overline{\text{ACK}}$ has been generated must be determined prior to wait cancellation.

(5) Stop condition detection

The INTIICn signal is generated when a stop condition is detected.

17.16.2 Master operation in multimaster system

Figure 17-19. Master Operation in Multimaster System (1/3)



Note Confirm that the bus release status (IICCLn.CLDn bit = 1, IICCLn.DADn bit = 1) has been maintained for a certain period (1 frame, for example). When the SDA0n pin is constantly low level, determine whether to release the I²C0n bus (SCL0n, SDA0n pins = high level) by referring to the specifications of the product involved in the communication.

Remark m = 0, 1

(12) Read values of DSAn and DDAn registers

If the DSAn and DDAn registers are read during a DMA transfer, the values before and after the registers were updated might be read.

For example, if the DSAnH register and then the DSAnL register are read when the DMA transfer source address (DSAn register) is 0000FFFFH and the count direction is incremental (DADCn.SAD1 and DADCn.SAD0 bits = 00), the value of the DSAnL register differs as follows, depending on whether DMA transfer is executed immediately after the DSAnH register is read.

(a) If DMA transfer does not occur while DSAn register is being read

<1> Reading DSAnH register value: DSAnH register = 0000H

<2> Reading DSAnL register value: DSAnL register = FFFFH

(b) If DMA transfer occurs while DSAn register is being read

<1> Reading DSAnH register value: DSAnH register = 0000H

<2> Occurrence of DMA transfer

<3> Incrementing DSAn register: DSAn register = 00010000H

<4> Reading DSAnL register value: DSAnL register = 0000H

(13) Setting up DMA transfer again

When re-specifying DMA settings by using the DDAnH, DDAnL, DSAnH, DSAnL, DBCn, and DADCn registers during the current DMA (the TCn bit is set to 1), be sure to initialize the DMA channels first. The DMA transfer must be initialized using the procedure described in **18.11 (4) DMA transfer initialization procedure**.