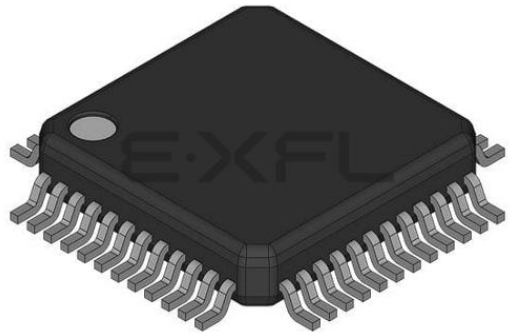

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Applications of "Embedded - Microcontrollers"

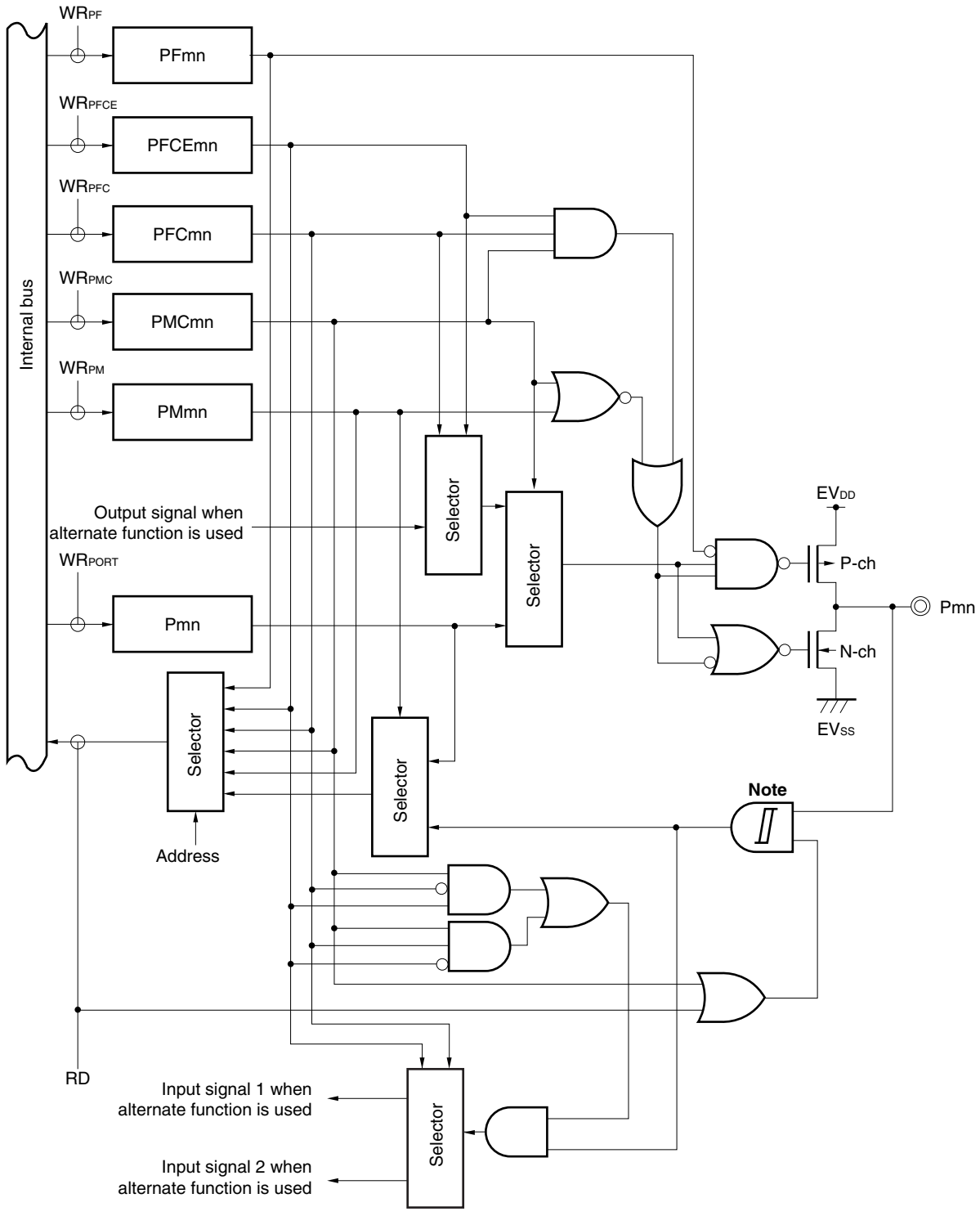
Details	
Product Status	Active
Core Processor	V850ES
Core Size	32-Bit Single-Core
Speed	20MHz
Connectivity	CSI, EBI/EMI, I²C, UART/USART
Peripherals	DMA, LVD, PWM, WDT
Number of I/O	34
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 3.6V
Data Converters	A/D 6x10b; D/A 1x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd70f3839ga-gam-ax

Table 1-2. V850ES/JE3-L Product List

Generic Name		V850ES/JE3-L				
Part Number		μPD70F3805	μPD70F3806	μPD70F3807	μPD70F3808	μPD70F3840
Internal memory	Flash memory	16 KB	32 KB	64 KB	128 KB	256 KB
	RAM	8 KB	8 KB	8 KB	8 KB	16 KB
Memory space		64 MB				
General-purpose register		32 bits × 32 registers				
Clock	Main clock (oscillation frequency)	Ceramic/crystal (in PLL mode: f_X = 2.5 to 5 MHz (multiplied by 4), in clock through mode: f_X = 2.5 to 10 MHz) External clock (in PLL mode: f_X = 2.5 to 5 MHz (multiplied by 4), in clock through mode: f_X = 2.5 to 5 MHz)				
	Subclock (oscillation frequency)	Crystal (f_{XT} = 32.768 kHz)				
	Internal oscillator	f_R = 220 kHz (TYP.)				
	Minimum instruction execution time	50 ns (main clock (f_{XX}) = 20 MHz)				
I/O port		I/O: 50 (5 V tolerant/N-ch open-drain output selectable: 28)				
Timer	16-bit TMP	6 channels				
	16-bit TMQ	1 channel				
	16-bit TMM	1 channel				
	Watch timer	1 channel				
	RTC	1 channel				
	WDT	1 channel				
Real-time output port		4 bits × 1 channel, 2 bits × 1 channel, or 6 bits × 1 channel				
10-bit A/D converter		10 channels				
8-bit D/A converter		1 channel				
Serial interface	CSIB	3 channels				
	UARTA/CSIB	1 channel				
	CSIB/I^2C bus	1 channel				
	UARTA/I^2C bus	2 channels				
	UARTA	–				
DMA controller		4 channels (transfer target: on-chip peripheral I/O, internal RAM)				
Interrupt source	External	9 (9)[Note]				
	Internal	48				
Power save function		HALT/IDLE1/IDLE2/STOP/subclock/sub-IDLE/ low-voltage STOP/low-voltage subclock/low-voltage sub-IDLE mode				
Reset source		$\overline{\text{RESET}}$ pin input, watchdog timer 2 (WDT2), clock monitor (CLM), low-voltage detector (LVI)				
CRC function		16-bit error detection code generated for 8-bit unit data				
On-chip debug		MINICUBE, MINICUBE2 supported				
Operating power supply voltage		2.2 to 3.6 V @5 MHz, 2.7 to 3.6 V @20 MHz				
Operating ambient temperature		–40 to +85°C				
Package		64-pin LQFP (10 × 10 mm)				

Notes The figure in parentheses indicates the number of external interrupts that can release STOP mode.

Figure 4-33. Block Diagram of Type U-22



Note There are no hysteresis characteristics in port mode.

Table 4-17. Settings When Pins Are Used for Alternate Functions (2/5)

Function Name	Alternate Function		Pnx Bit of Pn Register	PMnx Bit of PMn Register	PMCnx Bit of PMCn Register	PFCEnx Bit of PFCEn Register	PFCnx Bit of PFCn Register	Other Bits (Registers)
	Name	I/O						
P38	TXDA2	Output	P38 = Setting not required	PM38 = Setting not required	PMC38 = 1	–	PFC38 = 0	
	SDA00	I/O	P38 = Setting not required	PM38 = Setting not required	PMC38 = 1	–	PFC38 = 1	PF38 (PF3) = 1
P39	RXDA2	Input	P39 = Setting not required	PM39 = Setting not required	PMC39 = 1	–	PFC39 = 0	
	SCL00	I/O	P39 = Setting not required	PM39 = Setting not required	PMC39 = 1	–	PFC39 = 1	PF39 (PF3) = 1
P40	SIB0	Input	P40 = Setting not required	PM40 = Setting not required	PMC40 = 1	–	PFC40 = 0	
	SDA01	I/O	P40 = Setting not required	PM40 = Setting not required	PMC40 = 1	–	PFC40 = 1	PF40 (PF4) = 1
P41	SOB0	Output	P41 = Setting not required	PM41 = Setting not required	PMC41 = 1	–	PFC41 = 0	
	SCL01	I/O	P41 = Setting not required	PM41 = Setting not required	PMC41 = 1	–	PFC41 = 1	PF41 (PF4) = 1
P42	$\overline{\text{SCKB0}}$	I/O	P42 = Setting not required	PM42 = Setting not required	PMC42 = 1	–	–	
P50	TIQ01	Input	P50 = Setting not required	PM50 = Setting not required	PMC50 = 1	PFCE50 = 0	PFC50 = 1	KRM0 (KRM) = 0
	KR0	Input	P50 = Setting not required	PM50 = Setting not required	PMC50 = 1	PFCE50 = 0	PFC50 = 1	TQ0TIG2,TQ0TIG3 (TQ0IOC1) = 0
	TOQ01	Output	P50 = Setting not required	PM50 = Setting not required	PMC50 = 1	PFCE50 = 1	PFC50 = 0	
	RTP00	Output	P50 = Setting not required	PM50 = Setting not required	PMC50 = 1	PFCE50 = 1	PFC50 = 1	
P51	TIQ02	Input	P51 = Setting not required	PM51 = Setting not required	PMC51 = 1	PFCE51 = 0	PFC51 = 1	KRM1 (KRM) = 0
	KR1	Input	P51 = Setting not required	PM51 = Setting not required	PMC51 = 1	PFCE51 = 0	PFC51 = 1	TQ0TIG4,TQ0TIG5 (TQ0IOC1) = 0
	TOQ02	Output	P51 = Setting not required	PM51 = Setting not required	PMC51 = 1	PFCE51 = 1	PFC51 = 0	
	RTP01	Output	P51 = Setting not required	PM51 = Setting not required	PMC51 = 1	PFCE51 = 1	PFC51 = 1	
P52	TIQ03	Input	P52 = Setting not required	PM52 = Setting not required	PMC52 = 1	PFCE52 = 0	PFC52 = 1	KRM2 (KRM) = 0
	KR2	Input	P52 = Setting not required	PM52 = Setting not required	PMC52 = 1	PFCE52 = 0	PFC52 = 1	TQ0TIG6,TQ0TIG7 (TQ0IOC1) = 0
	TOQ03	Output	P52 = Setting not required	PM52 = Setting not required	PMC52 = 1	PFCE52 = 1	PFC52 = 0	
	RTP02	Output	P52 = Setting not required	PM52 = Setting not required	PMC52 = 1	PFCE52 = 1	PFC52 = 1	
	DDI	Input	P52 = Setting not required	PM52 = Setting not required	PMC52 = Setting not required	PMCE52 = Setting not required	PFC52 = Setting not required	OCDM0 (OCDM) = 1

(2) Clock control register (CKC)

The CKC register is a special register. Data can be written to this register only in a combination of specific sequences (see **3.4.7 Special registers**).

The CKC register controls the internal system clock in the PLL mode.

This register can be read or written in 8-bit or 1-bit units.

Reset sets this register to 0AH.

After reset: 0AH R/W Address: FFFFF822H

	7	6	5	4	3	2	1	0
CKC	0	0	0	0	1	0	1	CKDIV0

CKDIV0	Internal system clock (f_{XX}) in PLL mode
0	$f_{XX} = 4 \times f_X$ (f_X = 2.5 to 5.0 MHz)
1	Setting prohibited

Cautions 1. The PLL mode cannot be used when f_X = 5.0 to 10.0 MHz.

2. Be sure to set the CKC register to 0AH. If a value other than 0AH is set, the operation is not guaranteed.

(4) PLL lockup time specification register (PLLS)

The PLLS register is an 8-bit register used to select the PLL lockup time when the PLLCTL.PLLON bit is changed from 0 to 1.

This register can be read or written in 8-bit units.

Reset sets this register to 03H.

After reset: 03H R/W Address: FFFFF6C1H

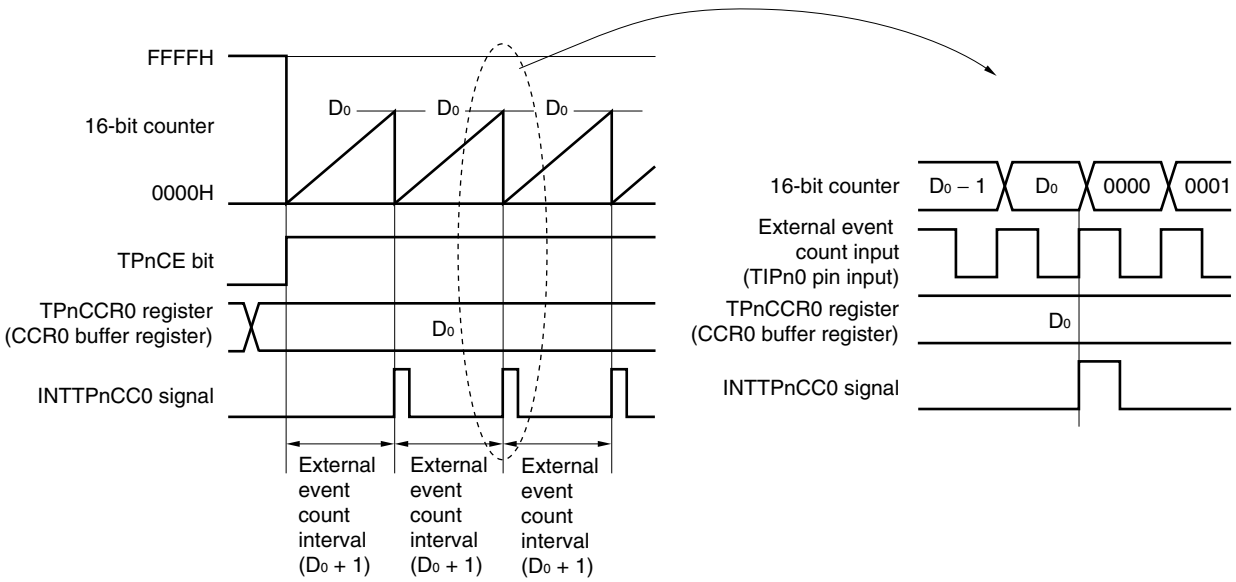
	7	6	5	4	3	2	1	0
PLLS	0	0	0	0	0	0	PLLS1	PLLS0

PLLS1	PLLS0	Selection of PLL lockup time
0	0	$2^{10}/f_X$
0	1	$2^{11}/f_X$
1	0	$2^{12}/f_X$
1	1	$2^{13}/f_X$ (default value)

Cautions 1. Set so that the lockup time is at least 400 μs.

2. Do not change the PLLS register setting during the lockup period.

Figure 6-18. Basic Timing of Operations in External Event Count Mode



Remark This figure shows the basic timing when the rising edge is specified as the valid edge of the external event count input.

Figure 6-28. Register Settings in External Trigger Pulse Output Mode (2/2)

(d) TMPn I/O control register 2 (TPnIOC2)

							TPnEES1	TPnEES0	TPnETS1	TPnETS0
TPnIOC2	0	0	0	0	0	0	0/1	0/1		

These bits select the valid edge of the external trigger input.

(e) TMPn counter read buffer register (TPnCNT)

The value of the 16-bit counter can be read by reading this register.

(f) TMPn capture/compare registers 0 and 1 (TPnCCR0 and TPnCCR1)

If the TPnCCR0 register is set to D_0 and the TPnCCR1 register is set to D_1, the PWM waveform is as follows:

PWM waveform cycle = (D_0 + 1) × Count clock cycle
PWM waveform active level width = D_1 × Count clock cycle

Remark TMPn I/O control register 1 (TPnIOC1) and TMPn option register 0 (TPnOPT0) are not used in the external trigger pulse output mode.

CHAPTER 7 16-BIT TIMER/EVENT COUNTER Q (TMQ)

Timer Q (TMQ) is a 16-bit timer/event counter.
The V850ES/JC3-L, V850ES/JE3-L incorporate one TMQ timer/counter, TMQ0.

7.1 Functions

TMQ0 has the following features:

(1) Interval timer
TMQ0 generates an interrupt at a preset interval and can output a square wave.

(2) External event counter
TMQ0 counts the number of externally input signal pulses.

(3) External trigger pulse output
TMQ0 starts counting and outputs a pulse when the specified external signal is input.

(4) One-shot pulse output
TMQ0 outputs a one-shot pulse with an output width that can be freely specified.

(5) PWM output
TMQ0 outputs a pulse with a constant cycle whose active width can be changed.
The pulse duty can also be changed freely even while the timer is operating.

(6) Free-running timer
The 16-bit counter increments from 0000H to FFFFH and then resets.

(7) Pulse width measurement
TMQ0 can be used to measure the pulses of a signal input externally.

(2) Using external event count mode

(a) Operation when TQ0CCR0 register is set to FFFFH

When the TQ0CCR0 register is set to FFFFH, the 16-bit counter increments up to FFFFH upon detection of the valid edge of the external event count signal and is reset to 0000H in synchronization with the next increment timing. The INTTQ0CC0 signal is then generated. At this time, the TQ0OPT0.TQ0OVF bit is not set to 1.

Figure 7-21. Operation When TQ0CCR0 Register Is Set to FFFFH

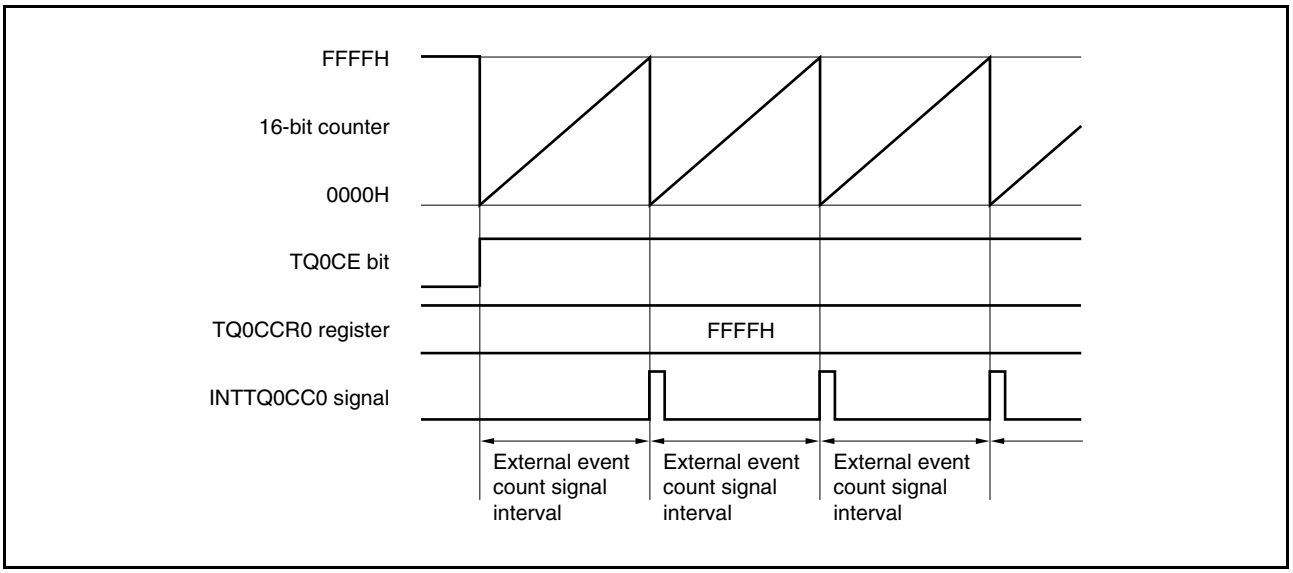


Figure 7-46. Register Settings in PWM Output Mode (3/3)

(f) TMQ0 capture/compare registers 0 to 3 (TQ0CCR0 to TQ0CCR3)

If the TQ0CCR0 register is set to D_0 and the TQ0CCRk register is set to D_k, the PWM waveform is as follows:

PWM waveform cycle = $(D_0 + 1) \times$ Count clock cycle
PWM waveform active level width = $D_k \times$ Count clock cycle

Remarks 1. TMQ0 I/O control register 1 (TQ0IOC1) and TMQ0 option register 0 (TQ0OPT0) are not used in the PWM output mode.

2. Updating TMQ0 capture/compare register 2 (TQ0CCR2) and TMQ0 capture/compare register 3 (TQ0CCR3) is enabled by writing to TMQ0 capture/compare register 1 (TQ0CCR1).

7.4.7 Pulse width measurement mode (TQ0MD2 to TQ0MD0 bits = 110)

In the pulse width measurement mode, TMQ0 starts incrementing when the TQ0CTL0.TQ0CE bit is set to 1. Each time it is detected that a valid edge has been input to the TIQ0m pin, the value of the 16-bit counter is stored in the TQ0CCRm register, and the 16-bit counter is cleared to 0000H.

The interval of the valid edge can be measured by reading the TQ0CCRm register after a capture interrupt request signal (INTTQ0CCm) occurs.

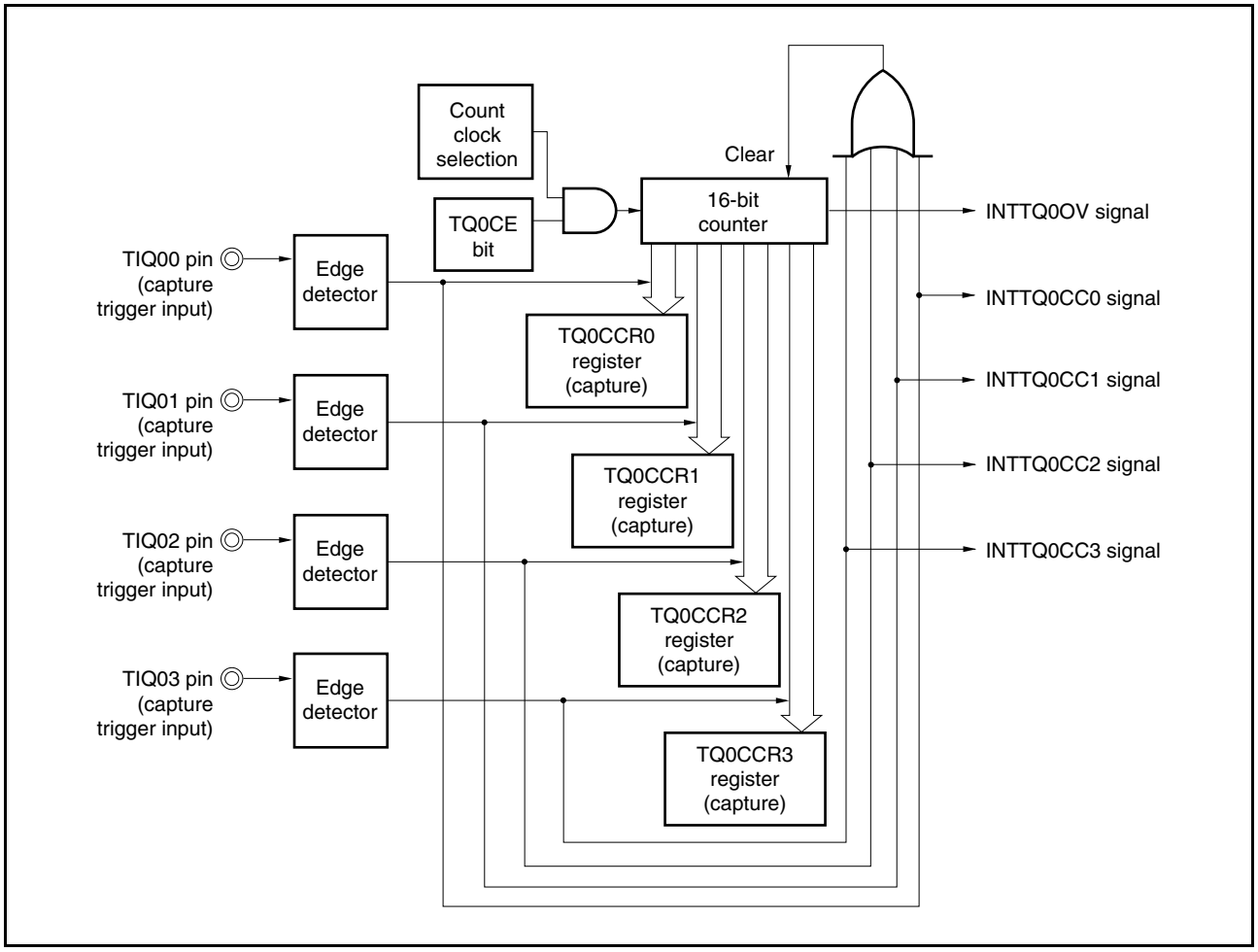
Select one of the TIQ00 to TIQ03 pins as the capture trigger input pin. Specify “No edge detected” by using the TQ0IOC1 register for the unused pins.

Remarks 1. For how to set the TIQ0m pin, see **Table 7-2 Pins Used by TMQ0** and **Table 4-17 Settings When Pins Are Used for Alternate Functions**.

2. For how to enable the INTTQ0CCm interrupt signal, see **CHAPTER 19 INTERRUPT SERVICING/ EXCEPTION PROCESSING FUNCTION**.

3. m = 0 to 3
k = 1 to 3

Figure 7-65. Configuration of TMQ0 in Pulse Width Measurement Mode



(3) Watch timer operation mode register (WTM)

The WTM register enables or disables the count clock and operation of the watch timer, sets the interval time of the prescaler, controls the operation of the 5-bit counter, and sets the set time of the watch flag.

Set the PRSM0, PRSCM0 register before setting the WTM register.

This register can be read or written in 8-bit or 1-bit units.

Reset sets this register to 00H.

(1/2)

After reset: 00H R/W Address: FFFFF680H

	7	6	5	4	3	2	<1>	<0>
WTM	WTM7	WTM6	WTM5	WTM4	WTM3	WTM2	WTM1	WTM0

WTM7	WTM6	WTM5	WTM4	Selection of interval time of prescaler
0	0	0	0	2^4/fw (488 μs: fw = fXT)
0	0	0	1	2^5/fw (977 μs: fw = fXT)
0	0	1	0	2^6/fw (1.95 ms: fw = fXT)
0	0	1	1	2^7/fw (3.91 ms: fw = fXT)
0	1	0	0	2^8/fw (7.81 ms: fw = fXT)
0	1	0	1	2^9/fw (15.6 ms: fw = fXT)
0	1	1	0	2^{10}/fw (31.3 ms: fw = fXT)
0	1	1	1	2^{11}/fw (62.5 ms: fw = fXT)
1	0	0	0	2^4/fw (488 μs: fw = fBRG)
1	0	0	1	2^5/fw (977 μs: fw = fBRG)
1	0	1	0	2^6/fw (1.95 ms: fw = fBRG)
1	0	1	1	2^7/fw (3.90 ms: fw = fBRG)
1	1	0	0	2^8/fw (7.81 ms: fw = fBRG)
1	1	0	1	2^9/fw (15.6 ms: fw = fBRG)
1	1	1	0	2^{10}/fw (31.2 ms: fw = fBRG)
1	1	1	1	2^{11}/fw (62.5 ms: fw = fBRG)

Table 11-2. Loop Detection Time Interval of Watchdog Timer 2

	WDCS24	WDCS23	WDCS22	WDCS21	WDCS20	Selected Clock	100 kHz (MIN.)	220 kHz (TYP.)	400 kHz (MAX.)
Internal oscillator clock	0	0	0	0	0	$2^{12}/f_R$	41.0 ms	18.6 ms	10.2 ms
	0	0	0	0	1	$2^{13}/f_R$	81.9 ms	37.2 ms	20.5 ms
	0	0	0	1	0	$2^{14}/f_R$	163.8 ms	74.5 ms	41.0 ms
	0	0	0	1	1	$2^{15}/f_R$	327.7 ms	148.9 ms	81.9 ms
	0	0	1	0	0	$2^{16}/f_R$	655.4 ms	297.9 ms	163.8 ms
	0	0	1	0	1	$2^{17}/f_R$	1310.7 ms	595.8 ms	327.7 ms
	0	0	1	1	0	$2^{18}/f_R$	2621.4 ms	1191.6 ms	655.4 ms
	0	0	1	1	1	$2^{19}/f_R$	5242.9 ms	2383.1 ms	1310.7 ms
Main clock							f_{XX} = 20 MHz	f_{XX} = 16 MHz	f_{XX} = 10 MHz
	0	1	0	0	0	$2^{18}/f_{XX}$	13.1 ms	16.4 ms	26.2 ms
	0	1	0	0	1	$2^{19}/f_{XX}$	26.2 ms	32.8 ms	52.4 ms
	0	1	0	1	0	$2^{20}/f_{XX}$	52.4 ms	65.5 ms	104.9 ms
	0	1	0	1	1	$2^{21}/f_{XX}$	104.9 ms	131.1 ms	209.7 ms
	0	1	1	0	0	$2^{22}/f_{XX}$	209.7 ms	262.1 ms	419.4 ms
	0	1	1	0	1	$2^{23}/f_{XX}$	419.4 ms	524.3 ms	838.9 ms
	0	1	1	1	0	$2^{24}/f_{XX}$	838.9 ms	1048.6 ms	1677.7 ms
	0	1	1	1	1	$2^{25}/f_{XX}$	1677.7 ms	2097.2 ms	3355.4 ms
Subclock							f_{XT} = 32.768 kHz		
	1	×	0	0	0	$2^9/f_{XT}$	15.625 ms		
	1	×	0	0	1	$2^{10}/f_{XT}$	31.25 ms		
	1	×	0	1	0	$2^{11}/f_{XT}$	62.5 ms		
	1	×	0	1	1	$2^{12}/f_{XT}$	125 ms		
	1	×	1	0	0	$2^{13}/f_{XT}$	250 ms		
	1	×	1	0	1	$2^{14}/f_{XT}$	500 ms		
	1	×	1	1	0	$2^{15}/f_{XT}$	1000 ms		
	1	×	1	1	1	$2^{16}/f_{XT}$	2000 ms		

Remark × = Either 0 or 1

(4/4)

SPTn	Stop condition trigger
0	Stop condition is not generated.
1	Stop condition is generated (termination of master device's transfer). After the SDA0n line goes to low level, either set the SCL0n line to high level or wait until the SCL0n pin goes to high level. Next, after the rated amount of time has elapsed, the SDA0n line is changed from low level to high level and a stop condition is generated.

Cautions concerning set timing

For master reception: Cannot be set to 1 during transfer.
Can be set to 1 only when the ACKEn bit has been set to 0 and during the wait period after the slave has been notified of final reception.

For master transmission: A stop condition cannot be generated normally during the $\overline{\text{ACK}}$ reception period. Set to 1 during the wait period that follows output of the ninth clock.

- Cannot be set to 1 at the same time as the STTn bit.
- The SPTn bit can be set to 1 only when in master mode[Note].
- When the WTIMn bit has been set to 0, if the SPTn bit is set to 1 during the wait period that follows output of eight clocks, note that a stop condition will be generated during the high-level period of the ninth clock.
  The WTIMn bit should be changed from 0 to 1 during the wait period following output of eight clocks, and the SPTn bit should be set to 1 during the wait period that follows output of the ninth clock.
- When the SPTn bit is set to 1, setting the SPTn bit to 1 again is disabled until the setting is cleared to 0.

Condition for clearing (SPTn bit = 0)	Condition for setting (SPTn bit = 1)
• Cleared by loss in arbitration • Automatically cleared after stop condition is detected • When the LRELn bit = 1 (communication save) • When the IICEn bit = 0 (operation stop) • After reset	• Set by instruction

Note Set the SPTn bit to 1 only in master mode. However, when the IICRSVn bit is 0, the SPTn bit must be set to 1 and a stop condition generated before the first stop condition is detected following the switch to the operation enabled status. For details, see **17.15 Cautions**.

Caution When the TRCn bit = 1, the WRELn bit is set to 1 during the ninth clock and the wait state is canceled, after which the TRCn bit is cleared to 0 and the SDA0n line is set to high impedance.

Remarks The SPTn bit is 0 if it is read immediately after data setting.

29.2.3 Allocation of user resources

The user must prepare the following resources to perform communication between MINICUBE2 and the target device and implement each debug function. These items need to be set in the user program or using the compiler options.

(1) Allocation of memory space

The shaded portions in Figure 29-5 are the areas reserved for placing the debug monitor program, so user programs and data cannot be allocated to these spaces. These spaces must be secured so as not to be used by the user program.

(2) Security ID setting

The ID code must be embedded in the area between 0000070H and 0000079H in Figure 29-5, to prevent the memory from being read by an unauthorized person. For details, see **29.3 ROM Security Function**.

32.6.2 Supply current characteristics

(T_A = –40 to +85°C, V_{DD} = EV_{DD} = AV_{REF0} = AV_{REF1}, V_{SS} = EV_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.[Note 1]	MAX.[Note 2]	Unit
Supply current[Note 3]	I_{DD1}	Normal operation	f_{XX} = 20 MHz (f_X = 5 MHz)[Note 4]		8.2[Note 5]	20	mA
			f_{XX} = 10 MHz (f_X = 10 MHz), PLL off[Note 4]		4.1[Note 5]	10	mA
	I_{DD2}	HALT mode	f_{XX} = 20 MHz (f_X = 5 MHz)[Note 4]		5.3	14	mA
	I_{DD3}	IDLE1 mode	f_{XX} = 5 MHz (f_X = 5 MHz), PLL off[Note 4]		0.5	1	mA
	I_{DD4}	IDLE2 mode	f_{XX} = 5 MHz (f_X = 5 MHz), PLL off[Note 4]		0.21	0.5	mA
	I_{DD5}	Subclock operation mode	f_{XT} = 32.768 kHz, main clock stopped, internal oscillator stopped, PLL off REGOVL0 = 02H (low-voltage subclock operation mode)		9.6		μA
	I_{DD6}	Sub-IDLE mode	f_{XT} = 32.768 kHz, main clock stopped, internal oscillator stopped, PLL off REGOVL0 = 02H (low-voltage sub-IDLE mode)		1.9	30	μA
	I_{DD7}	STOP mode	Subclock stopped, internal oscillator stopped REGOVL0 = 01H (low-voltage STOP mode) T_A = 25°C		1.1	3.0	μA
			Subclock stopped, internal oscillator stopped REGOVL0 = 01H (low-voltage STOP mode) T_A = 85°C			25	μA
			Subclock operating, internal oscillator stopped REGOVL0 = 01H (low-voltage STOP mode)		1.9	30	μA
	I_{DD8}	Self programming mode	f_{XX} = 20 MHz (f_X = 5 MHz)		14	24	mA
LVI current	I_{LVI}				1.2	3	μA
WDT, internal oscillation current	I_{WDT}				5		μA

Notes 1. TYP. current is a value at V_{DD} = EV_{DD} = 3.3 V, T_A = 25°C.
The TYP. value is not a value guaranteed for each device.

2. MAX. current is a value at which the characteristic in question is at the worst-case value at V_{DD} = EV_{DD} = 3.6 V, T_A = –40 to +85°C.

3. Total of V_{DD} and EV_{DD} currents. Currents I_{LVI} and I_{WDT} flowing through the output buffers, A/D converter, D/A converter, and on-chip pull-down resistor are not included.

4. TYP. value indicates the current value when "RTC" or "watch timer + TMM (count by watch timer interrupt)" operate as peripheral functions.
MAX. value indicates the current value when all the functions operable in a range in which the pin status is not changed operate as peripheral functions.
However, I_{LVI} and I_{WDT} are excluded.

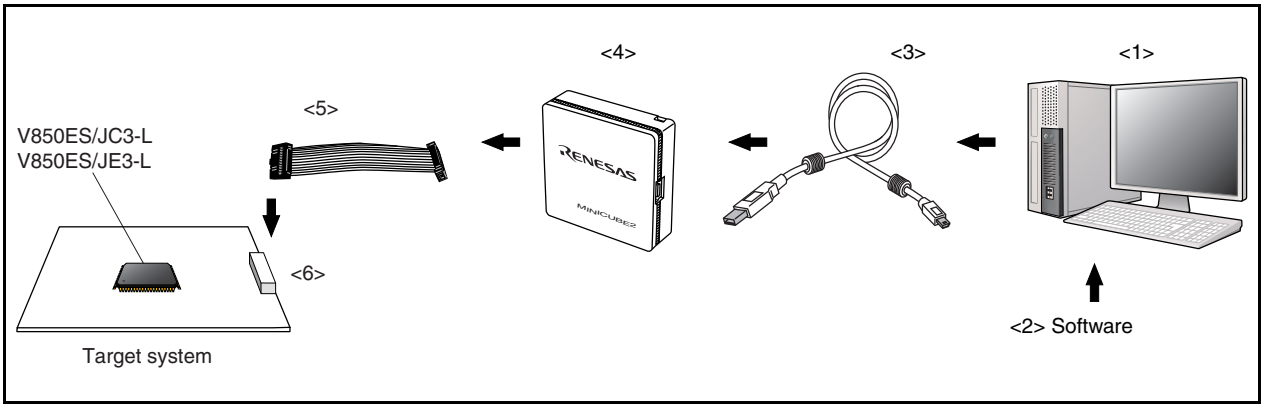
5. TYP. value of I_{DD1} is a value when all instructions are executed.

Remark For details about the operating voltage, see **32.3 Operating Conditions**.

A.4.3 When using MINICUBE2 QB-MINI2

The system configuration when connecting MINICUBE2 to the host machine (PC-9821 series, PC/AT compatible) is shown below.

Figure A-4. System Configuration of On-Chip Emulation System



<1> Host machine	PC with USB ports
<2> Software	The integrated debugger ID850QB, device file, etc. Download the device file from the Renesas Electronics website. http://www2.renesas.com/micro/en/ods/index.html
<3> USB interface cable	USB cable to connect the host machine and MINICUBE. It is supplied with MINICUBE. The cable length is approximately 2 m.
<4> MINICUBE2 On-chip debug emulator	This on-chip debug emulator serves to debug hardware and software when developing application systems using the V850ES/JC3-L, V850ES/JE3-L. It supports integrated debugger ID850QB.
<5> 16-pin target cable	Cable to connect MINICUBE2 and the target system. It is supplied with MINICUBE. The cable length is approximately 15 cm.
<6> Target connector (sold separately)	Use a 16-pin general-purpose connector with 2.54 mm pitch.

Remark The numbers in the angular brackets correspond to the numbers in Figure A-4.

A.5 Debugging Tools (Software)

ID850QB Integrated debugger	This debugger supports the in-circuit emulators for V850 microcontrollers. The ID850QB is Windows-based software. It has improved C-compatible debugging functions and can display the results of tracing with the source program using an integrating window function that associates the source program, disassemble display, and memory display with the trace result. It should be used in combination with the device file.

APPENDIX D INSTRUCTION SET LIST

D.1 Conventions

(1) Register symbols used to describe operands

Register Symbol	Explanation
reg1	General-purpose registers: Used as source registers.
reg2	General-purpose registers: Used mainly as destination registers. Also used as source register in some instructions.
reg3	General-purpose registers: Used mainly to store the remainders of division results and the higher 32 bits of multiplication results.
bit#3	3-bit data for specifying the bit number
immX	X bit immediate data
dispX	X bit displacement data
regID	System register number
vector	5-bit data that specifies the trap vector (00H to 1FH)
cccc	4-bit data that shows the conditions code
sp	Stack pointer (r3)
ep	Element pointer (r30)
listX	X item register list

(2) Register symbols used to describe opcodes

Register Symbol	Explanation
R	1-bit data of a code that specifies reg1 or regID
r	1-bit data of the code that specifies reg2
w	1-bit data of the code that specifies reg3
d	1-bit displacement data
I	1-bit immediate data (indicates the higher bits of immediate data)
i	1-bit immediate data
cccc	4-bit data that shows the condition codes
CCCC	4-bit data that shows the condition codes of Bcond instruction
bbb	3-bit data for specifying the bit number
L	1-bit data that specifies a program register in the register list

(2/6)

Mnemonic	Operand	Opcode	Operation	Execution Clock			Flags				
				i	r	l	CY	OV	S	Z	SAT
DBTRAP		1111100001000000	DBPC←PC+2 (restored PC) DBPSW←PSW PSW.NP←1 PSW.EP←1 PSW.ID←1 PC←00000060H	3	3	3					
DI		0000011111100000 0000000101100000	PSW.ID←1	1	1	1					
DISPOSE	imm5,list12	0000011001iiiiiL LLLLLLLLLLL00000	sp←sp+zero-extend(imm5 logically shift left by 2) GR[reg in list12]←Load-memory(sp,Word) sp←sp+4 repeat 2 steps above until all regs in list12 is loaded	n+1 Note 4	n+1 Note 4	n+1 Note 4					
	imm5,list12,[reg1]	0000011001iiiiiL LLLLLLLLLLRRRRR **Note 5**	sp←sp+zero-extend(imm5 logically shift left by 2) GR[reg in list12]←Load-memory(sp,Word) sp←sp+4 repeat 2 steps above until all regs in list12 is loaded PC←GR[reg1]	n+3 Note 4	n+3 Note 4	n+3 Note 4					
DIV	reg1,reg2,reg3	rrrrr111111RRRRR wwwww01011000000	GR[reg2]←GR[reg2]÷GR[reg1] GR[reg3]←GR[reg2]%GR[reg1]	35	35	35		×	×	×	
DIVH	reg1,reg2	rrrrr000010RRRRR	GR[reg2]←GR[reg2]÷GR[reg1]Note 6	35	35	35		×	×	×	
	reg1,reg2,reg3	rrrrr111111RRRRR wwwww01010000000	GR[reg2]←GR[reg2]÷GR[reg1]Note 6 GR[reg3]←GR[reg2]%GR[reg1]	35	35	35		×	×	×	
DIVHU	reg1,reg2,reg3	rrrrr111111RRRRR wwwww01010000010	GR[reg2]←GR[reg2]÷GR[reg1]Note 6 GR[reg3]←GR[reg2]%GR[reg1]	34	34	34		×	×	×	
DIVU	reg1,reg2,reg3	rrrrr111111RRRRR wwwww01011000010	GR[reg2]←GR[reg2]÷GR[reg1] GR[reg3]←GR[reg2]%GR[reg1]	34	34	34		×	×	×	
EI		1000011111100000 0000000101100000	PSW.ID←0	1	1	1					
HALT		0000011111100000 0000000100100000	Stop	1	1	1					
HSW	reg2,reg3	rrrrr11111100000 wwwww01101000100	GR[reg3]←GR[reg2](15 : 0) ll GR[reg2] (31 : 16)	1	1	1	×	0	×	×	
JARL	disp22,reg2	rrrrr11110ddddd ddddddddddddddd0 **Note 7**	GR[reg2]←PC+4 PC←PC+sign-extend(disp22)	2	2	2					
JMP	[reg1]	00000000011RRRRR	PC←GR[reg1]	3	3	3					
JR	disp22	0000011110ddddd ddddddddddddddd0 **Note 7**	PC←PC+sign-extend(disp22)	2	2	2					
LD.B	disp16[reg1],reg2	rrrrr111000RRRRR ddddddddddddddd	adr←GR[reg1]+sign-extend(disp16) GR[reg2]←sign-extend(Load-memory(adr,Byte))	1	1	Note 11					
LD.BU	disp16[reg1],reg2	rrrrr11110bRRRRR ddddddddddddd1 **Notes 8, 10**	adr←GR[reg1]+sign-extend(disp16) GR[reg2]←zero-extend(Load-memory(adr,Byte))	1	1	Note 11					

V850ES/JC3-L, V850ES/JE3-L
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