Renesas Electronics America Inc - UPD70F3840GB(R)-GAH-AX Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	V850ES
Core Size	32-Bit Single-Core
Speed	20MHz
Connectivity	CSI, EBI/EMI, I²C, UART/USART
Peripherals	DMA, LVD, PWM, WDT
Number of I/O	50
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 3.6V
Data Converters	A/D 10x10b; D/A 1x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd70f3840gb-r-gah-ax

(3/4)

(c) V850ES/JE3-L (1/2)

After reset: 0000H R/W Address: PMC9 FFFFF452H,
PMC9L FFFFF452H, PMC9H FFFFF453H

	15	14	13	12	11	10	9	8
PMC9 (PMC9H)	PMC915	PMC914	PMC913	PMC912	PMC911	PMC910	PMC99	PMC98

	7	6	5	4	3	2	1	0
(PMC9L)	PMC97	PMC96	0	PMC94	PMC93	PMC92	PMC91	PMC90

PMC915	Specification of pin operation
0	I/O port (P915)
1	INTP6 input/TIP50 input/TOP50 output

PMC914	Specification of pin operation
0	I/O port (P914)
1	INTP5 input/TIP51 input/TOP51 output

PMC913	Specification of pin operation
0	I/O port (P913)
1	INTP4 input

PMC912	Specification of pin operation
0	I/O port (P912)
1	$\overline{\text{SCKB3}}$ I/O

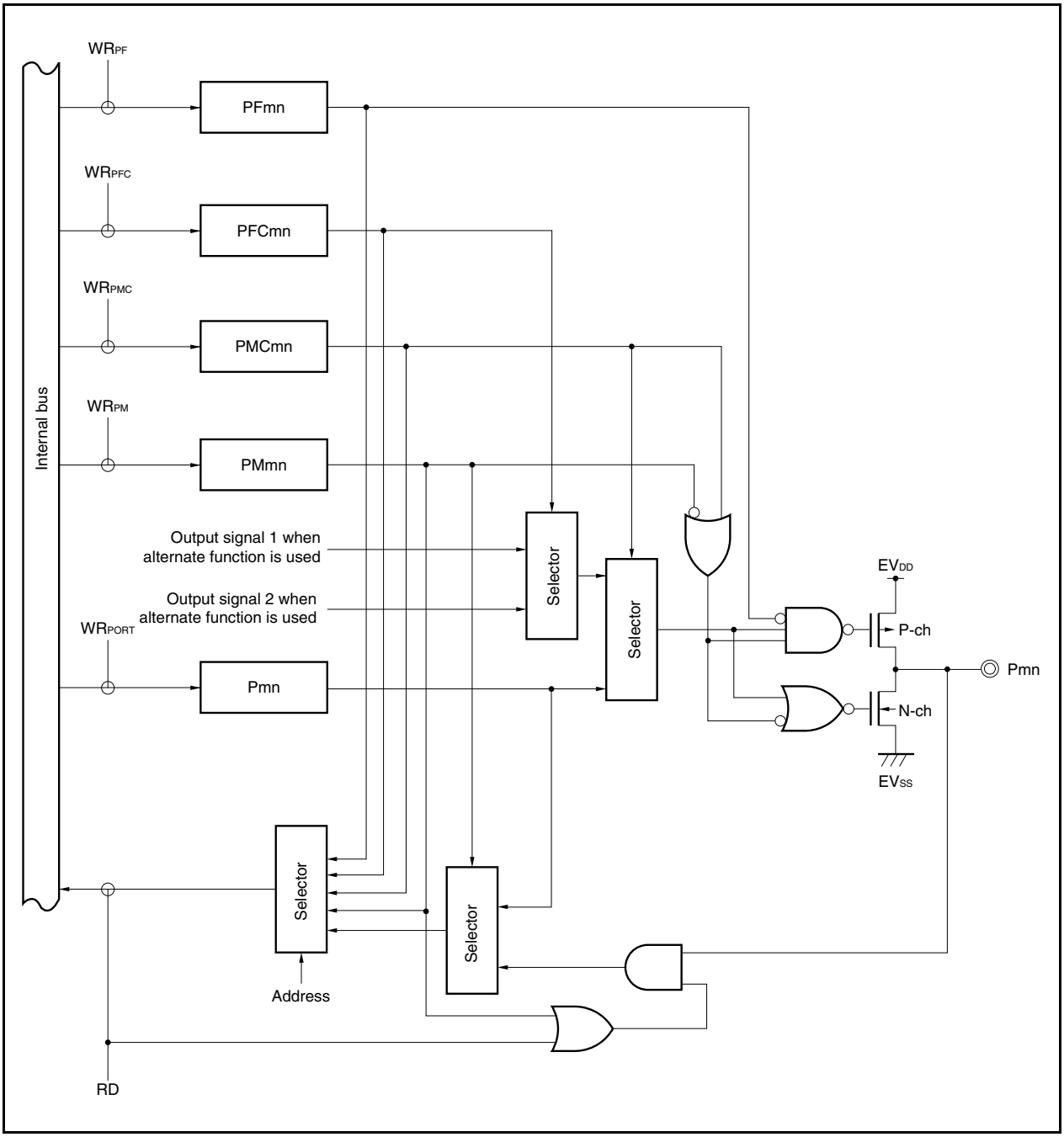
PMC911	Specification of pin operation
0	I/O port (P911)
1	SOB3 output

PMC910	Specification of pin operation
0	I/O port (P910)
1	SIB3 input

PMC99	Specification of pin operation
0	I/O port (P99)
1	$\overline{\text{SCKB1}}$ I/O

PMC98	Specification of pin operation
0	I/O port (P98)
1	SOB1 output

Figure 4-10. Block Diagram of Type G-3



6.2.2 Register configuraiton

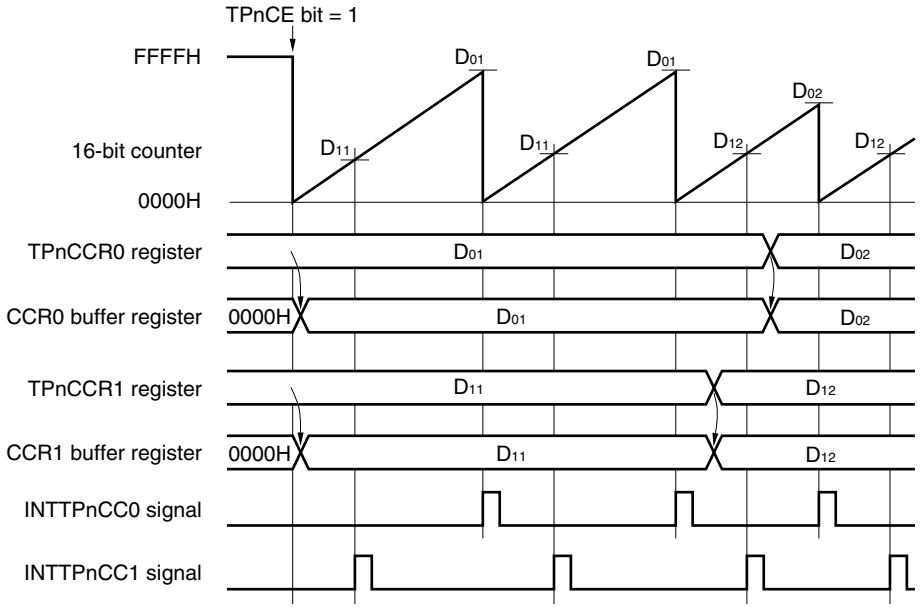
For the V850ES/JC3-L and V850ES/JE3-L, the registers and their bit assignment differ for each product.
The register configuration for each product is shown in the following tables

(1) V850ES/JC3-L (40-pin)

Channel	Register name	Bit position							
		7	6	5	4	3	2	1	0
TMP0	TP0CTL0	TP0CE	0	0	0	0	TP0CKS2	TP0CKS1	TP0CKS0
	TP0CTL1	0	0	0	0	0	TP0MD2	TP0MD1	TP0MD0
TMP1	TP1CTL0	TP1CE	0	0	0	0	TP1CKS2	TP1CKS1	TP1CKS0
	TP1CTL1	0			0	0	TP1MD2	TP1MD1	TP1MD0
TMP2	TP2CTL0	TP2CE	0	0	0	0	TP2CKS2	TP2CKS1	TP2CKS0
	TP2CTL1	0	TP2EST	TP2EEE	0	0	TP2MD2	TP2MD1	TP2MD0
	TP2IOC0	0	0	0	0	TP2OL1	TP2OE1	TP2OL0	TP2OE0
	TP2IOC1	0	0	0	0	TP2IS3	TP2IS2	TP2IS1	TP2IS0
	TP2IOC2	0	0	0	0	TP2EES1	TP2EES0	TP2ETS1	TP2ETS0
	TP2OPT0	0	0	TP2CCS1	TP2CCS0	0	0	0	TP2OVF
TMP3	TP3CTL0	TP3CE	0	0	0	0	TP3CKS2	TP3CKS1	TP3CKS0
	TP3CTL1	0	0	0	0	0	TP3MD2	TP3MD1	TP3MD0
TMP4	TP4CTL0	TP4CE	0	0	0	0	TP4CKS2	TP4CKS1	TP4CKS0
	TP4CTL1	0	0	0	0	0	TP4MD2	TP4MD1	TP4MD0
TMP5	TP5CTL0	TP5CE	0	0	0	0	TP5CKS2	TP5CKS1	TP5CKS0
	TP5CTL1	0	TP5EST	TP5EEE	0	0	TP5MD2	TP5MD1	TP5MD0
	TP5IOC0	0	0	0	0	TP5OL1	TP5OE1	TP5OL0	TP5OE0
	TP5IOC1	0	0	0	0	TP5IS3	TP5IS2	TP5IS1	TP5IS0
	TP5IOC2	0	0	0	0	TP5EES1	TP5EES0	TP5ETS1	TP5ETS0
	TP5OPT0	0	0	TP5CCS1	TP5CCS0	0	0	0	TP5OVF

Remark The TPnCCR0, TPnCCR1, and TPnCNT registers are available for all channels.

Figure 6-3. Anytime Write Timing

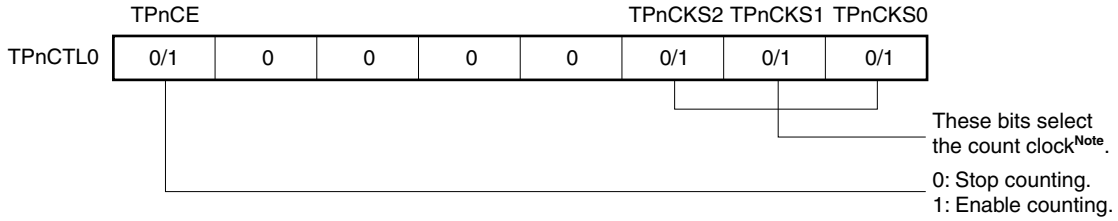


Remarks 1. D_{01}, D_{02}: Set value of TPnCCR0 register
D_{11}, D_{12}: Set value of TPnCCR1 register

2. The timing chart applies to the case when TMP is being used as an interval timer.

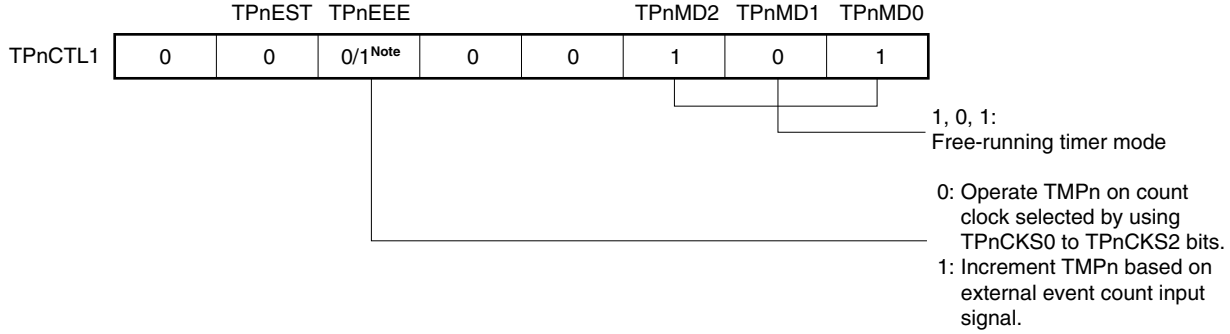
Figure 6-55. Register Settings in Free-Running Timer Mode (1/2)

(a) TMPn control register 0 (TPnCTL0)



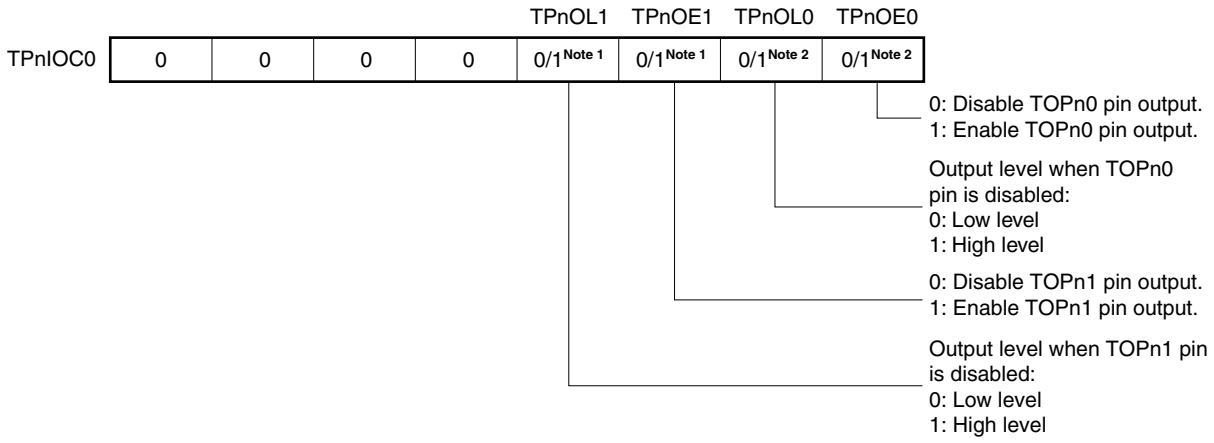
Note The setting of these bits is invalid when the TPnCTL1.TPnEEE bit is 1.

(b) TMPn control register 1 (TPnCTL1)



Note The capture function of the TIPn0 pin cannot be used if the TPnCTL1.TPnEEE bit is 1.

(c) TMPn I/O control register 0 (TPnIOC0)



Notes 1. The TOPn1 pin cannot be used when the TIPn1 pin is being used.

2. The TOPn0 pin cannot be used when the TIPn0 pin is being used.

(10) TMQ0 capture/compare register 3 (TQ0CCR3)

The TQ0CCR3 register can be used as a capture register or a compare register depending on the mode.

This register can be selected as a capture register or a compare register only in the free-running timer mode, according to the setting of the TQ0OPT0.TQ0CCS3 bit. In the pulse width measurement mode, the TQ0CCR3 register can be used only as a capture register. In any other mode, this register can be used only as a compare register.

The TQ0CCR3 register can be read or written during operation.

This register can be read or written in 16-bit units.

Reset sets this register to 0000H.

Caution Accessing the TQ0CCR3 register is prohibited in the following statuses. Moreover, if the system is in the wait status, the only way to cancel the wait status is to execute a reset. For details, see 3.4.9 (1) Accessing specific on-chip peripheral I/O registers.

- **When the CPU operates on the subclock and main clock oscillation is stopped**
- **When the CPU operates on the internal oscillator clock**

After reset: 0000H R/W Address: FFFFF54CH

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TQ0CCR3																

(a) Function as compare register

The TQ0CCR3 register can be rewritten even when the TQ0CTL0.TQ0CE bit = 1.

The set value of the TQ0CCR3 register is transferred to the CCR3 buffer register. When the value of the 16-bit counter matches the value of the CCR3 buffer register, a compare match interrupt request signal (INTTQ0CC3) is generated. If TOQ03 pin output is enabled at this time, the output of the TOQ03 pin is inverted (For details, see the descriptions of each operating mode.).

(b) Function as capture register

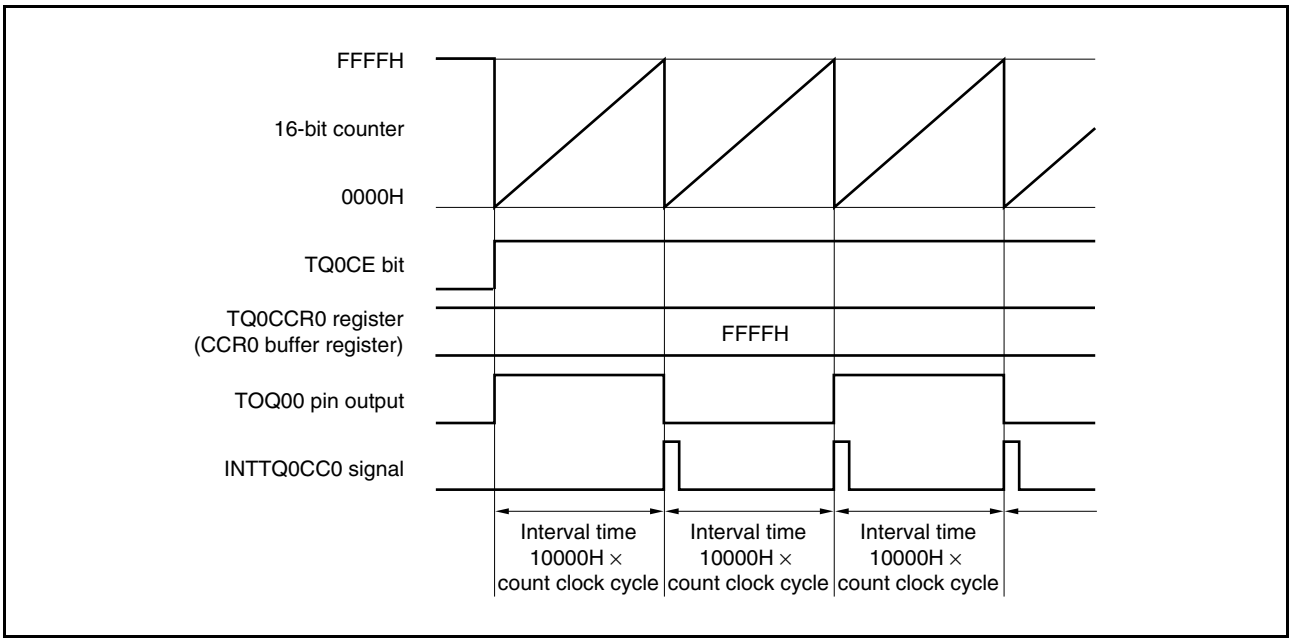
When the TQ0CCR3 register is used as a capture register in the free-running timer mode, the count value of the 16-bit counter is stored in the TQ0CCR3 register if the valid edge of the capture trigger input pin (TIQ03 pin) is detected. In the pulse-width measurement mode, the count value of the 16-bit counter is stored in the TQ0CCR3 register and the 16-bit counter is cleared (0000H) if the valid edge of the capture trigger input pin (TIQ03 pin) is detected.

Even if the capture operation and reading the TQ0CCR3 register conflict, the correct value of the TQ0CCR3 register can be read.

(b) Operation when TQ0CCR0 register is set to FFFFH

When the TQ0CCR0 register is set to FFFFH, the 16-bit counter increments up to FFFFH and is reset to 0000H in synchronization with the next increment timing. The INTTQ0CC0 signal is then generated and the output of the TOQ00 pin is inverted. At this time, an overflow interrupt request signal (INTTQ0OV) is not generated, nor is the overflow flag (TQ0OPT0.TQ0OVF bit) set to 1.

Figure 7-11. Operation of Interval Timer When TQ0CCR0 Register Is Set to FFFFH



(13) A/D conversion result hysteresis characteristics

The successive comparison type A/D converter holds the analog input voltage in the internal sample & hold capacitor and then performs A/D conversion. After A/D conversion has finished, the analog input voltage remains in the internal sample & hold capacitor. As a result, the following phenomena may occur.

- When the same channel is used for A/D conversions, if the voltage is higher or lower than the previous A/D conversion, then hysteresis characteristics may appear where the conversion result is affected by the previous value. Thus, even if the conversion is performed at the same potential, the result may vary.
- When switching the analog input channel, hysteresis characteristics may appear where the conversion result is affected by the previous channel value. This is because one A/D converter is used for the A/D conversions. Thus, even if the conversion is performed at the same potential, the result may vary.

Therefore, to obtain a more accurate conversion result, perform A/D conversion twice successively for the same channel, and discard the first conversion result.

(2/2)

UAnDIR	Data transfer order
0	MSB first
1	LSB first

- This register can be rewritten only when the UAnPWR bit is 0 or the UAnTXE bit and the UAnRXE bit are 0.
- When transmission and reception are performed in the LIN format, set the UAnDIR bit to 1.

UAnPS1	UAnPS0	Parity selection during transmission	Parity selection during reception
0	0	No parity output	Reception with no parity
0	1	0 parity output	Reception with 0 parity
1	0	Odd parity output	Odd parity check
1	1	Even parity output	Even parity check

- This register is rewritten only when the UAnPWR bit is 0 or the UAnTXE bit and the UAnRXE bit are 0.
- If “Reception with 0 parity” is selected during reception, a parity check is not performed. Therefore, the UAnSTR.UAnPE bit is not set.
- When transmission and reception are performed in the LIN format, clear the UAnPS1 and UAnPS0 bits to 00.

UAnCL	Specification of data character length of 1 frame of transmit/receive data
0	7 bits
1	8 bits

- This register can be rewritten only when the UAnPWR bit is 0 or the UAnTXE bit and the UAnRXE bit are 0.
- When transmission and reception are performed in the LIN format, set the UAnCL bit to 1.

UAnSL	Specification of length of stop bit for transmit data
0	1 bit
1	2 bits

This register can be rewritten only when the UAnPWR bit is 0 or the UAnTXE bit and the UAnRXE bit are 0.

Remark For details of parity, see **15.6.6 Parity types and operations**.

(2) UARTAn control register 1 (UAnCTL1)

For details, see **15.7 (2) UARTAn control register 1 (UAnCTL1)**.

(3) UARTAn control register 2 (UAnCTL2)

For details, see **15.7 (3) UARTAn control register 2 (UAnCTL2)**.

17.4 Registers

I²C0n is controlled by the following registers.

- IIC control registers n (IICCn)
- IIC status registers n (IICSn)
- IIC flag registers n (IICFn)
- IIC clock select registers n (IICCLn)
- IIC function expansion registers n (IICXn)
- IIC division clock select registers 0, 1 (OCKS0, OCKS1)

The following registers are also used.

- IIC shift registers n (IICn)
- Slave address registers n (SVAn)

Remark For the alternate-function pin settings, see **Table 4-17 Settings When Pins Are Used for Alternate Functions**.

(1) IIC control registers n (IICCn)

The IICCn register enables/stops I²C0n operations, sets the wait timing, and sets other I²C operations.

These registers can be read or written in 8-bit or 1-bit units. However, set the SPIEn, WTIMn, and ACKEn bits when the IICEn bit is 0 or during the wait period. When setting the IICEn bit from “0” to “1”, these bits can also be set at the same time.

Reset sets these registers to 00H.

(3) IIC flag registers n (IICFn)

The IICFn register sets the I²C0n operation mode and indicates the I²C bus status.

These registers can be read or written in 8-bit or 1-bit units. However, the STCFn and IICBSYn bits are read-only.

IICRSVn enables/disables the communication reservation function (see **17.14 Communication Reservation**).

The initial value of the IICBSYn bit is set by using the STCENn bit (see **17.15 Cautions**).

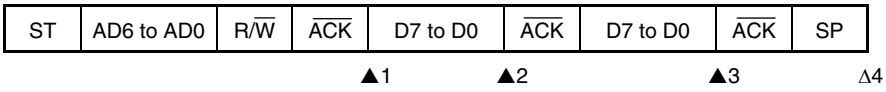
The IICRSVn and STCENn bits can be written only when operation of I²C0n is disabled (IICCn.IICEn bit = 0). After operation is enabled, IICFn can be read.

Reset sets these registers to 00H.

17.7.2 Slave device operation (when receiving slave address data (address match))

(1) Start ~ Address ~ Data ~ Data ~ Stop

<1> When IICCn.WTIMn bit = 0



▲1: IICSn register = 0001X110B

▲2: IICSn register = 0001X000B

▲3: IICSn register = 0001X000B

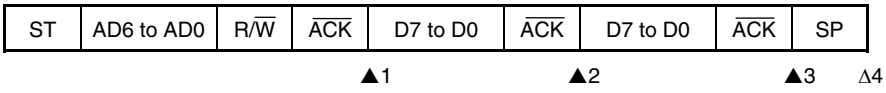
Δ 4: IICSn register = 00000001B

Remark ▲:Always generated

Δ: Generated only when IICCn.SPIEn bit = 1

X: don't care

<2> When WTIMn bit = 1



▲1: IICSn register = 0001X110B

▲2: IICSn register = 0001X100B

▲3: IICSn register = 0001XX00B

Δ 4: IICSn register = 00000001B

Remark ▲: Always generated

Δ: Generated only when SPIEn bit = 1

X: don't care

(4) Start ~ Code ~ Data ~ Start ~ Address ~ Data ~ Stop

<1> When WTIMn bit = 0 (after restart, address mismatch (= not extension code))

ST	AD6 to AD0	R/$\overline{W}$	$\overline{ACK}$	D7 to D0	$\overline{ACK}$	ST	AD6 to AD0	R/$\overline{W}$	$\overline{ACK}$	D7 to D0	$\overline{ACK}$	SP
			▲1		▲2					▲3		Δ4

▲1: IICSn register = 0010X010B

▲2: IICSn register = 0010X000B

▲3: IICSn register = 00000X10B

Δ 4: IICSn register = 00000001B

Remark ▲:Always generated

Δ: Generated only when SPIEn bit = 1

X: don't care

<2> When WTIMn bit = 1 (after restart, address mismatch (= not extension code))

ST	AD6 to AD0	R/$\overline{W}$	$\overline{ACK}$	D7 to D0	$\overline{ACK}$	ST	AD6 to AD0	R/$\overline{W}$	$\overline{ACK}$	D7 to D0	$\overline{ACK}$	SP
			▲1	▲2		▲3				▲4		Δ5

▲1: IICSn register = 0010X010B

▲2: IICSn register = 0010X110B

▲3: IICSn register = 0010XX00B

▲4: IICSn register = 00000X10B

Δ 5: IICSn register = 00000001B

Remark ▲:Always generated

Δ: Generated only when SPIEn bit = 1

X: don't care

(3) External interrupt falling, rising edge specification register 9H (INTF9H, INTR9H)

The INTF9H and INTR9H registers are 8-bit registers that specify detection of the falling and rising edges of the external interrupt pins (INTP4 to INTP6).

These registers can be read or written in 8-bit or 1-bit units.

Reset sets these registers to 00H.

Caution When switching from the port function to the external interrupt function (alternate function), an edge might be detected. Therefore, set the INTF9n and INTR9n bits to 00, and then specify the external interrupt function (PMC9.PMC9n bit = 1).

When switching from the external interrupt function to the port function, an edge might be detected as well. Therefore, set the INTF9n and INTR9n bits to 00, and then specify the port function (PMC9.PMC9n bit = 0).

After reset: 00H R/W Address: INTF9H FFFFFC13H, INTR9H FFFFFC33H

	15	14	13	12	11	10	9	8
INTF9H	INTF915	INTF914	INTF913Note	0	0	0	0	0
	INTP6	INTP5	INTP4					
INTR9H	INTR915	INTR914	INTR913Note	0	0	0	0	0
	INTP6	INTP5	INTP4					

Note For the V850ES/JE3-L, 0 or 1 can be specified for this bit. For the V850ES/JC3-L, this bit must be cleared to 0.

Remark For how to specify a valid edge, see **Table 19-6**.

Table 19-6. Valid Edge Specification

INTF9n	INTR9n	Valid Edge Specification (n = 13 to 15)
0	0	No edge detected
0	1	Rising edge
1	0	Falling edge
1	1	Both rising and falling edges

Caution Be sure to clear the INTF9n and INTR9n bits to 00 when these registers are not used for the INTP4 to INTP6 pins.

Remark n = 13 to 15: Control of INTP4 to INTP6 pins

29.3 ROM Security Function

29.3.1 Security ID

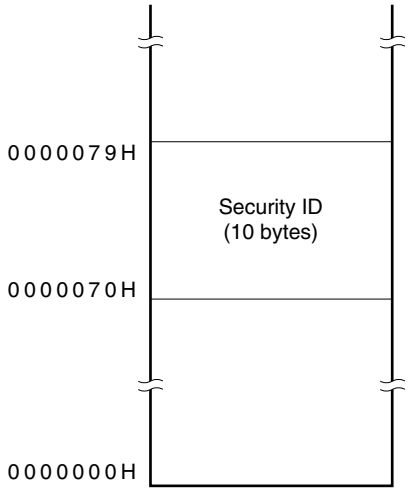
The flash memory versions of the V850ES/JC3-L and V850ES/JE3-L perform authentication using a 10-byte ID code to prevent the contents of the flash memory from being read by an unauthorized person during on-chip debugging by the on-chip debug emulator.

Set the ID code in the 10-byte internal flash memory area from 0000070H to 0000079H to allow the debugger perform ID authentication.

If the IDs match, the security is released and reading the flash memory and using the on-chip debug emulator are enabled.

- Set the 10-byte ID code to 0000070H to 0000079H.
- Bit 7 of 0000079H is the on-chip debug emulator enable flag.
  (0: Disable, 1: Enable)
- When the on-chip debug emulator is started, the debugger requests ID input. When the ID code input to the debugger and the ID code set in 0000070H to 0000079H match, the debugger starts.
- Debugging cannot be performed if the on-chip debug emulator enable flag is 0, even if the ID codes match.

Figure 29-6. Security ID Area



Caution After the flash memory is erased, 1 is written to the entire area.

CHAPTER 30 ELECTRICAL SPECIFICATIONS (V850ES/JC3-L (40-pin))

30.1 Absolute Maximum Ratings

Absolute Maximum Ratings (T_A = 25°C) (1/2)

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{DD}	$V_{DD} = EV_{DD} = AV_{REF0}$	−0.5 to +4.6	V
	EV_{DD}	$V_{DD} = EV_{DD} = AV_{REF0}$	−0.5 to +4.6	V
	AV_{REF0}	$V_{DD} = EV_{DD} = AV_{REF0}$	−0.5 to +4.6	V
	V_{SS}	$V_{SS} = EV_{SS} = AV_{SS}$	−0.5 to +0.5	V
	AV_{SS}	$V_{SS} = EV_{SS} = AV_{SS}$	−0.5 to +0.5	V
	EV_{SS}	$V_{SS} = EV_{SS} = AV_{SS}$	−0.5 to +0.5	V
Input voltage	V_{I1}	P97, P914, P915, PCM0, PDL5, $\overline{\text{RESET}}$, FLMD0	−0.5 to EV_{DD} + 0.5 Note 1	V
	V_{I3}	X1	−0.5 to V_{DD} + 0.5 Note 1	V
		X2	−0.5 to V_{RO} Note 2 + 0.5 Note 1	
	V_{I4}	P02, P03, P05, P30, P31, P40 to P42, P50 to P55, P90, P91, P96	−0.5 to +6.0	V
	V_{I5}	XT1, XT2	−0.5 to V_{RO} Note 2 + 0.5	V
Analog input voltage	V_{IAN}	P70 to P74	−0.5 to AV_{REF0} + 0.5 Note 1	V

Notes 1. Be sure not to exceed the absolute maximum ratings (MAX. value) of each supply voltage.

2. On-chip regulator output voltage

Cautions 1. Do not directly connect the output (or I/O) pins of IC products to each other, or to V_{DD}, V_{CC}, and GND. Open-drain pins or open-collector pins, however, can be directly connected to each other. Direct connection of the output pins between an IC product and an external circuit is possible, if the output pins can be set to the high-impedance state and the output timing of the external circuit is designed to avoid output conflict.

2. Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

The ratings and conditions indicated for DC characteristics, AC characteristics, and operating conditions represent the quality assurance range during normal operation.

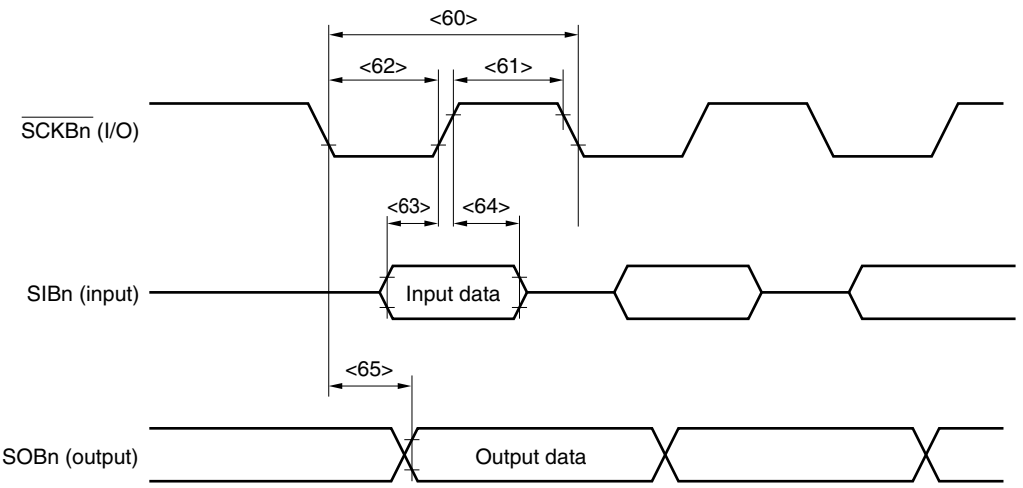
Remark Unless specified otherwise, the ratings of alternate-function pins are the same as those of port pins.

(2) Slave mode

(T_A = –40 to +85°C, V_{DD} = EV_{DD} = AV_{REF0} = AV_{REF1}, V_{SS} = EV_{SS} = AV_{SS} = 0 V, C_L = 50 pF)

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
$\overline{SCKBn}$ cycle time	t_{KCY2}	<60>	2.7 V ≤ V_{DD} ≤ 3.6 V	125		ns
			2.2 V ≤ V_{DD} < 2.7 V	800		ns
$\overline{SCKBn}$ high-level width	t_{KH2}	<61>	2.2 V ≤ V_{DD} ≤ 3.6 V	54.5		ns
$\overline{SCKBn}$ low-level width	t_{KL2}	<62>	2.2 V ≤ V_{DD} ≤ 3.6 V	54.5		ns
SIBn setup time (to $\overline{SCKBn}$↑)	t_{SIK2}	<63>	2.7 V ≤ V_{DD} ≤ 3.6 V	27		ns
			2.2 V ≤ V_{DD} < 2.7 V	100		ns
SIBn hold time (from $\overline{SCKBn}$↑)	t_{KSI2}	<64>	2.7 V ≤ V_{DD} ≤ 3.6 V	27		ns
			2.2 V ≤ V_{DD} < 2.7 V	100		ns
Delay time from $\overline{SCKBn}$↓ to SOBn output	t_{KSO2}	<65>	2.7 V ≤ V_{DD} ≤ 3.6 V		27	ns
			2.2 V ≤ V_{DD} < 2.7 V		95	ns

Remark n = 0 to 2, 4



Remark n = 0 to 2, 4

31.9 Flash Memory Programming Characteristics

(1) Basic characteristics

(T_A = –40 to +85°C, V_{DD} = EV_{DD} = AV_{REF0} = AV_{REF1} = 2.7 to 3.6 V, V_{SS} = EV_{SS} = AV_{SS} = 0 V, C_L = 50 pF)

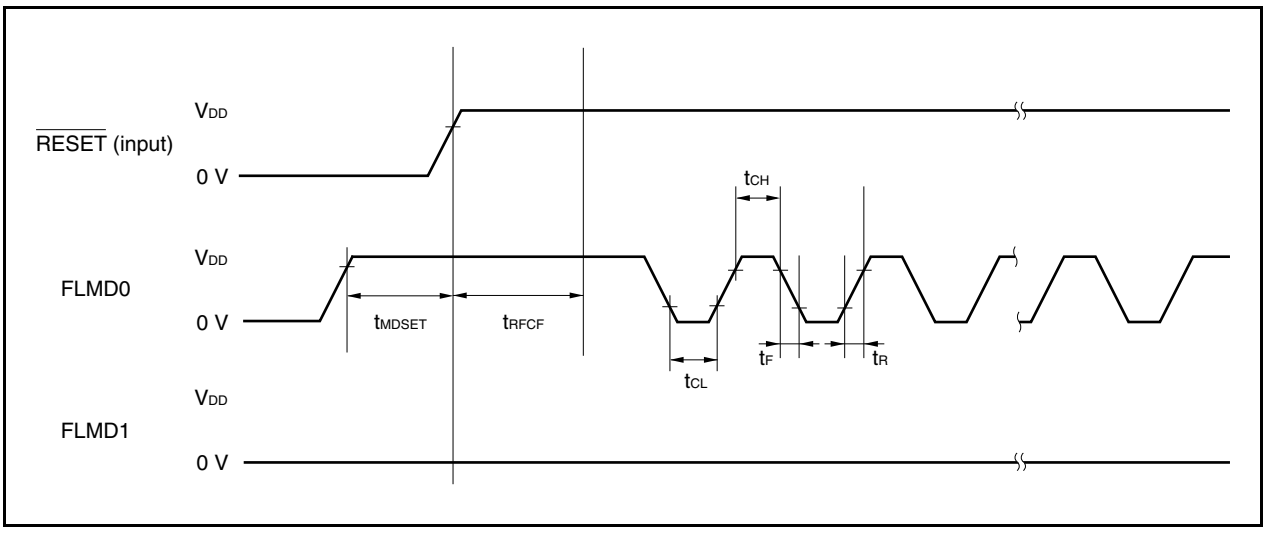
Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Operating frequency	f_{CPU}			2.5		20	MHz
Supply voltage	V_{DD}	2.5 MHz ≤ f_{XX} ≤ 20 MHz		2.7		3.6	V
Number of rewrites	C_{WRT}	Used for updating programs When using flash memory programmer and Renesas Electronics self programming library	Retained for 15 years	1,000			times
		Used for updating data When using Renesas Electronics EEPROM emulation library (usable ROM size: 12 KB of 6 consecutive blocks, or 6 KB of 3 consecutive blocks)	Retained for 5 years	10,000			times
Programming temperature	t_{PRG}			–40		+85	°C

(2) Serial write operation characteristics

(T_A = –40 to +85°C, V_{DD} = EV_{DD} = AV_{REF0} = AV_{REF1} = 2.7 to 3.6 V, V_{SS} = EV_{SS} = AV_{SS} = 0 V, C_L = 50 pF)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
FLMD0, FLMD1 setup time	t_{MDSET}		2		3000	ms
FLMD0 count start time from $\overline{\text{RESET}}$↑	t_{RFCF}	f_X = 2.5 to 10 MHz	800			μs
FLMD0 counter high-level width/ low-level width	t_{CH}/t_{CL}		10		100	μs
FLMD0 counter rise time/fall time	t_R/t_F				1	μs

Flash write mode setup timing

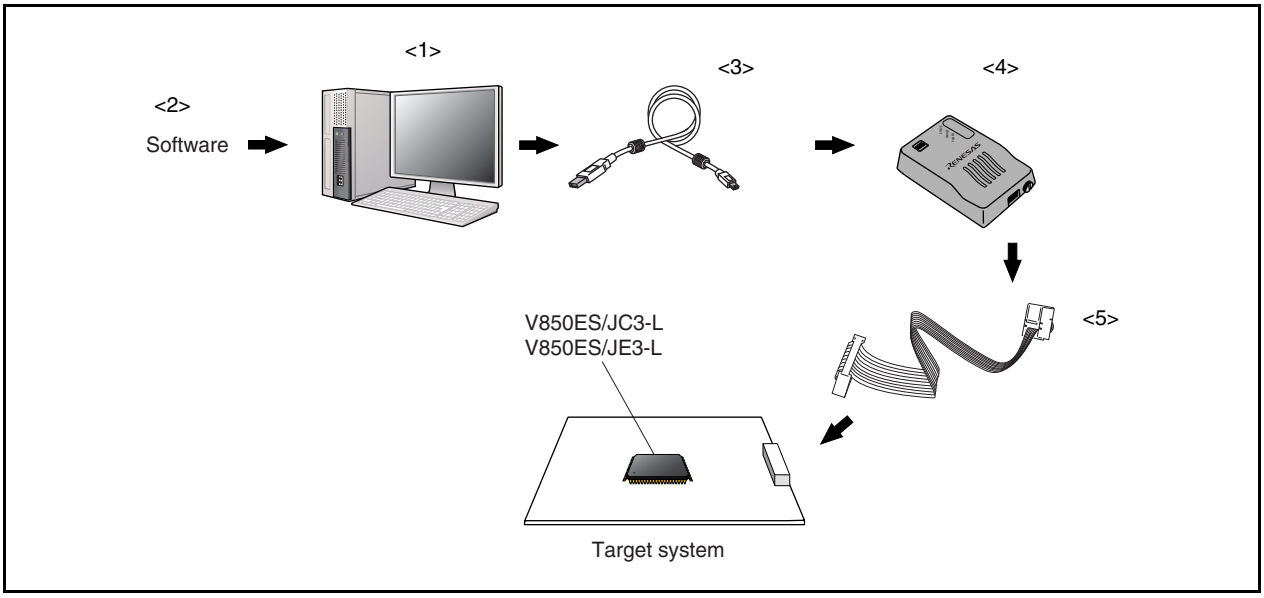


A.4.2 When using MINICUBE QB-V850MINIL

(1) On-chip emulation using MINICUBE

The system configuration when connecting MINICUBE to the host machine (PC-9821 series, PC/AT compatible) is shown below.

Figure A-3. On-Chip Emulation System Configuration



<1> Host machine	PC with USB ports
<2> Software	The integrated debugger ID850QB, device file, etc. Download the device file from the Renesas Electronics website. http://www2.renesas.com/micro/en/ods/index.html
<3> USB interface cable	USB cable to connect the host machine and MINICUBE. It is supplied with MINICUBE. The cable length is approximately 2 m.
<4> MINICUBE On-chip debug emulator	This on-chip debug emulator serves to debug hardware and software when developing application systems using the V850ES/JC3-L, V850ES/JE3-L. It supports integrated debugger ID850QB.
<5> OCD cable	Cable to connect MINICUBE and the target system. It is supplied with MINICUBE. The cable length is approximately 20 cm.

Remark The numbers in the angular brackets correspond to the numbers in Figure A-3.